RELIABILITY REPORT

FOR

MAX3748HETE+T

PLASTIC ENCAPSULATED DEVICES

February 28, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX3748HETE+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3748H multirate limiting amplifier functions as a data quantizer for SONET, Fibre Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds. A received-signal-strength indicator (RSSI) is available when the MAX3748H is combined with the MAX3744 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744 and the MAX3748H can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output signal polarity reversal (OUTPOL). Output disable can be used to implement squelch. The combination of the MAX3748H and the MAX3744 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header. The MAX3748H is packaged in a 3mm x 3mm, 16-pin thin QFN package with an exposed pad.

II. Manufacturing Information

A. Description/Function:	Compact, Low-Power, 155Mbps to 4.25Gbps Limiting Amplifier
B. Process:	CB53
C. Number of Device Transistors:	3151
D. Fabrication Location:	USA
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	September 23, 2011

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4342
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	68°C/W
K. Single Layer Theta Jc:	10°C/W
L. Multi Layer Theta Ja:	48°C/W
M. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	68.90 X 65.35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 1.2 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.4 / Metal2 = 0.4 / Metal3 = 1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 133C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 3881 \times 49 \times 2}$$ (Chi square value for MTTF upper limit)

(where 3881 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 25.1 \times 10^{-9}$

λ = 25.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the CB53 Process results in a FIT Rate of 0.46 @ 25C and 7.85 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JV9ZBQ002B, D/C 1116)

The HQ42 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX3748HETE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 133C Biased Time = 192 hrs.	DC Parameters & functionality	49	0	JV9ZBQ002B, D/C 1116

Note 1: Life Test Data may represent plastic DIP qualification lots.