RELIABILITY REPORT

FOR

**MAX3724E/D**

Die

December 14, 2004

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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## Conclusion

The MAX3724 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents



## I. Device Description

### A. General

The MAX3724 transimpedance amplifiers provide a compact, low-power solution for communication up to 3.2Gbps. It features 325nA input-referred noise at 2.1GHz bandwidth (BW) with 0.6pF input capacitance. The parts also have >2$mA_{P-P}$ AC input overload.

The part operates from a single +3.3V supply and consumes 93mW. The MAX3724 is in a compact 30-mil x 50-mil die and require no external compensation capacitor. A space-saving filter connection is provided for positive bias to the photodiode through an on-chip 580Ω resistor to $V_{CC}$. These features allow easy assembly into a low-cost TO-46 or TO-56 header with a photodiode.

The MAX3724 and MAX3748A receiver chip set provides an RSSI output using a Maxim-proprietary* interface technique. The MAX3724 preamplifier, MAX3748A postamplifier, and the DS1858/DS1859 SFP controller meet all the SFF-8472 digital diagnostic requirements.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Power-Supply Voltage (VCC) | -0.5V to +6.0V |
| Continuous CML Output Current (OUT+, OUT-) | -25mA to +25mA |
| Continuous Input Current (IN) | -4mA to +4mA |
| Continuous Input Current (FILTER) | -8mA to +8mA |
| Operating Junction Temperature Range (TJ) | -55°C to +150°C |
| Storage Ambient Temperature Range (TSTG) | -55°C to +150°C |
| Die Attach Temperature | +400°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 3.2Gbps SFP Transimpedance Amplifiers with RSSI |
| B. Process: | GST4-F60 |
| C. Number of Device Transistors: | 301 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | N/A |
| F. Date of Initial Production: | January, 2004 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | Die |
| B. Lead Frame: | N/A |
| C. Lead Finish: | N/A |
| D. Die Attach: | N/A |
| E. Bondwire: | N/A |
| F. Mold Material: | N/A |
| G. Assembly Diagram: | N/A |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | N/A |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 30 x 50 mils |
| B. Passivation: | $Si_3N_4$ (Silicon nitride) |
| C. Interconnect: | Au |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn) |
| F. Minimum Metal Spacing: | Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.11 \times 10^{-8}$ $\lambda$ = 10.11 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-7115) shows the static Burn-In circuit.Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-B3A**). Current monitor data for the GST4 Process results in a FIT Rate of 0.10 @ 25C and 1.70 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HD65 die type has been found to have all pins able to withstand a transient pulse of <+/-200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX3724E/D**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | |
| | Tj = 150°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 48 | 0 |
| **Moisture Testing** (Note 2) | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters & functionality | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process data for packaged device.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

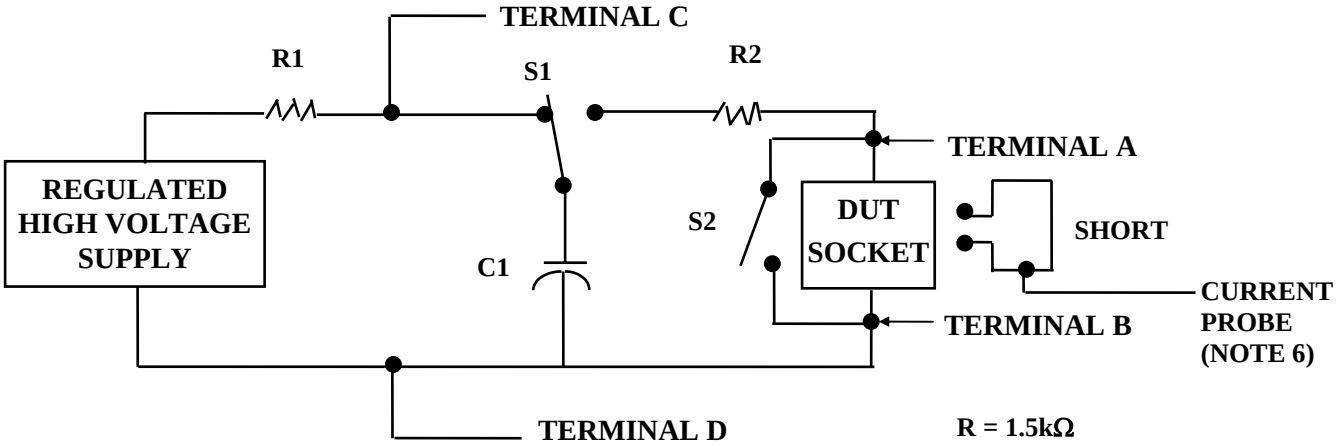
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

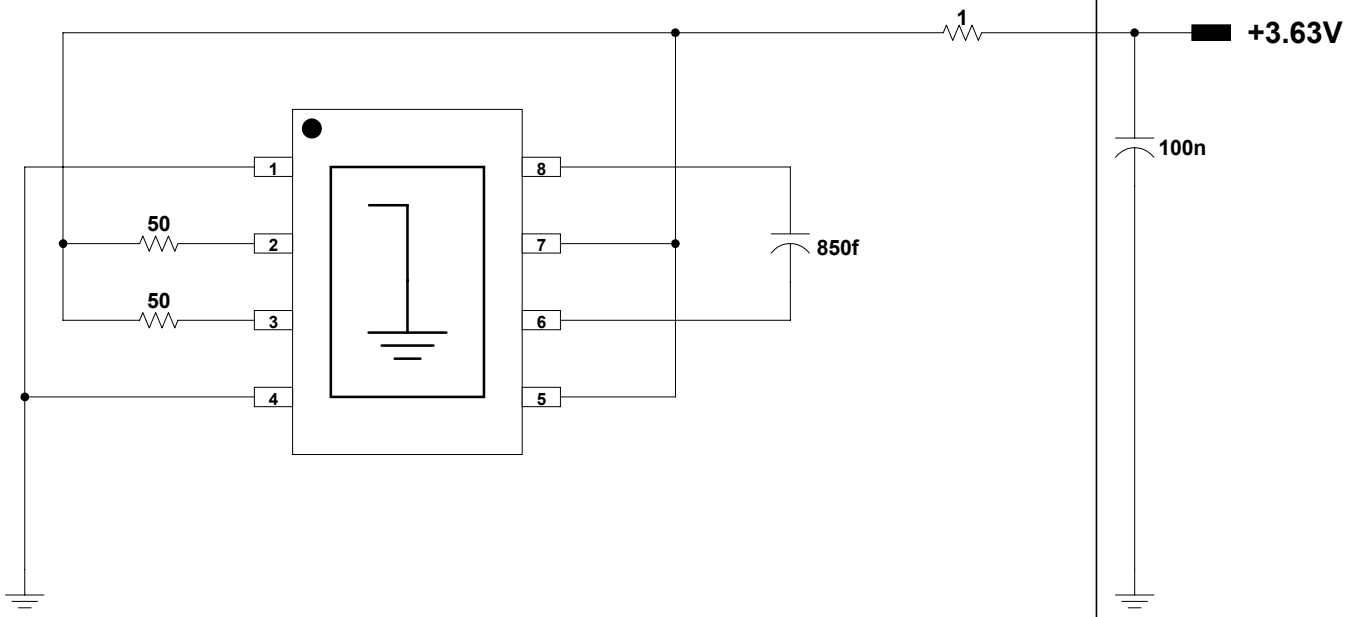
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.




Mil Std 883D
Method 3015.7
Notice 8

**ONCE PER SOCKET**

**ONCE PER BOARD**




**DEVICES: MAX 3744/3745 (HD40) MAX3724/3725 (HD65)**
**PACKAGE: 8-NSO**
**MAX. EXPECTED CURRENT = 33mA**