RELIABILITY REPORT

FOR

MAX3454EExx

PLASTIC ENCAPSULATED DEVICES

October 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
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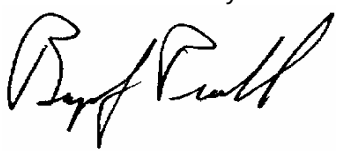
Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX3454E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3454E ±15kV ESD-protected USB compliant transceiver interfaces low-voltage ASICs with USB devices. The device fully complies with USB 1.1 and USB 2.0 when operating at full (12Mbps) and low (1.5Mbps) speeds. The MAX3454E operatse with V_L as low as +1.65V, ensuring compatibility with low-voltage ASICs. The MAX3454E features a logic-selectable suspend mode that reduces current consumption to less than 40µA. Integrated ±15kV ESD protection protects the USB D+ and D- bidirectional bus connections.

The MAX3454E features an internal 1.5k. USB pullup resistor and an enumeration function that allows devices to logically disconnect while plugged in. The MAX3454E operates over the extended temperature range (-40°C to +85°C) and is available in 14-pin TSSOP and 16-pin (3mm x 3mm) thin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
VBUS, VL, D+, D- to GND	-0.3V to +6.0V
VTRM to GND	-0.3V to (VBUS + 0.3V)
VP, VM, SUS, SPD, ENUM, RCV, OE, BD to GND	-0.3V to (VL + 0.3V)
Current (into any pin)	±15mA
Short-Circuit Current (D+ and D-)	±150mA
Continuous Power Dissipation (TA = +70°C)	
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin TSSOP	727mW
16-Pin Thin QFN 3mm x 3mm	1176mW
Derates above +70°C	
14-Pin TSSOP	9.1mW/°C
16-Pin Thin QFN 3mm x 3mm	14.7mW/°C

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected USB Transceivers
B. Process:	B8 (Standard 0.8 micron silicon gate CMOS)
C. Number of Device Transistors:	873
D. Fabrication Location:	California, USA
E. Assembly Location:	Hong Kong, Philippines or Thailand
F. Date of Initial Production:	October, 2003

III. Packaging Information

A. Package Type:	**14-Pin TSSOP**	**16-Pin QFN (3x3)**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Conductive Epoxy	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0507	# 05-9000-0509
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	61 x 61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 43 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 25.25 \times 10^{-9}$

$\lambda = 25.25$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6179) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RT68-4 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3454EExx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		43	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP QFN	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

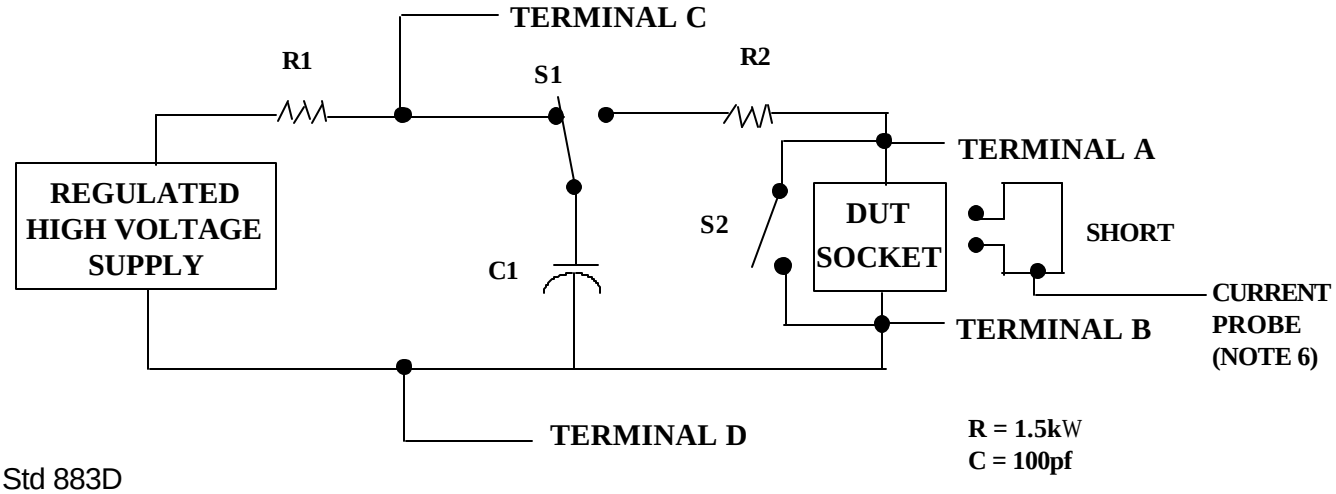
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

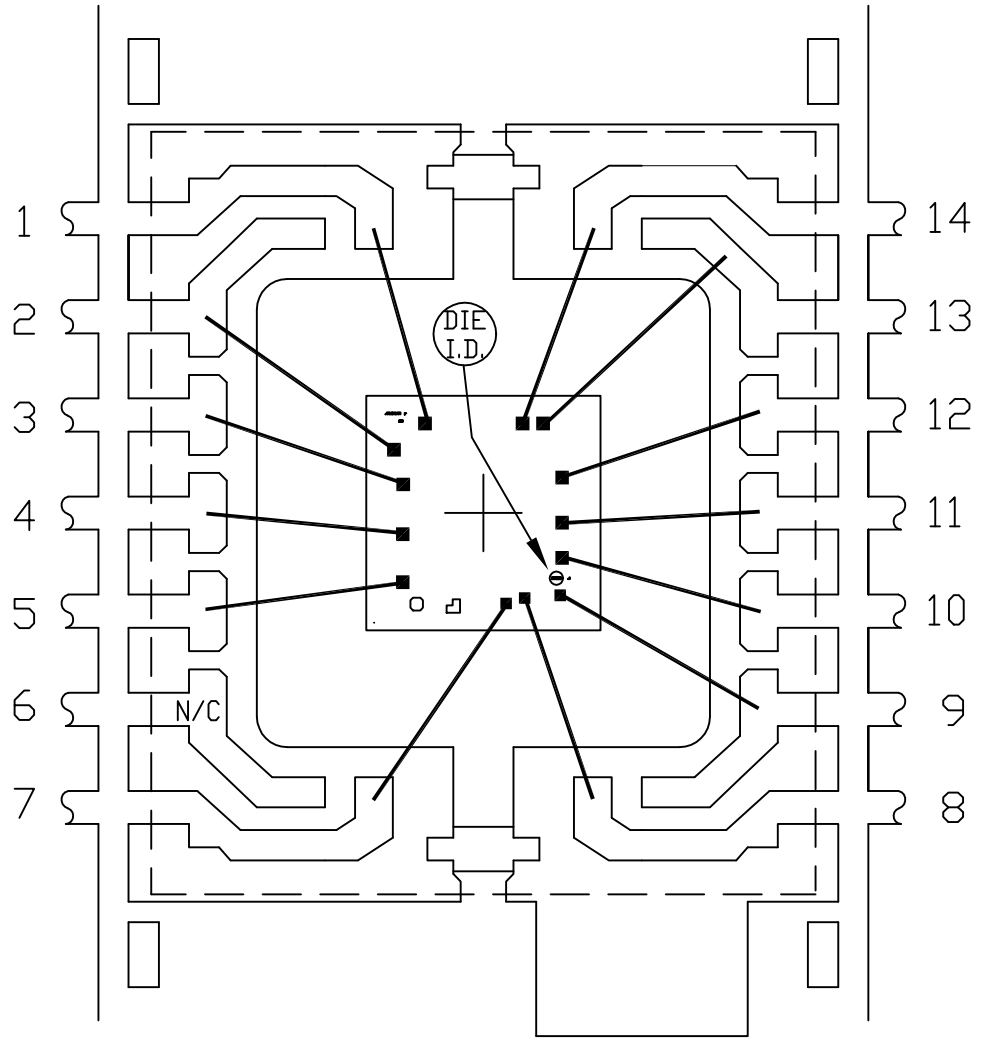
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

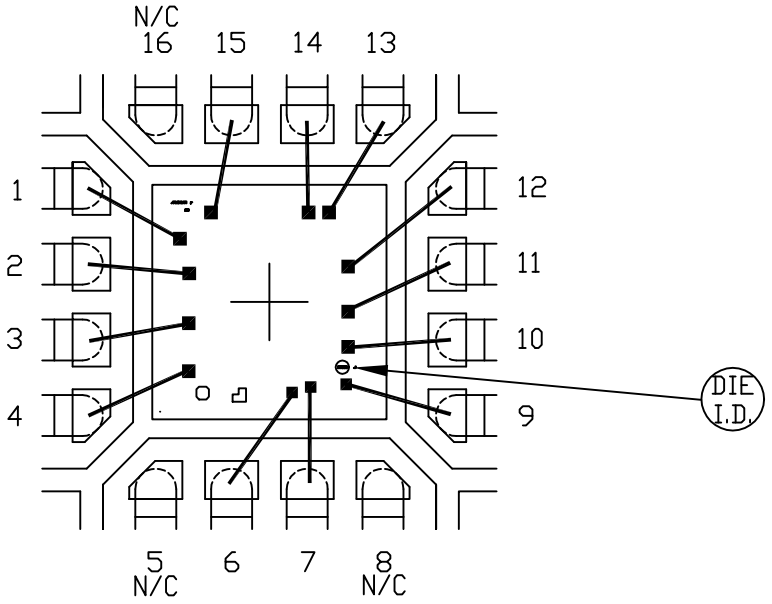


Mil Std 883D
Method 3015.7
Notice 8

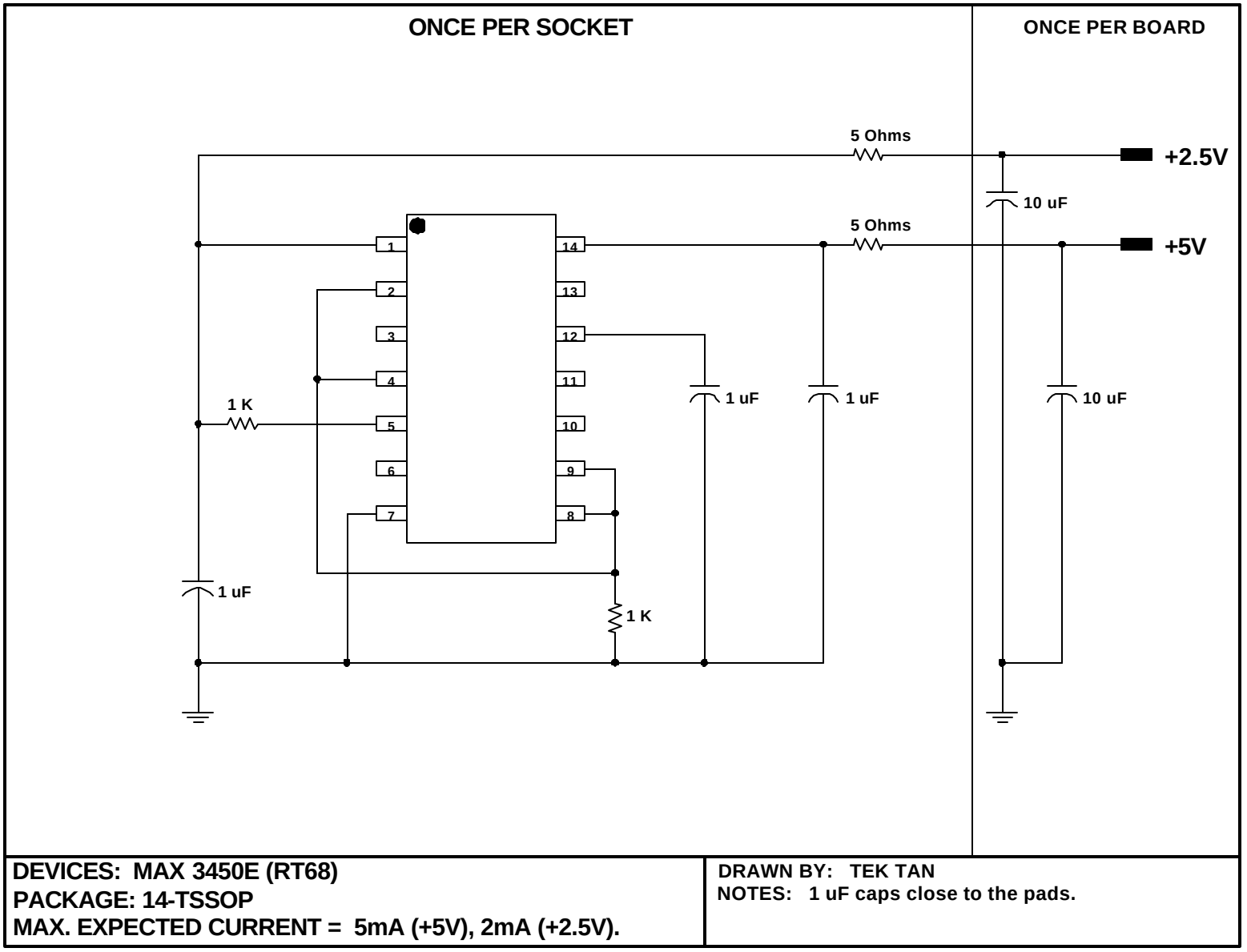


PKG. CODE: U14-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118×122	PKG.			BOND DIAGRAM #: 05-9000-0509	REV: A
	DESIGN				

3x3x0.80mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T1633-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 71x71	PKG.			BOND DIAGRAM #: 05-9000-0507	REV: A
	DESIGN				



DEVICES: MAX 3450E (RT68)
PACKAGE: 14-TSSOP
MAX. EXPECTED CURRENT = 5mA (+5V), 2mA (+2.5V).

DRAWN BY: TEK TAN
NOTES: 1 uF caps close to the pads.