RELIABILITY REPORT

FOR

**MAX3341EEUD**

PLASTIC ENCAPSULATED DEVICES

August 25, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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**Conclusion**

The MAX3341E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX3341E USB level translator converts logic-level signals to USB signals, and USB signals to logic-level signals. An internal 1.5kΩ USB termination resistor supports full-speed (12Mbps) USB operation. The MAX3341E provides built-in ±15kV ESD-protection circuitry on the USB I/O pins, D+ and D-, and $V_{CC}$.

The MAX3341E operates with logic supply voltages as low as 1.8V, ensuring compatibility with low-voltage ASICs. The suspend mode lowers supply current to less than 50µA. A unique enumerate feature allows changes in USB communication protocol while power is applied. The MAX3341E is fully compliant with USB specification 1.1, and full-speed operation under USB specification 2.0.

The MAX3341E has a USB detect that monitors the USB bus for insertion and signals this event.

The MAX3341E is available in the miniature 4 5 4 UCSP™, as well as the small 16-pin TSSOP, and is specified over the extended temperature range, -40°C to +85°C

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| (All Voltages Refer to GND Unless Otherwise Noted.) | |
| Supply Voltage (VCC) | -0.3V to +6V |
| Output of Internal Regulator (VTRM) (Note 1) | -0.3V to +6V |
| Input Voltage (D+, D-) (Notes 1, 2) | -0.3V to +6V |
| System Supply Voltage (VL) | -0.3V to +6V |
| RCV, SUSP, VMO, MODE, VPO, OE , VMI, VPI, USB_DET, ENUM | -0.3V to (VL + 0.3V) |
| Short-Circuit Current (D+, D-) to VCC or Ground (Note 3) | Continuous |
| Maximum Continuous Current (all other pins) | ±15mA |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Continuous Power Dissipation (TA = +70°C) 16-Pin TSSOP | 571mW |
| Derates above +70°C 16-Pin TSSOP | 7.1mW/°C |

Note 1: Guaranteed for VCC < +3.7V only.
Note 2: Absolute Maximum Rating for input voltage (D+, D-) with VCC > +3.7V is -0.3V to (VCC +0.3V).
Note 3: External 23.7..resistors connected to D+ and D-.

## II. Manufacturing Information

| | |
|---|---|
| A. Description: | ±15kV ESD-Protected USB Level Translator with USB Detect |
| B. Process: | S12 (Standard 1.2 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 2162 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Thailand or Philippines |
| F. Date of Initial Production: | April, 2002 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | **16-Lead TSSOP** |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-2601-0078 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 55 x 42 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 24.12 \times 10^{-9}$ $\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5903) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RT44 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

**Table 1**
Reliability Evaluation Test Results

**MAX3341EEUD**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 45 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | TSSOP | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test may represent DIP qualification packages.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

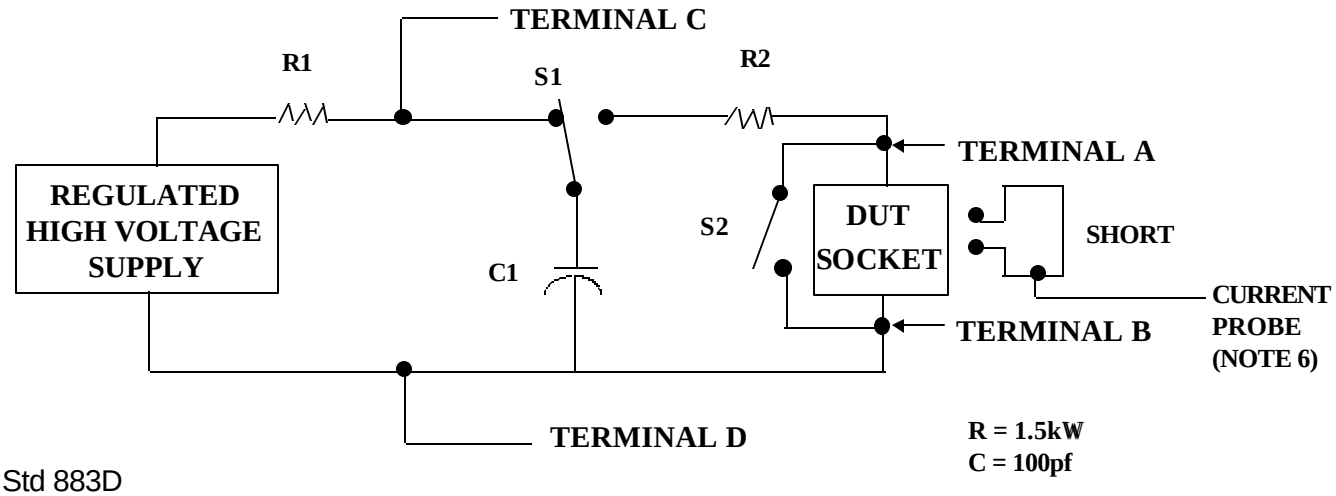
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

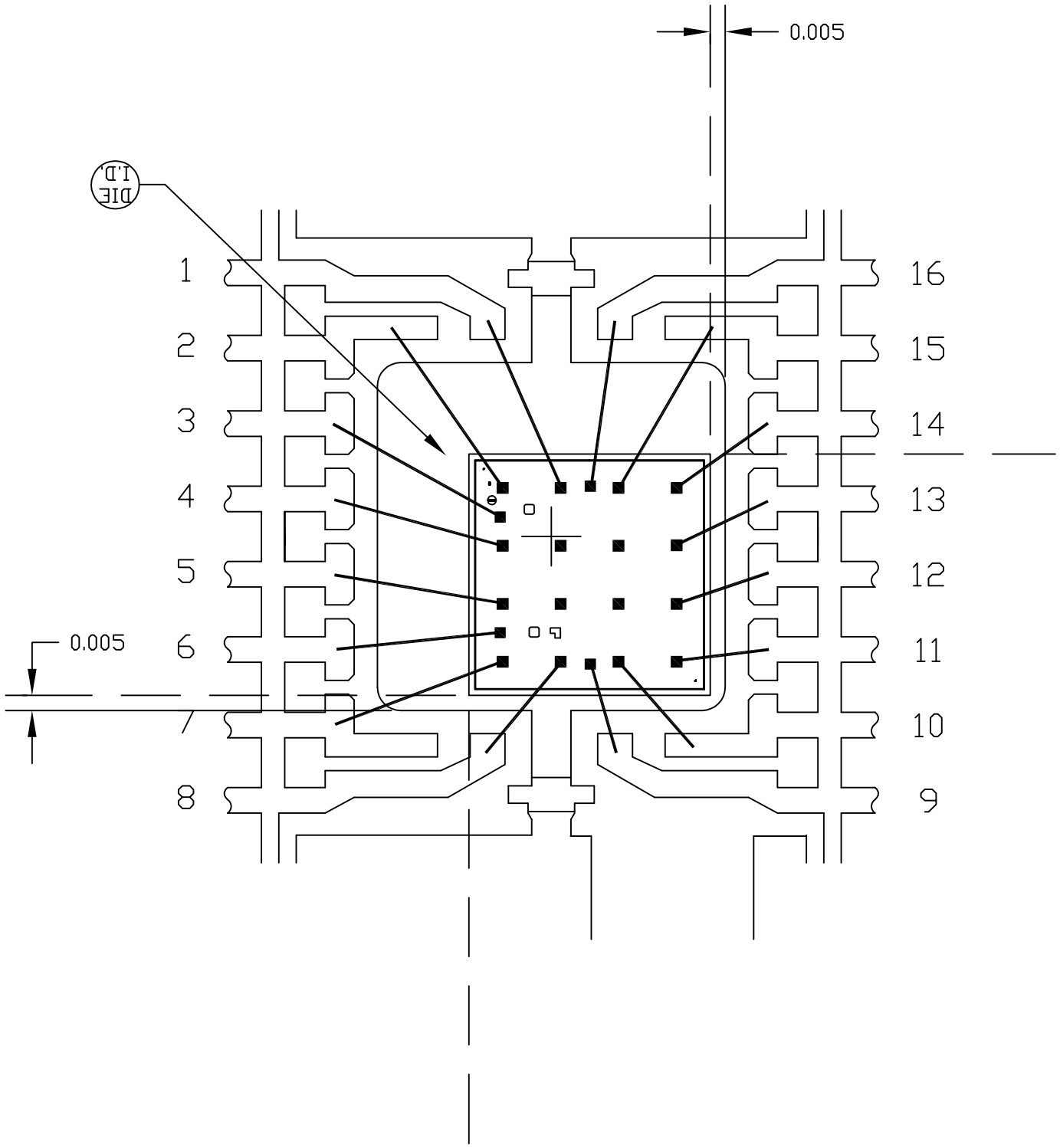
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

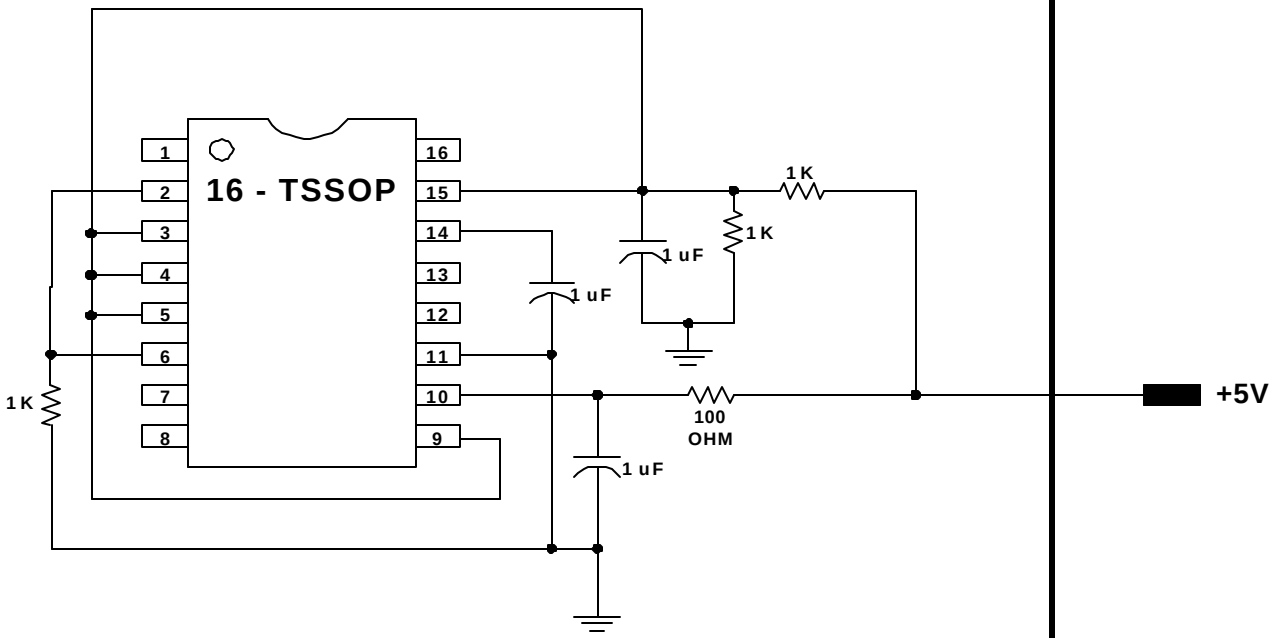



Mil Std 883D
Method 3015.7
Notice 8




| PKG. CODE: U16-2 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 118X118 | PKG. | | | BOND DIAGRAM #: 05-2601-0078 | REV: A |
| | DESIGN | | | | |

## ONCE PER SOCKET




## ONCE PER BOARD

**DEVICES: MAX 3341**

**MAX. EXPECTED CURRENT = 5mA**

**DRAWN BY: HAK TAN**

**NOTES:**