

RELIABILITY REPORT  
FOR  
**MAX3284EAUT**  
PLASTIC ENCAPSULATED DEVICES

January 27, 2004

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Manager, Reliability Operations

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX3284E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX3284E is a single receivers designed for RS-485 and RS-422 communication. This device guarantees data rates up to 52Mbps, even with a 3V power supply. Excellent propagation delay (15ns max) and package-to-package skew time (8ns max) makes this device ideal for multidrop clock distribution applications.

The MAX3284E has true fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are opened or shorted. The receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). This device features 1/4-unit-load receiver input impedance, allowing up to 128 receivers on the same bus.

The MAX3284E features a voltage logic pin that allows compatibility with low-voltage logic levels, as in digital FPGAs/ASICs. On the MAX3284E, the voltage threshold for a logic high is user-defined by setting  $V_L$  in the range from 1.65V to  $V_{CC}$ . The MAX3284E is also offered in a 6-pin SOT23 package

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(All Voltages Referenced to GND)	
Supply Voltage (VCC)	-0.3V to +6V
Control Input Voltage (EN, EN)	-0.3V to +6V
VL Input Voltage	-0.3V to +6V
Receiver Input Voltage (A, B)	-7.5V to +12.5V
Receiver Output Voltage (RO)	-0.3V to (VCC + 0.3V)
Receiver Output Voltage (RO) (MAX3284E)	-0.3V to (VL + 0.3V)
Receiver Output Short-Circuit Current	Continuous
Operating Temperature Range	
MAX3284EA_	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
6-Pin SOT23	696mW
Derates above +70°C	
6-Pin SOT23	8.7mW/°C

## II. Manufacturing Information

- A. Description/Function:  $\pm 15\text{kV}$  ESD-Protected 52Mbps, 3V to 5.5V, SOT23 RS-485/RS-422 True Fail-Safe Receivers
- B. Process: B8 (Standard 0.8 micron silicon gate CMOS)
- C. Number of Device Transistors: 233
- D. Fabrication Location: California, USA
- E. Assembly Location: Malaysia or Thailand
- F. Date of Initial Production: January, 2002

## III. Packaging Information

- A. Package Type: **6-Lead SOT**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-Filled Epoxy
- E. Bondwire: Gold (1 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-9000-0327
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

## IV. Die Information

- A. Dimensions: 43 x 35 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 0.8 microns (as drawn)
- F. Minimum Metal Spacing: 0.8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 320 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.39 \times 10^{-9}$$

$$\lambda = 3.39 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5876) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The RT33-3 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1000\text{V}$  per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX3284EAUT**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>PACKAGE</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		320	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

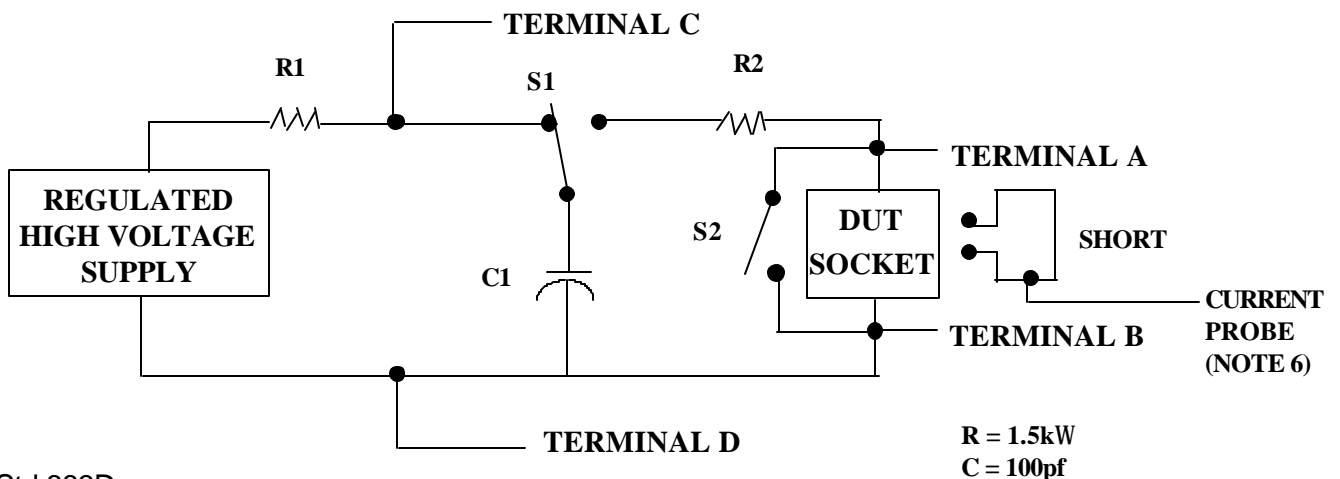
2/ No connects are not to be tested.

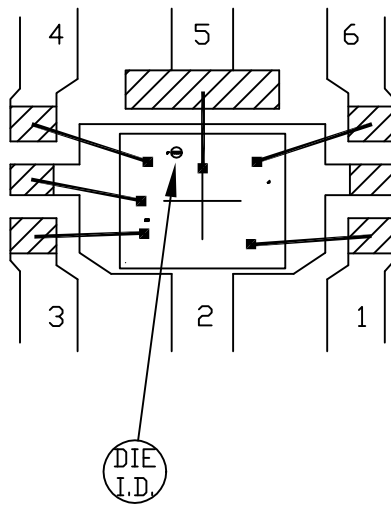
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



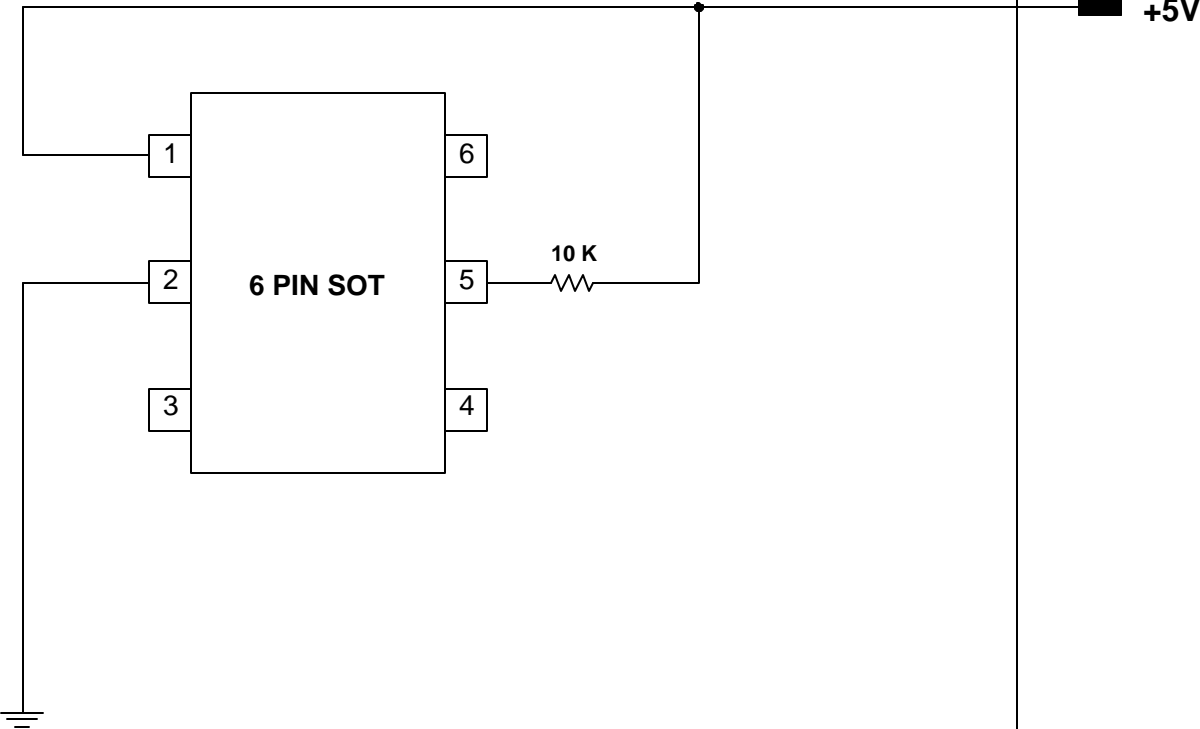


NOTE: CAVITY DOWN

PKG. CODE: U6-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x39	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0327	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 3281

DRAWN BY: TEK TAN

MAX. EXPECTED CURRENT = 12 mA

NOTES: