

RELIABILITY REPORT  
FOR  
**MAX3100xxx**  
PLASTIC ENCAPSULATED DEVICES

May 1, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX3100 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

## I. Device Description

### A. General

The MAX3100 universal asynchronous receiver transmitter (UART) is the first UART specifically optimized for small microcontroller-based systems. Using an SPI™/Microwire™ interface for communication with the host microcontroller (μC), the MAX3100 comes in a compact 16-pin QSOP. The asynchronous I/O is suitable for use in RS-232, RS-485, IR, and opto-isolated data links. IR-link communication is easy with the MAX3100's infrared data association (IrDA) timing mode.

The MAX3100 includes a crystal oscillator and a baud-rate generator with software-programmable divider ratios for all common baud rates from 300 baud to 230k baud. A software- or hardware-invoked shutdown lowers quiescent current to 10μA, while allowing the MAX3100 to detect receiver activity.

An 8-word-deep first-in/first-out (FIFO) buffer minimizes processor overhead. This device also includes a flexible interrupt with four maskable sources, including address recognition on 9-bit networks. Two hardware-handshaking control lines are included (one input and one output).

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V <sub>CC</sub> to GND	+6V
Input Voltage to GND (/CS, /SHDN, X1, /CTS, RX, DIN, SCLK)	-0.3V to (V <sub>CC</sub> + 0.3V)
Output Voltage to GND (DOUT, /RTS, TX, X2)	-0.3V to (V <sub>CC</sub> + 0.3V)
/IRQ	-0.3V to 6V
TX, /RTS Output Current	100mA
X2, DOUT, /IRQ Short-Circuit Duration (to V <sub>CC</sub> or GND)	Indefinite
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	667mW
Derates above +70°C	8.30mW/°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
14-Pin PDIP	800mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C
14-Pin PDIP	10.0mW/°C

## II. Manufacturing Information

A. Description/Function:	SPI™/Microwire™-Compatible UART
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	6848
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea, Malaysia, Philippines or Thailand
F. Date of Initial Production:	July, 1997

## III. Packaging Information

A. Package Type:	16-Lead QSOP	14-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0146	# 05-1901-0144
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

## IV. Die Information

A. Dimensions:	75 x 92 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Si
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5208) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The RS40 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250$ mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX3100xxx**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

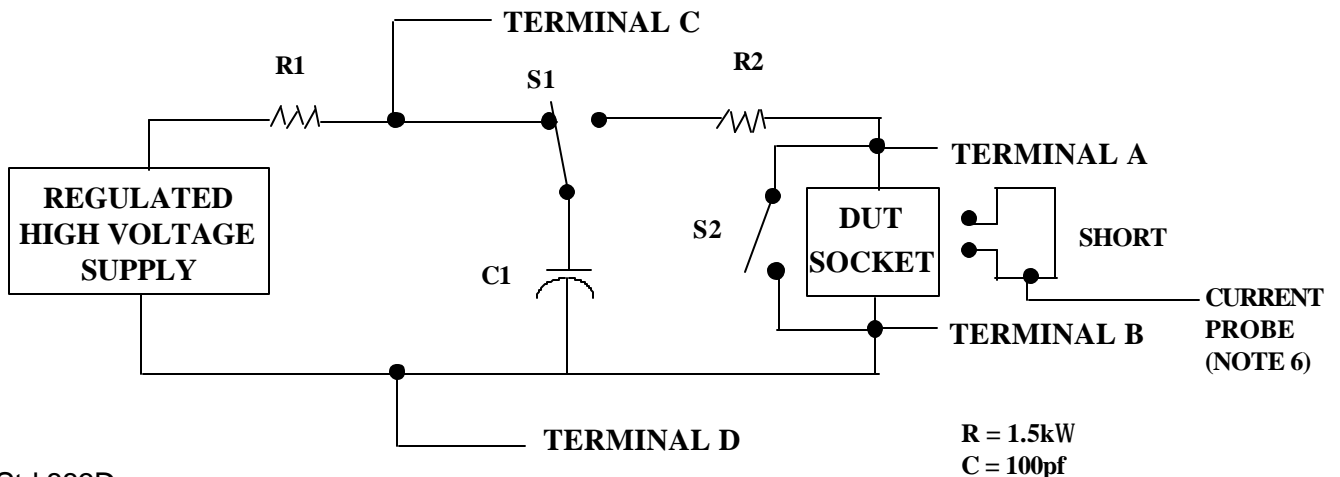
2/ No connects are not to be tested.

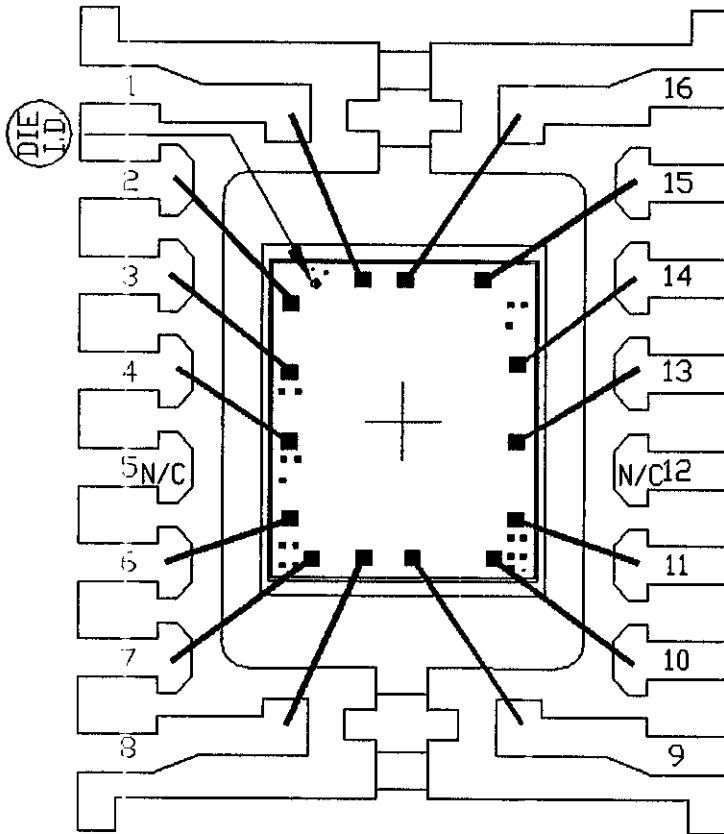
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E16-1

CAV./PAD SIZE:  
96X130

APPROVALS

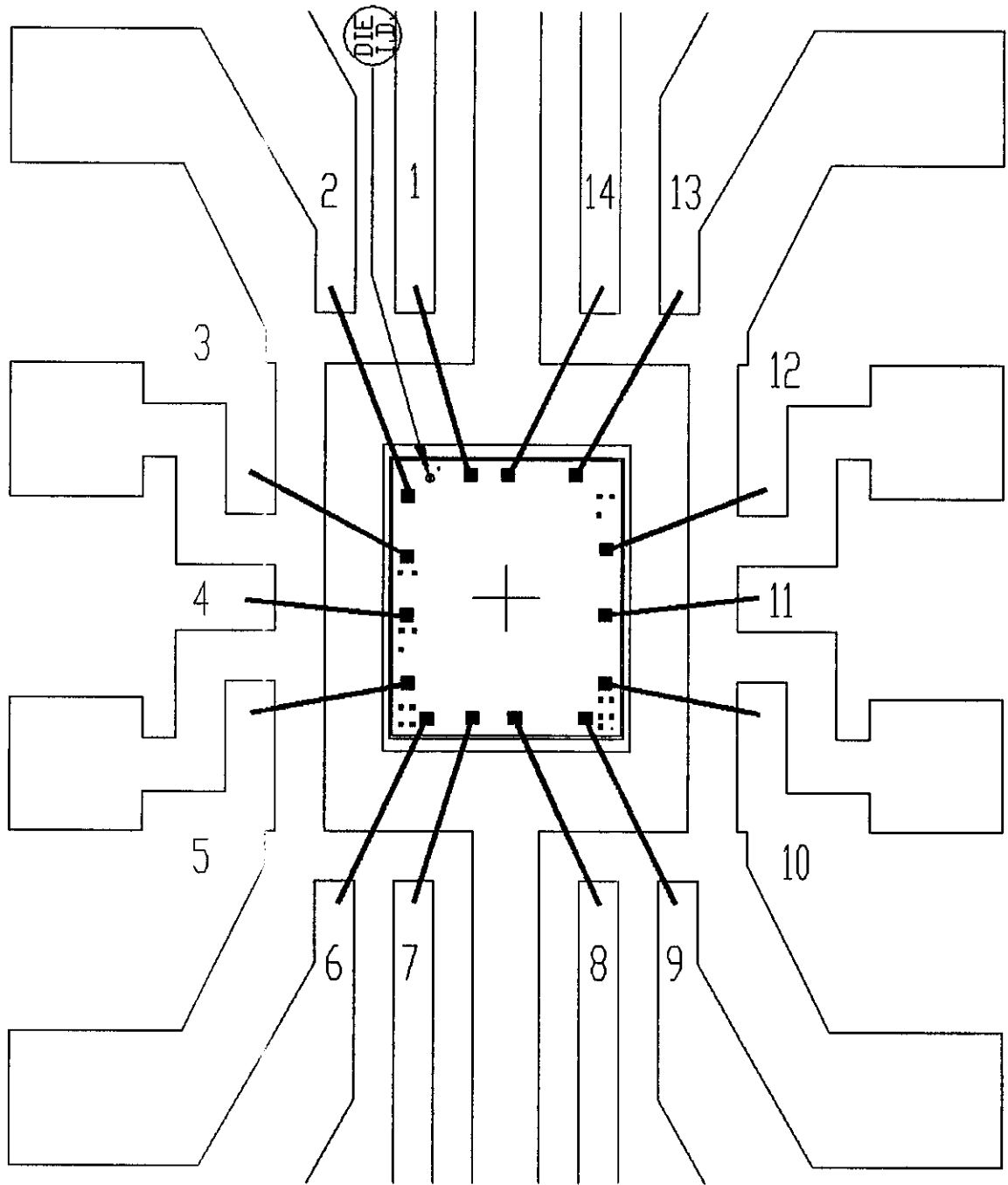
DATE

**MAXIM**

BUILDSHEET NUMBER:  
05-1901-0146

REV.:  
A

PKG.  
DESIGN



PKG.CODE: P14-3

APPROVALS

DATE



CAV./PAD SIZE:  
110 X 140

PKG.  
DESIGN

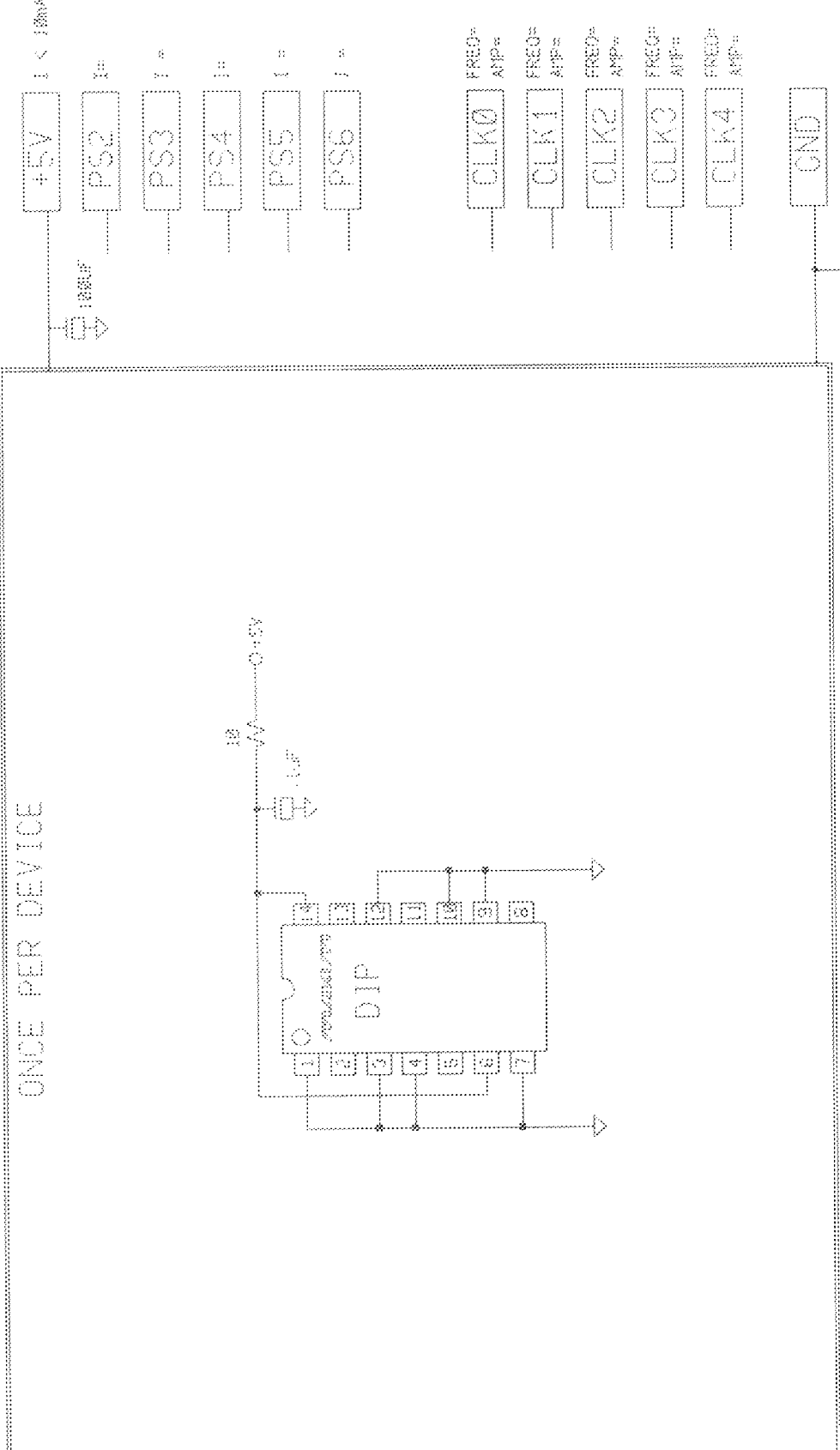
BUILDSHEET NUMBER:  
05-1901-0144

REV:  
A



ONCE PER BOARD

ONCE PER DEVICE



---STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD JMOS.  
 ---BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES :

1. TEMPERATURE : 125C OR EQUIVALENT
2. TIME : 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND INTERNAL PUST STAND 150C CONTINUOUS
4. APPROVED FOR EXJ COMMERCIAL EXJ HR/880

SPEC. NO. 06-5208 REV: A

MAXIM BURN-IN SCHEMATIC

DATE : 5/7/96

DEVICE TYPE(S) :

MAX3100

DRAWN BY :