RELIABILITY REPORT

FOR

MAX2701ECM

PLASTIC ENCAPSULATED DEVICES

February 12, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2701 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2701 is a highly integrated direct downconversion (zero-IF) receiver designed for wideband wireless local loop (WLL) systems operating in the 1.8GHz to 2.5GHz band. The MAX2701s' zero-IF architecture eliminates the need for IF downconversion stages and the use of an IF SAW filter. This reduces the overall receiver cost by reducing the component count and required board space.

The MAX2701 has three main blocks: low-noise amplifier (LNA), quadrature downconverter, and baseband variable gain amplifiers (VGAs). The LNA is a single-ended amplifier with selectable gain and shutdown options. It provides a high input third-order intercept point (IP3), which reduces cross-modulation and gain compression due to high-level RF interference. The quadrature downconverter section consists of two highly linear double-balanced mixers driven by an external local oscillator (LO) with a selectable LO doubler. The double-balanced mixers are optimized to provide high input IP3 and minimum added noise. The mixers' high input second-order intercept point (IIP2) helps minimize receiver desensitization due to high-level AM-modulated interferers.

The two baseband VGAs in each channel provide 80dB of total maximum gain and greater than 60dB of gain control. The first AGC amplifier is optimized for low noise, low power dissipation, and high linearity over the entire gain range to ensure high gain compression performance. An external lowpass filter between baseband VGAs provides the required channel selectivity at the adjacent channel. An integrated gain offset correction loop circuit provides <0.3dB amplitude mismatch between the I and Q channels.

The MAX2701 operate from a single +2.7V to +3.3V power supply, drawing only 165mA of supply current and 20µA in shutdown mode. The device is available in small 48-pin TQFP packages with exposed paddle (EP) for optimum high-frequency performance.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6V
RF Signals: PRFIN, PLNAIN, PLO	+15dBm
Baseband Signals	
IIN1+ to IIN1-, IIN2+ to IIN2-,QIN1+ to QIN1-, QIN2+ to QIN2-	±2V
Input Voltages	
AGC, GAIN_SET, SHDN , X2_EN ,CEXT_, RFIN_, LO, LNAIN, IIN_ _, QIN_ _ , DCI_ _ , DCQ_ _ to GND	-0.3V to (VCC + 0.3V)
Input Current	
AGC	±50mA
All Digital Inputs	±10mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
48-Pin TQFP-EP	2000mW
Derates above +70°C	
48-Pin TQFP-EP	27mW/°C

II. Manufacturing Information

A. Description/Function:	1.8GHz to 2.5GHz Direct Downconversion Receivers
B. Process:	GST3
C. Number of Device Transistors:	3307
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	April, 2000

III. Packaging Information

A. Package Type:	**48-Lead TQFP-EP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-7001-0384
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 3

IV. Die Information

A. Dimensions:	98 x 98 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 2.8; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.3; Metal2: 1.2; Metal3: 2.6; Metal4: 2.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.11 \times 10^{-8}$ $\lambda = 10.11$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR47-2 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX2701ECM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

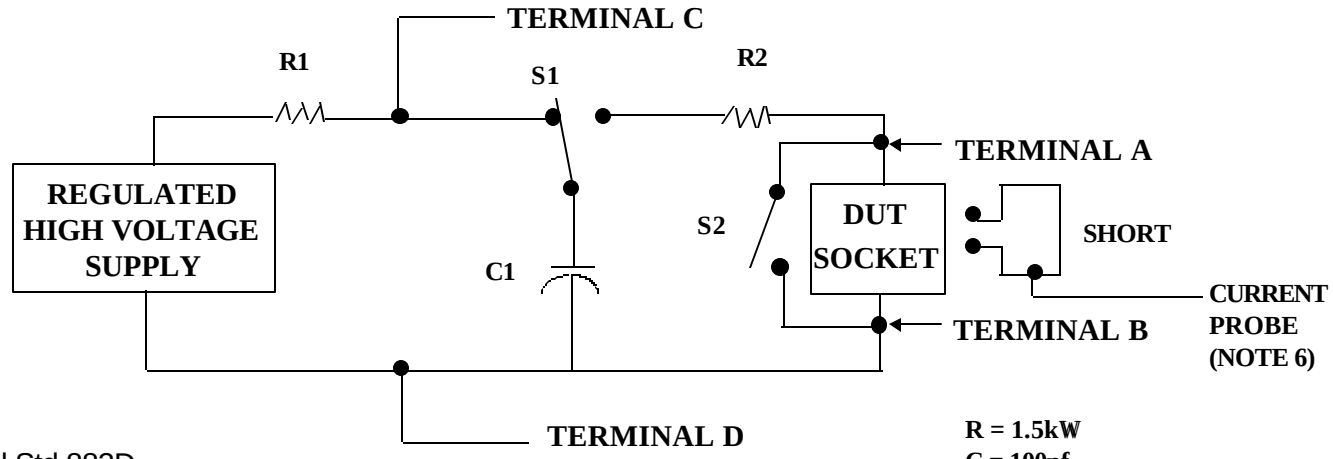
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

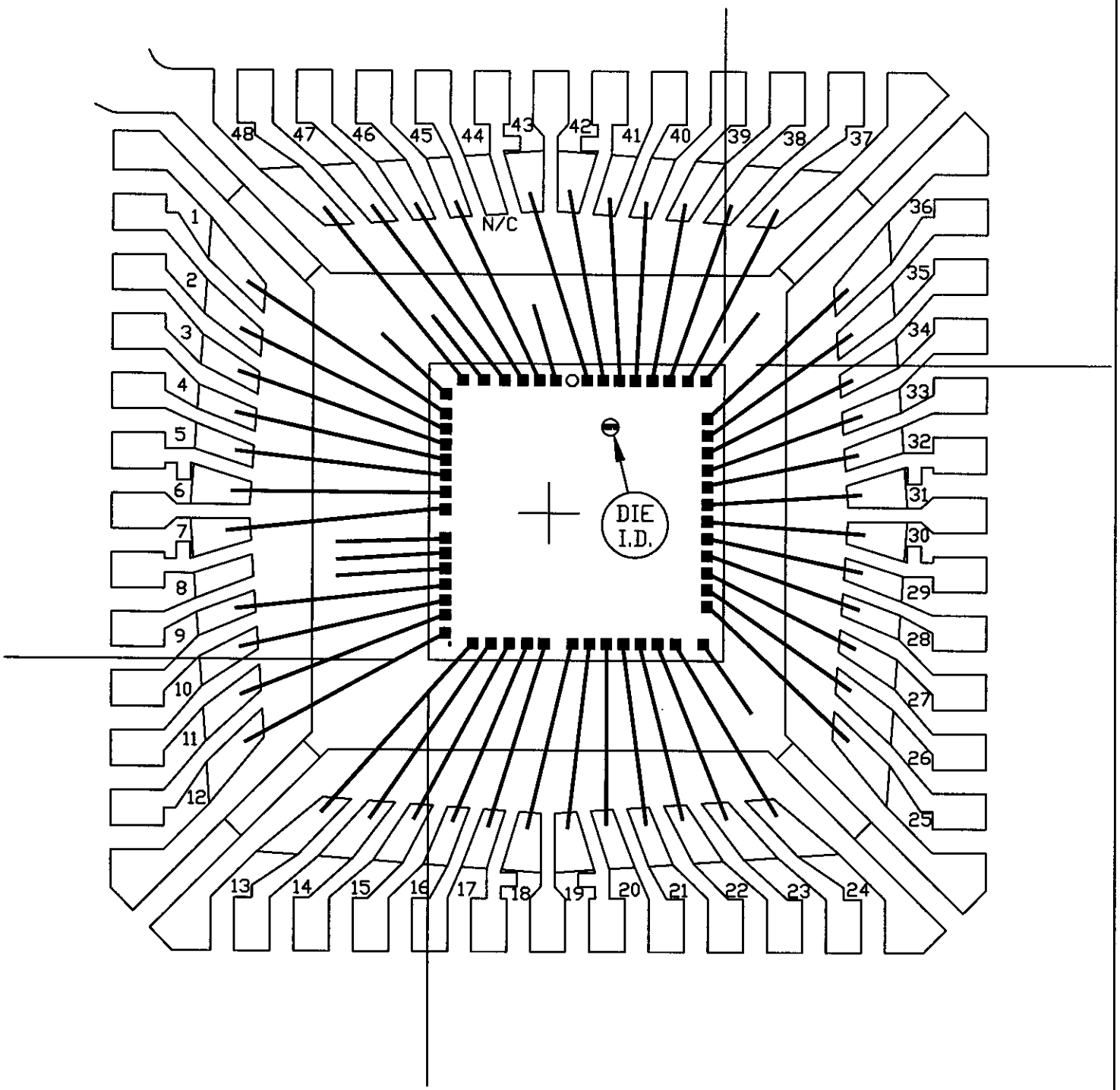
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



NOTES:
1. OFFSET DIE 9 MILS. TO RIGHT AS SHOWN.
2. DOWNBONDS BETWEEN LEADS 7 & 9 MUST BE AT LEAST 35 MILS OR GREATER LENGTH.

PKG.CODE: C48E-7		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 157x157	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0384 / REV.: B