RELIABILITY REPORT

FOR

MAX24104ELT+T

WAFER LEVEL DEVICES

November 12, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineering

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Conclusion

The MAX24104ELT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX24104 restores high-frequency signal level at the decision-feedback equalizer (DFE) receiver for high-loss backplane and cable channels. This permits the DFE receiver to meet BER goals. At 15Gbps, the MAX24104 can operate in channels with FR4 and cable HF loss of more than 30dB at 7.5GHz. The linear transfer function is transparent to Adaptive DFE equalizers, permitting DFE adaptation to track temperature and changing channel conditions. Together with the DFE, integrated into Serializer/Deserializer (SERDES), the device adds increased margin rather than full signal regeneration. Unlike conventional equalizers with limiting output stages, the device preserves the linear channel characteristics, allowing the DFE to operate linearly over the entire channel. This permits extending total channel reach and/or improving signal-to-noise ratio (SNR). The device typically compensates for up to 19dB of the total loss in a long channel, effectively reducing the channel length seen by the DFE receiver. The device has four channels and is packaged in a space-saving, 4mm x 6.5mm, FCLGA package.

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II. Manufacturing Information

A. Description/Function:	15Gbps Quad Linear Equalizer
B. Process:	SBC18
C. Number of Device Transistors:	8099
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	October 16, 2014

III. Packaging Information

A. Package Type:	34-pad thin LGA; flip chip
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-5697
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	N/A°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	73.6614 X 134.4882 mils
B. Passivation:	Si_3N_4/SiO_2
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 159 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.1 \times 10^{-9}$

λ = 7.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the SBC18 Process results in a FIT Rate of 0.04 @ 25°C and 0.69 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot KAKV1AQ, D/C 1324)

The HQ39-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/-2000V per JEDEC JESD22-A114
ESD-CDM: +/- 250V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX24104ELT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	159	0	KAKV1AQ, D/C 1325

Note 1: Life Test Data may represent plastic DIP qualification lots.

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