RELIABILITY REPORT

FOR

MAX2326EUP

PLASTIC ENCAPSULATED DEVICES

August 16, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX2326 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX2320/MAX2321/MAX2322/MAX2324/MAX2326/MAX2327/MAX2329 high-performance SiGe receiver front-end ICs set a new industry standard for low noise and high linearity at a low supply current. This family integrates a variety of unique features such as an LO frequency doubler and divider, dual low-noise amplifier (LNA) gain settings, and a low-current paging mode that extends the handset standby time.

The MAX2320 family includes seven ICs: four operate at both cellular and PCS frequencies, one operates at cellular frequencies, one at PCS frequencies, and one is configured as a dual PCS device (see *Selector Guide*). Each part includes an LNA with a high input third-order intercept point (IIP3) to minimize intermodulation and cross-modulation in the presence of large interfering signals. In low-gain mode, the LNA is bypassed to provide higher cascaded IIP3 at a lower current. For paging, a low-current, high-gain mode is provided.

The CDMA mixers in cellular and PCS bands have high linearity, low noise, and differential IF outputs. The FM mixer is designed for lower current and a single-ended output.

All devices come in a 20-pin TSSOP-EP package with exposed paddle and are specified for the extended temperature range (-40°C to +85°C).

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +4.3V
Digital Input Voltage to GND	-0.3V to (VCC + 0.3V)
RF Input Signals	1.0V peak
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP-EP (derate 80mW/°C above +70°C)	6.4W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	Adjustable, High-Linearity, SiGe Dual-Band LNA/Mixer ICs
B. Process:	GST3
C. Number of Device Transistors:	1315
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	July, 1999

III. Packaging Information

A. Package Type:	20-Pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2201-0016
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	57 x 41 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 2.8; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.3; Metal2: 1.4; Metal3: 2.6; Metal4: 2.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 45 \times 2}$$

1.83: (Chi square value for MTTF upper limit)

192 x 9706 x 45 x 2: Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.93 \times 10^{-8}$ $\lambda = 10.93$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B3A**). Current monitor data for the GST3 Process results in a FIT Rate of 0.23 @ 25C and 3.99 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR49 die type has been found to have all pins able to withstand a transient pulse of +/-250V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2326EUP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

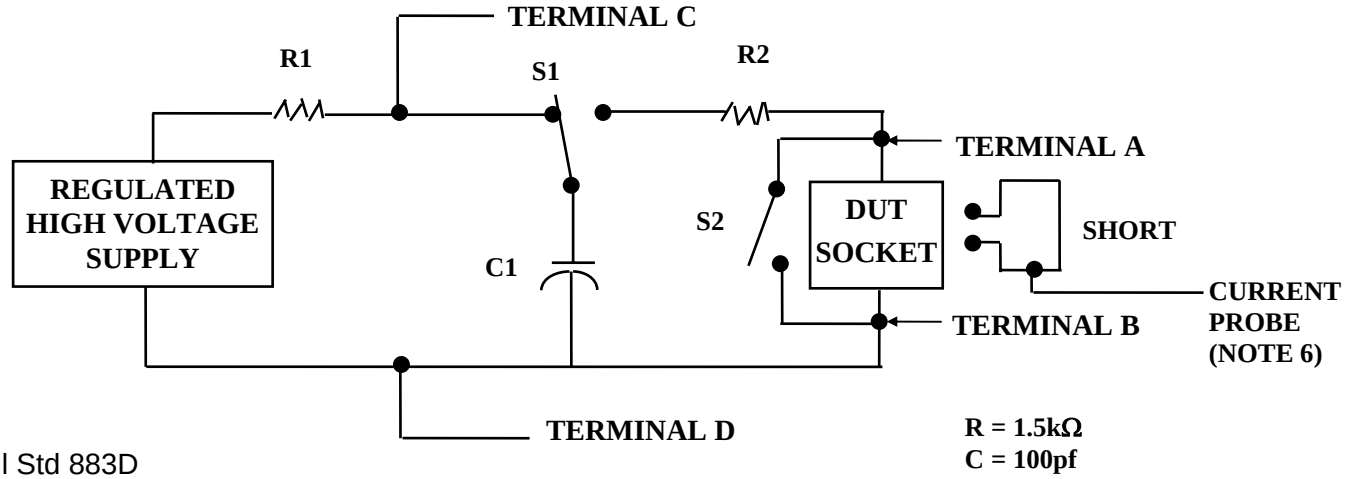
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

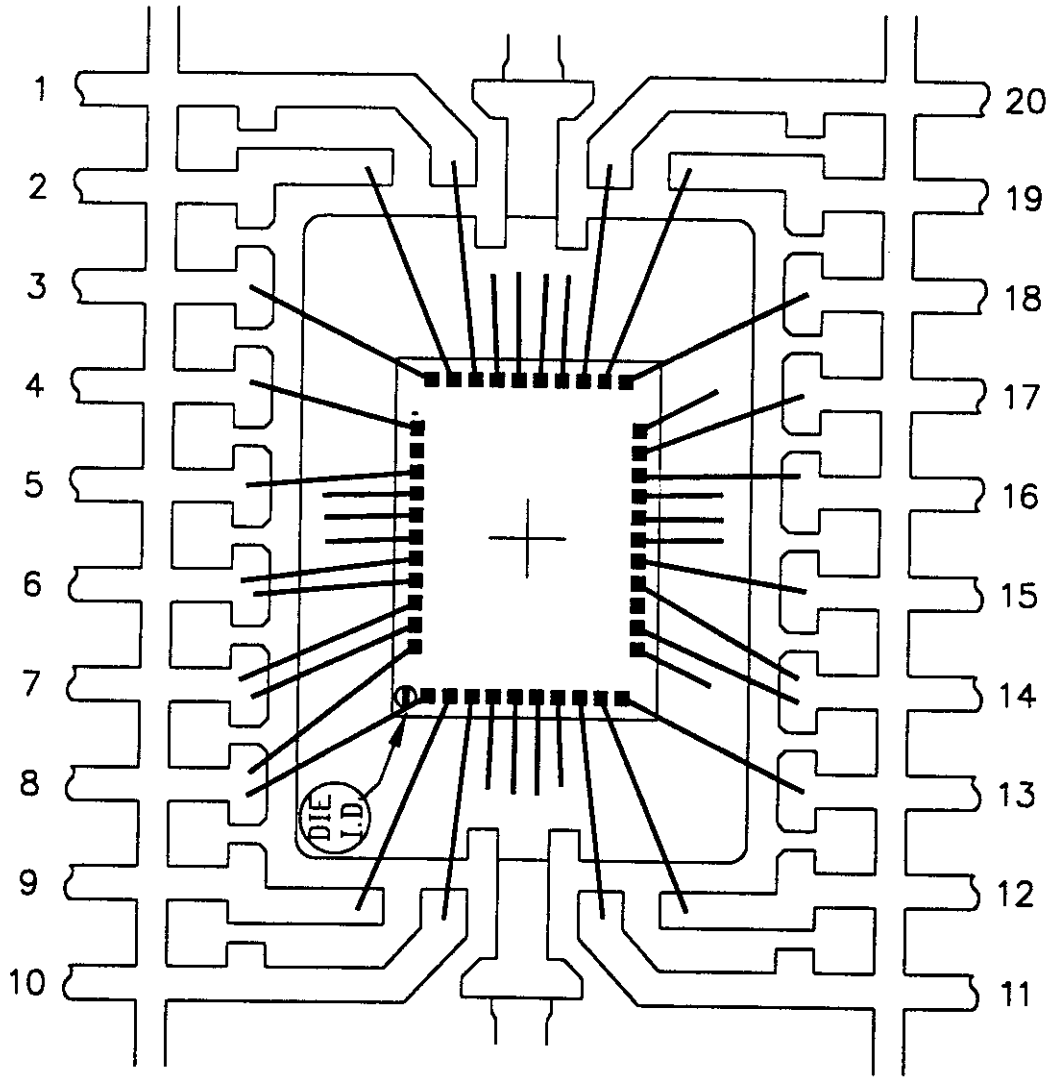
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: U20E-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118x165	PKG. DESIGN			BUILDSHEET NUMBER: 05-2201-0016 / REV.: B