

RELIABILITY REPORT
FOR
MAX207ExxG
PLASTIC ENCAPSULATED DEVICES

January 28, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX207E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX207E line driver/reciever is designed for RS-232 and V.28 communication in harsh environments. Each transmitter output and receiver input is protected against $\pm 15\text{kV}$ electrostatic discharge (ESD) shocks, without latchup. This device has four drivers and three receivers. The drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX207E operates with four $0.1\mu\text{F}$ capacitors, reducing cost and board space.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V_{CC}	-0.3V to +6V
V+	($V_{CC} - 0.3\text{V}$) to +14V
V-	-14V to +0.3V
Input Voltages	
T_IN	-0.3V to (V+ +0.3V)
R_IN	$\pm 30\text{V}$
Output Voltages	
T_OUT	(V- -0.3V) to (V+ +0.3V)
R_OUT	-0.3V to ($V_{CC} + 0.3\text{V}$)
Short Circuit Duration, T_OUT	Continuous
Storage Temp.	-65°C to +165°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin SO	941mW
24-Pin SSOP	640mW
24-Pin NPDIP	1.07W
Derates above +70°C	
24-Pin SO	11.76mW/°C
24-Pin SSOP	8.00mW/°C
24-Pin NPDIP	13.33mW

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected, +5V RS-232 Transceiver
B. Process:	MG2 (5 micron metal gate CMOS)
C. Number of Device Transistors:	328
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Korea
F. Date of Initial Production:	April, 1996

III. Packaging Information

A. Package Type:	24-Lead SSOP	24-Lead SO	24-Lead PDIP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0130	# 05-1901-0129	# 05-1901-0128
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	144x181 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 100 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9}$$

$$\lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0264) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RS39-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX207E has achieved $\pm 15\text{kV}$ ESD protection using both methods 3015 and IEC 801-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX207ExxG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO	77	0
			SSOP	77	0
			NPDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.

Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

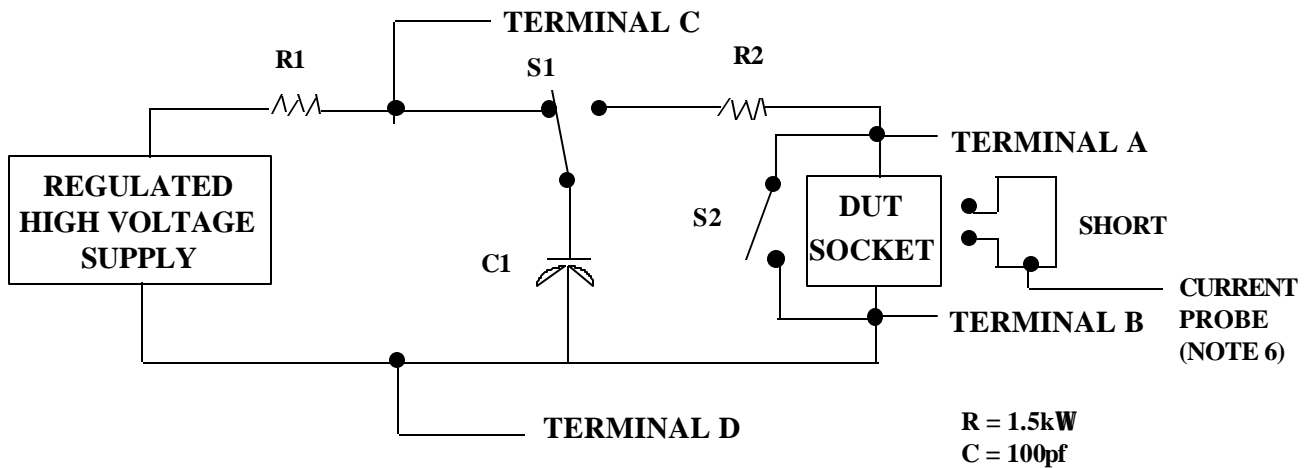
1/ Table II is restated in narrative form in 3.4 below.

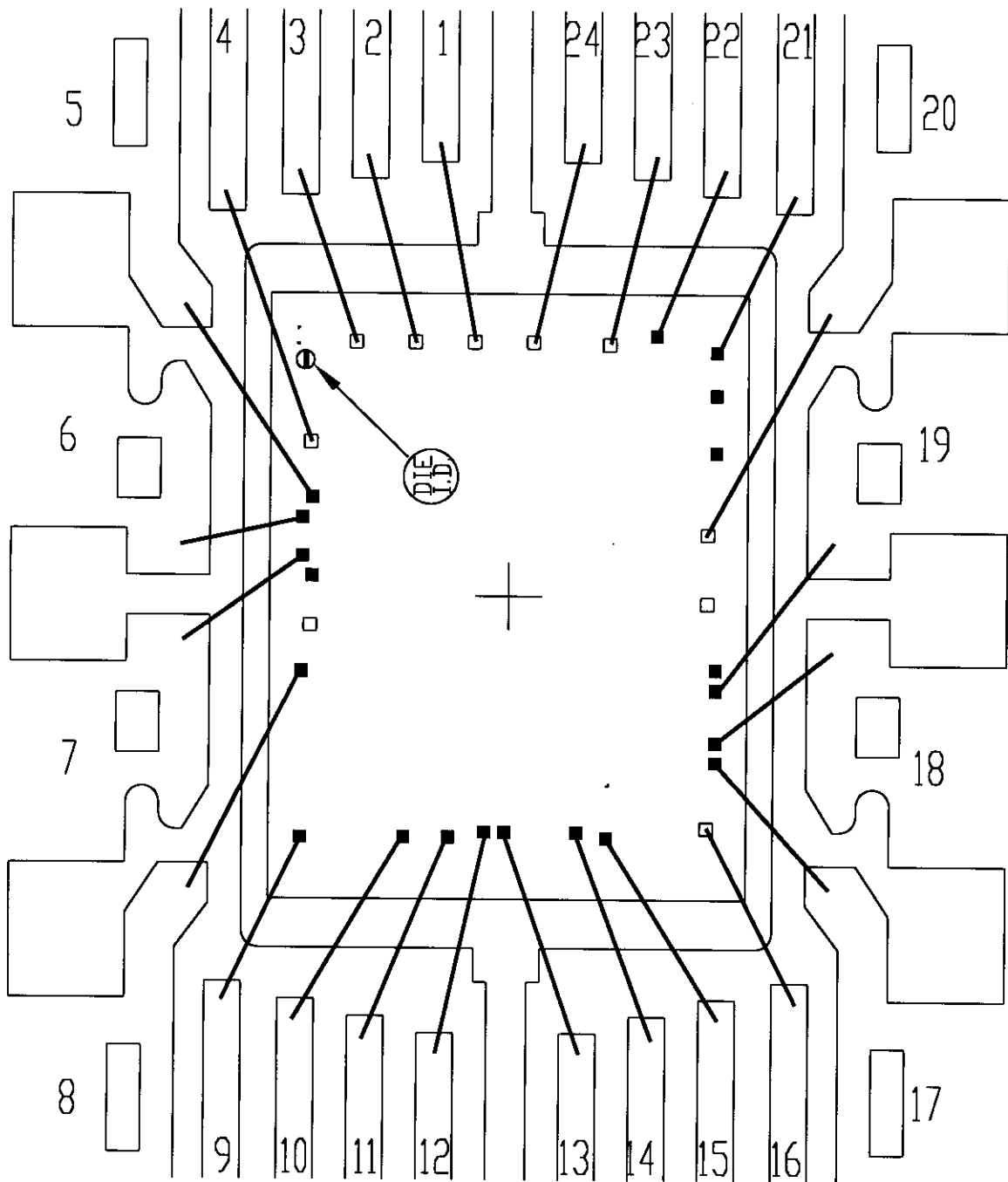
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: N24-3

CAV./PAD SIZE:
160 X 210

PKG.
DESIGN

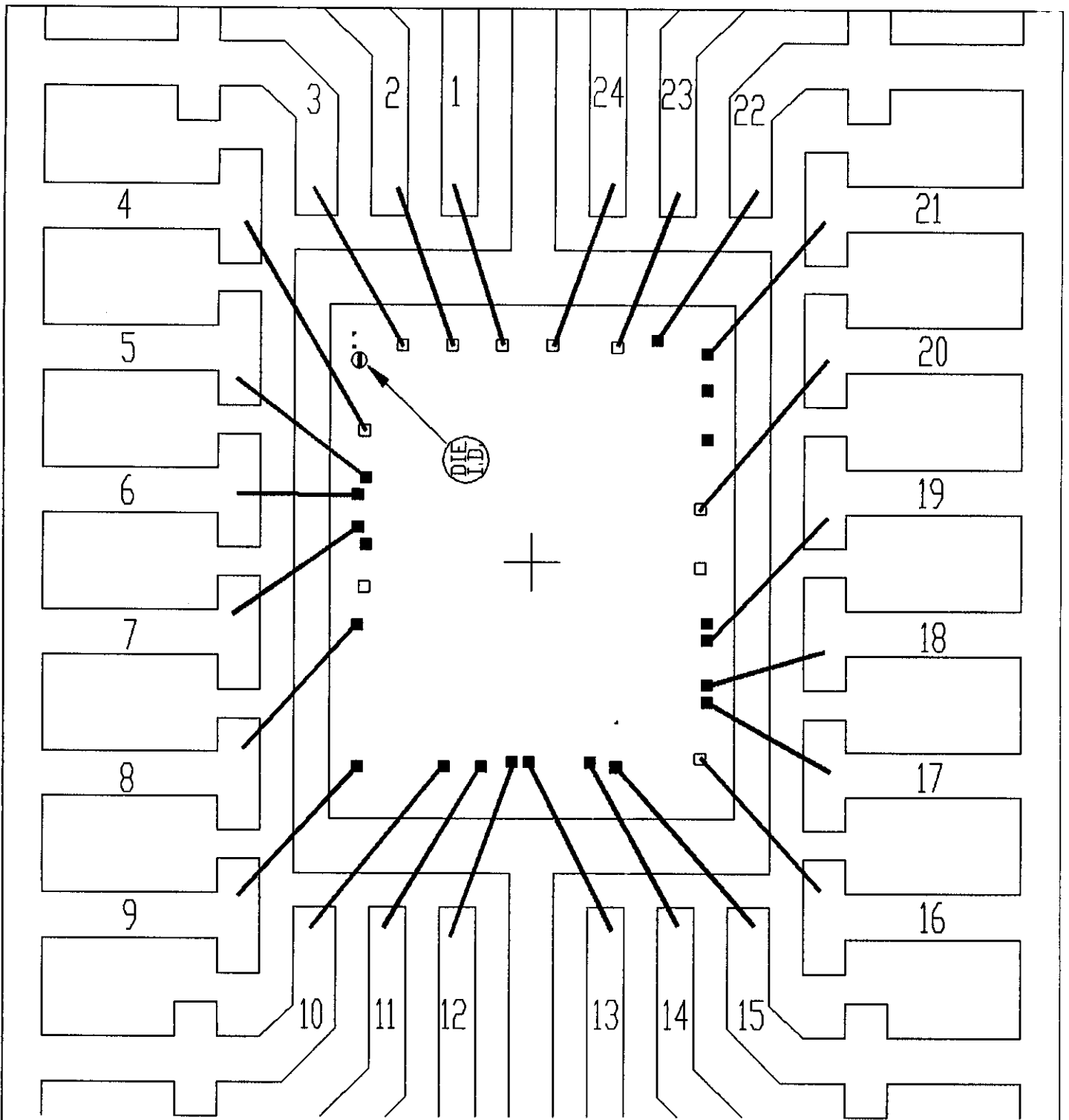
APPROVALS

DATE

MAXIM

BUILDSHEET NUMBER:
05-1901-0128

REV.:
B



PKG.CODE: W24-2

CAV./PAD SIZE: 170 X 220

PKG.
DESIGN

APPROVALS

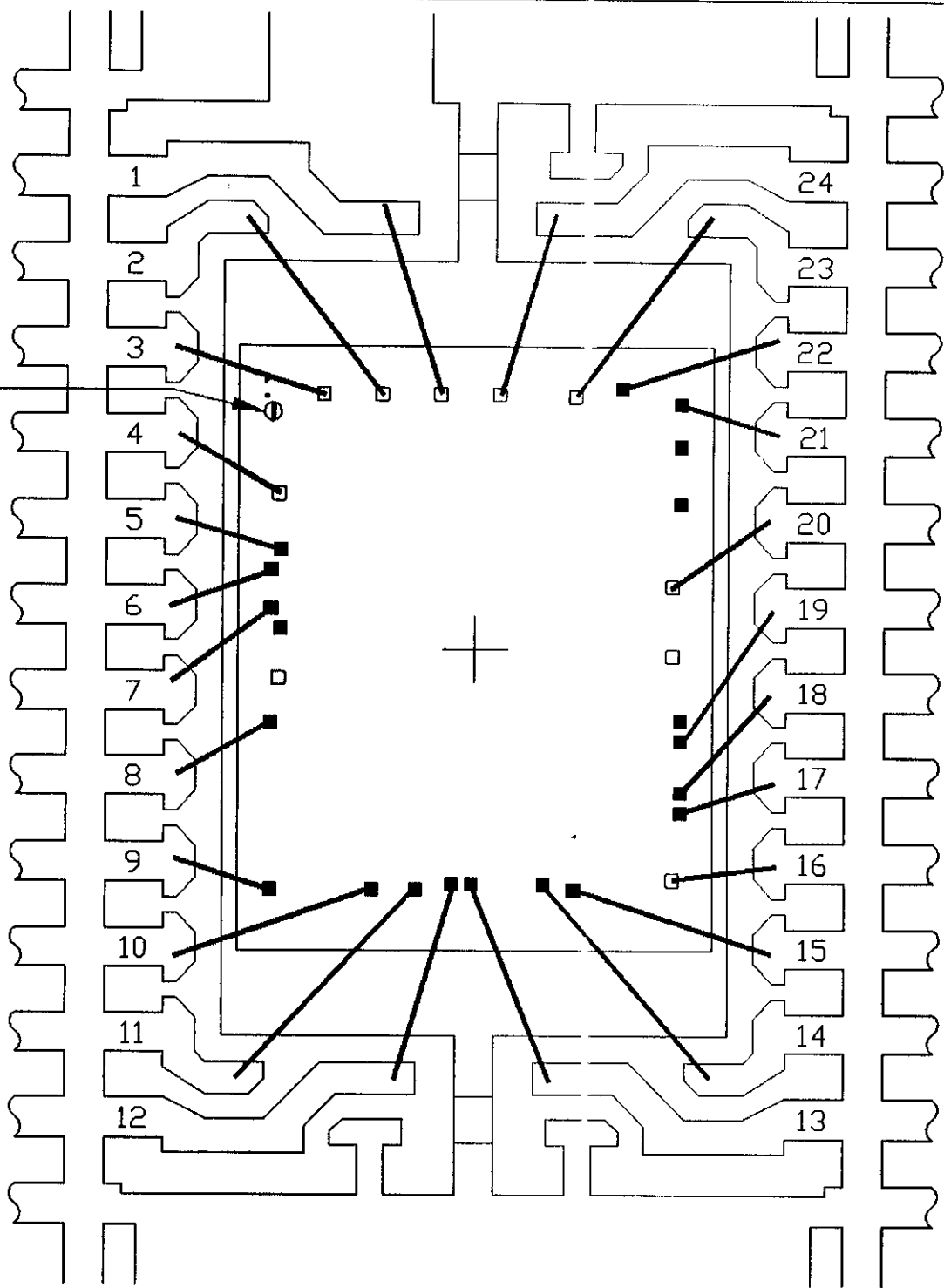
DATE



BUILDSHEET NUMBER:
05-1901-0129

REV:
A

PIE
T.D.



PKG.CODE: A24-3

CAV./PAD SIZE:
154X232

APPROVALS

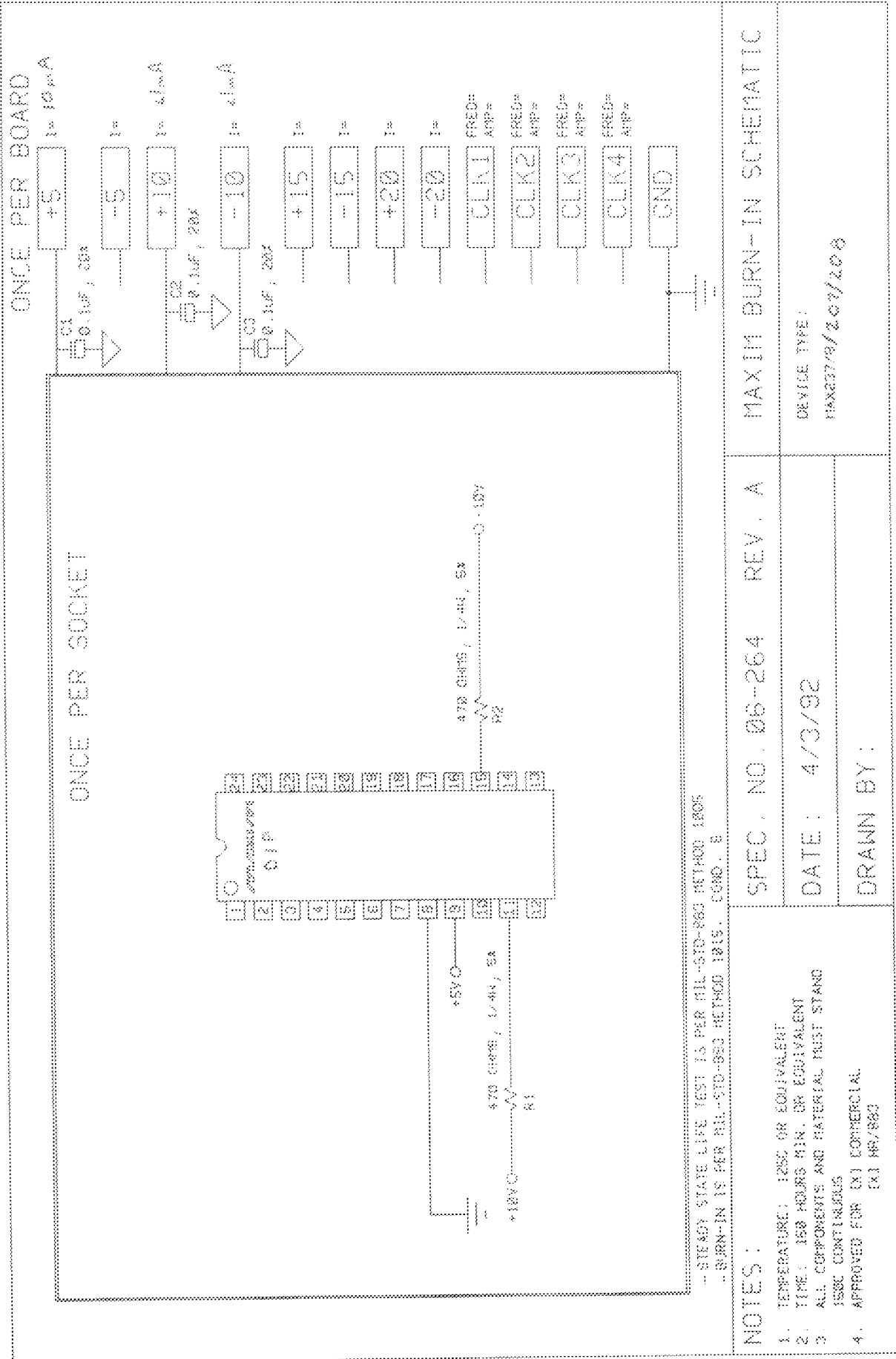
DATE

MAXIM

BUILDSHEET NUMBER:
05-1901-0130

REV.:
A

PKG.
DESIGN



SPEC. NO. 06-264 REV. A

MAXIM BURN-IN SCHEMATIC

DATE: 4/3/92

DEVICE TYPE:

MAX837A/201/208

DRANN BY: