RELIABILITY REPORT

FOR

MAX19794ETX+T

PLASTIC ENCAPSULATED DEVICES

August 1, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX19794ETX+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX19794 dual general-purpose analog voltage variable attenuator (VVA) is designed to interface with 50 systems operating in the 10MHz to 500MHz frequency range. This device includes a patented control circuit that provides 22.4dB of attenuation range (per attenuator) with a typical linear control slope of 8dB/V. Both attenuators share a common analog control. They can be cascaded together to yield 44.7dB of total attenuation range with a typical combined linear control slope of 16dB/V (5V operation). Alternatively, the on-chip, 4-wire SPI-controlled 10-bit DAC can be used to control both attenuators. In addition, a step-up/down feature allows user-programmable attenuator stepping through command pulses without re-programming the SPI interface. The MAX19794 is a monolithic device designed using one of Maxim's proprietary SiGe BiCMOS processes. The part operates from a single +5V supply or alternatively operates from a single +3.3V supply. It is available in a compact 36-pin TQFN package (6mm x 6mm x 0.8mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +100°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	10MHz to 500MHz Dual Analog Voltage Variable Attenuator with On-Chip 10-Bit SPI-Controlled DAC
B. Process:	MB3
C. Number of Device Transistors:	22862
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	June 29, 2012

III. Packaging Information

A. Package Type:	36-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (0.8 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-4867
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	38°C/W
J. Single Layer Theta Jc:	1.4°C/W
K. Multi Layer Theta Ja:	28°C/W
L. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	108.2677X130.7086 mils
B. Passivation:	BCB
C. Interconnect:	Al with top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.58 \times 10^{-9}$

$\lambda = 4.58$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The CR61-3 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX19794ETX+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	240	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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