RELIABILITY REPORT

FOR

MAX1854EEG

PLASTIC ENCAPSULATED DEVICES

May 7, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX1854EEG successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1716/MAX1854/MAX1855 step-down controllers are intended for core CPU DC-DC converters in notebook computers. They feature a dynamically adjustable output (5-bit DAC), ultra-fast transient response, high DC accuracy, and high efficiency needed for leading-edge CPU core power supplies. Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency. The MAX1716/MAX1854/MAX1855 are designed specifically for CPU core applications requiring a voltage-positioned supply. The voltage-positioning input (VPS), combined with a high DC accuracy control loop, is used to implement a power supply that modifies its output set point in response to the load current. This arrangement decreases full-load power dissipation and reduces the required number of output capacitors. The 28V input range of the MAX1716/MAX1854/MAX1855 enables single-stage buck conversion from high-voltage batteries for the maximum possible efficiency. Alternatively, the devices' high-frequency capability combined with two-stage conversion (stepping down the +5V system supply instead of the battery) allows the smallest possible physical size. The output voltage can be dynamically adjusted through the 5-bit digital-to-analog converter (DAC) inputs. The MAX1716/MAX1854/MAX1855 are available in a 24-pin QSOP package. For applications requiring SpeedStep® power control (see the MAX1717).

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II. Manufacturing Information

A. Description/Function:	High-Speed, Adjustable, Synchronous Step-Down Controllers with Integrated Voltage Positioning
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Malaysia, Philippines, or Thailand
F. Date of Initial Production:	July 22, 2000

III. Packaging Information

A. Package Type:	24-pin QSOP
B. Lead Frame:	Copper
C. Lead Finish:	85Sn/15Pb plate
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2301-0047
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	105°C/W
K. Single Layer Theta Jc:	34°C/W
L. Multi Layer Theta Ja:	88°C/W
M. Multi Layer Theta Jc:	34°C/W

IV. Die Information

A. Dimensions:	105 X 86 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.02 @ 25C and 0.33 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot NORBCA004A D/C 0209, Latch-up lot IORCBQ001B D/C 0026)

The PY43-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX1854EEG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	IORBBQ001B, D/C 0026

Note 1: Life Test Data may represent plastic DIP qualification lots.

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