MAX1845Exx
Rev. A

RELIABILITY REPORT

FOR

MAX1845Exx

PLASTIC ENCAPSULATED DEVICES

April 17, 2003

MAXIM INTEGRATED PRODUCTS

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SUNNYVALE, CA 94086

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Conclusion

The MAX1845 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1845 is a dual PWM controller configured for step-down (buck) topologies that provides high efficiency, excellent transient response, and high DC output accuracy necessary for stepping down high-voltage batteries to generate low-voltage chipset and RAM power supplies in notebook computers. The CS_ inputs can be used with low-side sense resistors to provide accurate current limits or can be connected to LX_, using low-side MOSFETs as current-sense elements. The on-demand PWM controllers are free running, constant on-time with input feed-forward. This configuration provides ultra-fast transient response, wide input-output differential range, low supply current, and tight load-regulation characteristics. The MAX1845 is simple and easy to compensate.

Single-stage buck conversion allows the MAX1845 to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery at a higher switching frequency) allows the minimum possible physical size.

The MAX1845 is intended for generating chipset, DRAM, CPU I/O, or other low-voltage supplies down to 1V. For a single-output version, refer to the MAX1844 data sheet. The MAX1845 is available in 28-pin QSOP and 36-pin thin QFN packages.

B. Absolute Maximum Ratings (Note 1)

Item	Rating
V+ to AGND	-0.3 to +30V
VCC to AGND	-0.3V to +6V
VDD to PGND	-0.3V to +6V
AGND to PGND	-0.3V to +0.3V
PGOOD, OUT_ to AGND	-0.3V to +6V
OVP, UVP, ILIM_, FB_, REF,SKIP, TON, ON_ to AGND	-0.3V to (VCC + 0.3V)
DL_ to PGND	-0.3V to (VDD + 0.3V)
BST_ to AGND	-0.3V to +36V
CS_ to AGND	-6V to +30V
DH1 to LX1	-0.3V to (VBST1 + 0.3V)
LX_ to BST_	-6V to +0.3V
DH2 to LX2	-0.3V to (VBST2 + 0.3V)
REF Short Circuit to GND	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QSOP	860mW
36-Pin QFN (6 x 6)	2105mW
Derates above +70°C	
28-Pin QSOP	10.8W/°C
36-Pin QFN (6 x 6)	26.3mW/°C

Note 1: For the MAX1845EEI, AGND and PGND refer to a single pin designated GND.

II. Manufacturing Information

A. Description/Function:	Dual, High-Efficiency, Step-Down Controller with Accurate Current Limit
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	4795
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Malaysia, Thailand, Philippines or USA
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**28-Pin QSOP**	**36-Pin QFN (6x6)**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05- 2301-0087	# 05- 9000-0514
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	83 x 153mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°Cbiased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(4389:) Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

λ = 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5671) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PY74 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX1845Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP QFN(6x6)	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

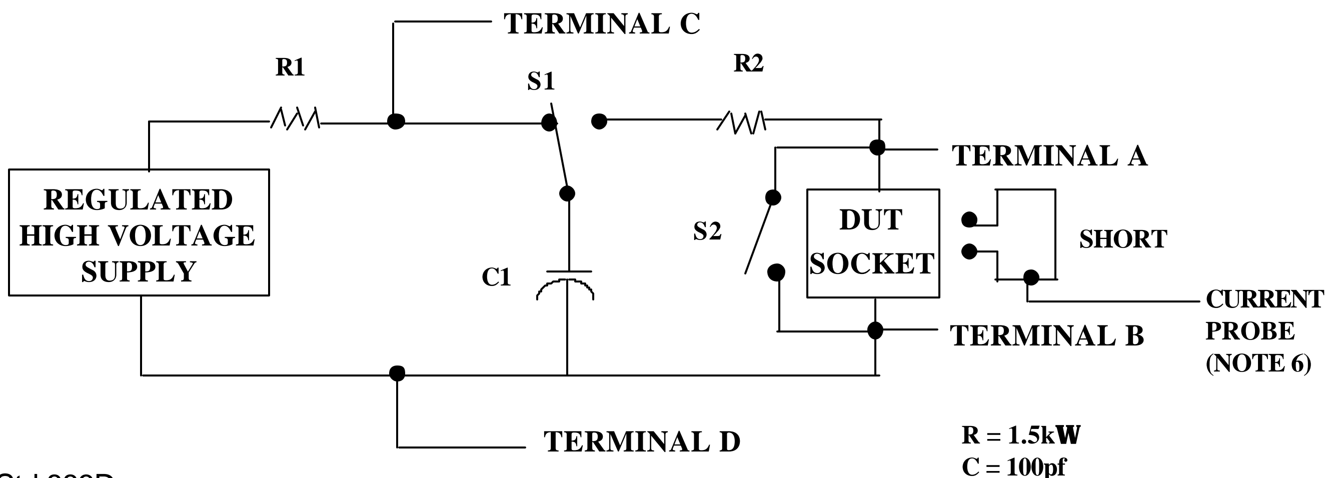
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

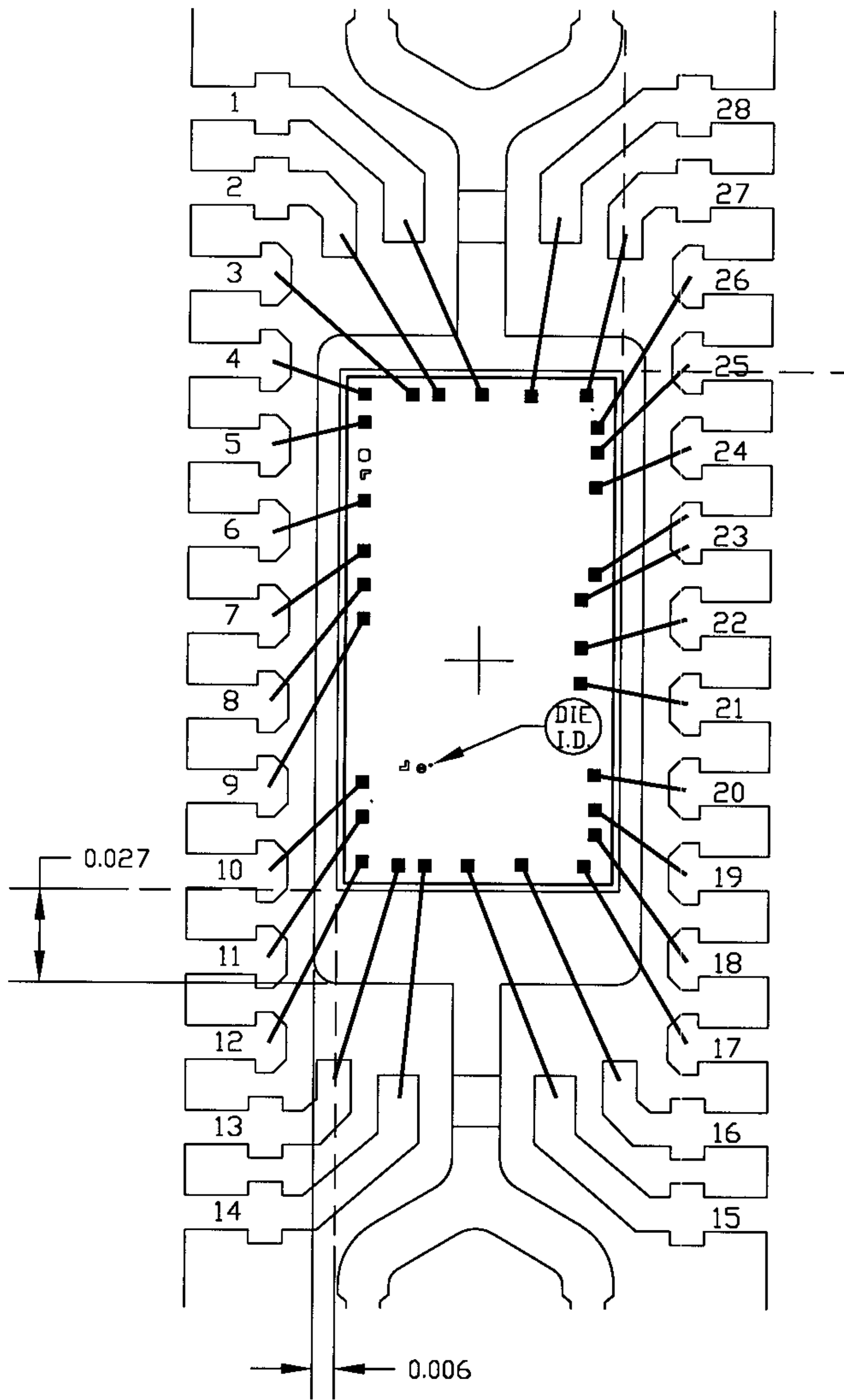
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E28-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG.			BOND DIAGRAM #: 05-2301-0087	REV: A
	DESIGN				

6x6x0.8mm QFN THIN PKG.

EXPOSED PAD PKG.

N/C 36 35 34 33 32 31 30 N/C 29 28

1 2 3 4 5 N/C 6 7 8 N/C 9

27 26 25 N/C 24 23 22 21 20 19

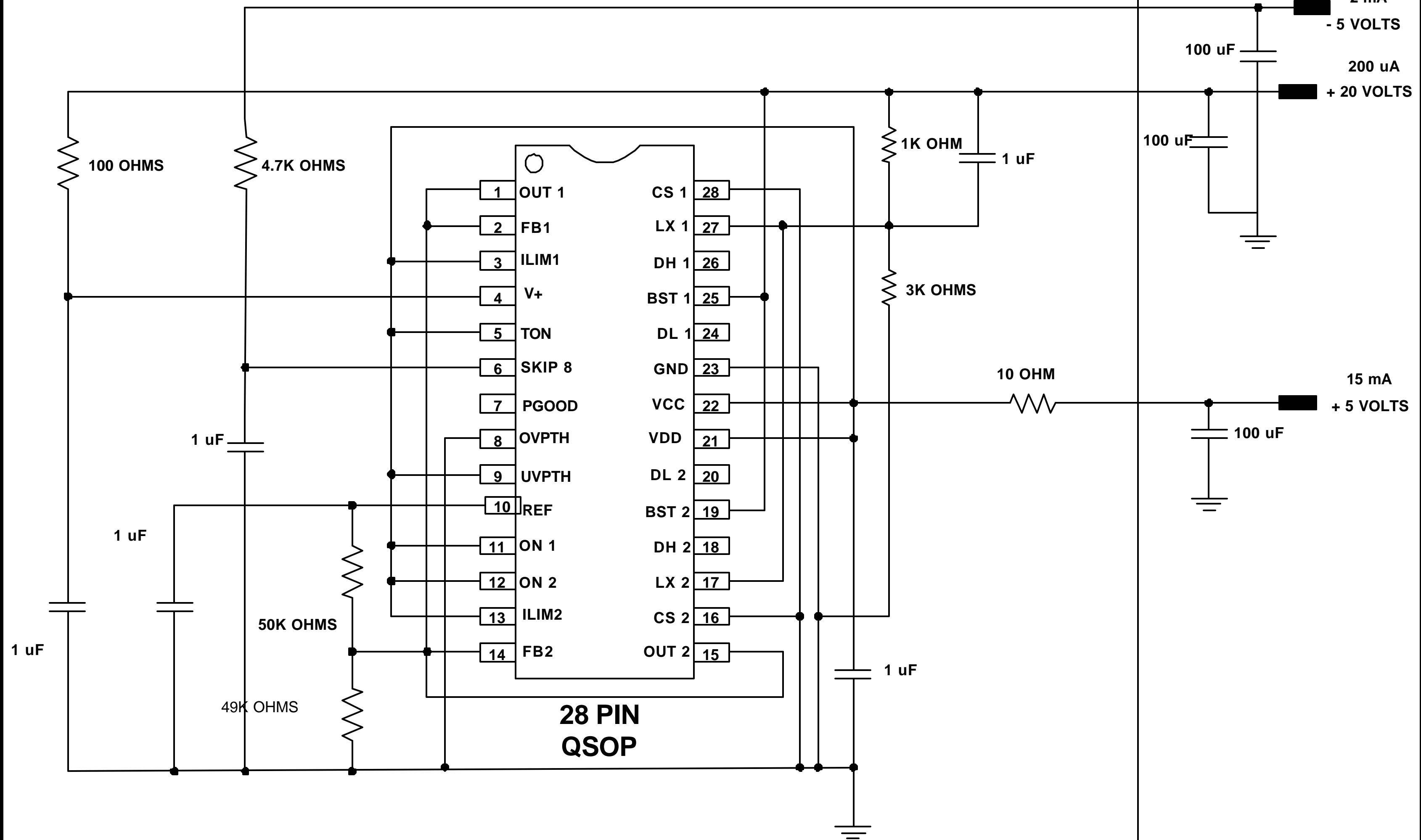
DIE I.D.

10 N/C 11 12 13 14 15 16 17 N/C 18

PKG. CODE: T3666-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 177x177	PKG.			BOND DIAGRAM #: 05-9000-0514	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES : MAX 1845

MAX. EXPECTED CURRENT : -5 (2 mA); +5 (15 mA); +20 (200 uA)

DRAWN BY:

NOTES: