RELIABILITY REPORT

FOR

MAX17682ATP+T

PLASTIC ENCAPSULATED DEVICES

November 14, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX17682ATP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17682 is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 10W. The device operates over a wide 4.5V to 42V input voltage range and uses primary-side feedback to regulate the output voltage. It delivers primary peak current up to 3.7A and regulates primary output voltage to within ±1.2% over -40°C to +125°C. The device features peak-current-mode control with pulse-width modulation (PWM) scheme. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. An open-drain RESETB pin provides a delayed power-good signal to the system upon achieving successful regulation of the primary output voltage. The device operates over the -40°C to +125°C industrial temperature range and is available in a compact 20-pin (4mm x 4mm) TQFN package. Simulation models are available.

II. Manufacturing Information

A. Description/Function:	4.5V to 42V Input, Ultra-Small, High-Efficiency, Iso-Buck DC-DC Converter
B. Process:	S18
C. Number of Device Transistors:	22304
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	October 6, 2016

III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Da_en4900g
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5249
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	33°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	85.0394X100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.28 \times 10^{-9}$

$\lambda = 14.28$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI02-5 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX17682ATP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.