RELIABILITY REPORT

FOR

MAX17599ATE+T

PLASTIC ENCAPSULATED DEVICES

September 18, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX17599ATE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17598/MAX17599 low IQ, active clamp current-mode PWM controllers contain all the control circuitry required for the design of wide-input isolated/non-isolated forward-converter industrial power supplies. The MAX17598 is well-suited for universal input (rectified 85V AC to 265V AC) or telecom (36V DC to 72V DC) power supplies. The MAX17599 is optimized for low-voltage industrial supplies (4.5V DC to 36V DC). The devices include an AUX driver that drives an auxiliary MOSFET (clamp switch) that helps implement the active-clamp transformer reset topology for forward converters. Such a reset topology has several advantages including reduced voltage stress on the switches, transformer size reduction due to larger allowable flux swing, and improved efficiency due to elimination of dissipative snubber circuitry. Programmable dead time between the AUX and main driver allows for zero voltage switching (ZVS). The switching frequency is programmable from 100kHz to 1MHz for the devices with an accuracy of ±8% using an external resistor. This allows optimization of the magnetic and filter components, resulting in compact, cost-effective isolated/nonisolated power supplies. For EMI-sensitive applications, the ICs incorporate a programmable frequency-dithering scheme, enabling low-EMI spread-spectrum operation. An input undervoltage lockout (EN/UVLO) is provided for programming input-supply start voltage, and to ensure proper operation during brownout conditions. EN/UVLO input is also used to turn on/off the ICs. Input overvoltage (OVI) protection scheme is provided to make sure that the regulator shuts down when input supply exceeds its maximum allowed value. To control inrush current, the devices incorporate an SS pin to set the soft-start time for the regulators. Power dissipation under fault conditions is minimized by hiccup overcurrent protection (hiccup mode). Soft-stop feature provides safe discharging of the clamp capacitor when the device is turned off, and allows the controller to restart in a well-controlled manner. Additionally, negative current limit is provided in the current-sense circuitry, helping limit clamp switch current under dynamic operating conditions. SYNC feature is provided to synchronize multiple converters to a common external clock in noise-sensitive applications. Overtemperature fault triggers thermal shutdown for reliable protection of the device. The ICs are available in a 16-pin, TQFN package with 0.5 mm lead spacing.

II. Manufacturing Information

A. Description/Function:	Low-I_Q Wide-Input-Range Active-Clamp Current-Mode PWM Controllers
B. Process:	S18
C. Number of Device Transistors:	6831
D. Fabrication Location:	California
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	December 22, 2011

III. Packaging Information

A. Package Type:	16L TQFN-CU
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5605
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	64°C/W
K. Single Layer Theta Jc:	7°C/W
L. Multi Layer Theta Ja:	48°C/W
M. Multi Layer Theta Jc:	7°C/W

IV. Die Information

A. Dimensions:	49.6063X51.1811 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{264 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 10.1 \times 10^{-9}$

λ = 10.1 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot SABE2Q001A D/C, SABE2Q001B D/C 1139)

The PI17-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX17599ATE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 264 hrs.	DC Parameters & functionality	79	0	SABE2Q001A, D/C 1139

Note 1: Life Test Data may represent plastic DIP qualification lots.