

RELIABILITY REPORT FOR  
MAX17544ATP+T  
PLASTIC ENCAPSULATED DEVICES

September 30, 2014

**MAXIM INTEGRATED**  
160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
Eric Wright
Quality Assurance
Reliability Engineering

## Conclusion

The MAX17544ATP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

## Table of Contents

<b>I. ....Device Description</b>	<b>IV. ....Die Information</b>
<b>II. ....Manufacturing Information</b>	<b>V. ....Quality Assurance Information</b>
<b>III. ....Packaging Information</b>	<b>VI. ....Reliability Evaluation</b>
<b>.....Attachments</b>	

### I. Device Description

#### A. General

The MAX17544 high-efficiency, high voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over 4.5V to 42V input. The converter can deliver up to 3.5A and generates output voltages from 0.9V up to  $0.9 \times V_{in}$ . The feedback (FB) voltage is accurate to within  $\pm 1.1\%$  over -40°C to +125°C. The MAX17544 uses peak current mode control. The device can be operated in pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous conduction mode (DCM) control schemes. The device is available in a 20-pin (5mm x 5mm) TQFN package. Simulation models are available.

## II. Manufacturing Information

A. Description/Function:	4.5V-42V, 3.5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation
B. Process:	S18
C. Number of Device Transistors:	22048
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	September 23, 2014

## III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5249
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	33°C/W
M. Multi Layer Theta Jc:	2°C/W

## IV. Die Information

A. Dimensions:	
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA)            |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 77 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 14.3 \times 10^{-9}$$

$$\lambda = 14.3 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot SANQ4Q001A, D/C 1326)

The MAX17544 has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114.

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78  
With the following exceptions:

EN/UVLO pin passes +100mA/-30mA per JEDEC JESD78

**Table 1**  
Reliability Evaluation Test Results

**MAX17544ATP+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	SANQ4Q001D, D/C 1326

Note 1: Life Test Data may represent plastic DIP qualification lots.