RELIABILITY REPORT

FOR

MAX17113ETL+T

PLASTIC ENCAPSULATED DEVICES

February 15, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX17113ETL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17113 multiple-output power-supply controller generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors operating from a regulated 12V input. It includes a step-down and a step-up regulator, a positive and a negative charge pump, a Dual Mode™ logic-controlled high-voltage switch control block, and an adjustable-timing power-good output. The MAX17113 can operate from 8V to 16.5V input voltages and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supplies. The step-up and step-down regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. Both switching regulators use fixed-frequency current-mode control architectures, providing fast load-transient response and easy compensation. A current-limit function for internal switches and output-fault shutdown protect the step-up and step-down power supplies against fault conditions. The MAX17113 provides soft-start functions to limit inrush current during startup. The MAX17113 provides adjustable power-up timing. The positive and negative charge-pump regulators provide TFT gate-driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers. The switch control block allows the manipulation of the positive TFT gate-driver voltage. A series p-channel MOSFET is integrated to sequence power to AVDD after the MAX17113 has proceeded through normal startup, and provides True Shutdown™. The MAX17113 is available in a small (5mm x 5mm), low-profile (0.8mm), 40-pin thin QFN package and operates over a -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Low-Cost Multiple-Output Power Supply for LCD TVs
B. Process:	S45
C. Number of Device Transistors:	19187
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	July 24, 2009

III. Packaging Information

A. Package Type:	40-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3528
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	45°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	112 X 112 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TSYZDQ001E, D/C 0939)

The PF57 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX17113ETL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TSYZDQ001E, D/C 0939

Note 1: Life Test Data may represent plastic DIP qualification lots.