

RELIABILITY REPORT
FOR
MAX14890EATJ+T
PLASTIC ENCAPSULATED DEVICES

July 7, 2015

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14890EATJ+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14890E incremental encoder receiver contains four differential receivers and two single-ended receivers. The differential receivers can be operated in RS-422 or differential high-threshold logic (HTL) modes and are optionally configurable for single-ended TTL/HTL operation. The MAX14890E features a wide common mode input range of -20V to +20V in RS-422 mode. The auxiliary IEC 61131-2 Type-1/Type-3 digital inputs are designed for operation with switches or proximity sensors and can be individually configured for TTL operation. All receiver input signals are fault protected to voltage shorts in the $\pm 40V$ range. Per channel fault detection provides warning of irregular conditions such as small differential signals, shorts, opens, overvoltages, and undervoltages. The MAX14890E features a pin-selectable SPI or parallel-logic interface. SPI control provides detailed diagnostics and individual configurations for receivers. The MAX14890E is available in a 32-pin TQFN-EP (5mm x 5mm) and operates over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	Incremental Encoder Interface for RS-422, HTL, and TTL with Digital Inputs
B. Process:	S18
C. Number of Device Transistors:	25038
D. Fabrication Location:	USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	June 17, 2015

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5811
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	3°C/W

IV. Die Information

A. Dimensions:	75.5905 X 64.5669 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RU96-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14890EATJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.