

RELIABILITY REPORT
FOR
MAX14855GWE+T
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
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Conclusion

The MAX14855GWE+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14853/MAX14855 isolated RS-485/RS-422 transceivers provide 2750VRMS (60s) of galvanic isolation between the cable-side (RS-485/RS-422 driver/ receiver-side) and the UART-side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. These devices allow for robust communication up to 500kbps (MAX14853) or 25Mbps (MAX14855). The MAX14853/MAX14855 includes an integrated 450kHz transformer driver for power transfer to the cable-side of the transceiver using an external transformer. An integrated LDO provides a simple and space-efficient architecture for providing power to the cable-side of the IC. The MAX14853/MAX14855 includes one drive channel and one receive channel. The receiver is ¼-unit load, allowing up to 128 transceivers on a common bus. Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when cable-side or UART-side power supplies are below functional levels. The driver outputs and receiver inputs are protected from ±35kV electrostatic discharge (ESD) to GNDB on the cable-side, as specified by the Human Body Model (HBM). The MAX14853/MAX14855 are available in a wide body 16-pin SOIC package and operate over the -40°C to +105°C temperature range.

II. Manufacturing Information

A. Description/Function:	2.75kV _{RMS} Isolated 500kbps/25Mbps Full-Duplex RS-485/RS-422 Transceivers with ±35kV ESD Protection and Integrated Transformer Driver
B. Process:	S18
C. Fabrication Location:	USA
D. Assembly Location:	USA, Taiwan
E. Date of Initial Production:	March 18, 2015

III. Packaging Information

A. Package Type:	16-pin SOIC
B. Lead Frame:	Copper
C. Lead Finish:	100% Matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#31-4930
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	71°C/W
K. Multi Layer Theta Jc:	23°C/W

IV. Die Information

A. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
B. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
C. Backside Metallization:	None
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Bondpad Dimensions:	
G. Isolation Dielectric:	SiO ₂
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05@ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RU85-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14855GWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.