RELIABILITY REPORT

FOR

MAX14656EWE+

WAFER LEVEL PRODUCT

February 7, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX14656EWE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14656 is a USB charger detector compliant with USB Battery Charging Specification Revision 1.2. The USB charger detection circuitry detects USB standard downstream ports (SDPs), USB charging downstream ports (CDPs), or dedicated charger ports (DCPs), and controls an external lithium-ion (Li+) battery charger. The device implements USB Battery Charging Specification Revision 1.2-compliant detection logic. The device also includes Apple® charger detection that allows identification of resistor divider networks on D+/D-. The internal double-pole double-throw (DPDT) USB switch is compliant to Hi-Speed USB, full-speed USB, low-speed USB, and UART signals. The deviceâ€™s internal switch features low on-resistance, low on-resistance flatness, and very low capacitance. The ID pin controls the DPDT switch position. The MAX14656 features high-ESD protection up to ±15kV Human Body Model (HBM) on CD+, CD-, and ID pins. The MAX14656 is available in a 16-bump, 0.4mm pitch, 1.8mm x 1.9mm WLP package and operates over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	USB Charger Detection with Integrated Overvoltage Protection
B. Process:	S18
C. Number of Device Transistors:	49142
D. Fabrication Location:	California
E. Assembly Location:	Japan, Texas
F. Date of Initial Production:	December 20, 2012

III. Packaging Information

A. Package Type:	16 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	
G. Assembly Diagram:	#05-9000-4492
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	58°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	75.9842X72.0472 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 56 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.77 \times 10^{-9}$

$\lambda = 3.77$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot S1GZBQ001C, D/C 1126)

The AL32-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14656EWE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	56	0	S1GZBQ001E, D/C 1126

Note 1: Life Test Data may represent plastic DIP qualification lots.