

RELIABILITY REPORT
FOR
MAX14636EVB+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14636EVB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14576/MAX14636/MAX14637 are USB charger detectors. The MAX14576/MAX14636/MAX14637 will pass USB Battery Charger Specification Revision 1.2 (USB BC 1.2) compliance tests. The MAX14636/MAX14637 can also detect Apple chargers, and other nonstandard types. These devices are capable of detecting multiple USB battery charging methods including standard downstream ports (SDP), charging downstream ports (CDP), and dedicated charger ports (DCP). The devices also feature USB BC 1.2 defined dead-battery option support. The MAX14576/MAX14636/MAX14637 feature analog switches that are capable of passing USB Hi-Speed, full-speed, and low-speed signals. The switches have low on-resistance (3 Ω , typ) and low on-capacitance (4.5pF, typ). The CDN and CDP are high ESD protected up to ± 15 kV Human Body Model (HBM), ± 15 kV IEC61000-4-2 Air Gap Discharge, and ± 8 kV IEC61000-4-2 Contact Discharge. The MAX14576/MAX14636/MAX14637 are available in a 10-pin (1.6mm x 2.1mm) UTQFN package and operate over the -40°C to $+85^{\circ}\text{C}$ extended temperature range.

II. Manufacturing Information

A. Description/Function:	USB Charger Detectors
B. Process:	S18
C. Number of Device Transistors:	34331
D. Fabrication Location:	California
E. Assembly Location:	Taiwan
F. Date of Initial Production:	March 28, 2013

III. Packaging Information

A. Package Type:	ULTRA TQFN
B. Lead Frame:	NiPdAu
C. Lead Finish:	NICKEL-PALLADIUM
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4911
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A°
K. Single Layer Theta Jc:	N/A°
L. Multi Layer Theta Ja:	110.8°C/W
M. Multi Layer Theta Jc:	62.1°C/W

IV. Die Information

A. Dimensions:	38.9764X57.48 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 235 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 0.9 \times 10^{-9}$$

$$\lambda = 0.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SAHS3Q001B D/C 1243)

The AL45-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14636EVB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	235	0	SAEM2Q001E, D/C 1223

Note 1: Life Test Data may represent plastic DIP qualification lots.