RELIABILITY REPORT

FOR

MAX14530EEWC+

WAFER LEVEL PRODUCT

September 28, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX14530EEWC+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14529E/MAX14530E are overvoltage-protection devices with USB charger detection, a low-dropout (LDO) regulator, and ESD protection. These devices feature a low 35mΩ (typ) RON internal FET switch and protect low-voltage systems against voltage faults up to 28V. When the input voltage exceeds the overvoltage threshold, the internal FET switch is turned off to prevent damage to the protected components.

The charger detection detects a short between the USB D+ and D- data lines. If the data lines are shorted together and a dedicated charger is attached, the phone draws more than 500mA to charge the battery.

The overvoltage thresholds (OVLO) are preset to 5.75V (MAX14529E) or 6.8V (MAX14530E).

The LDO output (LOUT) is powered from OUT and supplies 3.3V to the USB transceiver. The LDO features a 100mA (min) current capability and low output noise.

The MAX14529E/MAX14530E feature ±15kV HBM ESD protection with low (3pF) capacitance suitable for Hi-Speed USB 2.0.

Both devices are offered in a small 12-bump, 1.5mm x 2mm WLP package and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Overvoltage Protection with USB Charger Detection, LDO, and ESD Protection on D+/D-
B. Process:	S45
C. Number of Device Transistors:	2296
D. Fabrication Location:	Texas
E. Assembly Location:	Japan
F. Date of Initial Production:	January 21, 2009

III. Packaging Information

A. Package Type:	12-bump WLP 3x4 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-3556
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	62°C/W
K. Single Layer Theta Jc:	19°C/W

IV. Die Information

A. Dimensions:	83 X 64 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 2.33 @ 25C and 28.16 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TTCYAQ001E, D/C 0844)

The AJ65-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14530E

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TTCYAQ001E, D/C 0844

Note 1: Life Test Data may represent plastic DIP qualification lots.