RELIABILITY REPORT

FOR

MAX12000ETB+T

PLASTIC ENCAPSULATED DEVICES

October 14, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX12000ETB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX12000 GPS front-end amplifier IC is designed for automotive and marine GPS satellite navigation antenna modules or for any application that needs to compensate for cable losses from the GPS antenna to receiver. Two unconditionally stable low-noise amplifier stages provide the high gain and integrated I/O matching to minimize the need for external matching components and eliminate the need for additional gain stages. The MAX12000 features the option to place a bandpass ceramic or SAW filter between the two amplifier stages to provide a narrow-band output to further improve the noise performance of the GPS receiver. Additionally, a 3.4dB gain step is provided to compensate for cable loss variation between different applications. The MAX12000 is designed to operate at the GPS frequency of 1575MHz with a 34.8dB typical cascaded gain and a 25mA supply current. The two LNA stages allow the use of a wide range of GPS filter types for maximum flexibility in system design. The final RF output pin, which drives the cable to the GPS receiver, is also the power-supply connection that accepts a DC supply in the +3.0V to +5.5V range. Alternatively, the DC supply can be applied to pin 4. The GPS front-end amplifier is designed on a low-noise, advanced SiGe process and is available in a lead-free, 10-pin TDFN surface-mount package (3mm x 3mm).

II. Manufacturing Information

A. Description/Function:	1575MHz GPS Front-End Amplifier
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	USA
E. Assembly Location:	China, Malaysia, Taiwan and Thailand
F. Date of Initial Production:	April 20, 2006

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1967
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	9°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	9°C/W

IV. Die Information

A. Dimensions:	58 X 49 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1-3 = 1.2 / Metal 4 = 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1-3 = 1.6 / Metal 4 = 4.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 239 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.6 \times 10^{-9}$

$\lambda = 4.6$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NZD0A3010C, D/C 1131)

The WG25 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per JEDEC JESD22-A114
ESD-CDM:	+/- 500V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX12000ETB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C	DC Parameters	80	0	NXD0AQ001F, D/C 0613
	Biased	& functionality	80	0	NZD0AA009C, D/C 1108
	Time = 192 hrs.		79	0	NZD0A3010C, D/C 1131

Note 1: Life Test Data may represent plastic DIP qualification lots.