AD7705/AD7706/AD7707 Instrumentation Converter FAQs: General

What are the advantages and disadvantages of sigma-delta ADCs?

The penalty paid for the high resolution achievable with sigma-delta technology has always been speed: the hardware has to operate at the over-sampled rate, much larger than the maximum signal bandwidth, thus demanding great complexity of the digital circuitry. Because of this limitation, Σ–Δ converters have traditionally been relegated to high-resolution, very-low frequency applications and more recently speech, audio and medium speeds (100 kHz to 1 MHz).

The digital filtering stage results in long latency between the start of the sampling cycle, and the first valid digital output; similarly, there is a significant lag thereafter between digital outputs and their corresponding sampling instants. These characteristics reduce the throughput time in multiplexed systems as it takes many clock cycles for the digital filter to settle after switching from one channel to the next.

Most of the circuitry in sigma-delta converters is digital, allowing these converters to be fabricated on a wide range of IC processes. This implies that performance will not drift significantly with time and temperature. They are inherently monotonic (i.e., a change in the digital output has always the same slope as the analog input). This is of particular importance in closed-loop control systems, where misinterpretation of the direction of change of a measured variable may cause the system to become unstable. They are inherently linear, and present little differential non-linearity. External sample & hold circuits are not required due to the high input sampling rate and low precision of the A to D conversion in the modulator, (the devices are inherently self-sampling and tracking). Requirements for analog anti-aliasing filters are minimum - in most cases, a simple single pole RC-filter suffices as the bandwidth of interest is considerably lower than the first image that occurs about the modulator frequency. In contrast, the filters required for medium- to high-resolution applications using other (non-oversampling) technologies are very sophisticated, difficult to design, large, and expensive.

What are the main applications?

These devices provide a complete analog front end for low frequency measurement applications. These applications include portable instrumentation, process control, smart transmitters, weighscale, transducer-based applications, temperature and pressure measurement systems. In pressure and temperature measurement systems, for example, the system designer is faced with the task of measuring small signals that are generated from pressure sensors, RTDs (Resistance Temperature Detectors) or thermocouples and resolving these to resolutions of 16 bits or higher. The major design tasks include signal conditioning of the output signal from the transducer, processing the signal to achieve the required resolution and accuracy and ensuring power consumption is low enough for portable applications. This family of sigma delta converters are fully integrated solutions that incorporate the required signal conditioning, filtering and analog to digital converter onto a single chip allowing direct transducer interface without the need for front end signal conditioning. The AD7705/6/7 provides 16-bit resolution and power consumption of typically 1mW, making them ideal choices for portable data acquisition applications.

What was the traditional approach to analog front-end solutions and how do sigma delta solutions overcome their shortcomings?

Traditional approaches to the problem of measuring signals from transducers have been to use a high resolution Analog to Digital Converter (ADC) as the core element in the process. These were generally integrating ADCs or voltage to frequency converters (VFC) that provided high resolution for low input bandwidth signals. This ADC had to be surrounded by a considerable amount of analog signal conditioning circuitry to boost the transducer output signal so that the full dynamic range of these converters could be used to achieve the required performance. The performance of this signal conditioning circuitry, rather than the high-resolution converter, often determined the system success in measuring low-level signals. In designing gain stages, a number of factors have to be taken into account; the first and most critical is noise, both in the measurement environment and in the components that constitute the high gain stage. Common sources of noise in the circuit design environment are mains frequency noise and power supply noise. Other causes for concern include common mode rejection of the gain stage as the transducer output may sit on a large DC signal, therefore necessitating conversion from a differential input signal to a single ended output. Offset in the amplifiers along with drift performance play havoc with circuit performance, leading to the use of expensive chopper stabilized amplifiers. Programmability was difficult to design into these systems and calibration was performed mainly with the use of the system micro-controller. This leads to the requirement for external memory to store calibration coefficients.

Recent advances in design techniques incorporating switched capacitor and sigma delta technologies have enabled low cost, low power, highly accurate and integrated solutions to be developed. These architectures address the real-world problem of low-power design required for data acquisition applications. The advantages that an integrated solution offers the system designer include signal conditioning necessary for direct transducer interface integrated on-chip that greatly reduces analog

circuit design and layout complexity. Integrated solutions also offer better control of specifications and error budgets than those of discrete solutions. Sigma delta converters provide enough dynamic range to allow direct transducer interface, thus removing the need for a high gain signal conditioning stage in front of the ADC.

The datasheet mentions that large external capacitors between the input and ground can affect measurement accuracy in unbuffered mode. Can you explain why this is the case? Does it only affect AC input signals or are DC input signals affected also?

If you use the ADC in unbuffered mode, large RC constants on the input can interact with the internal sampling capacitor, and effectively starve the sampling cap of charging current. This will cause gain errors in the ADC. The solution is either to use buffered mode or ensure that you respect the maximum RC values given in the datasheet.

The reference inputs are also unbuffered so, as with using the analog inputs in unbuffered mode, the RC loading on the reference inputs must be sufficiently low to avoid introducing errors into the conversion process.

What is the Data Update Rate when the AD7705/06/07 is used with a master clock other than that specified in the datasheet?

The output data rate is determined by the formula:

Update Rate= Fclkin/128/code

Where Fclkin is the master clock and code is the decimal number loaded to the filter register.

On the AD7705/06/07, a limited number of update rates are made available to the user. These update rates are decoded using the CLK, FS1 and FS0 bits in the Clock register. The following table shows the actual update rates for a 2.4576MHz Fclk with CLK=1 and 1MHz with CLK=0.

CLK	FS1	FS0	CODE	Update Rate (Hz)
0	0	0	391	19.98
0	0	1	312	25.04
0	1	0	78	100.2
0	1	1	39	200.3
1	0	0	384	50
1	0	1	320	60
1	1	0	77	249.4
1	1	1	38	505.3

Any clock frequency within specification can be accommodated with these parts, the ones chosen in the data sheet being selected to allow notches at 50 and 60 Hz to be easily implemented with cheap, small and easy to get oscillators. The above formula with the code in the table will determine the update rate for any clock frequency.

How low can I run the Master Clock frequency and what performance can I expect when operating at the reduced clock frequency?

The AD7705/06/07 can be operated with a master clock of 400 kHz minimum. The output data rate will scale with the master clock. For example, with a 1 MHz master clock and CLK = F1 = F0 = 0, the device has an output data rate of 20 Hz. The notches will be placed at integer values of the output data rate i.e. 20 Hz, 40 Hz, 60 Hz, etc. If the master clock is halved, the output data rate will be reduced by a factor of 2 to 10 Hz. The notches now occur at 10 Hz, 20 Hz, 30 Hz, etc. Therefore, with an output data rate of 10 Hz, simultaneous 50 Hz/60 Hz rejection will be obtained

At low input frequencies, the noise is dominated by the internal device noise rather than quantization noise and, therefore, the noise is fairly independent of the master clock frequency. So, using the above example, the rms noise is 4.1 uV when a gain of 1, a master clock of 1 MHz and a 5 V power supply is used from the datasheet table. If the master clock is reduced to 500 kHz, the noise will still equal 4.1 uV with a gain of 1 and a 5 V power supply. This results in a peak-to-peak resolution of 16 bits for both clock speeds.

Many users use lower master clock frequencies so that smaller, low cost ceramic resonators can be used to generate the clock. The disadvantage of resonators is their accuracy – the frequency is not tightly specified and they drift with temperature. Frequency drift will cause the notches to drift that may lead to more noise as spurious signals may pass through.

Is there any suggested protection schemes against ESD that should be considered with these products?
These converters are manufactured on a standard CMOS process and, therefore, all standard practices and protection schemes apply to these devices as with all other CMOS devices. There are ESD protection diodes on all the inputs that protect the device from possible ESD hits due to handling and production. These ESD protection diodes will act to clamp the voltage at any pin to within 0.5V of the supplies. They can carry quite high currents but only for a short period of time so, they can protect the IC from large pulses of short duration (the total energy is still quite low). The latchup current is typically 100mA on all pins.

The maximum DC current that these protection diodes can withstand is 10mA. Therefore, the maximum current that can be applied to any input is 10 mA. If it is possible for a current in excess of 10 mA to be applied to a pin due to an overvoltage, external protection is required. Protection schemes that can be applied include transzorbs on the power supply lines, series resistors on digital input lines, and resistors and diodes on analog inputs. For example, the external protection could be a resistor in series with the input pin to limit the current into the pin to less than 10 mA. For example, if the maximum overvoltage applied to a pin will be 5V, a 1kOhm series resistor in each line will limit the current to 5 mA.

There are a number of application notes and seminar material etc available on this topic. These are available on the Analog Devices web site:

1) AN-202 : IC Amplifier User's Guide to Decoupling, Grounding and Making Things go Right for a Change.
http://www.analog.com/UploadedFiles/Application_Notes/135208865AN-202.pdf

2) AN-311 : How to reliably protect CMOS circuits against power supply overvoltage.
http://www.analog.com/UploadedFiles/Application_Notes/52614692AN311.pdf

3) AN-397 : Electrically Induced Damage to Standard Linear Integrated Circuits.
http://www.analog.com/UploadedFiles/Application_Notes/262799190AN-397.pdf

4) Overvoltage Affects on Analog ICs
http://www.analog.com/UploadedFiles/Associated_Docs/334653243Section7.pdf

What about susceptibility to conducted and radiated electromagnetic emmissions?
Any sigma delta ADC will be susceptible to conducted RF into either the inputs, the power supply pins or into the reference. The reason is that spurious RF signals and their harmonics can be averaged by the sigma-delta modulator and show up as a DC offset or an increase in the noise floor. Radiated RF is a little more difficult to discuss but, similar problems can occur and, there are situations where it is necessary to shield the sigma-delta ADC in a system from large RF fields generated locally within the system.

The amount of protection required will depend on the strength of the local field. There are no hard and fast rules when designing for EMC compatibility as every system will be different but, there are general guidelines that can be followed. Consider the inputs, reference and power supply pins and ensure that each of these lines are properly filtered up to the required maximum frequency. Decoupling capacitors on the power supply, mounted locally to the IC, possibly a small inductor between the analog and digital supplies, filtering on the Reference and the inputs is also critical. A solid low impedance ground plane, and separation of the analog and digital grounds - all the usual good practices with the ground plane running under the whole of the IC. The evaluation board provides a good starting point.

Occasionally it is necessary to provide a Faraday shield for an ADC if the part is operating in the presence of high EM fields such as next to a power supply or relay or RF transmitter but, this is an exceptional case.

As a component manufacturer, Analog Devices do not perform EMC testing as a general rule since EMC is a system level specification rather than a component specification. It is the responsibility of the PCB designer to ensure that sensitive parts of the circuitry are protected from spurious signals. We don't have guaranteed bullet proof EMC design that we can give to customers but if you use the evaluation board and follow standard practices for layout, grounding and decoupling, it is possible to design a system which meets the CE mark and beyond without expending too much design effort. The final chapter in all our seminar books is dedicated to hardware design techniques and deals with such issues as grounding, decoupling, parasitic thermocouples and good PCB design.

http://www.analog.com/UploadedFiles/Associated_Docs/116618369Fsect10.PDF

The evaluation board fails to interface via the printer port what needs to be checked?

All evaluation boards are fully tested as part of our evaluation board production process and should interface directly via the PC printer port without any issues. After power up, ensure that communication with the evaluation board has been established by attempting to read the default values from one of the registers. When evaluating the AD7705, for example, read from the calibration registers after power up and reset. The word 1F4000H should be output from the zero-scale register and 5761ABH from the full-scale register.

If the interface does not operate, there may be a problem running the evaluation board software with Windows NT because that operating system tends to restrict the software access to hardware such as the printer port. The software definitely runs on Windows95 and Windows98 but does not operate on Windows 2000. It is also worth configuring the PC printer port as an output only port. The input lines used on the evaluation boards use the dedicated input lines that cannot be re-configured. An issue may arise with the other lines if they have been re-configured by other pieces of software used in configuring scanners etc.

The following is a quick debug that will also help to source the issue.

Use an oscilloscope probe to check the SCLK pin of the device. This comes into the board on pin 5 of the printer port connector. Load the software and click on the "Program Calibration Coefficients" button. This will cause the software to write to the ADC and then attempt to read the calibration data back. Going in and out of this section will repeat the write/read sequence. A burst of clock pulses should appear on the SCLK pin.

If the SCLK pulses do not occur, it is possible that the printer port has been set as an input port and any attempt to write to it is being ignored. To overcome this, set the port to AT/Unidirectional mode. This must be done in the BIOS software. The method used to edit the BIOS depends on the PC but it is normally some combination of keystrokes when the PC is booting up (typically DEL or CTRL + ALT + ENTER).

If the SCLK pulses are present but the data is read back as all 1's or all 0's, there may be a fault on the board or in the printer port. This can be checked by tracing the SCLK signal from the edge connector to the ADC and tracing the SDATA signal from the part to the edge connector.

What other problems are encountered when using the Evaluation Board.

If the ADC can be configured but conversions cannot be read from the ADC, ensure that the ADC has been brought out of SYNC mode (FSYNC = 0). The part powers up with the FSYNC bit set to 1 which holds the digital filter in a known state and prevents DRDY going low. When a read operation is attempted, the software waits for DRDY and if it doesn't see a transition after a specified time it will timeout and return an error. Of course if the FSYNC bit is set to 1, there will be no DRDY transition.

To ensure that the specified performance is obtained, onnect the inputs together and connect them to a common mode voltage within the common mode range (for example, connect both inputs to the reference), select the required gain, update rate and filter bandwidth, bipolar/unipolar and perform an internal calibration. Use the evaluation software to perform 1000 conversions and use the noise analysis feature to calculate the peak-to-peak resolution. Compare the results from your conversions with the expected results from the datasheet.

Are there any potential issues in driving opto-isolators?

The digital outputs can sink currents greater than 800 uA, if required. These ADCs are capable of sinking up to 5mA on each digital output and still provide a good logic low voltage. Note that the timing characteristics in the datasheet are not performed at these load conditions. The current should be limited to 5mA per output or 10mA maximum combined to avoid any reliability issues from the high currents.

For this reason, a series resistor should be placed between the ADC and the diode to limit the maximum current. It is the total resistance of the opto-isolator plus the series resistor that is important.

For 3.3 V supplies, a 500 ohm resistance will limit the current to 5mA,and the Vol is approximately 120mV. With 5V supplies, an 850 ohm resistance will limit the current to 5mA, and give a Vol of 100mV approximately. The DOUT pin will not draw any current through the opto-isolator when it is tristated. However, 5mA will be sunk through DRDY while it is low.

Is the AD7705 pin compatible with the AD7715: is it possible to auto-detect which part is in a socket?

The AD7715 can be used in the AD7705 socket and a single channel result can be obtained. The register configurations are slightly different so it is important that the user detect which part is in the socket and then run the appropriate software routine. The most effective way to determine which ADC resides in the socket is to read the default value from the SETUP

register on power-up. The default value of this register is 28Hex for the AD7715 while, on the AD7705, it will read as 01Hex. This will indicate which part is in the socket immediately. When the user identifies which part is in the socket, they should assign a unique identifier to it and then run the required routines to program it correctly. This unique identifier is useful if the user looses communication with the interface and needs to re program the device using the correct routines.

Does Analog Devices provide C code for interfacing the AD7705/AD7706/AD7707 to microcontrollers?

Sample C code for interfacing the AD7705/AD7706/AD7707 to the 68HC11 is given in the datasheet. However, Analog Devices does not provide C code for interfacing the ADCs to microcontrollers in general. The sample code is only intended as a guide for programmers. Most customers re-write this code for their own particular purposes and their own microcontroller. The datasheet gives a general description on interfacing the ADCs to various Digital Signal Processors and microcontrollers. The sample code given in the datasheet along with the descriptions can be used to write code for a particular Digital Signal Processor or microcontroller.