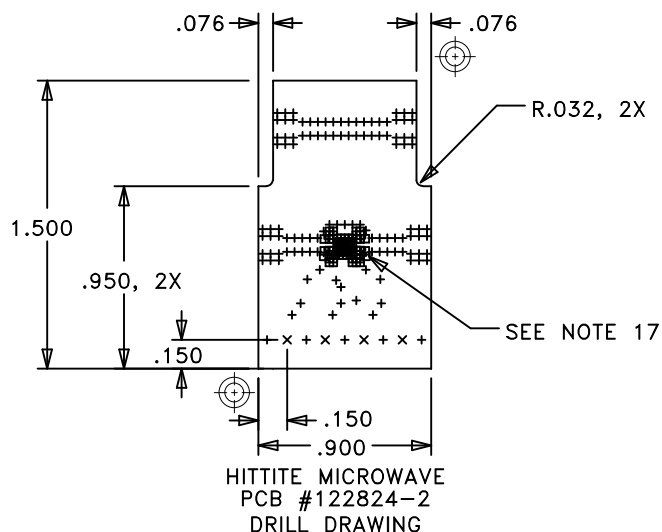


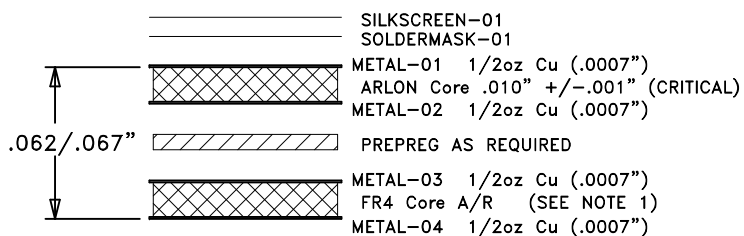
DO NOT SCALE PRINT

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
1		ENGINEERING RELEASE	08/05/08	M.LYONS
2		CORRECTED U1 PIN OUT, C8-C9 POLARITY	11/03/08	M.LYONS



SIZE	QTY	SYM	PLATED	TOL
10	63	□	YES	FILLED
14	117	+	YES	+/- .3
43	4	×	YES	+/- .3

LAYER	DESCRIPTION
1	RF & GND PLANE
2	GND PLANE
3	GND PLANE
4	BOTTOM GND PLANE



LAYER STACKUP

PROPRIETARY TO HITTITE MICROWAVE CORPORATION

UNLESS OTHERWISE SPECIFIED:	
DIMENSIONS ARE IN INCHES (MM)	
DRAWING PRACTICES PER MIL-STD-100	
TOLERANCES:	
.XX	+/- 0.010
.XXX	+/- 0.005
.XXXX	+/- 0.002
ANGLES	+/- .5 DEG

DWN BY:	MARTIN LYONS
ENGINEER:	VINCENT CANNISTRARO



HITTITE MICROWAVE CORPORATION
20 Alpha Road Chelmsford, MA 01824

TITLE

PCB, EVAL,
HMC4788LP4HE

SIZE	CODE ID NO.	DRAWING NO.	REV
A	1CN88	122824	2
SCALE:		WT	SHEET 1 of 1

NOTES:
UNLESS OTHERWISE SPECIFIED

1. MATERIAL: MULTILAYER. OVERALL STACKUP AS SHOWN. TYPE ARLON 25FR, OR ROGERS 4350, HALF OUNCE COPPER BOTH SIDES, TOPSIDE ONLY. FR4 TO BE USED AS FILLER TO MEET CRITICAL OVERALL THICKNESS.
2. FINISH: GOLD PLATE PER ASTM B-488, TYPE III, CODE A, 8 TO 40 MICROINCHES, OVER NICKEL PER QQ-N-290, 100 MICROINCHES MINIMUM.
3. PLATED THRU HOLES: .001" MINIMUM WALL THICKNESS.
4. HOLE SIZES AND POSITIONS PER ARTWORK AND/OR DRILL FILE.
5. ALL HOLES TO BE LOCATED WITHIN ± 0.003 " OF THE CENTER OF THE PAD OR OTHER TRUE POSITION.
6. FRONT TO BACK REGISTRATION ± 0.003 " MAX.
7. BOARD WARPAGE: .010" PER LINEAR INCH MAX.
8. SILKSCREEN TOPSIDE ONLY WITH WHITE EPOXY INK.
9. TOLERANCE ON PCB ROUTE IS ± 0.005 ".
10. PLATING THICKNESS $.002 \pm 0.0005$ FOR METAL-01 AND METAL-04.
11. SOLDERMASK: LPI SOLDERMASK TOP SIDE. COLOR: GREEN REGISTRATION: ± 0.004 MAX.
12. REMOVE METAL BURRS FROM EDGE OF PCB AFTER PANEL SEPERATION.
13. ARTWORK IS 1:1. VENDOR TO ADJUST FOR ETCH FACTOR.
14. "SIZE" IN DRILL LEGEND IS IN MILS AND REFERS TO FINISHED HOLE SIZE.
15. MANUFACTURE PER IPC-600 CLASS II
16. CRITICAL LINE WIDTH = $.016 \pm .001$ " ADJUST PROCESS TO ACHIEVE WIDTH.
17. ALL .010" SIZE VIAS TO BE FILLED WITH NON-CONDUCTIVE VIA FILL AND OVERPLATED WITH Cu BOTH SIDES.