

FEATURES

Single-ended and differential input capability
Optimized EMI suppression filter assembled on board
SYNC functionality to work with other chips

GENERAL DESCRIPTION

The SSM2319 is a fully integrated, single-chip, mono Class-D audio amplifier that is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with less than 1% THD + N driving a 3 Ω load from a single 5.0 V supply.

The SSM2319 is equipped with a differential mode input port and a high efficiency, full H-bridge at the output that enables direct coupling of the audio power signal to the loudspeaker. The differential mode input stage allows for cancelling of common-mode noise.

Internal modulator synchronization (sync) allows an external clock signal to control the modulator of the SSM2319 (for setup configuration and sync operation, see the [SSM2319](#) data sheet).

The part also features a high efficiency, low noise output modulation scheme that does not require external LC output filters when attached to an inductive load. The modulation provides high efficiency even at low output power. Filterless operation also helps to decrease distortion due to the nonlinearities of output LC filters.

This data sheet describes how to configure and use the SSM2319 evaluation board to test the SSM2319. It is recommended that this data sheet be read in conjunction with the SSM2319 data sheet, which provides more detailed information about the specifications, internal block diagrams, and application guidance for the amplifier IC.

EVALUATION BOARD DESCRIPTION

The SSM2319 evaluation board carries a complete application circuit for driving a loudspeaker. Figure 1 shows the top view of the evaluation board, and Figure 2 shows the bottom view.



Figure 1. SSM2319 Evaluation Board, Top View

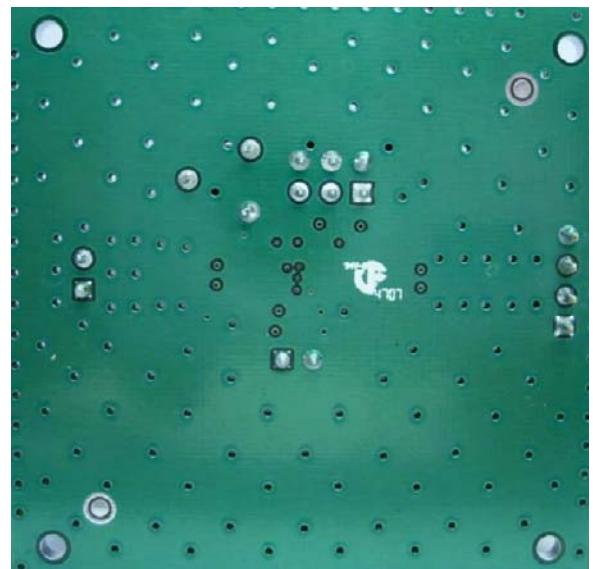


Figure 2. SSM2319 Evaluation Board, Bottom View

Rev. 0

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TABLE OF CONTENTS

Features	1	Component Selection	3
General Description	1	PCB Layout Guidelines.....	4
Evaluation Board Description.....	1	Getting Started.....	5
Revision History	2	What to Test	5
Evaluation Board Hardware.....	3	Evaluation Board Schematic and Artwork.....	6
Input Configuration	3	Ordering Information.....	9
Operation Mode Configuration	3	Bill of Materials.....	9
Output Configuration.....	3	Ordering Guide	9
Power Supply Configuration.....	3	ESD Caution.....	9

REVISION HISTORY

6/09—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

INPUT CONFIGURATION

A 4-pin header (J1) on the middle left side of the board feeds the audio signal into the board (see Figure 1). If the input audio signal is differential (IN+ and IN–), three pins of J1 are used for IN+, IN–, and signal ground. For a single-ended audio input, only two pins of J1 are used. One pin is for the signal ground and the other pin is for either IN+ or IN–. If IN+ is used, place a jumper between Pin 3 and Pin 4 of J1, shorting IN– to ground. If IN– is used, place the jumper between Pin 1 and Pin 2 of J1, connecting IN+ to ground.

OPERATION MODE CONFIGURATION

The 6-pin header, J2, is used to turn the SSM2319 amplifier on or off and to configure the sync operation modes. Placing a jumper across Pin 1 and Pin 2 of J2 shuts down the SSM2319 so that only a minimum current (about 20 nA) is drawn from the power supply (when R3 is shorted). Removing the jumper puts the SSM2319 in normal operation. Placing a jumper across Pin 2 and Pin 3 of J2 puts the SSM2319 in standalone modulator sync mode. This configuration allows the SSM2319 to operate independently, without an external clock source to control the modulator. Placing a jumper across Pin 3 and Pin 5 of J2 (SYNCO to SYNCI) puts the SSM2319 in master sync mode, allowing the SSM2319 SYNCO pin to act as the master to multiple sync slave devices.

OUTPUT CONFIGURATION

The output connector, J4, is located on the right side of the board (see Figure 1). J4 drives a loudspeaker whose impedance should be no less than 3 Ω.

Although the SSM2319 does not require any external LC output filters due to a low noise modulation scheme, if the speaker length is >10 cm, it is recommended to place ferrite beads (L1 and L2) near each output pin of the SSM2319 to reduce electromagnetic interference (EMI), as shown in the schematic in Figure 4. Some users may want to replace the ferrite beads with these inductors to evaluate applications with specific EMI vs. audio performance constraints. As an aid, a properly tuned ferrite bead-based EMI filter is assembled at the output terminals of the device.

For optimal performance, as specified in the SSM2319 data sheet (in particular, for THD and SNR), remove the entire EMI filter, short across the ferrite bead terminals, and open the capacitor terminals.

POWER SUPPLY CONFIGURATION

The evaluation board schematic is shown in Figure 4. The 2-pin header, J3, must be used to power the board. Care must be taken to connect the dc power with correct polarity and voltage. The positive voltage terminal, J3, is indicated with an arrow in Figure 1.

Polarity and Voltage

The wrong power supply polarity or overvoltage may damage the board permanently. The maximum peak current is approximately 0.33 A when driving an 8 Ω load and when the input voltage is 5 V.

COMPONENT SELECTION

Selecting the proper components is the key to achieving the performance required at the cost budgeted.

Input Coupling Capacitor Selection—C1 and C2

The input coupling capacitors, C1 and C2, should be large enough to couple the low frequency signal components in the incoming signal but small enough to filter out unnecessary low frequency signals. For music signals, the cutoff frequency chosen is, typically, between 20 Hz and 30 Hz. The value of the input capacitor is calculated by

$$C = 1/(2\pi Rf_c)$$

where:

$R = 40 \text{ k}\Omega + R_{ext}$ (the external resistor used to fine-tune the desired gain; on the schematics (see Figure 4), this is the 0 Ω resistor at the input pins).

f_c is the cutoff frequency.

Output Ferrite Beads—L1 and L2

The output beads, L1 and L2, are necessary components for filtering out the EMI caused at the switching output nodes when the length of the speaker wire is greater than 10 cm. The penalty for using ferrite beads for EMI filtering is slightly worse noise and distortion performance at the system level due to the nonlinearity of the beads.

Ensure that these beads have enough current-conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8 Ω load is approximately 420 mA, and impedance at 100 MHz should be $\geq 120 \Omega$. In addition, the lower the dc resistance (DCR) of these beads, the better for minimizing their power consumption.

Table 1 describes the recommended beads.

EVAL-SSM2319

Table 1. Recommended Output Beads (L1 and L2)

Part No.	Manufacturer	Z (Ω)	I _{MAX} (mA)	DCR (Ω)	Size (mm)
BLM18PG121SN1D	Murata	120	2000	0.05	1.6 × 0.8 × 0.8
MPZ1608S101A	TDK	100	3000	0.03	1.6 × 0.8 × 0.8
MPZ1608S221A	TDK	220	2000	0.05	1.6 × 0.8 × 0.8
BLM18EG221SN1D	Murata	220	2000	0.05	1.6 × 0.8 × 0.8

Table 2. Recommended Output Inductors (L3 and L4)

Part No.	Manufacturer	L (μH)	I _{MAX} (mA)	DCR (Ω)	Size (mm)
LQM31PNR47M00	Murata	0.47	1400	0.07	3.2 × 1.6 × 0.85
LQM31PN1R0M00	Murata	1.0	1200	0.12	3.2 × 1.6 × 0.85
LQM21PNR47MC0	Murata	0.47	1100	0.12	2.0 × 1.25 × 0.5
LQM21PN1R0MC0	Murata	1.0	800	0.19	2.0 × 1.25 × 0.5
LQH32CN2R2M53	Murata	2.2	790	0.1	3.2 × 2.5 × 1.55

Output Shunting Capacitors

There are two output shunting capacitors, C3 and C4, that work with the ferrite beads, L1 and L2. Use small size (0603 or 0402), multilayer ceramic capacitors that are made of X7R or COG (NPO) materials. Note that the capacitors can be used in pairs: a capacitor with small capacitance (up to 100 pF) plus a capacitor with a larger capacitance (less than 1 nF). This configuration provides thorough EMI reduction for the entire frequency spectrum. For BOM cost reduction and capable performance, a single capacitor of approximately 470 pF can be used.

Output Inductors

If you prefer using inductors for the purpose of EMI filtering at the output nodes, choose inductance that is <2.2 μH. The higher the inductance, the lower the EMI is at the output. However, the cost and power consumption by the inductors are higher. Using 0.47 μH to 2.2 μH inductors is recommended, and the current rating needs >600 mA (saturation current) for an 8 Ω load. Table 2 shows the recommended inductors. Note that these inductors are not populated on the evaluation board.

PCB LAYOUT GUIDELINES

To keep the EMI under the allowable limit and to ensure that the amplifier chip operates under the temperature limit, PCB layout is critical in application design. Figure 3 shows the preferred layout for the SSM2319. The SSM2319 works well only if these techniques are implemented in the PCB design to keep EMI and the amplifier temperature low.

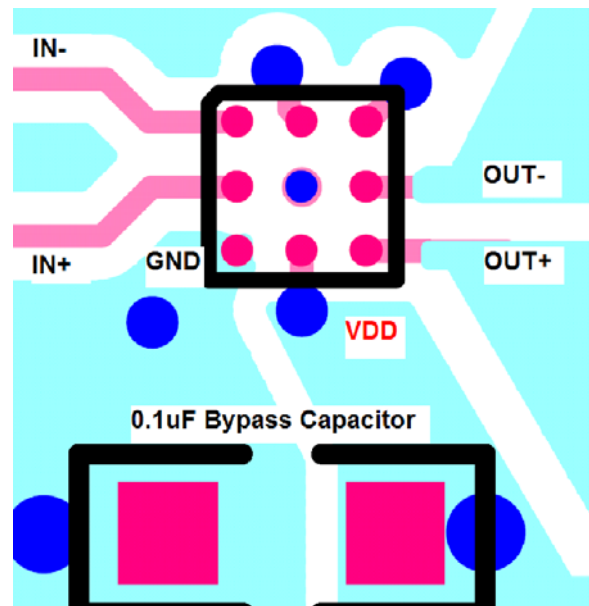


Figure 3. Preferred PCB Layout for the SSM2319 Evaluation Board

Layer Stacks and Grounding

The stack-up for the evaluation board is a 4-layer structure.

- Top layer—component layer with power and output copper land and ground copper pouring.
- Second layer—dedicated ground plane.
- Third layer—dedicated power plane.
- Bottom layer—bottom layer with ground copper pouring.

Component Placement and Clearance

Place all related components except decoupling capacitors on the same side as the SSM2319 and as close as possible to the chip to avoid vias (see Figure 5).

Place decoupling capacitors on the bottom side and close to the GND pin.

Top Layer Copper Land and Ground Pouring

The output peak current of this amplifier is more than 1 A; therefore, PCB traces should be wide (>2 mm) to handle the high current. For the best performance, use symmetrical copper lands as large as space allows, instead of traces, for the output pins (see Figure 3).

Pour ground copper on the top side and use many vias to connect the top layer ground copper to the dedicated ground plane. The copper pouring on the top layer serves as both the EMI shielding ground plane and the heat sink for the SSM2319.

GETTING STARTED

To ensure proper operation, carefully follow Step 1 through Step 6.

1. If a jumper is across Pin 1 and Pin 2 of J2, remove the jumper to enable the amplifier.
2. Insert a jumper across Pin 3 and Pin 4 of J2 to ensure that the device is in standalone sync mode.
3. For most audio quality testing, the EMI filtering (L1/L2 and C6/C7) must be removed. Short across the L1 and L2 terminals to make a direct connection from device output to the J4 speaker header.
4. Connect the load to the audio output connector, J4.
5. Connect the audio input to the board, either in differential mode or single-ended mode, depending on the application.
6. Connect the power supply with the proper polarity and voltage.

WHAT TO TEST

When implementing the SS72315 evaluation board, test the board for the following:

- Electromagnetic interference (EMI)—connect wires for the speakers, making sure that they are the same length as the wires required for the actual application environment; then complete the EMI test.
- Signal-to-noise ratio (SNR).
- Output noise—make sure to use an A-weighted filter to filter the output before reading the measurement meter.
- Maximum output power.
- Distortion.
- Efficiency.

EVALUATION BOARD SCHEMATIC AND ARTWORK

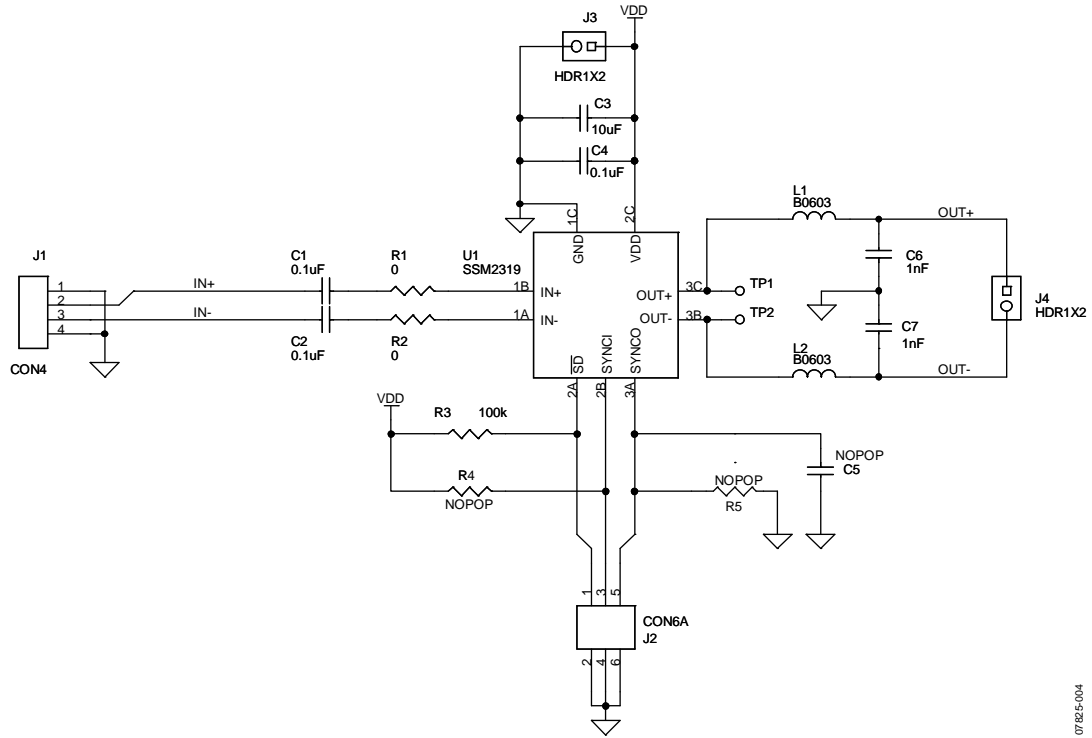


Figure 4. Schematic of the SSM2319 Evaluation Board

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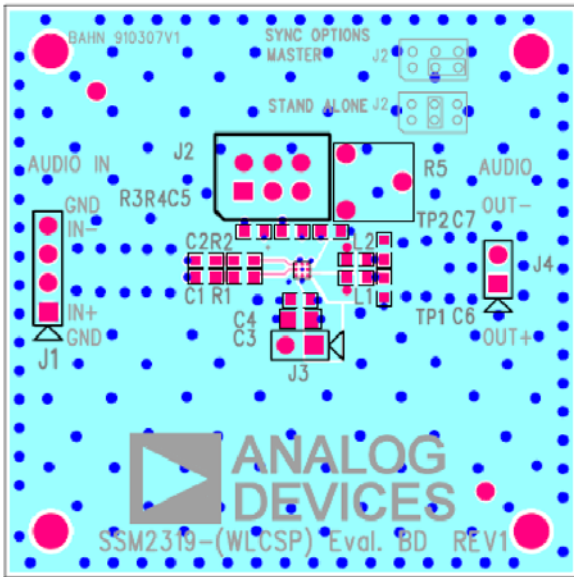


Figure 5. Top Layer with Top Silkscreen

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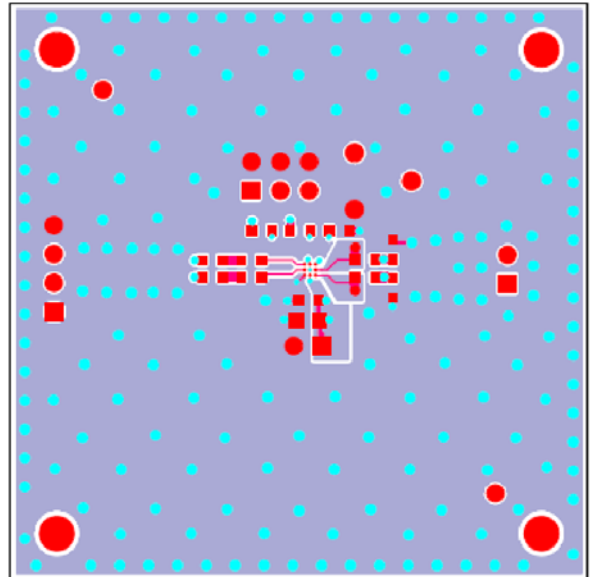


Figure 7. Top Layer

07825-008

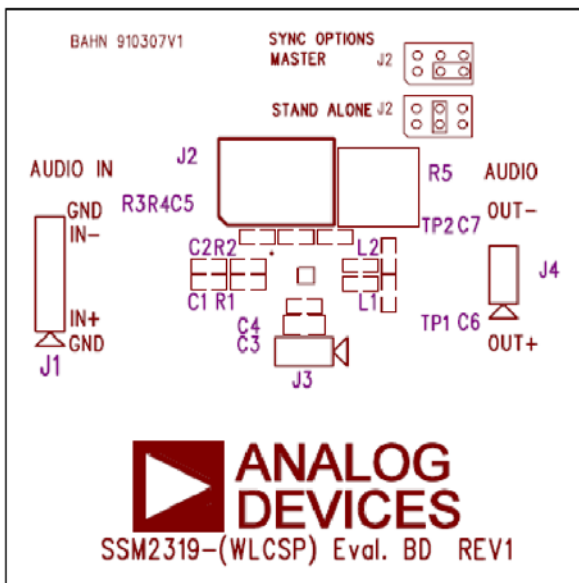


Figure 6. Top Silkscreen

07825-006

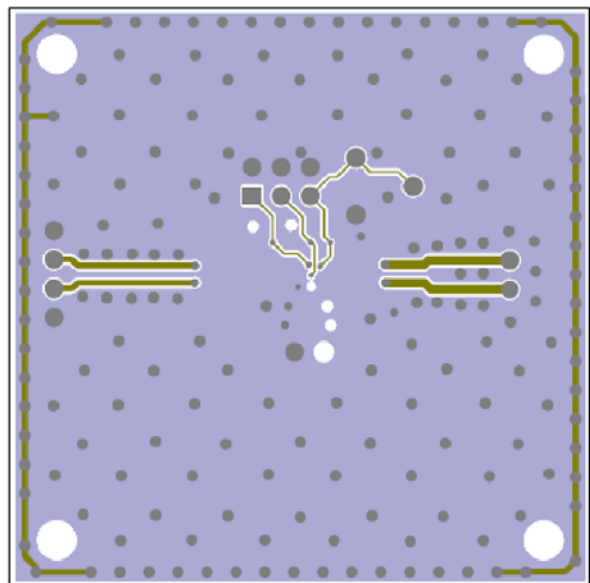
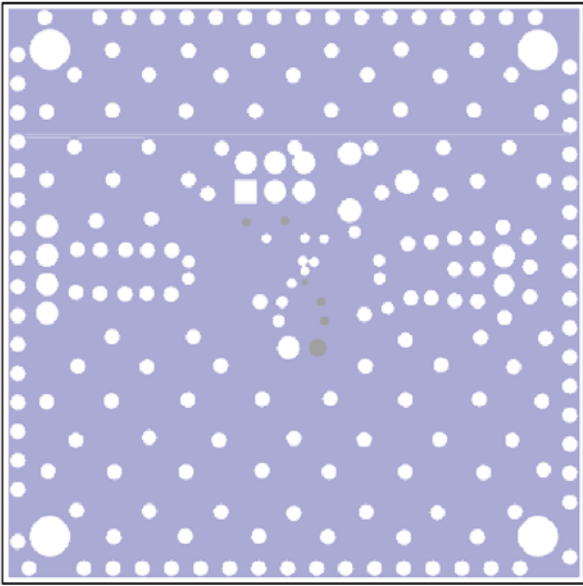


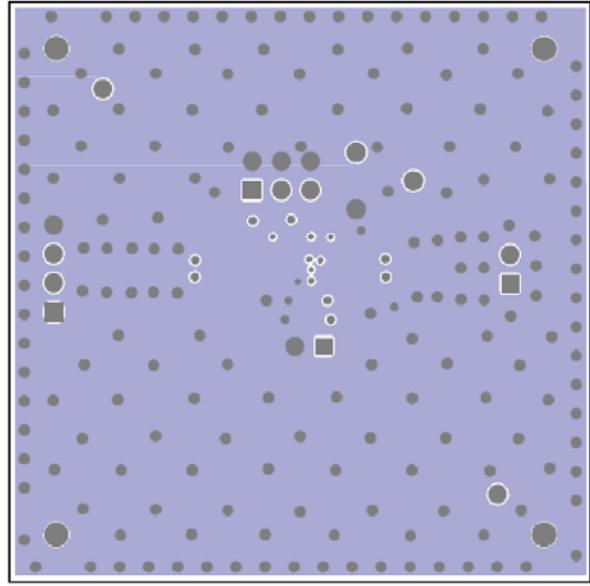
Figure 8. Layer 2 (Ground Plane)

07825-009



07825-010

Figure 9. Layer 3 (Power Plane)



07825-011

Figure 10. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Qty	Reference Designator	Description	Supplier/Part No.
3	C1, C2, C4	Ceramic capacitor, 0.1 μ F	Panasonic, ECJ-ZEB1A104M
1	C3	Ceramic capacitor, 10 μ F, 10 V	Murata, GRM31MF51A106ZA01L
2	C6, C7	Ceramic capacitor, 1 nF, 10%, 50 V	Kemet, C0603C102J5GACTU
1	J1	CON4, header connector	Tyco, 640452-4
1	J2	CON6A, six-position header connector	Tyco, 3-87589-6
2	J3, J4	HDR1X2 header connector	Tyco, 640452-2
2	L1, L2	Ferrite chip, B0603, 220 Ω	TDK, MPZ1608S221A
2	R1, R2	Resistor, 0 Ω	Panasonic, ERJ-3GEY0R00V
1	R3	Resistor, 100 k Ω	Yaego, RT0603FRE07100KL
2	TP1, TP2	Test pad	N/A
1	U1	SSM2319/BGA	Analog Devices, SSM2319
	C5	Ceramic capacitor, 0.1 uF, not populated	Panasonic, ECJ-ZEB1A104M
	R4	Resistor, 100 k Ω , not populated	Yaego, RT0603FRE07100KL
	R5	Resistor, 100 k Ω , not populated	Panasonic, EVN-D8AA03B15

ORDERING GUIDE

Model	Description
EVAL-SSM2319Z ¹	Evaluation Board

¹ Z = RoHS Compliant Part.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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