SCOPE: CMOS 8-Bit, µP-Compatible, 12-Bit D/A Converter

Device Type:	**Generic Number:**
-01	**MX7548S(x)/883B**
-02	**MX7548T(x)/883B**

Case Outline(s).

Outline Letter	**Mil-Std-1835**	**Case Outline**	**Package Code**
Q	GDIP1-T20 or CDIP2-T20	20 Lead CERDIP	J20
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings:

V_{DD} to DGND ..... +17V
VREF to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{OUT1} to DGND ..... -0.3V, V_{DD}
AGND to DGND ..... -0.3V, V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 pin CERDIP(derate 10mW/°C above +70°C) 889mW
20 pin LCC(derate 9.09mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
20 pin CERDIP..... 40°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
20 pin CERDIP..... 90°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS $-55°C \le T_A \le +125°C$ 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE							
Resolution	N		1,2,3	All	12		Bits
Integral Nonlinearity	INL		1,2,3	01 02		±1 ±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits	1,2,3	01 02		±1 ±0.5	LSB
Gain Error	FSE	Using internal feedback resistor	1 2,3	01		±2 ±3	LSB
Gain Error	FSE	Using internal feedback resistor	1 2,3	02		±1 ±2	LSB
Gain Tempco	TC_{FS}	NOTE 2 (ΔGain/ΔTemp)		All		±5	ppm/°C
DC Supply Rejection	PSR	ΔV_{DD}=±5% (ΔGain/ΔSupply)	1 2,3	All		±0.001 ±0.002	%/%
DYNAMIC PERFORMANCE		**NOTE 2**					
Current Settling Time	t_S	To 0.5LSB, OUT1 load: R_L=100 Ω: CL=13pF: DAC register alternately loaded with all 1s and all 0s.	4	All		1	µs
Digital to Analog Glitch Impulse	Q	V_{REF}=0V, OUT1 load: R_L=100 Ω: CL=13pF: DAC register alternately loaded with all 1s and all 0s.	4,5,6	All		200	nV-s
AC Feedthrough at OUT1 NOTE 3	FTE	V_{REF}=±10Vp-p at 10kHz, DAC register loaded with all 0s.	4,5,6	All		5	mVp-p
Total Harmonic Distortion	THD	V_{REF}=6V_{RMS} at 1kHz, DAC register loaded with all 1s.	4,5,6	All		-90	dB
Output Noise Voltage Density	en	10Hz to 100kHz. Measured between R_{FB} and OUT1.	4,5,6	All		15	nV/Hz
REFERENCE INPUT							
Input Resistance	R_{REF}	V_{REF} pin to OUT1	1,2,3	All	7	15	kΩ
ANALOG OUTPUT							
OUT1 Leakage Current	ILKG	DAC register loaded with all 0s.	4 5,6	All		±5 ±100	nA
OUT1 Capacitance NOTE 2	C_{OUT1}	DAC register loaded with all 0s DAC register loaded with all 1s	4,5,6	All		70 140	pF

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS $-55°C \le T_A \le +125°C$ 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}		1,2,3	All	2.4		V
Digital Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	Digital Inputs at 0V or V_{DD}	1,2,3	All		±1	µA
Input Capacitance NOTE 2	C_{IN}	Digital Inputs at 0V or V_{DD}	4,5,6	All		7	pF
SWITCHING CHARACTERISTICS NOTES 2, 4							
Data Valid Setup	t_{DS}		9,10,11	All	160		ns
Data Valid Hold	t_{DH}		9,10,11	All	10		ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup	t_{CWS}		9,10,11	All	0		ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold	t_{CWH}		9,10,11	All	0		ns
$\overline{LDAC}$ to $\overline{WR}$ Setup	t_{LWS}		9,10,11	All	0		ns
$\overline{LDAC}$ to $\overline{WR}$ Hold	t_{LWH}		9,10,11	All	0		ns
$\overline{WR}$ Pulse Width	t_{WR}		9,10,11	All	120		ns
POWER SUPPLY							
V_{DD} Range NOTE 5	V_{DD}	V_{DD}=+12V or +15V V_{DD}=+5V	1,2,3	All	+11.4 +4.75	+15.75 +5.25	V
I_{DD} Range	I_{DD}	All digital inputs at V_{IL} or V_{IH} V_{DD}=+12V or +15V V_{DD}=+5V	1,2,3	All		3 2	mA
		All digital inputs at 0V or V_{DD} V_{DD}=+12V or +15V V_{DD}=+5V	1,2,3	All		1 300	mA µA

NOTE 1: V_{DD}=+5V, +12V or +15V; V_{OUT1}=AGND=DGND=0V; V_{REF}=+10V, unless otherwise noted.
NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.
NOTE 3: Feedthrough can be further reduced by connecting the metal lid to DGND on the ceramic package.
NOTE 4: Timing shown in commercial datasheet, Figure 5.
NOTE 5: Specifications are guaranteed over these ranges.

TERMINAL CONNECTIONS:

	MX7548		
	J20 & L20		J20 & L20
1	I_{OUT}	11	DB3
2	AGND	12	DB2
3	DGND	13	DB1
4	$\overline{CS}_{MSB}$	14	DB0(LSB)
5	$\overline{DF/DOR}$	15	$\overline{LDAC}$
6	CTRL	16	$\overline{CS}_{LSB}$
7	(MSB)DB7	17	$\overline{WR}$
8	DB6	18	V_{DD}
9	DB5	19	VREF
10	DB4	20	R_{FB}

ORDERING INFORMATION:

01	J20	MX7548SQ/883B
01	L20	MX7548SE/883B
02	J20	MX7548TQ/883B
02	L20	MX7548TE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with Mil-Prf-38535, Appendix A as Specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. T_A = +125°C, minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, Including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883.
    1. Test condition A, B, C, D.
    2. T_A = +125°C, minimum.
    3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups Per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6**, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, 5, 6 shall be tested at initial qualification and upon redesign.
Sample size will be 116 units.