SCOPE: QUAD, CMOS, 8-BIT D/A CONVERTER WITH SEPARATE REFERENCES

Device Type	Generic Number	Circuit Function
01	MX7225T(x)/883B	DAC with 2 LSB
02	MX7225U(x)/883B	DAC with 1 LSB

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T24 or CDIP2-T24	24 LEAD CERDIP	R24
E	CQCC1-N28	28 LCC	L28

Absolute Maximum Ratings:

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to AGND ..... V_{SS}, V_{DD}

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
24 pin CERDIP(derate 12.5mW/°C above +70°C) 1000mW
28 pin LCC(derate 10.2mW/°C above +70°C) 816mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
24 pin CERDIP..... 40°C/W
28 pin LCC ..... 15°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
24 pin CERDIP..... 80°C/W
28 pin LCC ..... 98°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE							
Resolution	RES	Guaranteed but not tested	1,2,3	All	8.0		Bits
Total Unadjusted Error	ET	V_{DD}=+14V, VREF=+10V	1,2,3	01 02	-2.0 -1.0	2.0 1.0	LSB
Relative Accuracy	RA	V_{DD}=+14V, VREF=+10V	1,2,3	01 02	-1.0 -0.5	1.0 0.5	LSB
Differential Nonlinearity	DNL	V_{DD}=+14V, VREF=+10V 2/	1,2,3	All	-1.0	1.0	LSB
Full-Scale Error	AE	V_{DD}=+14V, VREF=+10V	1,2,3	01 02	-1.0 -0.5	1.0 0.5	LSB
Zero-Code Error		V_{DD}=16.5V, 11.4V, 14V, VREF=V_{DD}-4V	1 2,3	01	-25 30	20 30	mV
Zero-Code Error		V_{DD}=16.5V, 11.4V, 14V, VREF=V_{DD}-4V	1 2,3	02	-15 20	15 20	mV
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate	T_{SR}		4	All	2.5		V/µs
Voltage Output Settling Time	T_{SL}	VREF=+10V; to 0.5LSB, 2kΩ and 100pF Load	4	All		5	µs
Minimum Load Resistance	RL_{MIN}	V_{OUT}=+10V, V_{DD}=14V	4	All	2		kΩ
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}			All	2	V_{DD}-4	V
Reference Input Resistance	R_{IN}	V_{DD}=14V	1,2,3	All	11		kΩ
Reference Input Capacitance	C_{IN}	DAC loaded with all 1s.	4	All		100	pF
Channel to Channel Isolation		VREF=10Vp-p, Sinewave at 10kHz	4	All	60		dB
AC Feedthrough		VREF=10kHz, 10Vp-p, Sinewave at 10kHz	4	All	70		dB
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}	V_{DD}=14V	1,2,3	All	2.4		V
Digital Input Low Voltage	V_{IL}	V_{DD}=11.4V and 14V	1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD}, V_{DD}=16.5V	1,2,3	All	-1.0	+1.0	µA
Digital Input Capacitance	C_{IN}		4	All		8.0	pF
SWITCHING CHARACTERISTICS							
Write Pulse Width, t1	t_{WR}	NOTE 3	9	All	150		ns
Address to Write-Setup Time, t2	t_{AS}	NOTE 3	9	All	0		ns
Address to Write-Hold Time, t3	t_{AH}	NOTE 3	9	All	0		ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Data Valid to Write Set-up Time, t4	t_{DS}	NOTE 3	9	All	90		ns
Data Valid to Write Hold Time, t5	t_{DH}	NOTE 3	9	All	10		ns
Load DAC Pulse Width, t6	t_{LDAC}	NOTE 3	9	All	150		ns
POWER SUPPLIES							
Positive Supply Current	I_{DD}	V_{IN}=V_{IL} or V_{IH}, V_{DD}=16.5V, V_{SS}=-5.5V, VREF=12.5V 4/	1,2,3	All		12	mA
Negative Supply Current	I_{SS}	V_{IN}=V_{IL} or V_{IH}, V_{DD}=16.5V, V_{SS}=-5.5V, VREF=12.5V 4/	1,2,3	All		10	mA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 5/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE							
Resolution	RES	NOTE 6	1,2,3	All	8.0		Bits
Total Unadjusted Error	ET	V_{DD}=14V, VREF=10V	1,2,3	01 02	-2.0 -1.0	2.0 1.0	LSB
Differential Nonlinearity	DNL	V_{DD}=14V, VREF=10V	1,2,3	All	-1.0	1.0	LSB
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}			All	2	V_{DD}-4	V
Minimum Load Resistance	RL_{MIN}	V_{OUT}=10V, V_{DD}=14V	4	All	2.0		kΩ
Reference Input Resistance	R_{IN}	V_{DD}=14V	1,2,3	All	11		kΩ
Reference Input Capacitance	C_{IN}	DAC loaded with all 1s	4	All		100	pF
Channel to Channel Isolation		VREF=10Vp-p, Sinewave at 10kHz	4	All	-60		dB
AC Feedthrough		VREF=10Vp-p, Sinewave at 10kHz	4	All	-70		dB
DIGITAL INPUTS		Same as Dual Supply Operation					
DYNAMIC PERFORMANCE		Same as Dual Supply Operation					
SWITCHING CHARACTERISTICS		Same as Dual Supply Operation					
POWER SUPPLIES							
Positive Supply Current Output Unloaded	I_{DD}	V_{IN}=V_{IL} or V_{IH}	1,2,3	All		12	mA

NOTE 1: Dual-Supply operation, V_{DD}=+15V, V_{SS}=-5V, AGND=DGND=0V, VREF= +10V unless otherwise specified.

NOTE 2: Guaranteed monotonic to 8 bits.

NOTE 3: Timing shown in commercial datasheet..

NOTE 4: Outputs unloaded.

NOTE 5: Single-supply operation, V_{DD}=+15V ±5%, V_{SS}=0V, AGND=DGND=0V, VREF=+10V unless otherwise specified.

NOTE 6: Characteristics supplied for use as a typical design limit but not production tested.

MODE SELECTION:

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Registers
H	H	DAC D Input Registers

TRUTH TABLE:

$\overline{WR}$	$\overline{LDAC}$	FUNCTION
H	H	No operation. Device not selected.
L	H	Input register of selected DAC transparent.
↑	H	Input register of selected DAC latched.
H	L	All four DAC registers transparent (i.e. outputs respond to data held in respective input registers). Input registers are latched.
H	↑	Latch the four DAC registers. Input registers latched.
L	L	DAC registers and selected input registers transparent. Output follows input data for selected channel

TERMINAL CONNECTIONS:

Pin	R24	L28	Pin	L28
1	V_{OUTB}	NC	25	VREFC
2	V_{OUTA}	V_{OUTB}	26	V_{DD}
3	V_{SS}	V_{OUTA}	27	V_{OUTD}
4	VREFB	V_{SS}	28	V_{OUTC}
5	VREFA	VREFB		
6	AGND	VREFA		
7	DGND	AGND		
8	$\overline{LDAC}$	NC		
9	DB7(MSB)	DGND		
10	D6	$\overline{LDAC}$		
11	D5	D7(MSB)		
12	D4	D6		
13	D3	D5		
14	D2	D4		
15	D1	NC		
16	D0(LSB)	D3		
17	$\overline{WR}$	D2		
18	A1	D1		
19	A0	D0(LSB)		
20	VREFD	$\overline{WR}$		
21	VREFC	A1		
22	V_{DD}	NC		
23	V_{OUTD}	A0		
24	V_{OUTC}	V_{REFD}		

	Package	ORDERING INFORMATION:
01	24 pin CERDIP	MX7225TQ/883B
02	24 pin CERDIP	MX7225UQ/883B
01	28 pin LCC	MX7225TE/883B
02	28 pin LCC	MX7225UE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, capacitance tests shall be tested at initial qualification and upon redesign. Sample size will be 116 units.