SCOPE: CMOS MICROPROCESSOR-COMPATIBLE, 8-BIT ADC

Device Type	Generic Number
01	MAX160M(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JN	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18
LP	CQCC1-N20	20 Leadless Carrier	LCC

Absolute Maximum Ratings

V_{DD} to AGND ..... 0V to +7V
V_{DD} to DGND..... 0V to +7V
AGND to DGND ..... -0.3V to V_{DD}
Clock Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Input Voltage to DGND ..... -0.3V to V_{DD}
Digital Output Voltage to DGND ..... -0.3V to V_{DD}
V_{REF} ..... -20V, +20V
V_{BOFS} ..... -20V, +20V
V_{AINS} ..... -20V, +20V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
18 pin CERDIP(derate 10.5mW/°C above +70°C) 842mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
18 pin CERDIP..... 45°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
18 pin CERDIP..... 95°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Supply Voltage Range, V_{DD} ..... +5V
Reference Voltage, V_{REF} ..... -10V
Ground ..... AGND=DGND=0V
Clock Resistance 150k
Clock Capacitance, C_{CLK} 100pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES	NOTE 5		All	8		Bits
Relative Accuracy	RA	External clock frequency 2.0MHz	1,2,3	All	-0.5	0.5	LSB
Differential Nonlinearity	DNL	External clock frequency 2.0MHz	1,2,3	All	-0.75	+0.75	LSB
Gain Error	AE	Gain error is measured after calibrating out offset error. External clock frequency 2.0MHz	1 2,3	All	-3.0 -4.5	+3.0 +4.5	LSB
Offset Error	V_{OS}	External clock frequency 2.0MHz	1 2,3	All	-20 -30	+20 +30	mV
Resistance mismatch between B_{OFS} and A_{IN}	RM		1,2,3	All	-1.5	+1.5	%
Input Resistance	R_{IN}	At V_{REF} At B_{OFS} At A_{IN}	1,2,3	All	5 10 10	15 30 30	kΩ
Digital Input High Level Voltage	V_{IH}	$\overline{RD}$, $\overline{CS}$	1,2,3	All	2.4		V
Digital Input Low Level Voltage	V_{IL}	$\overline{RD}$, $\overline{CS}$	1,2,3	All		0.8	V
Digital Input Current	I_{IN}	V_{IN}=0V or V_{DD}	1 2,3	All	-1.0 -10	+1.0 +10	µA
Digital Input Capacitance	C_{ID}	NOTE 2	4	All		7.0	pF
Clock Input High Voltage	V_{IH}		1,2,3	All	3.0		V
Clock Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Clock Input High Current	I_{IH}		1 2,3	All	-2.0 -3.0	+2.0 +3.0	mA
Clock Input Low Current	I_{IL}		1 2,3	All	-1.0 -10	+1.0 +10	mA
Digital Output High Level Voltage	V_{OH}	I_{SOURCE}=200µA	1,2,3	All	4.0		V
Digital Output Low Level Voltage	V_{OL}	I_{SINK}=1.6mA	1,2,3	All		0.4	V
Floating State Leakage Current (D7-D0)	I_{LKG}	V_{OUT}=0V or V_{DD}	1 2,3	All	-1.0 -10	+1.0 +10	µA
Floating State Output Capacitance (D7-D0)	C_{OUT}	NOTE 2	4	All		7.0	pF
Supply Current	I_{DD}	A_{IN}=0V, $\overline{BUSY}$ and $\overline{RD}$=High	1,2,3	All		5.0	mA
$\overline{CS}$ Pulse Width	t_{CS}	NOTE 2	9	All	150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}	NOTE 2	9	All	0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	t_{CBPD}	$\overline{BUSY}$ Load=100pF $\overline{BUSY}$ Load=20pF	9,10,11	All		130 150	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		9,10,11	All	0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		9,10,11	All	0		ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Data Valid Access Time	t_{RAD}	D0-D7, Load=100pF	9,10,11	All		140	ns
Data Valid Hold Time	t_{RHD}		9,10,11	All		180	ns
$\overline{CS}$ to $\overline{RD}$ Hold time	t_{RHS}		9,10,11	All		500	ns
Reset Time Requirement	t_{RESET}		9,10,11	All	1.5		µs
$\overline{RD}$ to $\overline{BUSY}$	t_{WBPD}	$\overline{BUSY}$ Load =20pF NOTE 4	9,10,11	All		1.2	µs
Conversion Time	$t_{CONVERT}$	Ext CLK 2MHz NOTE 5		All	4.0		µs
Conversion Time Using Internal Clock	$t_{CONVERT}$	R_{CLK}=22kΩ	9,10,11	All	4.0	6.0	µs

NOTE 1: V_{DD}=+5.0V, V_{REF}=-10.0V. Unipolar Configuration, Slow Memory Mode using External Clock t_{CLK}=2.0MHz, R_{CLK}=22kΩ. C_{CLK}=100pF.
NOTE 2: Guaranteed at 25°C, if not tested to the limits specified in Table 1.
NOTE 3: Guaranteed by functional pattern testing in external clock RAM, ROM, and SLOW modes.
NOTE 4: Static RAM interface mode.
NOTE 5: __ Guaranteed over the full temperature range.
NOTE 6: If RD goes low to high, the ADC is internally reset, regardless of the state of $\overline{CS}$ or $\overline{BUSY}$.

TRUTH TABLE FOR STATIC RAM MODE:

INPUTS $\overline{CS}$	INPUTS $\overline{RD}$	OUTPUTS $\overline{BUSY}$	OUTPUTS DB7-DB0	OPERATION
L	H	H	HI-Z	Write Cycle (Start Convert)
L	↓	H	HI-Z to DATA	Read Cycle (Data Read)
L	↑	H	DATA to HI-Z	Reset Converter
H	X(Note 6)	X	HI-Z	Not Selected
L	H	L	HI-Z	No Effect (Converter Busy)
L	↓	L	HI-Z	No Effect (Converter Busy)
L	↑	L	HI-Z	Not Allowed, Conversion Error

TERMINAL CONNECTIONS:

	18 PIN CERDIP	20 LCC		18PIN CERDIP	20 LCC
1	V_{DD}	NC	11	DB2	NC
2	V_{REF}	V_{DD}	12	DB1	DB3
3	B_{OFS}	V_{REF}	13	DB0(LSB)	DB2
4	A_{IN}	B_{OFS}	14	$\overline{BUSY}$	DB1
5	AGND	A_{IN}	15	$\overline{RD}$	DB0(LSB)
6	DB7(MSB)	AGND	16	$\overline{CS}$	$\overline{BUSY}$
7	DB6	DB7(MSB)	17	CLK	$\overline{RD}$
8	DB5	DB6	18	DGND	$\overline{CS}$
9	DB4	DB5	19		CLK
10	DB3	DB4	20		DGND

Package	ORDERING INFORMATION:
18 pin CERDIP	MAX160MJN/883B
20 pin LCC	MAX160MLP/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10**, 11**
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in Table 1.