**SCOPE: 500ksps, 12-bit ADCs with Track/Hold and Reference**

| Device Type | Generic Number |
|---|---|
| 01 | MAX122(x)/883B |

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

| Outline Letter | Mil-Std-1835 | Case Outline | Package Code |
|---|---|---|---|
| YG | CDIP4-T24 | 24 LEAD SIDEBRAZE | Y24 |

**Absolute Maximum Ratings**

$V_{DD}$ to GND ..... -0.3V to 6V
VSS to DGND ..... -0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs/Outputs to DGND ..... -0.3V to ($V_{DD}$ +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +160°C

Continuous Power Dissipation ..... $T_A$=+70°C
24 pin narrow Sidebraxe (derate 14.3mW/°C above +70°C) ..... 1143mW
Junction Temperature $T_J$ ..... +150°C
Thermal Resistance, Junction to Case, ΘJC..... 25°C/W
Thermal Resistance, Junction to Ambient, ΘJA: ..... 70°C/W

**Recommended Operating Conditions**

Ambient Operating Range ($T_A$) ..... -55°C to +125°C
Positive Supply Voltage Range ($V_{CC}$) ..... 4.75V to 5.25V
Negative Supply Voltage Range ($V_{EE}$) ..... -10.8V to -15.75V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

| TEST | Symbol | CONDITIONS<br>-55 °C <=$T_A$<= +125°C<br>$V_{DD}$=+4.75V to +5.25V,<br>$V_{SS}$=-10.8 to -15.75V, $f_{CLK}$=5MHz<br>Unless otherwise specified | Group A Subgroup | Device type | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|---|---|
| **ACCURACY** | | | | | | | |
| Resolution | RES | | 1,2,3 | All | 12 | | Bits |
| Differential Non-linearity Note 1 | DNL | 12-bit no missing codes over temperature range | 1,2,3 | All | | ±1.0 | LSB |
| Integral Non-linearity Note 1 | INL | | 1,2,3 | All | | ±1.0 | LSB |
| Bipolar Zero Error Note 1 | | Code 00..00 to 00..01 transition, near $A_{IN}$=0V | 1,2,3 | All | | ±3.0 | LSB |
| Full-Scale Error Note 1,2 | | Including reference; adjusted for bipolar zero error | 1 | All | | ±8.0 | LSB |
| Power Supply Rejection Ratio (Change in FS, 3/) | PSRR | $V_{DD}$ only, 5V ±5%<br>$V_{SS}$ only, -12V ±10%<br>$V_{SS}$ only, -15V ±5% | 1,2,3 | All | | ±0.75<br>±1.0<br>±1.0 | LSB |
| **ANALOG INPUT** | | | | | | | |
| Input Range | | | 1,2,3 | All | -5 | +5 | V |
| Input Current | | $A_{IN}$=+5V (approvimately 6kΩ to REF) | 1,2,3 | All | | 2.5 | mA |
| Input Capacitance Note 4 | | | 4 | All | | 10 | pF |
| **REFERENCE** | | | | | | | |
| Output Voltage | | No external load, $A_{IN}$=5V | 1 | All | -5.02 | -4.98 | V |
| External Load Regulation | | 0mA<$I_{SINK}$<5mA, $A_{IN}$=0V | 1,2,3 | All | | 5.0 | mV |
| Temperature Drift | | Note 5 | 1,2,3 | All | | ±30 | ppm/°C |
| **DYNAMIC PERFORMANCE** | | fs=333kHz, $A_{IN}$=±5Vp-p, 50kHz | | | | | |
| Signal-to-Noise Plus Distortion | SINAD | | 1<br>2,3 | All | 70<br>69 | | dB |
| Total Harmonic Distortion | THD | First five harmonics | 1<br>2,3 | All | | -78<br>-75 | dB |
| Spurious-Free Dynamic Range | SFDR | | 1<br>2,3 | All | 78<br>75 | | dB |
| **CONVERSION TIME** | | | | | | | |
| Synchronous | $t_{CONV}$ | 13 $t_{CLK}$ | 1,2,3 | All | | 2.60 | µs |
| Clock Frequency | $f_{CLK}$ | | 1,2,3 | All | 0.1 | 5.0 | MHz |
| **DIGITAL INPUTS** | | $\overline{\text{CLKIN}}$, $\overline{\text{CONVST}}$, $\overline{\text{RD}}$, $\overline{\text{CS}}$ | | | | | |
| Input High Voltage | $V_{IH}$ | | 1,2,3 | All | 2.4 | | V |
| Input Low Voltage | $V_{IL}$ | | 1,2,3 | All | | 0.8 | V |
| Input Capacitance | | NOTE 4 | 4 | All | | 10 | pF |
| Input Current | | $V_{IN}$=0V or $V_{DD}$ | 1,2,3 | All | | ±5 | µA |

| TEST | Symbol | CONDITIONS<br>-55 °C <=$T_A$<= +125°C<br>$V_{DD}$=+4.75V to +5.25V,<br>$V_{SS}$=-10.8 to -15.75V, $f_{CLK}$=5MHz<br>Unless otherwise specified | Group A Subgroup | Device type | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|---|---|
| **DIGITAL OUTPUT** | | $\overline{\text{D11-D0, INT/BUSY}}$ | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$=1.6mA | 1,2,3 | All | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$=1mA | 1,2,3 | All | $V_{DD}$-0.5 | | V |
| Leakage Current | $I_{LKG}$ | $V_{IN}$=0V or $V_{DD}$, D11-D0 | 1,2,3 | All | | ±5 | µA |
| Output Capacitance | | NOTE 4 | 4 | All | | 10 | pF |
| **POWER REQUIREMENTS** | | | | | | | |
| Positive Supply Voltage | $V_{DD}$ | Guaranteed by supply rejection test | 1,2,3 | All | 4.75 | 5.25 | V |
| Negative Supply Voltage | $V_{SS}$ | Guaranteed by supply rejection test | 1,2,3 | All | -10.80 | -15.75 | V |
| Positive Supply Current 6/ | $I_{DD}$ | $V_{DD}$=5.25V, $V_{SS}$=-15.75V, $A_{IN}$=0V | 1,2,3 | All | | 15 | mA |
| Negative Supply Current 6/ | $I_{SS}$ | $V_{DD}$=5.25V, $V_{SS}$=-15.75V, $A_{IN}$=0V | 1,2,3 | All | | 20 | mA |
| Power Dissipation 6/ | | $V_{DD}$=5V, $V_{SS}$=-12V, $A_{IN}$=0V | 1,2,3 | All | | 315 | mW |
| **TIMING CHARACTERISTICS** 7/ | | $V_{DD}$=+5V, $V_{SS}$=-12V to -15V<br>Unless otherwise specified | | | | | |
| $\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time | $t_{CS}$ | | 9,10,11 | All | 0 | | ns |
| $\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time | $t_{CH}$ | | 9,10,11 | All | 0 | | ns |
| $\overline{\text{CONVST}}$ Pulse Width | $t_{CW}$ | | 9,10,11 | All | 30 | | ns |
| $\overline{\text{RD}}$ Pulse Width | $t_{RW}$ | | 9,10,11 | All | $t_{DA}$ | | ns |
| Data-Access Time | $t_{DA}$ | CL=100pF | 9<br>10,11 | All | | 75<br>120 | ns |
| Bus-Relinquish Time | $t_{DH}$ | | 9<br>10,11 | All | | 50<br>80 | ns |
| $\overline{\text{RD}}$ or $\overline{\text{CONVST}}$ to $\overline{\text{BUSY}}$ | $t_{B0}$ | CL=50pF | 9<br>10,11 | All | | 75<br>120 | ns |
| CLKIN to $\overline{\text{BUSY}}$ or $\overline{\text{INT}}$ | $t_{B1}$ | CL=50pF | 9<br>10,11 | All | | 110<br>180 | ns |
| CLKIN to $\overline{\text{BUSY}}$ Low | $t_{B2}$ | In mode 5 | 9<br>10,11 | All | | 90<br>150 | ns |
| $\overline{\text{RD}}$ to $\overline{\text{INT}}$ High | $t_{IH}$ | CL=50pF | 9<br>10,11 | All | | 50<br>90 | ns |
| $\overline{\text{BUSY}}$ or $\overline{\text{INT}}$ to Data Valid | $t_{BD}$ | $\overline{\text{INT}}$, $\overline{\text{BUSY}}$)=50pF<br>CL(Data)=100pF | 9<br>10,11 | All | | 20<br>35 | ns |
| Acquisition Time | $t_{AQ}$ | NOTE 4 | 9<br>10,11 | All | 350<br>400 | | ns |

NOTE 1: These tests are performed at $V_{DD}$=5V, $V_{SS}$=-15V. Operation over supply is guaranteed by supply rejection tests.

NOTE 2: Ideal full-scale transition is at +5V -3/2LSB=+4.9963V, adjusted for offset error.

NOTE 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage=(FS at nominal supply)-(FS at nominal supply ± tolerance), expressed in LSBs.

NOTE 4: For design guidance only, not tested.

NOTE 5: Temperature drift is defined as the change in output voltage from +25°C to $T_{MIN}$ or $T_{MAX}$. It is calculated as TC=(ΔREF/VREF)/(ΔT)

NOTE 6: $\overline{CS}$=$\overline{RD}$=$\overline{CONVST}$=0V, MODE=5V

NOTE 7: Control inputs specified with $t_r$=$t_f$=5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Commercial datasheet, Figures 1 and 2 for load circuits.

| **Package** | **ORDERING INFORMATION:** |
|---|---|
| 24 pin Sidebraze | MAX122BMYG/883B |
| | |

**TERMINAL CONNECTIONS**:

| | |
|---|---|
| | YG24 |
| 1 | MODE |
| 2 | $V_{SS}$ |
| 3 | $V_{DD}$ |
| 4 | $A_{IN}$ |
| 5 | VREF |
| 6 | AGND |
| 7 | D11 |
| 8 | D10 |
| 9 | D9 |
| 10 | D8 |
| 11 | D7 |
| 12 | DGND |
| 13 | D6 |
| 14 | D5 |
| 15 | D4 |
| 16 | D3 |
| 17 | D2 |
| 18 | D1 |
| 19 | D0 |
| 20 | $\overline{CONVST}$ |
| 21 | CLKIN |
| 22 | $\overline{INT/BUSY}$ |
| 23 | $\overline{CS}$ |
| 24 | $\overline{RD}$ |

**QUALITY ASSURANCE**

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

| Mil-Std-883 Test Requirements | Subgroups per Method 5005, Table 1 |
|---|---|
| Interim Electric Parameters Method 5004 | 1 |
| Final Electrical Parameters Method 5005 | 1*, 2, 3, 9, 10, 11 |
| Group A Test Requirements Method 5005 | 1, 2, 3, 9, 10, 11 |
| Group C and D End-Point Electrical Parameters Method 5005 | 1 |

* PDA applies to Subgroup 1 only.