Click here to ask an associate for production status of specific part numbers.

5.5V Input, 4.5A Switching Current High Efficiency Buck-Boost Converter

MAX77847

General Description

The MAX77847 is a highly efficient high-performance buck-boost regulator with an industry-leading quiescent current of 14µA targeted for battery-powered applications. It supports an input voltage range from 1.8V to 5.5V and an output voltage range from 1.8V to 5.2V. The IC provides two programmable switching current limits to optimize external component sizing based on load requirements. Analog Devices' unique buck-boost controller technology provides high efficiency, excellent load and line transient performance, and a seamless mode transition across the input and output range.

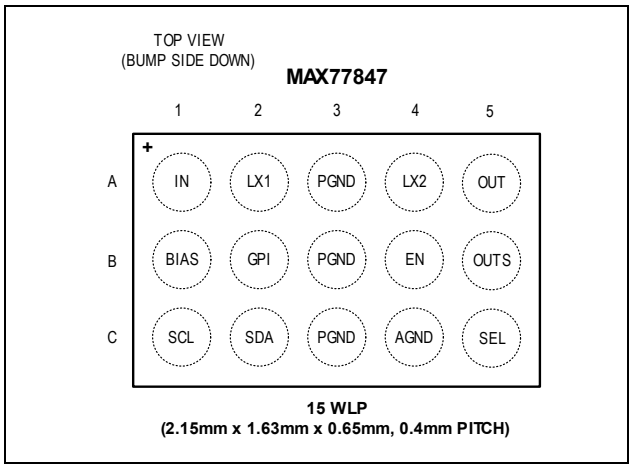
The device features a hardware configuration SEL pin which configures the default output voltage and I²C target address. A hardware dynamic voltage scaling (DVS) pin allows the user to change the output voltage between two output voltages without I²C interference. The I²C interface is optional and allows users to adjust the output voltage with 50mV steps.

The MAX77847 is available in a 2.18mm x 1.66mm 15-bump wafer-level package (WLP).

Key Applications

- 5G PA Supply
- Battery Power Equipment
- Internet of Things (IoT) Devices
- System Power Pre-Regulation
- Smartphones ToF/Facial and Gesture Recognition

Pin Configuration



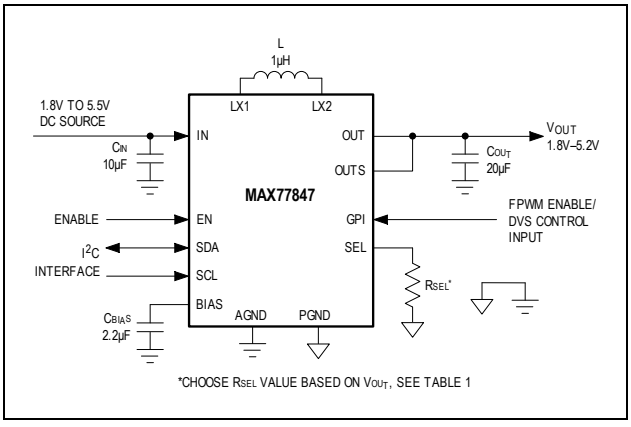
15 WLP
(2.15mm x 1.63mm x 0.65mm, 0.4mm PITCH)

Benefits and Features

- Flexible System Integration
  - 1.8V to 5.5V Input Voltage Range
  - 1.8V to 5.2V (50mV steps) Output Voltage Range
  - 4.5A/3.6A Switching Current Limit
  - 14µA Ultra-Low I_Q
- I²C Interface
  - Programmable Output Voltage
  - Programmable Output Slew Rate (DVS)
  - Forced PWM Mode Operation (FPWM)
  - Output Active Discharge
- I²C configurable GPI Pin
  - External FPWM Enable Input
  - DVS Control Input
- SEL Pin to Configure Device
  - Default Start-Up Voltage (16 Options)
  - I²C Target Address (2 Options)
- Soft-Start

Refer to ***Product Highlights*** for more details.

Simplified Application Diagram



***Ordering Information* appears at end of data sheet**

19-101705; Rev 0; 9/23

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Absolute Maximum Ratings

IN, OUT, BIAS, LX1, LX2 to PGND .....-0.3V to +6.0V

EN, GPI, SEL, SCL, SDA to AGND ..... -0.3V to V_{BIAS} + 0.3V

PGND to AGND.....-0.3V to +0.3V

OUTS to AGND .....-0.3V to +6.0V

Continuous Power Dissipation at T_A = 70˚C (Derate 16.22 mW/˚C above +70˚C) ((Note 1))..... +1297.65mW

Maximum Junction Temperature..... +150˚C

Storage Temperature Range .....-65˚C to +150˚C

Soldering Temperature (Reflow) ..... +260˚C

Note 1: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a FR-4, four-layer board. For detailed information on package thermal considerations, refer to http://www.maximintegrated.com/thermal-tutorial

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

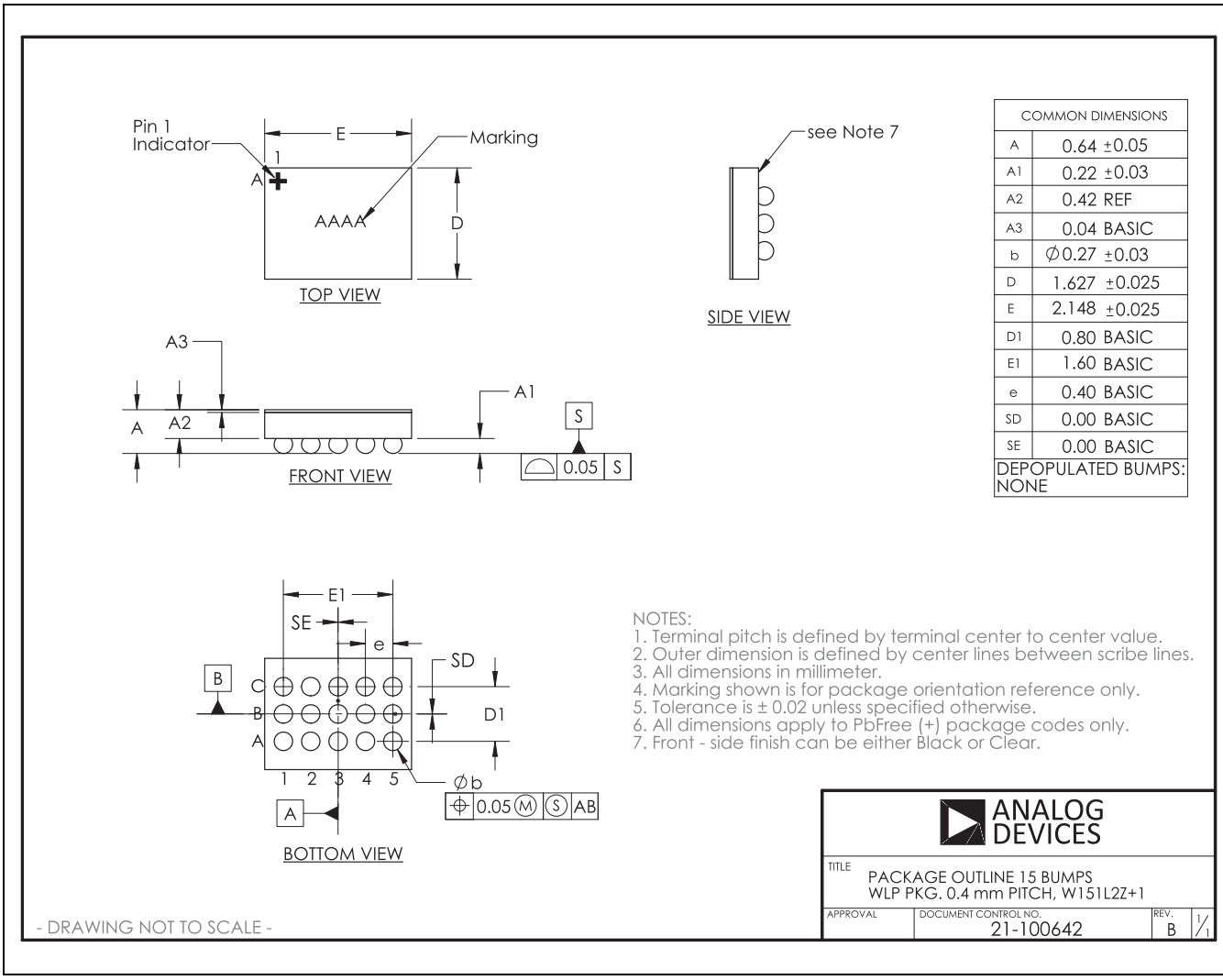
Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE
Input Voltage Range	V_{IN}	$V_{IN} \geq 2.3V$ or $V_{OUT} \geq 2.3V$	1.8V to 5.5V
Output Voltage Range	V_{OUT}	$V_{IN} \geq 2.3V$ or $V_{OUT} \geq 2.3V$	1.8V to 5.2V
Output Current Range	I_{OUT}	Maximum Output Current limited by Switching Current limit and Input Under Voltage Lockout (UVLO).	0A to 3A
Junction Temperature Range	T_J	—	-40˚C to +125˚C

Package Information

15 WLP

Package Code	W151L2Z+1
Outline Number	21-100642
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	61.65 °C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.22 ±0.03
A2	0.42 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	1.627 ±0.025
E	2.148 ±0.025
D1	0.80 BASIC
E1	1.60 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 15 BUMPS
WLP PKG. 0.4 mm PITCH, W151L2Z+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100642	B	1/1

Electrical Characteristics

($T_A \approx T_J$, V_{IN} = 3.8V, V_{OUT} = 3.3V, R_{SEL} = AGND, Typicals are at $T_A \approx T_J$ = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77847 is tested under pulsed load conditions such that $T_A \approx T_J$. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL INPUT SUPPLY						
Operating Input Voltage Range	V_{IN}		1.8		5.5	V
Input UVLO Voltage	V_{UVLO_rising}	Input rising	1.70	1.75	1.8	V
Input UVLO Hysteresis	V_{UVLO_Hys}	$V_{UVLO\_rising} - V_{UVLO\_falling}$		150		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = -40°C to +85°C			2	µA
Input Quiescent Current	I_Q	EN = HIGH, FPWM = LOW, T_J = -40°C to +85°C and no switching		14	30	µA
		EN = HIGH, FPWM = HIGH, T_J = -40°C to +85°C		3		mA
Turn-On Delay Time	T_{DLY_ON}	From EN HIGH to R_{SEL} reading (*Note 2*)		100		µs
R_{SEL} Reading Time	T_{RSEL}	(*Note 2*)	360	450	600	µs
BUCK-BOOST CONVERTER						
Output Voltage Range	V_{OUT}		1.8		5.2	V
Output Voltage Accuracy	V_{OUT_ACC}	FPWM enabled, no load, V_{OUT} = 3.3V, R_{SEL} = short to AGND	-1.5		+1.5	%
		Auto skip mode, no load, V_{OUT} = 3.3V, R_{SEL} = short to AGND	-1.5		+4.0	
Switching Frequency	f_{SW}		1.93	2.2	2.47	MHz
High-Side Switching Current Limit	I_{LIM}	I_{LIM} = 0b	4	4.5	4.95	A
		I_{LIM} = 1b	3.24	3.6	3.96	
Low-Side Switch On Resistance	R_{DSON_LOW}	LX1, LX2		58		mΩ
High-Side Switch On Resistance	R_{DSON_HIGH}	LX1, LX2		55		mΩ
Thermal Shutdown Threshold	T_{SHDN}	T_J rising (*Note 3*)		150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}	T_{SHDN_R} - T_{SHDN_F} (*Note 3*)		15		°C
Active Discharge Resistance	R_{DSCHG}			100		Ω
Minimum Effective Output Capacitance	C_{EFF_MIN}	(Note 2)		6.8		µF
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 1.8V to 5.5V, FPWM enabled, no load, V_{OUT} = 3.3V, R_{SEL}= short to AGND	-0.3		+0.3	%/V
Soft-Start Timeout	T_{SS}	(*Note 3*)		4		ms
Overvoltage Protection Threshold	V_{OVP}	V_{OUT}-V_{OUTS}		0.5		V
EN, GPI LOGIC LEVEL						
Input LOW Level	V_{IL}				0.4	V
Input HIGH Level	V_{IH}		1.3			V
EN Pin Internal Pulldown Resistance	R_{PD}			800		kΩ

Electrical Characteristics—I²C Serial Interface

($T_A \approx T_J$, V_{IN} = 3.8V, V_{OUT} = 3.3V, R_{SEL} = AGND, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25ºC. The MAX77847 is tested under pulsed load conditions such that $T_A \approx T_J$. Limits over the operating temperature range (T_J = -40ºC to +125ºC) and relevant voltage range are guaranteed by design and characterization using statistical process control methods.)

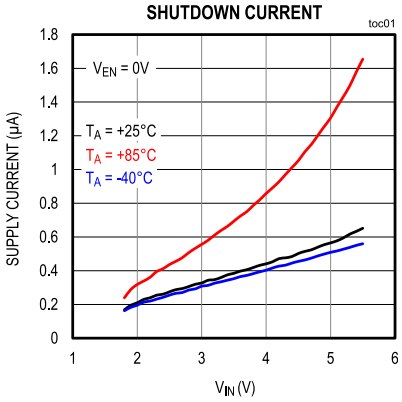
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}		1.4			V
SCL, SDA Input LOW Voltage	V_{IL}				0.4	V
SCL, SDA Input Hysteresis	V_{HYS}	(*Note 3*)		0.1		V
SDA Output LOW Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
SCL, SDA Input Capacitance	C_I				10	pF
SCL, SDA Input Leakage Current	I_{LK}		-10		+10	µA
TIMING (FAST-MODE PLUS)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.26			µs
DATA Setup Time	T_{SU_DATA}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Capacitance	C_B	(*Note 3*)			550	pF

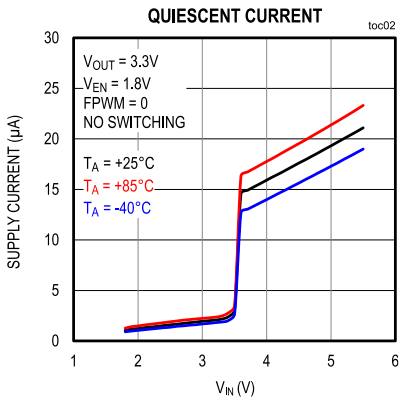
Note 2: Internal design target. Not production tested.

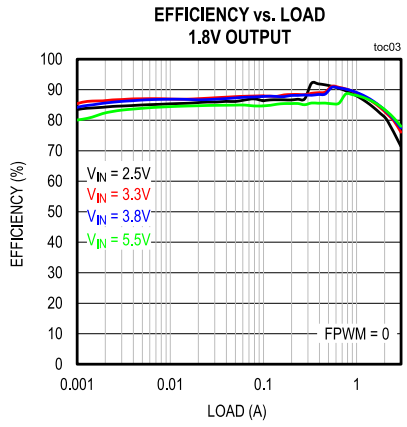
Note 3: Characterized by ATE or bench test. Not production tested.

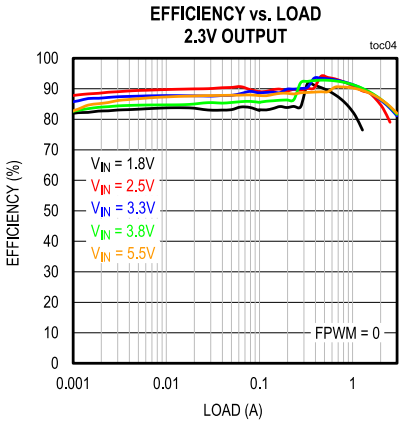
Typical Operating Characteristics

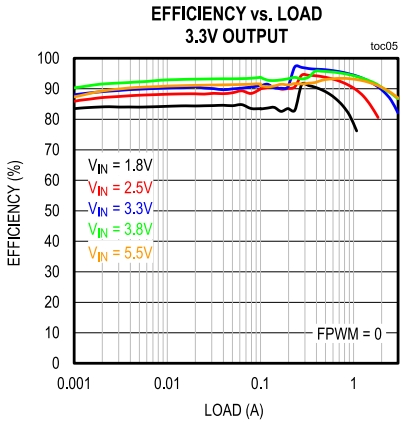
(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Samsung CIGT252010EH1R0M), Skip Mode, T_A = +25°C, unless otherwise noted.)

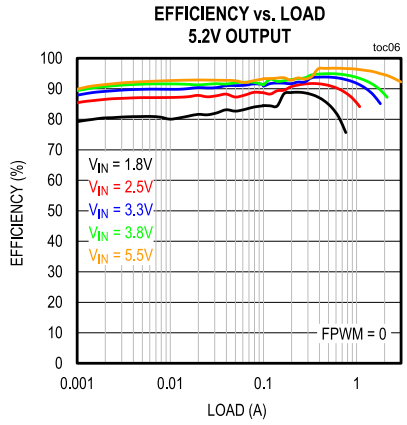


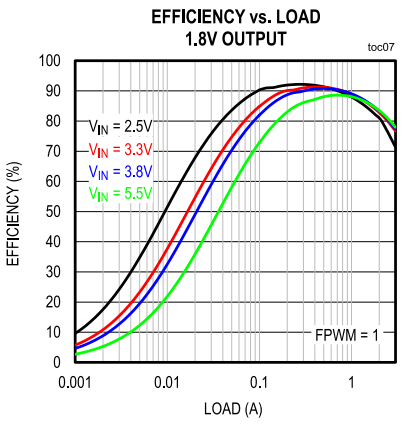


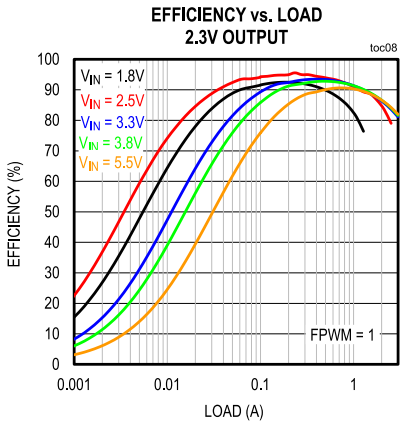


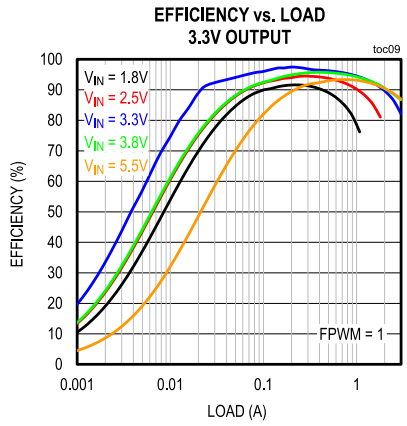






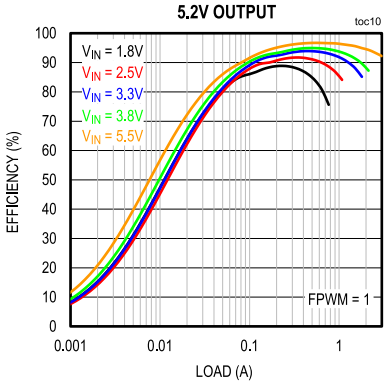




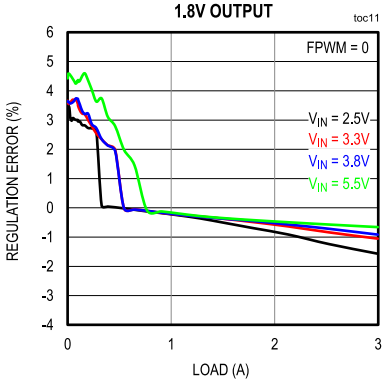


(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Samsung CIGT252010EH1R0M), Skip Mode, T_A = +25°C, unless otherwise noted.)

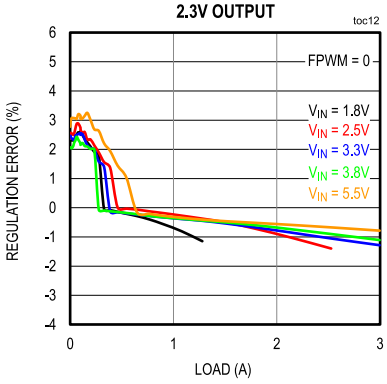
EFFICIENCY vs. LOAD
5.2V OUTPUT



LOAD REGULATION
1.8V OUTPUT



LOAD REGULATION
2.3V OUTPUT



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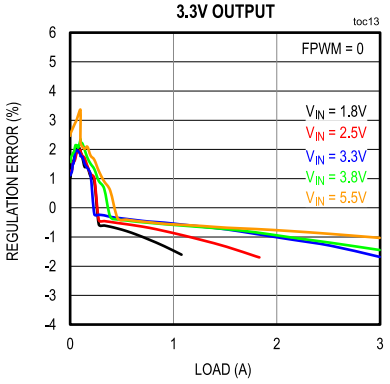
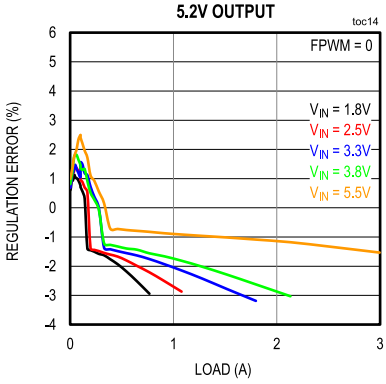
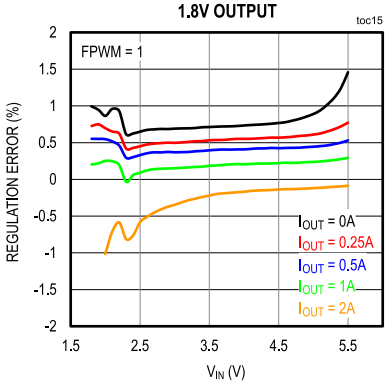
3.3V OUTPUT



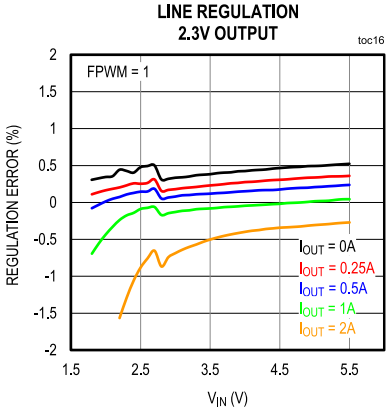
LOAD REGULATION
5.2V OUTPUT



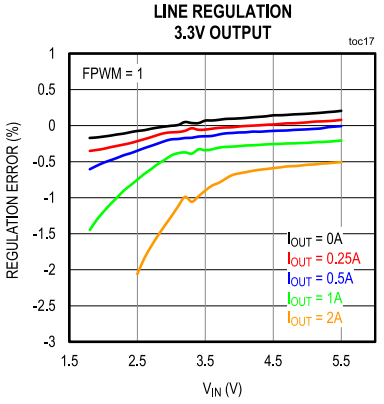
LINE REGULATION
1.8V OUTPUT



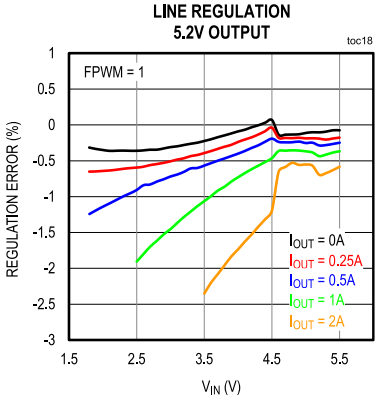
LINE REGULATION
2.3V OUTPUT



LINE REGULATION
3.3V OUTPUT

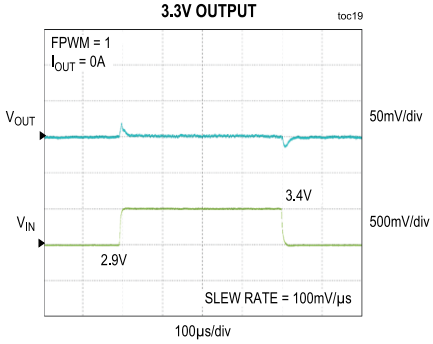


LINE REGULATION
5.2V OUTPUT

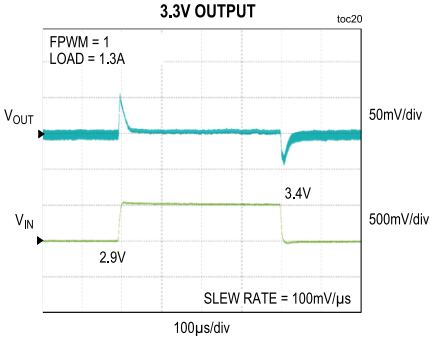


(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Samsung CIGT252010EH1R0M), Skip Mode, T_A = +25°C, unless otherwise noted.)

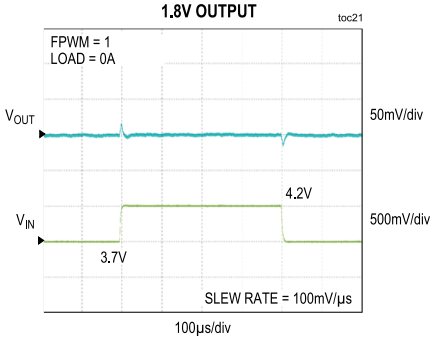
LINE TRANSIENT RESPONSE 3.3V OUTPUT



LINE TRANSIENT RESPONSE 3.3V OUTPUT



LINE TRANSIENT RESPONSE 1.8V OUTPUT



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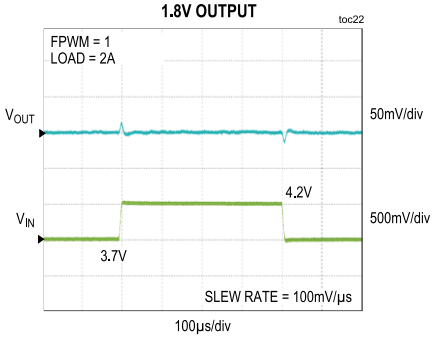
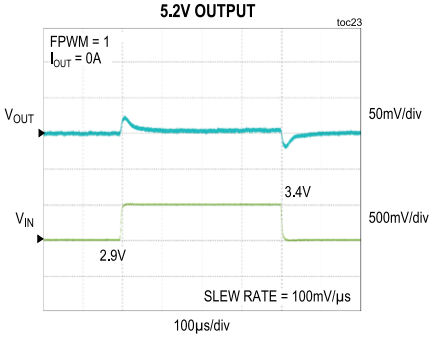
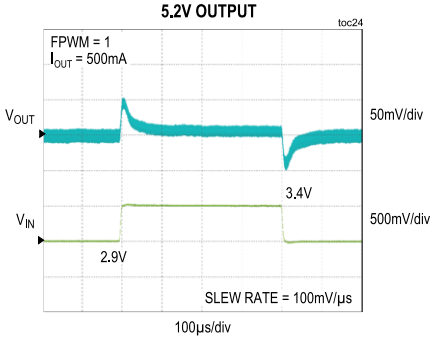


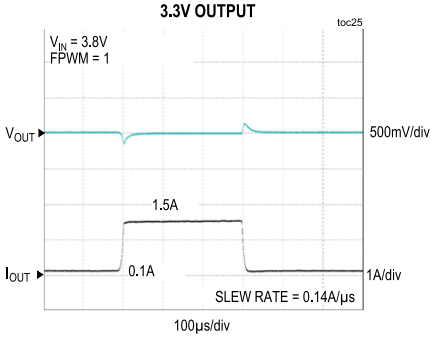
LINE TRANSIENT RESPONSE 5.2V OUTPUT



LINE TRANSIENT RESPONSE 5.2V OUTPUT



LOAD TRANSIENT RESPONSE 3.3V OUTPUT



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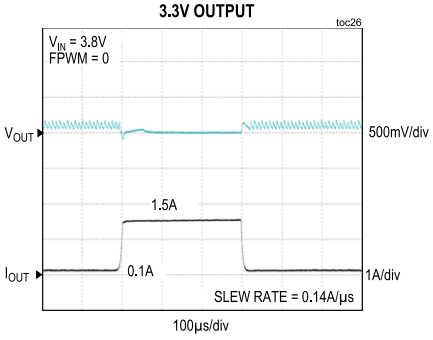
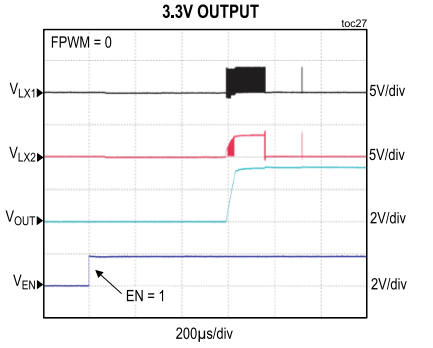
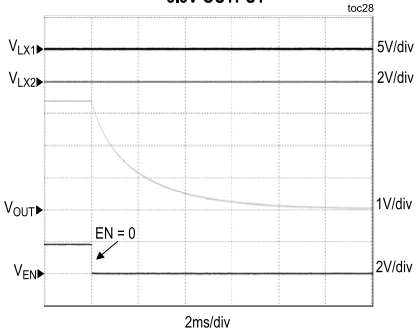


ENABLE STARTUP WAVEFORM 3.3V OUTPUT

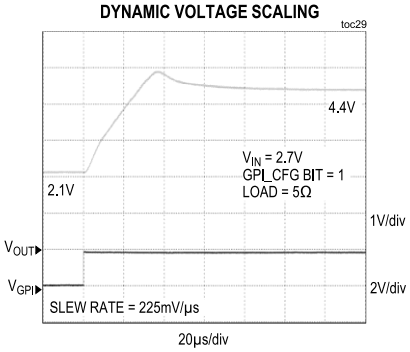


(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Samsung CIGT252010EH1R0M), Skip Mode, T_A = +25°C, unless otherwise noted.)

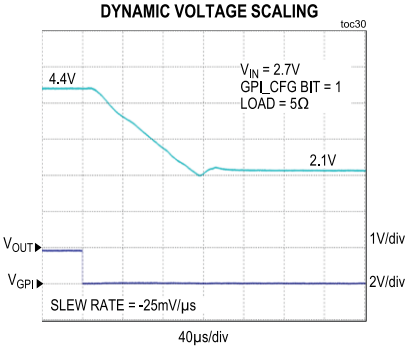
ENABLE SHUTDOWN WAVEFORM 3.3V OUTPUT



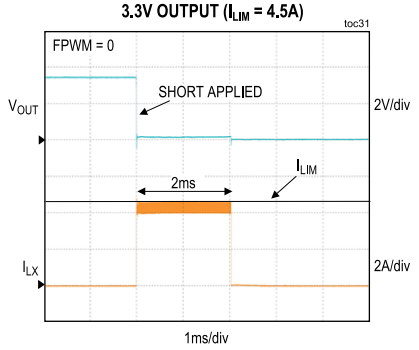
DYNAMIC VOLTAGE SCALING



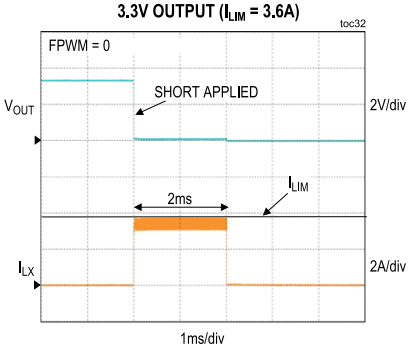
DYNAMIC VOLTAGE SCALING



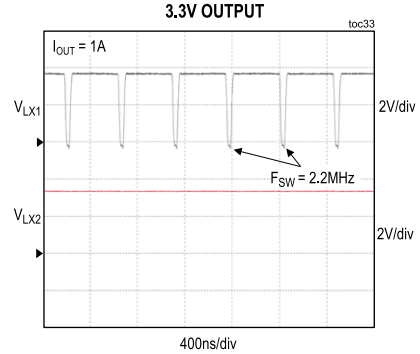
SHORT-CIRCUIT RESPONSE 3.3V OUTPUT (I_{LIM} = 4.5A)



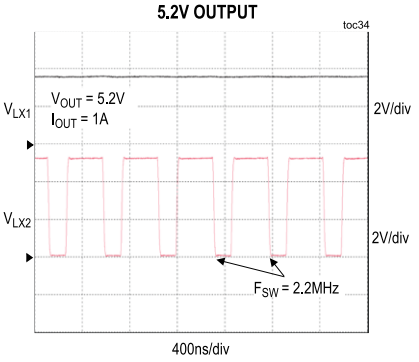
SHORT-CIRCUIT RESPONSE 3.3V OUTPUT (I_{LIM} = 3.6A)



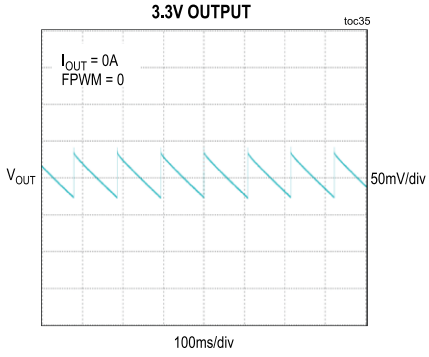
SWITCHING WAVEFORM 3.3V OUTPUT



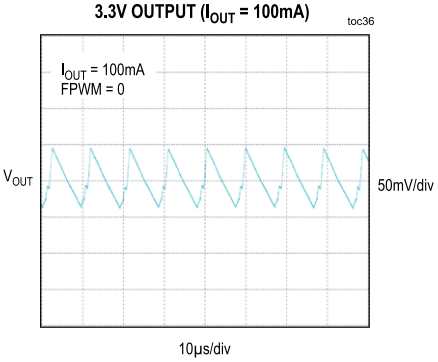
SWITCHING WAVEFORM 5.2V OUTPUT



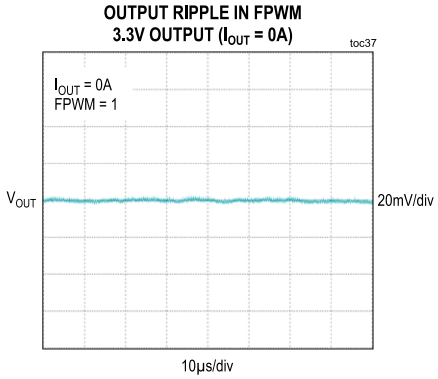
OUTPUT RIPPLE IN SKIP MODE 3.3V OUTPUT

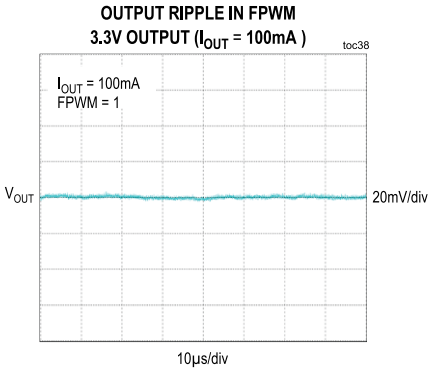


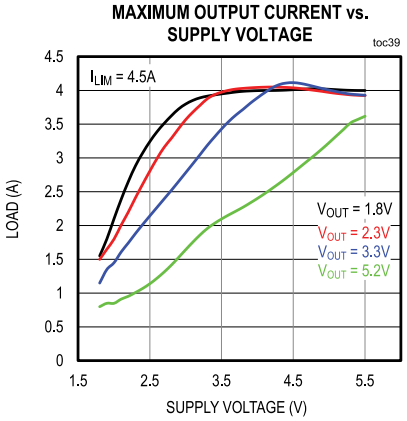
OUTPUT RIPPLE IN SKIP MODE 3.3V OUTPUT (I_{OUT} = 100mA)

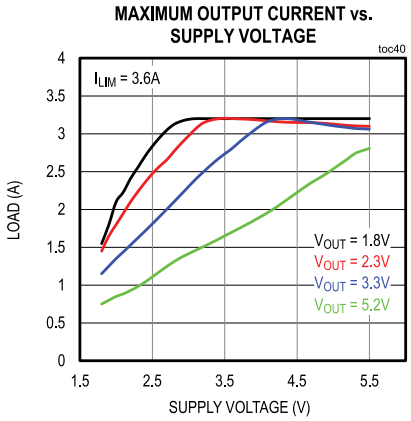


(V_{IN} = 3.8V, V_{OUT} = 3.3V, L = 1µH (Samsung CIGT252010EH1R0M), Skip Mode, T_A = +25°C, unless otherwise noted.)

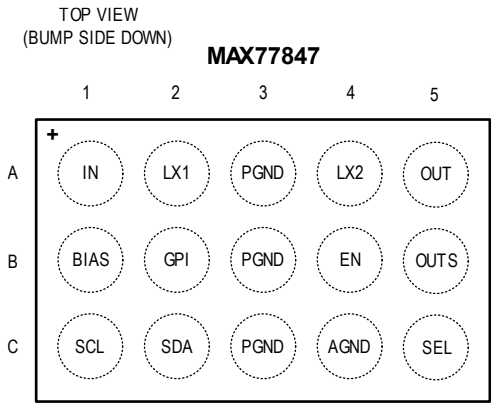








Pin Configurations

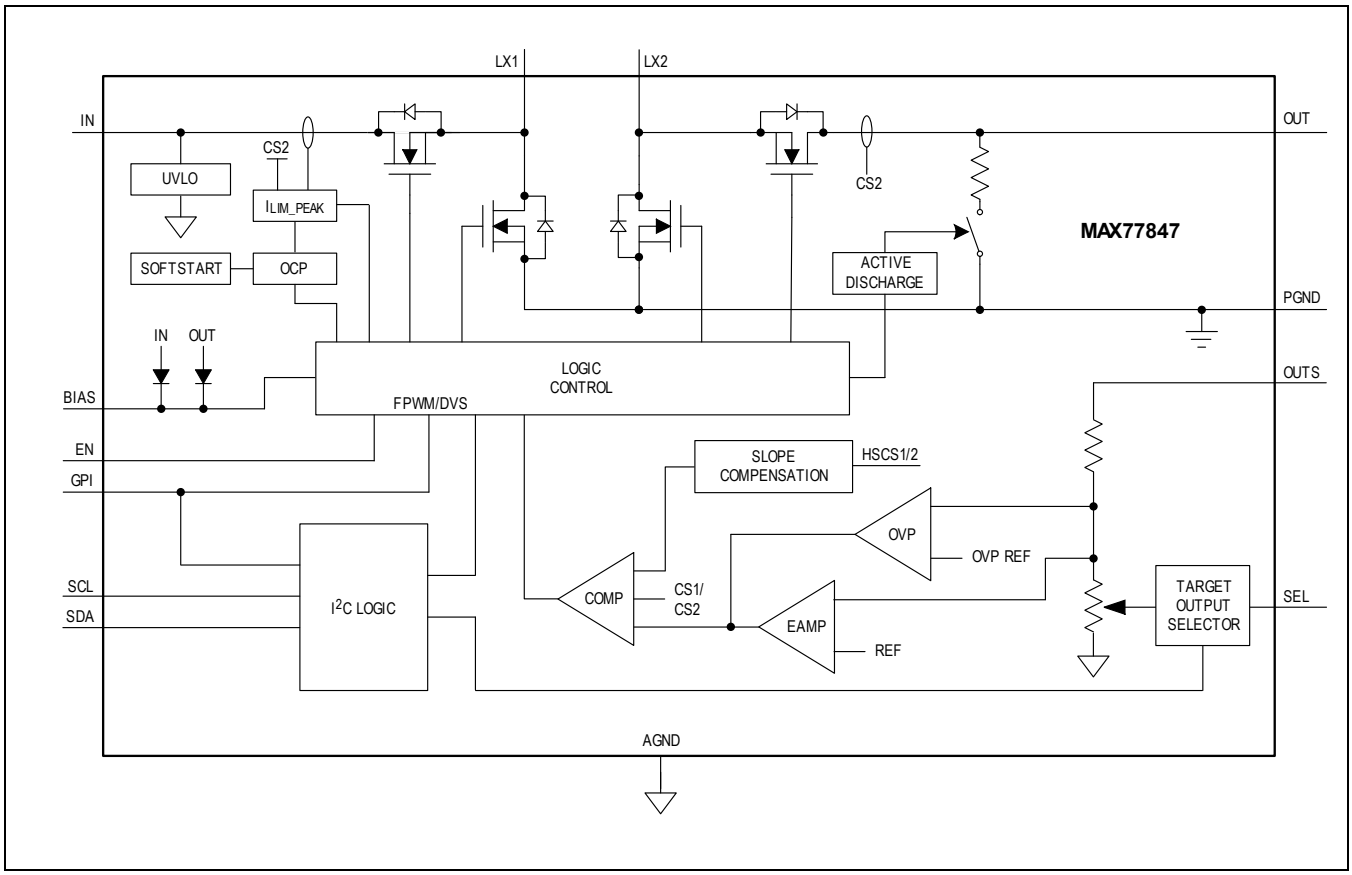


15 WLP
(2.15mm x 1.63mm x 0.65mm, 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION	Type
A1	IN	Buck-Boost Input. Bypass to PGND with 2x 10V 10µF X7R ceramic capacitor.	Power Input
A2	LX1	Input-Side Buck-Boost Switching Node.	Power
A3, B3, C3	PGND	Power Ground.	Ground
A4	LX2	Output-Side Buck-Boost Switching Node.	Power
A5	OUT	Buck-Boost Power Output. Bypass to PGND with 2x 10V X7R 10µF ceramic capacitor.	Power Output
B1	BIAS	Internal Bias Supply. Bypass to AGND with a 10V 2.2µF X7R ceramic capacitor. Do not load this pin externally.	Analog
B2	GPI	General Purpose Input Pin. Forced PWM mode control input (default) or DVS control input.	Digital Input
B4	EN	Buck-Boost Enable Input.	Digital Input
B5	OUTS	Buck-Boost Output Voltage Sense Input. Connect to the output at the point of load.	Analog Input
C1	SCL	I^2C Clock Input (Hi-Z in OFF State). This pin requires a pullup resistor to the system IO supply voltage. Connect to AGND if not used.	Digital Input
C2	SDA	I^2C Data I/O (Hi-Z in OFF state). This pin requires a pullup resistor to system IO supply. Connect to AGND if not used.	Digital I/O
C4	AGND	Analog Ground.	Ground
C5	SEL	Device Configuration Pin. Connect a resistor between this pin and AGND to configure output voltage and device target address. See SEL Pin Configuration section.	Analog Input

Functional Diagrams



Detailed Description

The MAX77847 is a low quiescent current, high-efficiency buck-boost converter with a wide input voltage range (1.8V to 5.5V) for single-cell Li-Ion batteries, two-cell Alkaline batteries, or $LiSOCl_2$ batteries. The converter features an output voltage range from 1.8V to 5.2V with 50mV steps. The converter seamlessly transitions between buck and boost modes of operation. An I^2C adjustable peak current limit lets the user maximize board space across various systems based on load requirements by allowing flexible inductor sizing. The device also provides a general-purpose input (GPI) pin, which can be configured as an FPWM to enable input or DVS control input through the I^2C interface. The active discharge function discharges the charge on the output capacitor when the device is disabled and stops switching.

The device is equipped with thermal shutdown and cycle-by-cycle switching current limit to protect the system and the device. The MAX77847 is available in a 2.18mm x 1.66mm 15-bump WLP package.

Startup and Shutdown

Startup

When the EN pin is set to high, the IC turns on the internal bias circuitry which typically takes 100µs (T_{ON_DLY}) to settle. For the MAX77847A (MAX77847B), the EN[0] bitfield in CFG(0x01) register is set to 0b0 (0b1) by default. When EN[0] is set to 0b1 through I^2C, the controller senses the SEL pin resistance to set the reference voltage. The R_{SEL} reading takes about 450µs (T_{SEL}). After the IC reads the R_{SEL} value, it begins the soft-start process. To limit the inrush current during startup, the device reduces the switching current limit level (I_{LIM_SS}) to about half of the I_{LIM}. Soft-start time ends when the output voltage reaches the target regulation point (90% of V_{TARGET}). After an additional 100µs of transition time, the device switches to normal switching control (Skip mode/FPWM) increasing the switching current limit to I_{LIM}. Note that the part operates in FPWM for the entire duration of the soft start time. Setting the switching current limit post startup is described in the *Switching Current Limit* section. The part operates in Skip Mode by default post startup but can be set to operate in FPWM mode as outlined in the *SKIP Mode and Forced-PWM (FPWM) Mode* section.

The device is equipped with a Soft-Start Time Out Timer (T_{SS} = 4ms(typ)), and if the output voltage does not reach the target regulation point (90% of V_{TARGET}) when the T_{SS} expires, the IC latches off and does not start up until EN pin or EN[0] bitfield, or V_{IN} is cycled. **Note:** The minimum output voltage the converter can start with is 2.3V, as shown in *Table 1*.

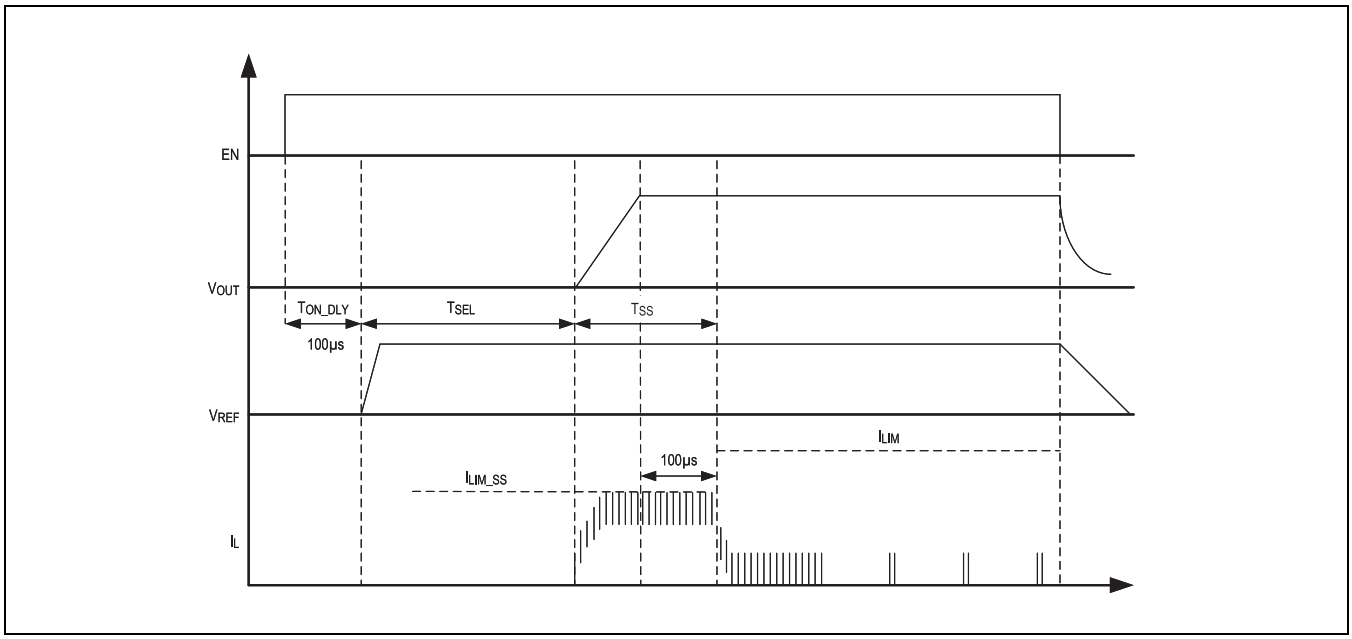


Figure 1. Startup Waveform

Immediate Shutdown Conditions

The converter stops switching whenever the MAX77847 is disabled by EN[0] bitfield or the EN pin is pulled low or is latched off by protections. After the converter stops switching, the MAX77847 turns on the active discharge switch between OUT and PGND to quickly discharge the output capacitor.

Several conditions cause the latch off, regardless of EN[0] bitfield or EN pin state;

1. *Thermal shutdown* (T_{SHDN})
2. Soft-start timeout (T_{SS})
3. Continuous I_{LIM} events for about 2ms (typ)
4. *Undervoltage Lockout* (UVLO)

The events in this category shutdown the output until fault conditions are removed from the system and V_{IN} or EN[0] bitfield or EN pin is cycled. See the *Protections* section for more details about the features listed above.

Active Discharge

The device features an active discharge resistor which quickly discharges the output voltage when the device is turned off. When the MAX77847 is disabled by the bitfield EN[0] or any protection, an internal 100Ω switch for the output active discharge function is turned ON and provides a path to discharge the energy stored in the output capacitor to PGND. While the MAX77847 is enabled, the internal switch for active discharge is disconnected from the output. The active discharge resistor can be disabled through I^2C using the AD[0] bitfield in the CFG(0x01) register.

General Purpose Input (GPI)

The GPI hardware pin can be configured either as a DVS or FPWM control pin through I^2C. When the GPI_CFG[0] bitfield in the CFG(0x01) register is set to 0b0, the GPI pin acts as an input to transition the part from Skip to FPWM mode. See the *Skip Mode and Forced-PWM (FPWM) mode* section for more information. When the GPI_CFG[0] bitfield is set to 0b1, the GPI pin acts as a DVS input. See the *Dynamic Voltage Scaling (DVS)* section for more information.

Buck-Boost Regulator

The MAX77847 utilizes a four-switch H-bridge architecture to operate in buck, boost and buck-boost mode. This topology maintains output voltage regulation over the entire input voltage range and ensures a smooth transition between the operating modes based on V_{IN} and V_{OUT}. The buck-boost regulator is ideal for operating in single-cell Li-ion battery-powered applications, providing a low quiescent current I_Q and output voltage between 1.8V and 5.2V. A fast switching frequency of 2.2MHz and a unique control algorithm allow small external components, low output noise, and high efficiency across the entire operating range.

Buck- Boost Control Scheme

The buck-boost converter uses a 2.2MHz fixed-frequency pulse width modulation (PWM) control scheme with current-mode compensation. The architecture integrates four FETs operating as switches: an input high-side FET (HS1), an input low-side FET (LS1), an output high-side FET (HS2), and an output low-side FET (LS2). A proprietary algorithm controls these switches in four different phases:

- Phase 1 (Φ1): HS1 and LS2 Switch on to store energy in the inductor by ramping up inductor current at a rate determined by the input voltage and the inductance: $dI_L/dt = V_{IN}/L$
- Phase 2 (Φ2): HS1 and HS2 switch on to either charge or discharge the inductor, depending on the input and output voltage difference. In boost mode, $V_{OUT} > V_{IN}$ and the inductor current ramps down. In buck mode, $V_{IN} > V_{OUT}$ and the inductor current ramps up: $dI_L/dt = (V_{IN} - V_{OUT})/L$
- Phase 3 (Φ3): LS1 and HS2 switch on to discharge the inductor by ramping down the inductor current at a rate determined by the output voltage and the inductance: $dI_L/dt = -V_{OUT}/L$
- Phase 4 (Φ4): LS1 and LS2 switch on to disconnect the inductor from the output and input voltages.

Soft-start utilizes Φ1 and Φ3 to ramp the output voltage up.

Boost mode ($V_{IN} < V_{OUT}$) utilizes Φ1 and Φ2 within a single clock period. See *Figure 2*. Buck mode ($V_{IN} > V_{OUT}$) utilizes Φ2 and Φ3 within a single clock period. See *Figure 2*. The buck-boost converter utilizes a proprietary 2-phase control topology to transition between Buck and Boost modes seamlessly.

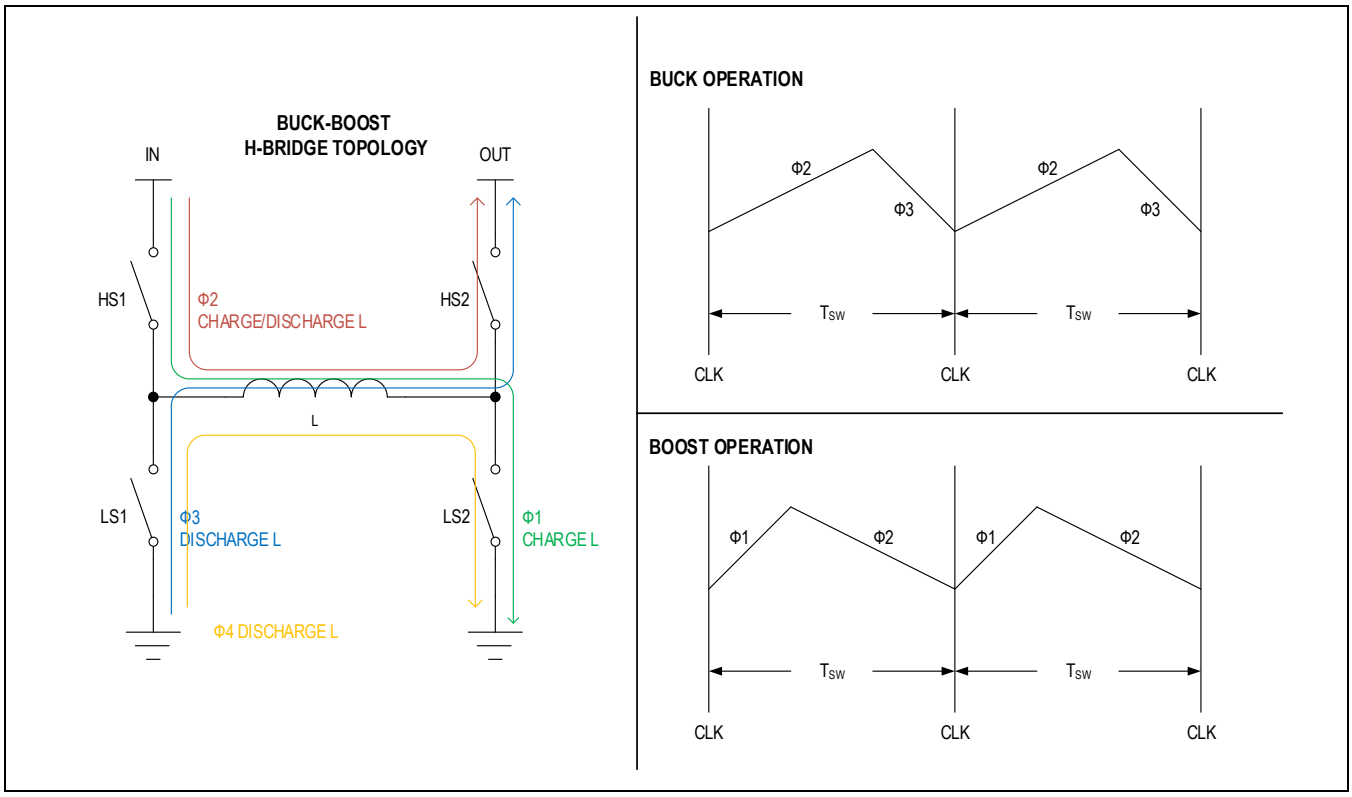


Figure 2. Buck-Boost H-Bridge Topology

SKIP Mode and Forced-PWM (FPWM) Mode

The MAX77847 supports SKIP mode operation for improving light load efficiency. The IC automatically enters SKIP mode operation at no load or light load conditions. In SKIP mode, output voltage V_{OUT} is regulated between SKIP mode upper threshold (V_{SKIP_UPPER}) and lower threshold (V_{SKIP_LOWER}), which are typically 75mV and 25mV above output voltage target (V_{TARGET}), respectively. The output voltage controls the device switching in SKIP mode. The part continues switching until V_{SKIP_UPPER} is reached and then uses Phase 4 (Φ4) to discharge the inductor current until the output voltage drops to V_{SKIP_LOWER}. See *Figure 3* for a typical Skip mode waveform. The IC automatically transitions from SKIP mode to PWM mode depending on the output load condition and input/output voltage ratio.

The device can be set to enter PWM mode regardless of load by writing 0b1 to the bitfield FPWM[0] in CFG(0x01) register through the I²C serial interface or by pulling the GPI pin high when the GPI pin is programmed to the FPWM feature by writing 0b0 to bitfield GPI_CFG[0] in CFG (0x01) register . See the *General Purpose Input (GPI)* section for more information. Forced-PWM (FPWM) mode benefits applications where the lowest output ripple is required, whereas SKIP mode helps maximize the buck-boost regulator's efficiency at light loads.

Regardless of the FPWM[0] bitfield setting, the IC enters FPWM mode when V_{OUT} is changed to a different V_{TARGET} (DVS) to quickly transition to the new output voltage. During DVS events that transition from a higher V_{OUT} to a lower one while operating in Skip mode, the IC enters FPWM mode when V_{OUT} falls to the old V_{TARGET} and stays in FPWM mode until V_{OUT} reaches the new V_{TARGET}. After the FPWM mode for DVS stops, the power converter resumes regulation based on Skip/FPWM mode.

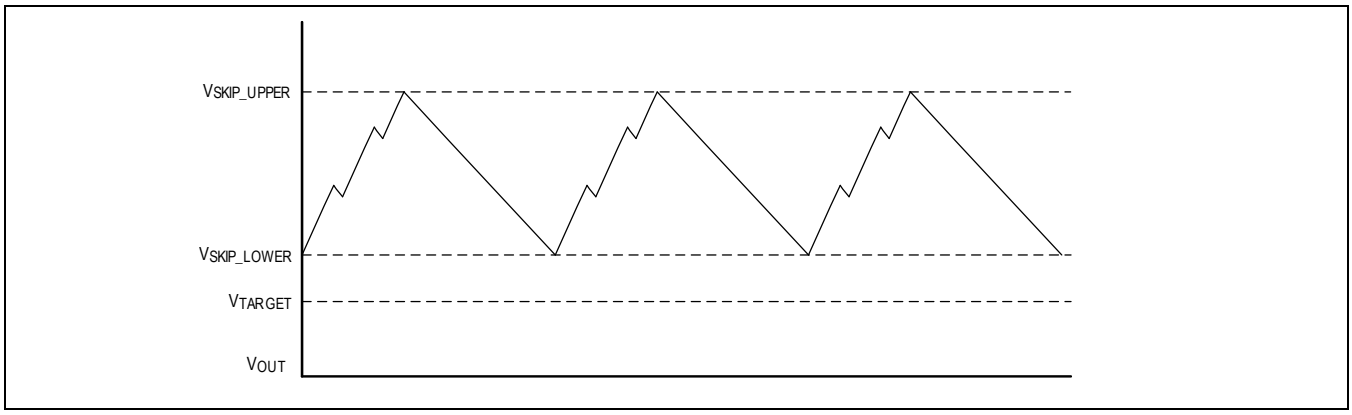


Figure 3. Skip Mode Waveform

Output Voltage Configuration

The IC supports a programmable output voltage between 1.8V to 5.2V with a step size of 50mV. The default output voltage is programmable through discrete steps with a single resistor connected between SEL and AGND. See the SEL Pin Configuration section for more information. The default output voltage value is written to the bitfield VOUT[6:0] in the VOUT_L(0x03) register when the part reads the R_{SEL} pin during *Startup*. The output voltage can be programmable between 1.8V to 5.2V through 50mV steps by writing to the bitfield VOUT[6:0] through I^2C. Note that the converter requires a minimum input OR output voltage of 2.3V.

SEL Pin Configuration

The SEL pin allows a single resistor (R_{SEL}) to be connected to AGND. Through R_{SEL} value, the MAX77847 can configure start up output voltage (16 options), and I^2C target addresses (2 options). During the startup, the device reads the R_{SEL} value to configure the device for the settings mentioned earlier. Choose a resistor with 1% tolerance or better. See *Table 1* for recommended values for R_{SEL} for each setting.

Table 1. R_{SEL} Selection Table

R_{SEL} (kΩ)	V_{OUT} (V)	TARGET ADDRESS (7bit)
Short (0)	3.3	110 0111b
4.99	2.3	
5.90	2.5	
7.15	2.6	
8.45	2.7	
100	2.8	
11.8	2.9	
14.0	3.0	
16.9	3.4	
20.0	3.6	
23.7	3.8	
28.0	4.0	
34.0	4.2	
40.2	4.5	
47.5	5.0	
56.2	5.2	

66.5	3.3	110 1111b
80.6	2.3	
95.3	2.5	
113	2.6	
133	2.7	
162	2.8	
191	2.9	
226	3.0	
267	3.4	
324	3.6	
383	3.8	
452	4.0	
536	4.2	
634	4.5	
768	5.0	
909 or OPEN	5.2	

Dynamic Voltage Scaling (DVS)

The MAX77847, with its low I_Q and high efficiency over its entire output voltage range of 1.8V to 5.2V, can be used as a power supply for RF Power Amplifiers (RFPA). The latest RFPA used in the cellular industry has an increased power output and, therefore a demand for higher efficiency while maintaining output linearity. This can be achieved through the DVS feature available in MAX77847 to modulate the power supply to the RFPA to increase system efficiency. The fast-rising slew rate of 225mV/µs (typ.) available for DVS enables changing the output voltage of MAX77847 within a few microseconds (T_{RISE}). The DVS feature is accessible through the external GPI pin, as shown in *Figure 4*. *Figure 4* also shows a typical DVS waveform to change the output voltage from V_{OUT1} and V_{OUT2} and back in time T_{RISE} and T_{FALL}, respectively. The times T_{RISE} and T_{FALL} depend on the input/output voltage, rising and falling slew rates and output load conditions.

The GPI pin can be configured as a DVS control input through the GPI_CFG[0] bitfield in the CFG(0x01) register. When this bit is programmed to 0b1, the GPI pin acts as a DVS input pin. When the pin is pulled to logic high, the output voltage switches to the value programmed in the bitfield VOUT_H[6:0], with a default value of 3.6V. When the pin is pulled to logic low, the output voltage switches to the value programmed in the bitfield VOUT[6:0]. Two rising and falling slew rates between the DVS voltage can be programmed through I^2C in the RU_SR[0] and RD_SR[0] bitfields, respectively, in the CFG(0x01) register. When GPI_CFG[0] bitfield is programmed to 0b0, the output voltage regulates the value programmed in VOUT [6:0] regardless of the state of the GPI pin. See the *Register Map* for details about the programmable slew rates supported by MAX77847.

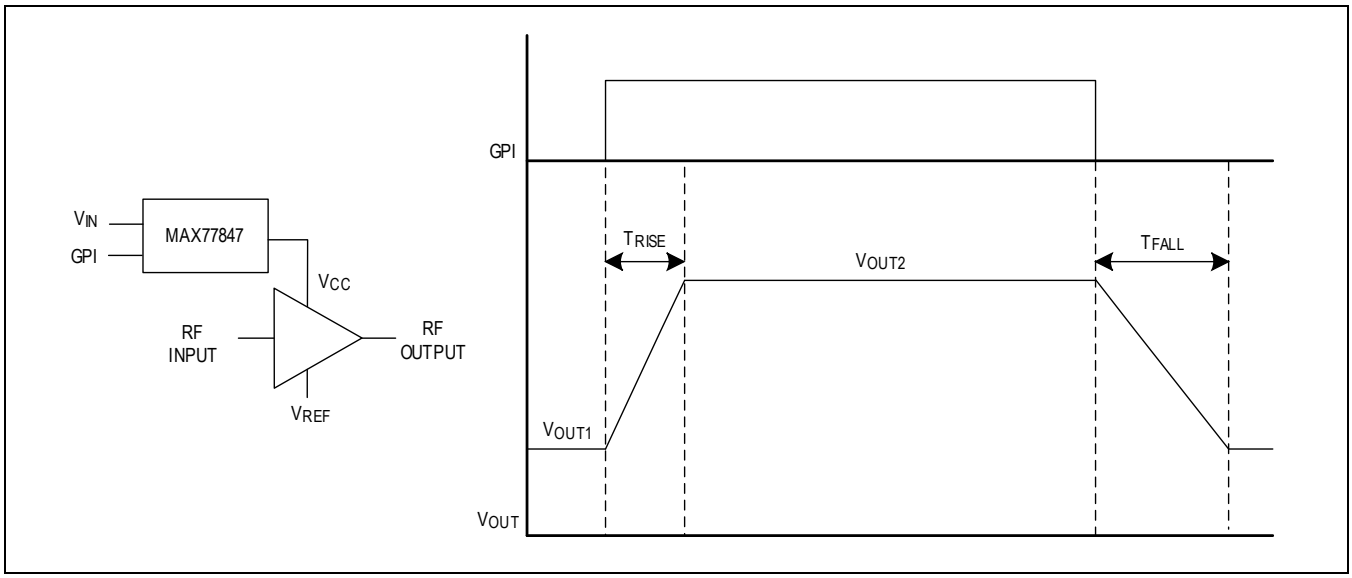


Figure 4. Dynamic Voltage Scaling

Protections

Thermal Shutdown

MAX77847 has an internal thermal-protection circuit that monitors die temperature. The device is designed to operate at an ambient temperature of -40˚C to +125˚C. The Thermal Shutdown Protection feature protects the die from overheating to the Thermal Shutdown Protection Threshold, T_{SHDN} (+150˚C (typ)) under load conditions. The buck-boost latches off if the die temperature exceeds T_{SHDN}. The buck-boost output must be enabled again by toggling V_{IN} or cycling the EN[0] bitfield or the EN pin after the die temperature cools by +15˚C.

Undervoltage Lockout (UVLO)

The MAX77847 supports a UVLO feature that prevents operation in abnormal input voltage conditions when V_{IN} falls below the $V_{UVLO\_falling}$ threshold. Therefore, regardless of the status of the EN[0] bitfield, the device disables until the input voltage V_{IN} rises above the V_{UVLO_rising} threshold. After the V_{IN} rises above the appropriate threshold, follow the steps in the *Startup* section to enable the buck-boost converter.

Overvoltage Protection

MAX77847 detects the voltage difference between OUT and OUTS, and if the voltage difference (OUT–OUTS) exceeds the OVP threshold voltage level (0.5V typ), the device turns off all switches. This prevents OUTS = OPEN conditions from overdriving the output beyond safe operating ranges and works with Soft Start Timeout Timer (T_{SS}) to turn off the switching converter. However, this protection does not trigger the Overvoltage Protection status bitfield, OVP[0], in the STAT(0x00) register.

Additionally, the device shuts off whenever OUTS detects a voltage over 20% of the target output value (10% when the OUT target is set above 5V) and sets the bitfield OVP[0] in the STAT(0x00) register.

Switching Current Limit

MAX77847 features a robust switching current limit scheme that protects the IC and inductor during overload and fast transient conditions. The current sensing circuit takes current information from the high-side MOSFETs to determine the peak switching current ($R_{DS(ON)}$ x I_L).

The IC provides two different switch current limit levels (4.5A(typ) and 3.6A(typ)), which can be programmed through the I^2C interface using the bitfield ILIM[0] in register CFG(0x01). If the switching current hits the current limit (I_{LIM}) for about 2ms, the IC latches off the output. The buck-boost can be enabled again by cycling bitfield EN[0] or EN pin or V_{IN}.

When the inductor current reaches the switching current limit level (I_{LIM}), the inductor charging phase terminates, and the discharging phase begins for the rest of the switching period. The charging phase begins again at the end of the switching period, determined by the falling edge of the clock cycle. As a result, the inductor current ripple and the switching frequency differ from the typical switching frequency (f_{SW}) of 2.2MHz.

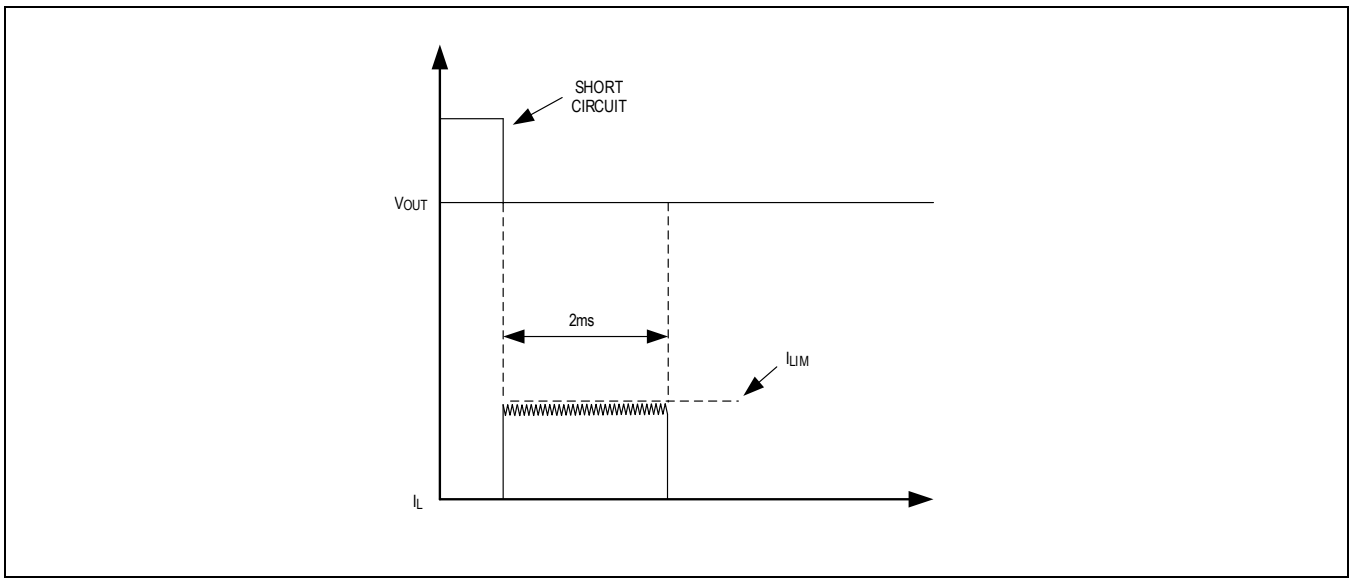


Figure 5. Short Circuit Waveform

Detailed Description—I²C Interface

The I²C-compatible, 2-wire serial interface is used for the regulator on/off control, setting output voltages, DVS slew rate and other functions. The MAX77847 supports the data rate of an I²C Bus, up to 1Mbps (Fast-Plus Mode). See the *Register Map* for details.

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pull-up resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-controller bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 6 shows an example of a typical I²C system. A device on the I²C bus sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a controller. Any device that is being addressed by the controller is considered a target. When the MAX77847 I²C-compatible interface is operating, it is a target on the I²C bus, and it can be both a transmitter and a receiver.

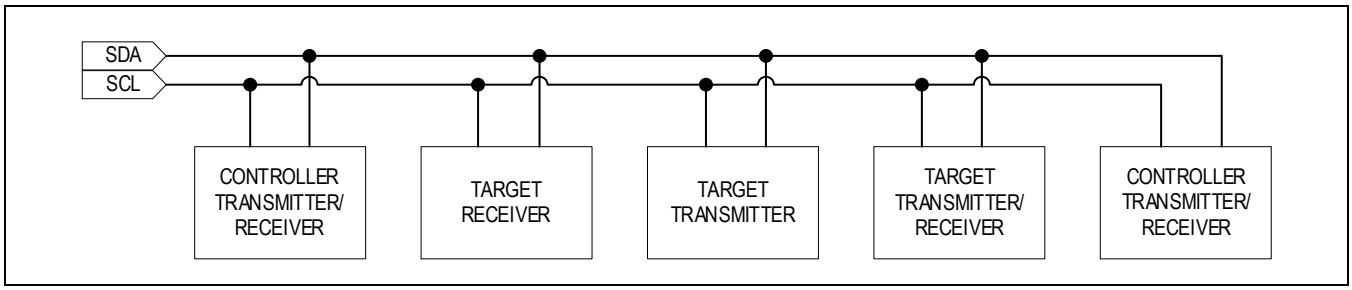


Figure 6. Functional Logic Diagram for Communications Controller

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of the SCL clock pulse. Changes in SDA, while SCL is high, are control signals (START and STOP conditions).

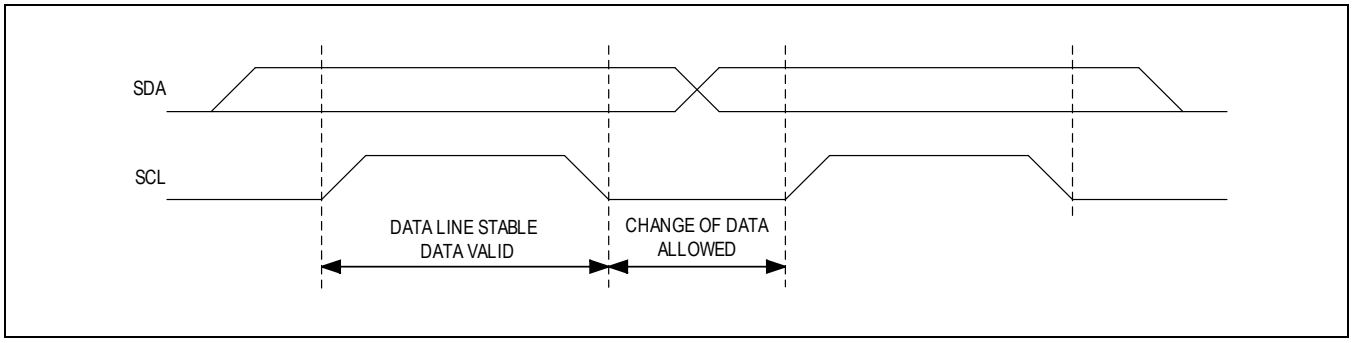


Figure 7. I²C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, the SDA and SCL idle high. A controller device initiates communication by issuing a START condition (S). A START condition (S) is a HIGH-to-LOW transition on SDA with SCL HIGH. A STOP condition (P) is a LOW-to-HIGH transition on SDA, while SCL is HIGH.

A START condition (S) from the controller signals the beginning of a transmission to the MAX77847. The controller terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

The STOP condition (P) frees the bus. To issue a series of commands to the target, the controller may issue REPEATED START (Sr) commands instead of a STOP condition (P) to maintain control of the bus. Generally, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or incorrect address is detected, the IC internally disconnects SCL from I2C serial interface until the next START condition, minimizing digital noise and feed through.

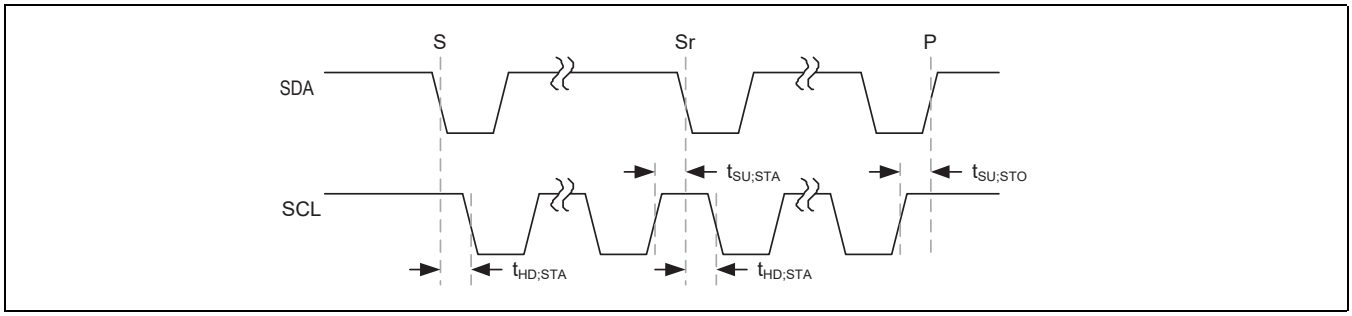


Figure 8. START and STOP Conditions

Acknowledge Bit

The I2C bus controller and MAX77847 (target) generate the acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA LOW before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and leaves it HIGH during the HIGH period of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller should reattempt communication later.

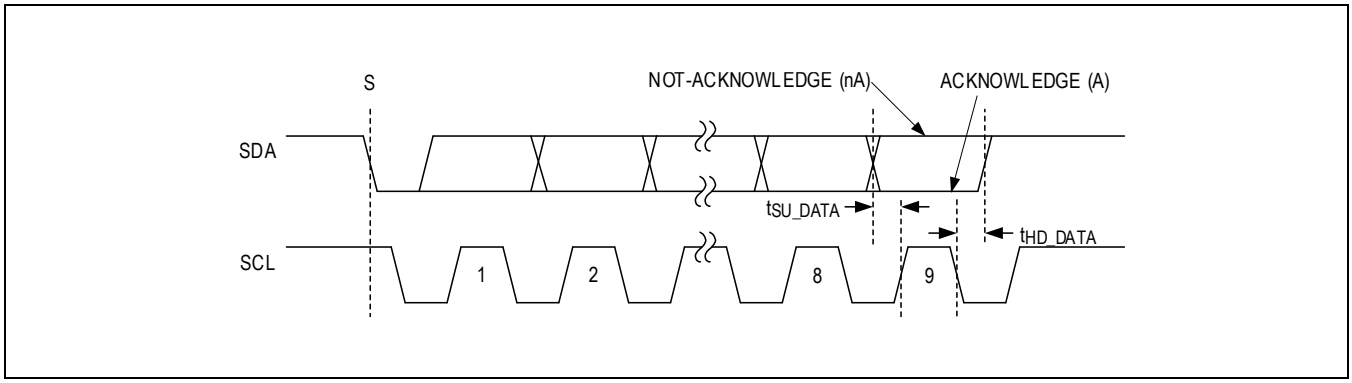


Figure 9. Acknowledge Bit

Target Address

The MAX77847 supports two different target addresses, which can be selected via R_{SEL}. The I²C target addresses of the IC are shown in *Table 2* . *Figure 10* shows the 7-bit target address at 0x67.

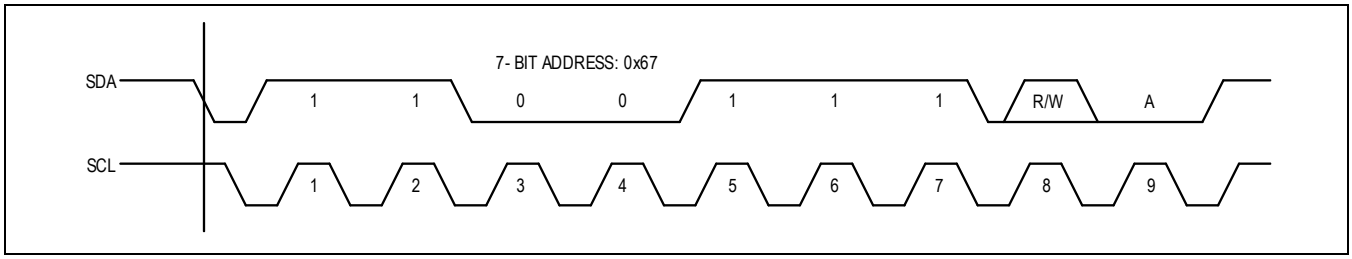


Figure 10. Target Address Byte Example

Table 2. MAX77847 I²C Target Address

TARGET ADDRESS (7 Bit)	TARGET ADDRESS (Write)	TARGET ADDRESS (Read)	R_{SEL} (kΩ)
0b110 0111 (0x67)	0b1100 1110	0b1100 1111	0 – 56.2
0b110 1111 (0x6F)	0b1101 1110	0b1101 1111	66.5 - OPEN

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows a slow target device to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The IC does not use the form of clock stretching to hold down the clock line.

General Call Address

The MAX77847 does not implement the I²C specification called a general call address. If the IC sees a general call address (0000 0000b), it will not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides an I²C 3.0-compatible (3.4MHz) serial interface.

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast-mode plus)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, the pullup resistance must be decreased when increasing bus speeds to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing section of I²C revision 3.0 specification* for detailed guidance on the pullup resistor selection. Generally, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note: The pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

At power-up and after each STOP condition (P), the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz).

Communication Protocols

The MAX77847 supports both writing and reading from its registers. The following sections show the I²C-communication protocols for each functional block. The power block uses the same communications protocols.

Writing to a Single Register

Figure 11 shows the protocol from the I2C controller device to write one byte of data to the IC. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

- The controller sends a START condition (S).
- The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ =0)
- The addressed target asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
- The controller sends an 8-bit register pointer.
- The target acknowledges the register pointer.
- The controller sends a data byte.
- The target acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register, and the data will become active.
- The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

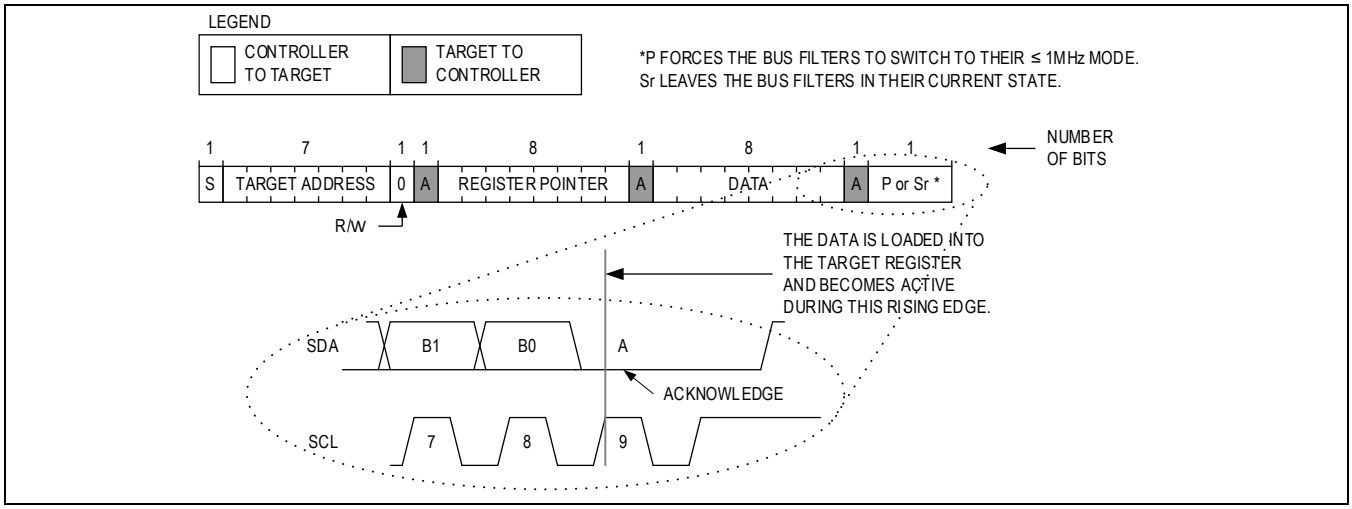


Figure 11. Writing to a Single Register with Write Byte Protocol

Writing to Sequential Register

Figure 12 shows the protocol for writing to sequential registers. This protocol is like the write byte protocol, except the controller continues to write after receiving the first data byte. When the controller is done writing, it issues a STOP or REPEATED START.

The writing to sequential registers protocol is as follows:

- The controller sends a START command (S).
- The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed target asserts an ACKNOWLEDGE (A) by pulling SDA low.
- The controller sends an 8-bit register pointer.
- The target acknowledges the register pointer.
- The controller sends a data byte.
- The target acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register, and the data will become active.
- Steps 6 to 7 are repeated as often as the controller requires.

- During the last acknowledge related clock pulse, the target issues an ACKNOWLEDGE (A).
- The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

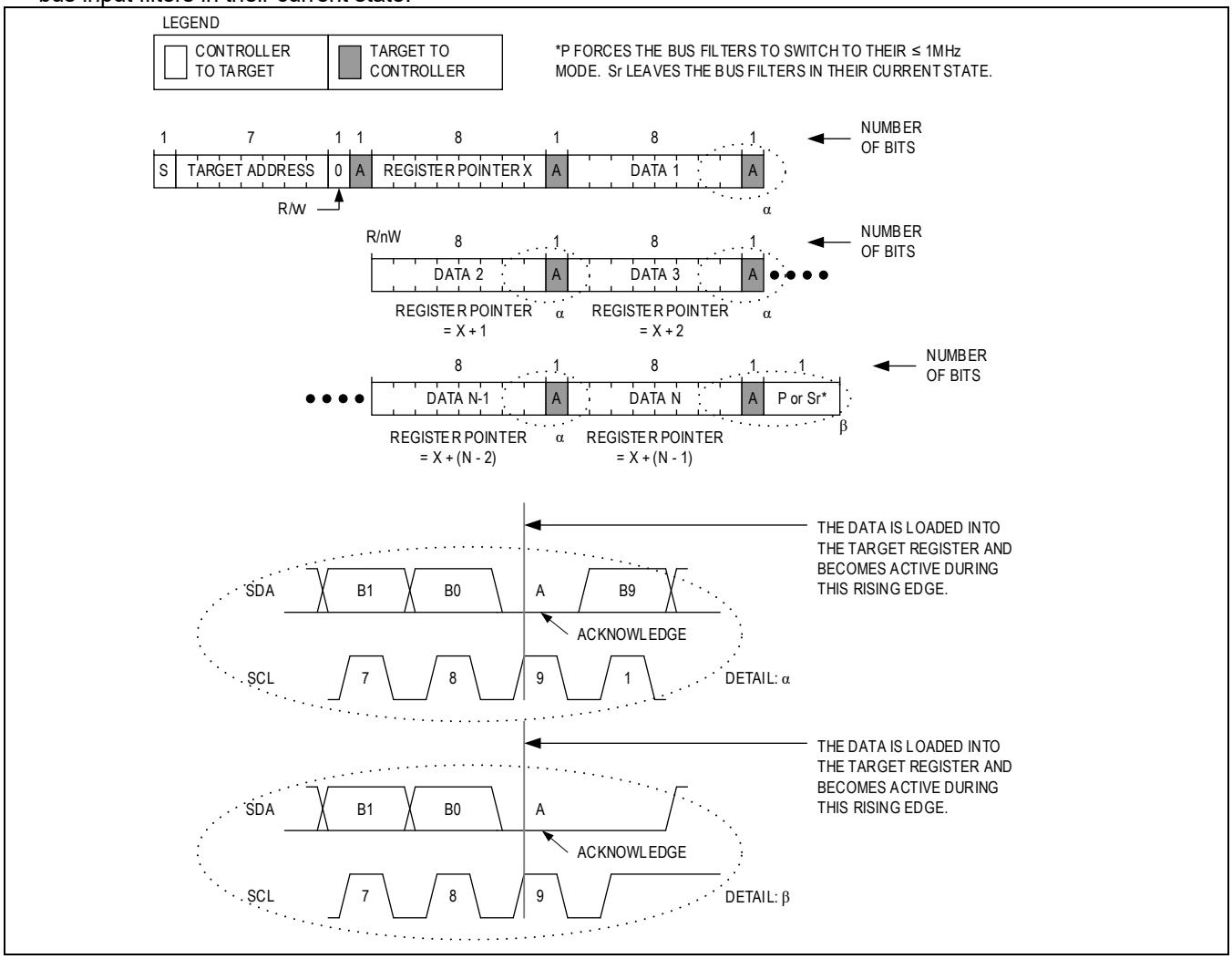


Figure 12. Writing to Sequential Registers

Reading from a Single Register

Figure 13 shows the protocol for reading from a single register. This protocol is identical to the “Read Byte” protocol in the SMBus specification.

The “Read Byte” protocol is as follows:

- The controller sends a START condition (S).
- The controller sends the 7-bit target address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
- The controller sends an 8-bit register pointer.
- The target acknowledges the register pointer.
- The controller sends a REPEATED START command (Sr).
- The controller sends the 7-bit target address followed by a read bit (R/$\overline{W}$ = 1).
- The addressed target asserts as ACKNOWLEDGE (A) by pulling SDA LOW.
- The addressed target places 8 bits of data from the location specified by the register pointer on the bus.

- The controller issues a NOT-ACKNOWLEDGE (nA).
- The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

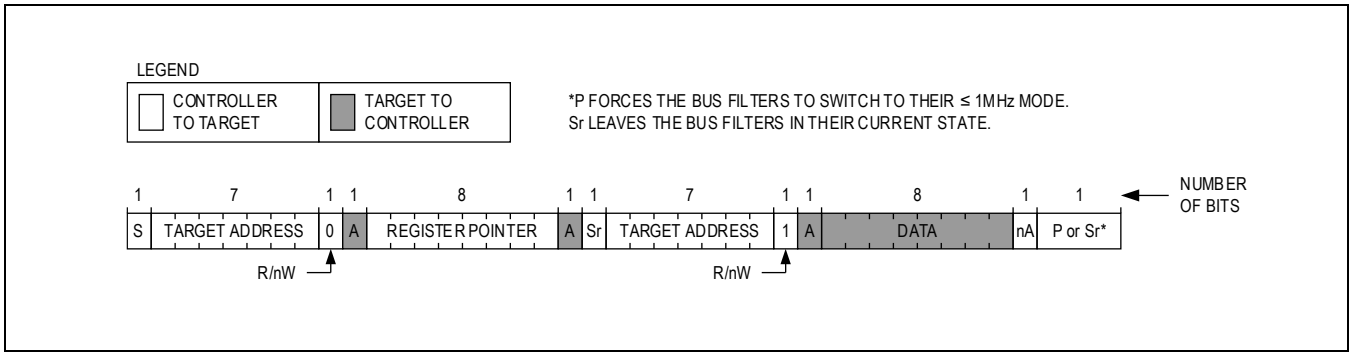


Figure 13. Reading to a Single Register

Reading from Sequential Registers

Figure 14 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol, except the controller device issues an ACKNOWLEDGE (A) to signal the target device that it wants more data. When the controller device has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

- The controller sends a START condition (S).
- The controller sends the 7-bit target address followed by a write bit ($R/\overline{W}$ = 0).
- The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
- The controller sends an 8-bit register pointer.
- The target acknowledges the register pointer.
- The controller sends a REPEATED START command (Sr).
- The controller sends the 7-bit target address followed by a read bit ($R/\overline{W}$ = 1).
- The addressed target asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
- The addressed target places 8-bits of data from the location specified by the register pointer on the bus.
- The controller issues an ACKNOWLEDGE (A), signalling the target that it wishes to receive more data.
- Steps 9 to 10 are repeated as often as the controller requires. Following the last byte of data, the controller must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
- The controller sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

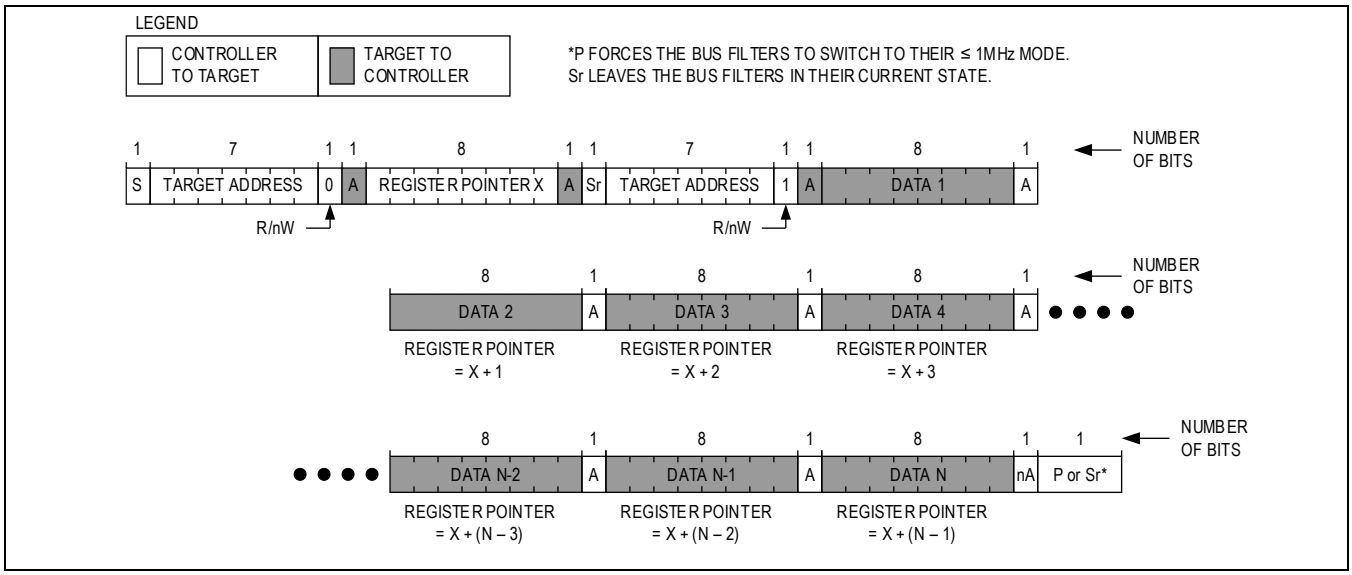


Figure 14. Reading from Sequential Registers

Register Map

MAX77847

ADDRESS	NAME	MSB							LSB
Global Configuration									
0x00	STAT[7:0]	DEV_ID[3:0]				RSVD	TSHDN	OVP	OCP
0x01	CFG[7:0]	ILIM	RU_SR	RD_SR	EN	EN_PD	AD	GPI_CFG	FPWM
0x02	VOUT_H[7:0]	RSVD_VOUTH	VOUT_H[6:0]						
0x03	VOUT_L[7:0]	RSVD_VOUT	VOUT[6:0]						

Register Details

STAT (0x0)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[3:0]				RSVD	TSHDN	OVP	OCP
Reset	0b0000				0x0	0b0	0b0	0b0
Access Type	Read Only				Read Only	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:4	Indicates the ID of the device in use.	MAX77847 = 0x0 (default)
RSVD	3	Reserved	N/A
TSHDN	2	Thermal Shutdown Status Bit.	0x0 = Thermal shutdown was NOT detected. 0x1 = Thermal shutdown was detected.
OVP	1	Overvoltage Protection Status Bit. Triggers when OVP is detected.	0x0 = Output overvoltage has NOT been detected. 0x1 = Output overvoltage detected. Buck-Boost actively discharged.
OCP	0	Overcurrent Protection Status Bit. Triggers when OCP is detected.	0x0 = Switching current limit has NOT been reached. 0x1 = Switching current limit protection triggered. Buck-boost actively discharged.

CFG (0x1)

BIT	7	6	5	4	3	2	1	0

Field	ILIM	RU_SR	RD_SR	EN	EN_PD	AD	GPI_CFG	FPWM
Reset	0b0	0b1	0b1	0bcustom	0b1	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM	7	Switching Current Limit Programming Register.	0x0 = 4.5A (default) 0x1 = 3.6 A
RU_SR	6	V_{OUT} Ramp-Up Slew Rate	0b0 = 100mV/µs 0b1 = 225mV/µs (default)
RD_SR	5	V_{OUT} Ramp-Down Slew Rate	0b0 = 12.5mV/µs 0b1 = 25mV/µs (default)
EN	4	Buck-Boost Enable Bit	0b0 = Buck-boost disabled (default for option A) 0b1 = Buck-boost enabled (default for option B)
EN_PD	3	Enable Pin Pull-Down Resistor Setting	0b0 = Disabled 0b1 = Enabled
AD	2	Output Active Discharge	0b0 = Active discharge disabled 0b1 = Active discharge enabled (default)
GPI_CFG	1	General Purpose Input Pin Configuration.	0b0 = FPWM mode enable input (default) 0b1 = DVS control input
FPWM	0	Forced PWM Mode. This signal is logic OR gated with GPI pin input when GPI_CFG is set to FPWM mode enable input.	0b0 = Auto skip mode (default) 0b1 = FPWM mode enabled

VOUT_H (0x2)

BIT	7	6	5	4	3	2	1	0
Field	RSVD_VOUTH	VOUT_H[6:0]						
Reset	0x0	0b010 0100						
Access Type	Read Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_VOUTH	7	Reserved	N/A
VOUT_H	6:0	Output Voltage for DVS = HIGH	000 0000b = 1.80V 000 0001b = 1.85V 000 0010b = 1.90V

BITFIELD	BITS	DESCRIPTION	DECODE
			... 010 0100b = 3.60V (default) ... 100 0100b = 5.2V, 50mV per steps

VOUT_L (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RSVD_VOUT	VOUT[6:0]						
Reset	0x0	0xCustom						
Access Type	Read Only	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_VOUT	7	Reserved	N/A
VOUT	6:0	Output Voltage for DVS = LOW.	000 0000b = 1.80V 000 0001b = 1.85V 000 0010b = 1.90V ... 001 1110b = 3.30V (default) ... 100 0100b = 5.2V, 50mV per steps

Applications Information

Input Capacitor Selection

Bypass IN with 2x 10V, X7R, 10µF nominal input capacitor (C_{IN}). Larger values improve the decoupling of the buck-boost regulator and filter the switching noise for the system. The RMS current rating of the input capacitor in buck-mode needs to be higher than

$$I_{RMS} = \sqrt{D \times (1-D) \times I_o^2 + (D \times dI^2/12)},$$

where dI is the inductor current ripple, D is the duty cycle, and I_o is the load current. Consider using multiple capacitors in parallel to meet this specification if necessary.

Output Capacitor Selection

The minimum effective output capacitance of 4.7µF is required for small output ripple and ensures stable operation of the buck-boost regulator. Determine the expected effective C_{OUT} carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias voltage. Refer to *Tutorial 5527* for more information. The RMS current rating of the effective output capacitor in boost mode needs to be higher than

$$I_{RMS} = \sqrt{D \times (1-D) \times I_o^2 + (D \times dI^2/12)},$$

where dI is the inductor current ripple, D is the duty cycle, and I_o is the load current.

A 16V, 22µF ceramic capacitor is recommended for most applications. Ceramic capacitors with X7R dielectrics are highly recommended for better effective capacitance, and capacitance tolerance over bias voltage and temperature variations. The typical applications circuit uses 2 x 10µF, 10V, X7R capacitors.

Inductor Selection

The MAX77847's current sensing circuit and compensation loop are optimized for 1µH inductance. An inductor with a saturation current greater than or equal to the peak current limit setting (I_{LIM}) and an RMS current rating based on the expected continuous peak inductor current at a given max load current is recommended. Lower DCR increases buck-boost efficiency. Recall that there are two different I_{LIM} options for the MAX77847. *Table 3* lists recommended inductors for each I_{LIM} option. Note that this table was generated in 2023, and as inductor technology improves rapidly, it may not be the most up-to-date at the time of reading.

Table 3. Recommended Inductors

MANUFACTURER	PART NUMBER	I_{LIM} (A)	INDUCTANCE (µH)	TYP.DC RESISTANCE (MAX) (mΩ)	TYP SATURATION CURRENT (Max) (A)	RMS CURRENT FOR 40°C TEMPERATURE RISE(A)	DIMENSIONS L x W x H (mm)
Cyntec	HTEK20161T-1R0MSR	3.6	1.0	35 (43)	4.6 (4.2)	4.1	2.0 x 1.6 x 1.0
Cyntec	HTEH20161T-1R0MSR	3.6	1.0	27 (36)	4.8 (4.2)	4.3	2.0 x 1.6 x 1.0
Samsung	CIGT252010TM1R0MLE	4.5	1.0	21 (23)	5.5 (5.3)	5.3	2.5 x 2.0 x 1.0
Cyntec	HTEP25201T-1R0MSR	4.5	1.0	18 (25)	5.5 (5.0)	5.2	2.5 x 2.0 x 1.0
Cyntec	HTEH25201T-1R0MTR	4.5	1.0	21 (26)	5.5 (5.0)	5.2	2.5 x 2.0 x 1.0
Samsung	CIGT252010EL1R0MLE	4.5	1.0	22 (25)	5.2 (5.0)	4.7	2.5 x 2.0 x 1.0
Samsung	CIGT252010EH1R0MNE	4.5	1.0	26 (30)	5.0 (4.7)	4.1	2.5 x 2.0 x 1.0

PCB Layout Guidelines

Careful circuit board layout is critical to achieving low switching power losses and clean, stable operation. For the WLP and FC2QFN package, a high-density interconnect (HDI) PCB is not required. *Figure 15* shows an example non-HDI PCB layout for the MAX77847 WLP package.

When designing the PCB, follow these guidelines:

- Place the input capacitors C_{IN} and output capacitors C_{OUT} immediately next to the IN pin and OUT pin, respectively, of the IC. The trace between the capacitors' ground pin and the IC PGND pin must be routed through the component mounting layer to minimize trace parasitics. Additionally, the trace for these connections must be as short and wide as possible. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
- Place the inductor next to the LX bumps/pins (as close as possible), route inductor traces through vias, and make the traces between the LX bumps/pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to reduce trace impedance further. Furthermore, do not allow LX traces to take up excessive area. The voltage on this node switches quickly and additional area creates more radiated emissions.
- Prioritize the low-impedance ground plane of the PCB directly underneath the IC, C_{OUT}, C_{IN}, and inductor. Cutting this ground plane risks interrupting the switching current loops.
- AGND must carefully connect to PGND on the PCB low-impedance ground plane. Connect AGND to the low-impedance ground plane on the PCB (the same net as PGND) away from any critical loops.
- The IC requires a supply input (BIAS), the same net as IN. Carefully bypass BIAS to PGND with a dedicated capacitor (C_{BIAS}) as close as possible to the IC. Route a dedicated trace between C_{BIAS} and the BIAS bump/pin. Avoid connecting BIAS directly to the nearest IN bumps/pins without dedicated bypassing.
- Connect the OUTS bump/pin to the regulating point with a dedicated trace away from noisy nets such as LX1 and LX2.
- Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
- Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

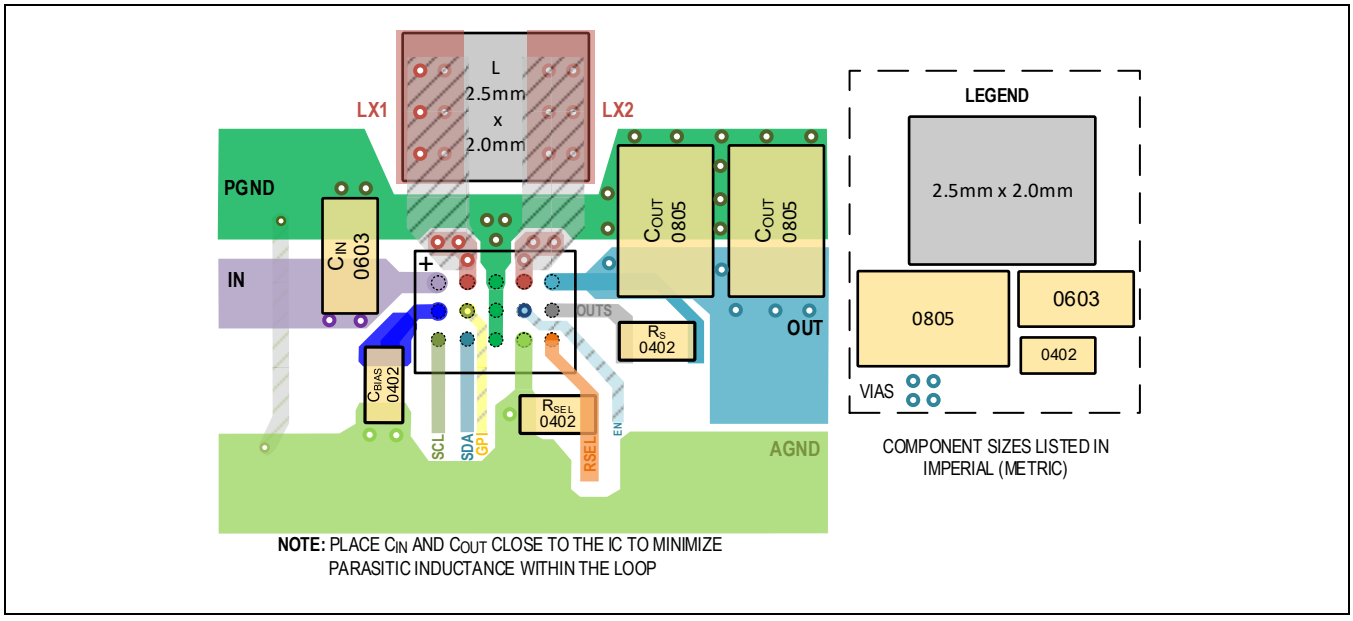


Figure 15. PCB Layout Example (WLP)

Typical Application Circuit

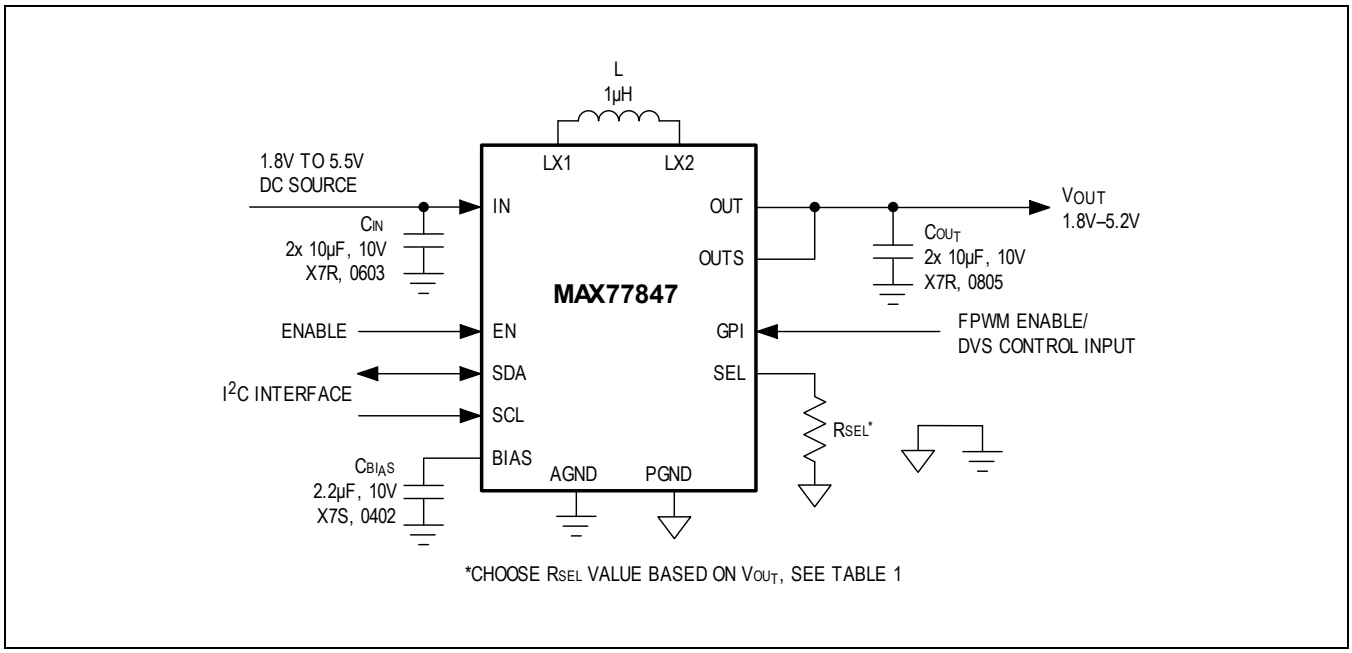


Figure 16. Typical Application Circuit

Ordering Information

PART NUMBER	DEFAULT EN BIT	PIN-PACKAGE
MAX77847AEWL+T	Disabled	15 Pin WLP
MAX77847BEWL+T	Enabled	15 Pin WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/23	Release for Market Intro	—

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