MAX33047E/MAX33048E/ MAX33049E

20Mbps Full-Duplex RS-485/ RS-422 Transceivers with ±40kV ESD Protection

General Description

The MAX33047E/MAX33048E/MAX33049E are ±40kV ESD-protected full-duplex RS-485/RS-422 transceivers that operate from 3.0V to 5.5V and provide design flexibility for robust communication of up to 20Mbps.

These transceivers are optimized for robust communication in harsh industrial environments. They include integrated hot-swap protection and a true fail-safe receiver, ensuring a logic-high output on the receiver when input signals are either shorted or open. The driver outputs/receiver inputs are protected against faults up to ±25V and can withstand ESD of up to ±15kV for air-gap discharge and ±10kV for contact discharge as per IEC 61000-4-2. The driver outputs are protected against short circuits and integrated thermal shutdown circuitry places the driver outputs into a high-impedance state during thermal overload events.

The MAX33047E/MAX33048E are available in an 8-pin SOIC package and the MAX33049E is available in a 14-pin SOIC package. These transceivers operate within a temperature range of -40°C to +125°.

Applications

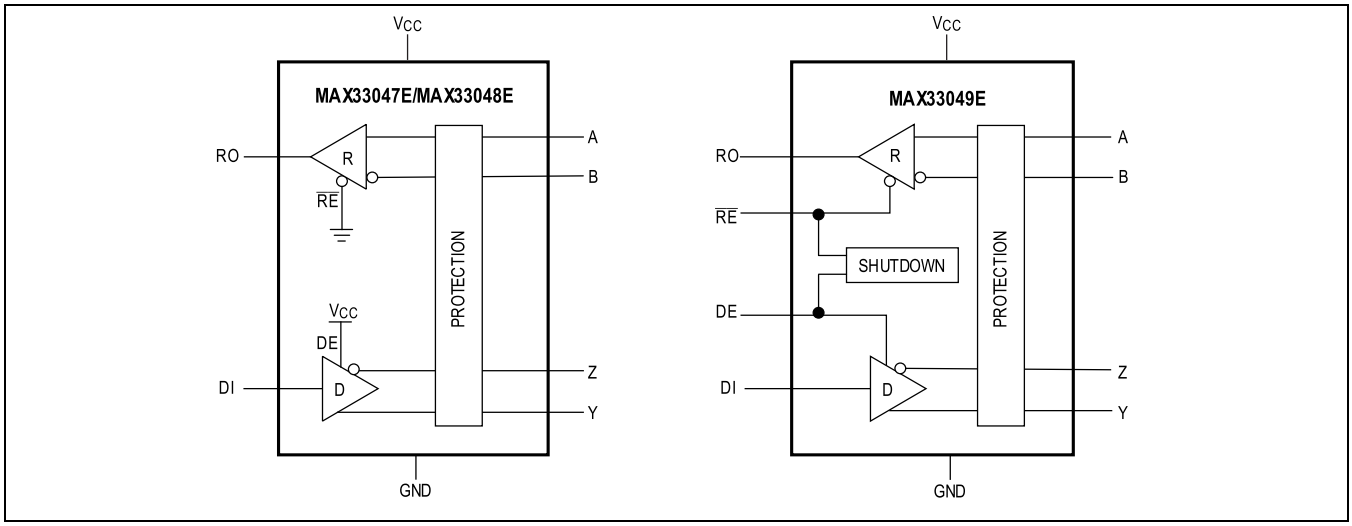
- Programmable Logic Controller (PLC)
- Factory Automation Equipment
- Industrial Control Systems

Benefits and Features

- Integrated Protection Ensures Robust Communication
  - ±25V Fault Protection Range on Driver Outputs/Receiver Inputs
  - High ESD Protection
    - ±40kV Human Body Model (HBM) ESD
    - ±15kV Air-Gap ESD as per IEC 61000-4-2
    - ±10kV Contact ESD as per IEC 61000-4-2
  - Short-Circuit Protected Outputs
  - True Fail-Safe Receiver
  - Hot-Swap Capability (MAX33049E)
- Flexibility for Many Different Applications
  - 3.0V to 5.5V Supply Range
  - Up to 500kbps Data Rates (MAX33047E)
  - Up to 20Mbps Data Rate (MAX33048E/MAX33049E)
  - Available in 8-Pin and 14-Pin SOIC Packages
  - Enables up to 256 Nodes on the Bus
  - Wide -40°C to +125°C Operating Temperature

Ordering Information appears at end of data sheet.

Simplified Block Diagram



19-101567; Rev 1; 12/24

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V

RO to GND ..... -0.3V to (V_{CC} + 0.3)V

DE, DI, $\overline{RE}$ to GND ..... -0.3V to +6V

A, B, Y, Z to GND ..... -30V to +30V

Short-Circuit Duration (RO, Y, Z) to GND ..... Continuous

Continuous Power Dissipation

8-Pin SOIC (T_A = +70°C, derate 7.4mW/°C above +70°C) 588mW

14-Pin SOIC (T_A = +70°C, derate 11.9mW/°C above +70°C) 952mW

Temperature Ratings

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature ..... -65°C to +150°C

Lead Temperature (soldering 10s) ..... +300°C

Reflow Temperature ..... +270°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

SOIC-8

Package Code	S8+2C
Outline Number	21-0041
Land Pattern Number	90-0096
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	136°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	38°C/W

SOIC-14

Package Code	S14+1C
Outline Number	21-0041
Land Pattern Number	90-0112
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	84°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	34°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html.* Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.*

Electrical Characteristics

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 5V and T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{CC}		3.0		5.5	V
Supply Current	I_{CC}	No load, no switching (DI = 0V or V_{CC}) (MAX33047E/MAX33048E)		6.0	9.0	mA
		DE = V_{CC}, $\overline{RE}$ = 0V, no load, no switching (DI = 0V or V_{CC}) (MAX33049E)		6.0	9.0	
		DE = 0V, $\overline{RE}$ = 0V no load, no switching (MAX33049E)		3.0	7.5	
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC} (MAX33049E)			10.0	µA
DRIVER						
Differential Driver Output	$\|V_{OD}\|$	RL = 54Ω (*Figure 1*), (*Note 2*)	1.5			V
		RL = 100Ω (*Figure 1*), (*Note 2*)	2			
Change in Magnitude of Differential Driver Output Voltage	ΔV_{OD}	RL = 54Ω or 100Ω (*Figure 1*)	-0.2		+0.2	V
Driver Common-Mode Output Voltage	V_{OC}	RL = 54Ω or 100Ω (*Figure 1*)		$V_{CC}/2$	V_{CC}	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	RL = 54Ω or 100Ω (*Figure 1*), (*Note 2*)	-0.2		+0.2	V
Single-Ended Driver Output Voltage High	V_{OH}	Z or Y output, output is high, I_{SOURCE} = 3mA	2.4	V_{CC} - 0.2		V
Single-Ended Driver Output Voltage Low	V_{OL}	Z or Y output, output is low, I_{SINK} = 3mA			0.2	V
Driver Short-Circuit Output Current	I_{SC_DR}	-7V ≤ (V_Y or V_Z) ≤ +12V			±250	mA
RECEIVER						
Input Current (A, B)	I_A, I_B	DE = 0V, 0V ≤ V_{CC} ≤ 5.5V, V_{IN} = +12V			+125	µA
		DE = 0V, 0V ≤ V_{CC} ≤ 5.5V, V_{IN} = -7V	-73			
Receiver Input Resistance	R_{IN}		96			kΩ
Common Mode Voltage Range	V_{CM}		-7		+12	V
Receiver Differential Threshold Voltage Rising	V_{TLH}				-50	mV
Receiver Differential Threshold Voltage Falling	V_{THL}		-200			mV
Receiver Input Hysteresis	ΔV_{TH}			100		mV
Differential Input Capacitance	C_{A_B}	Measured between A and B, f = 1MHz (*Note 3*)		5		pF
LOGIC OUTPUT (RO)						
Output Logic High Voltage	V_{OH}	I_{SOURCE} = 3mA, (V_A - V_B) ≥ -50mV	V_{CC} - 0.4			V
Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA, (V_A - V_B) ≤ -200mV			0.4	V

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 5V and T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current	I_{OZR}	$0V \le V_{RO} \le V_{CC}$	-1		+1	µA
Short-Circuit Current	$\|I_{OSR}\|$	$0V \le (V_A - V_B) \le V_{CC}$		200		mA
LOGIC INPUT (DE, $\overline{RE}$, DI)						
Input Logic High Voltage	V_{IH}		2			V
Input Logic Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			100		mV
Input Current	I_{IN}	After first transition of DE (MAX33049E)	-1		+1	µA
DE Input Impedance on First Transition	R_{IN_FT}	(MAX33049E)	1		10	kΩ
PROTECTION						
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising		+160		°C
Thermal Shutdown Hysteresis	T_{HYST}			12		°C
ESD Protection (A, B, Y, Z Pins to GND)		Human Body Model		±40		kV
		Air-Gap Discharge as per IEC 61000-4-2		±15		
		Contact Discharge as per IEC 61000-4-2		±10		
ESD Protection (All Other Pins)		Human Body Model		±4		kV
		Charge Device Model		±2		
Fault Protection (A, B, Y, Z Pins to GND)			-25		+25	V
SWITCHING DRIVER (MAX33047E) (*Note 5*)						
Differential Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF (*Figure 2*), (*Figure 3*)			1000	ns
Differential Driver Output Skew $\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF (*Figure 2*), (*Figure 3*)			140	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF (*Figure 3*)			600	ns
Maximum Data Rate	DR_{MAX}		500			kbps
SWITCHING DRIVER (MAX33048E, MAX33049E) (*Note 5*)						
Differential Driver Propagation Delay	t_{DPLH}, t_{DPHL}	R_L = 54Ω, C_L = 50pF (*Figure 2*), (*Figure 3*)			40	ns
Differential Driver Output Skew $\|t_{DPLH} - t_{DPHL}\|$	t_{DSKEW}	R_L = 54Ω, C_L = 50pF (*Figure 2*), (*Figure 3*)			9	ns
Driver Differential Output Rise or Fall Time	t_{LH}, t_{HL}	R_L = 54Ω, C_L = 50pF (*Figure 3*)		8	15	ns
Maximum Data Rate	DR_{MAX}		20			Mbps
Driver Enable to Output High	t_{DZH}	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 4*)			90	ns
Driver Enable to Output Low	t_{DZL}	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 5*)			90	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 4*)			60	ns
Driver Enable Time from High	t_{DHZ}	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 5*)			60	ns

(V_{CC} = 3.0V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 5V and T_A = +25°C.) (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable Time from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 4*), (*Note 4*)			170	µs
Driver Enable Time from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, MAX33049E (*Figure 5*), (*Note 4*)			170	µs
Time to Shutdown	t_{SHDN}	MAX33049E (*Note 4*)	250	800	1500	ns
SWITCHING RECEIVER (MAX33047E) (*Note 5*)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF (*Figure 7*)			200	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF (*Figure 7*)			30	ns
Maximum Data Rate	DR_{MAX}		500			kbps
SWITCHING RECEIVER (MAX33048E, MAX33049E) (*Note 5*)						
Receiver Propagation Delay	t_{RPLH}, t_{RPHL}	C_L = 15pF (*Figure 7*)			75	ns
Receiver Output Skew	t_{RSKEW}	C_L = 15pF (*Figure 7*)			10	ns
Maximum Data Rate	DR_{MAX}		20			Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*)			50	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*)			50	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*)			50	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*)			50	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*), (*Note 4*)			170	µs
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, MAX33049E (*Figure 8*), (*Note 4*)			170	µs
Time to Shutdown	t_{SHDN}	MAX33049E (*Note 4*)	250	800	1500	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to ground, unless otherwise noted.

Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI changes state.

Note 3: Capacitive load includes test probe and fixture capacitance.

Note 4: Shutdown is enabled when $\overline{RE}$ is high and DE is low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are held in this state for at least 1500ns, the device is guaranteed to have entered shutdown.

Note 5: Guaranteed by design, not production tested.

Test Circuits and Timing Diagrams

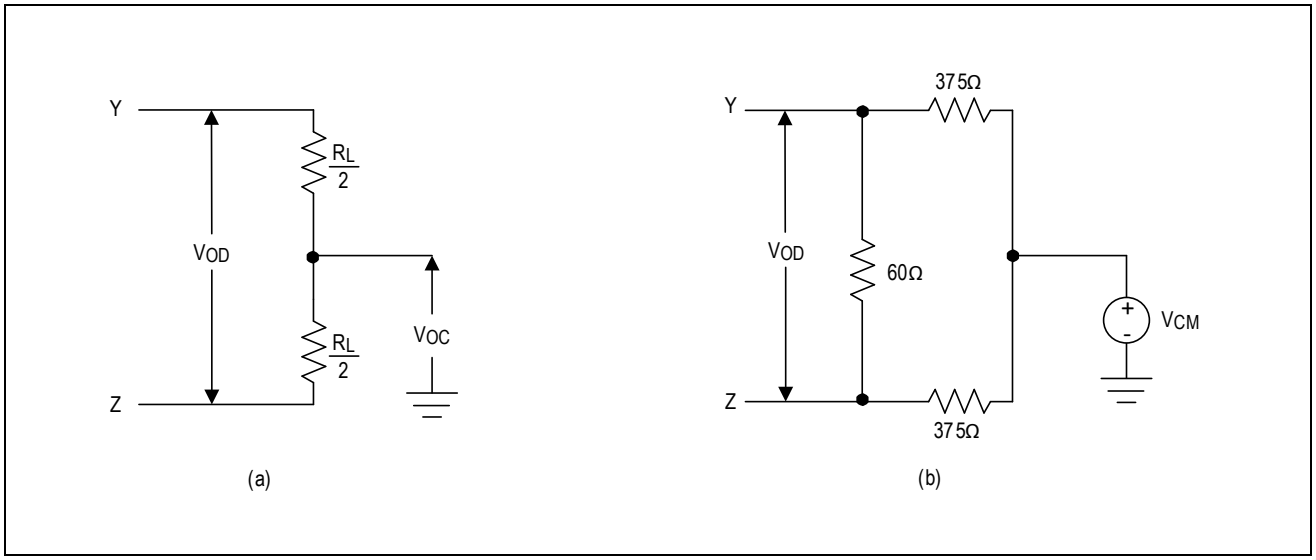


Figure 1. Driver DC Test Load

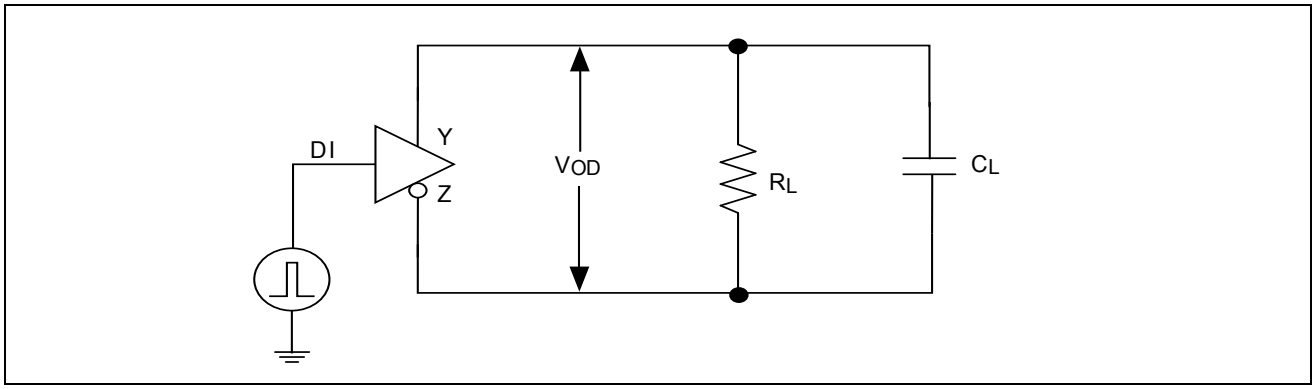


Figure 2. Driver Timer Test Circuit

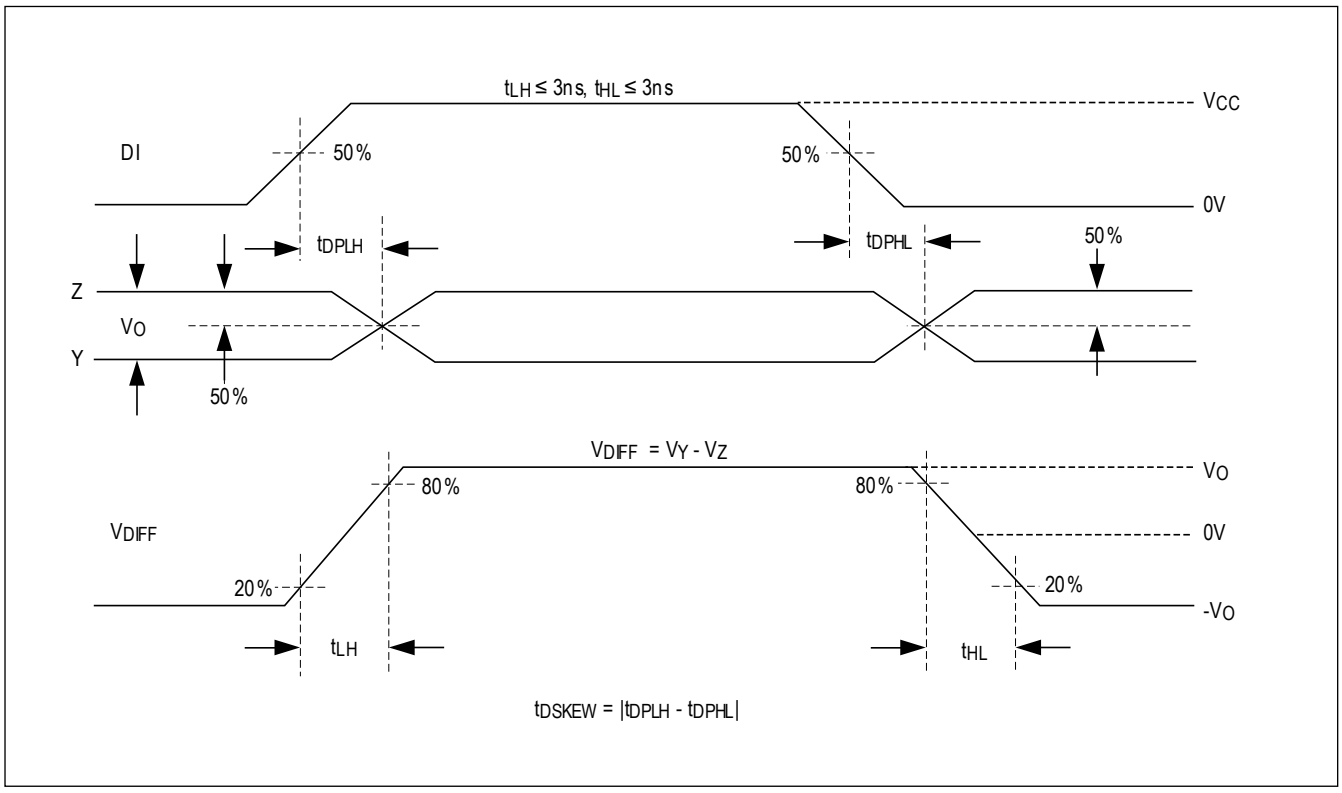


Figure 3. Driver Propagation Delays

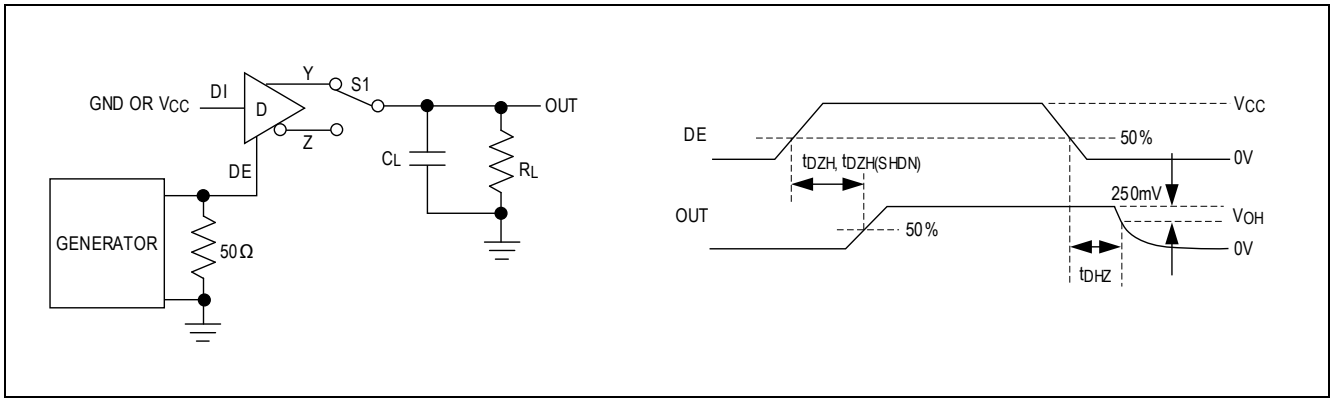


Figure 4. Driver Enable and Disable Times (t_{DHZ}, t_{DZH}, $t_{DZH(SHDN)}$)

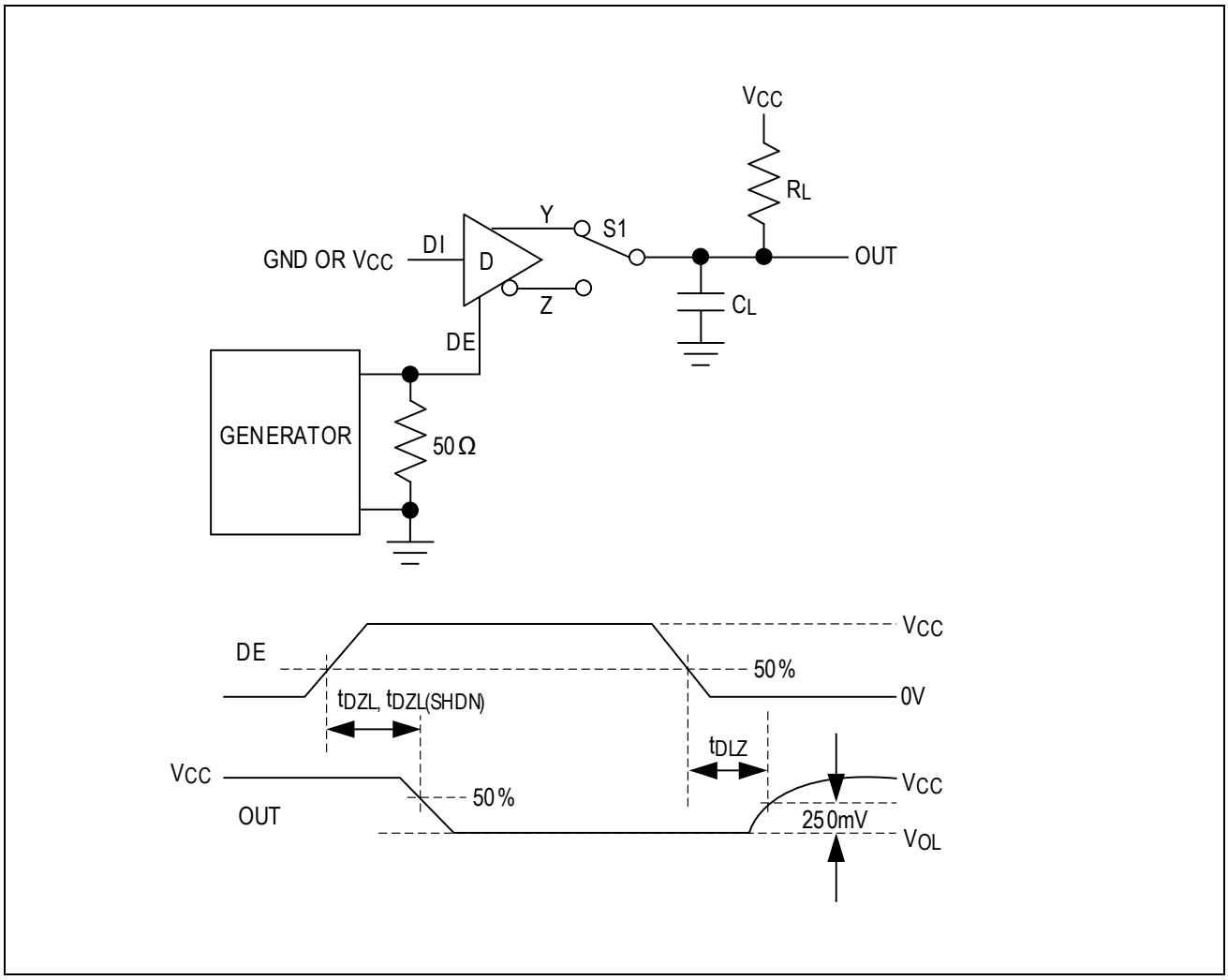


Figure 5. Driver Enable and Disable Times (t_{DZL}, $t_{DZL(SHDN)}$, t_{DLZ})

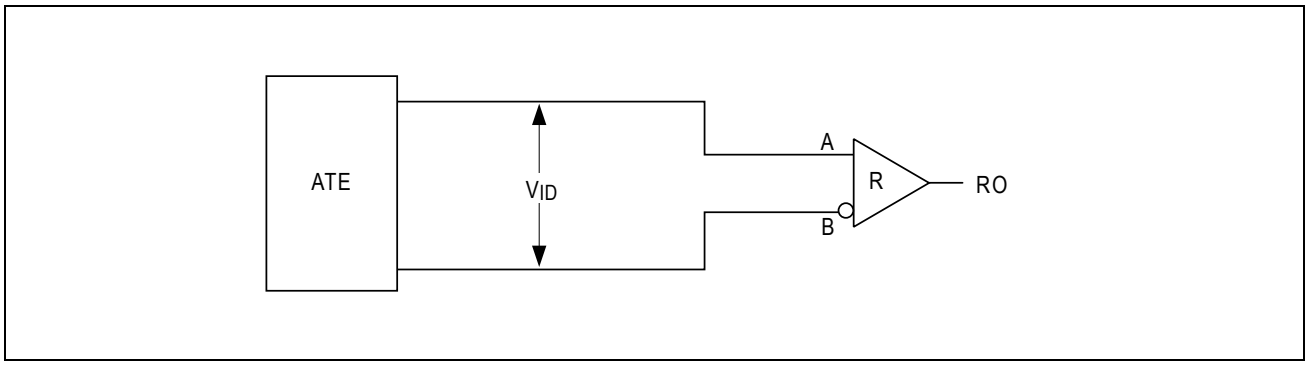


Figure 6. Receiver Propagation Delay Test Circuit

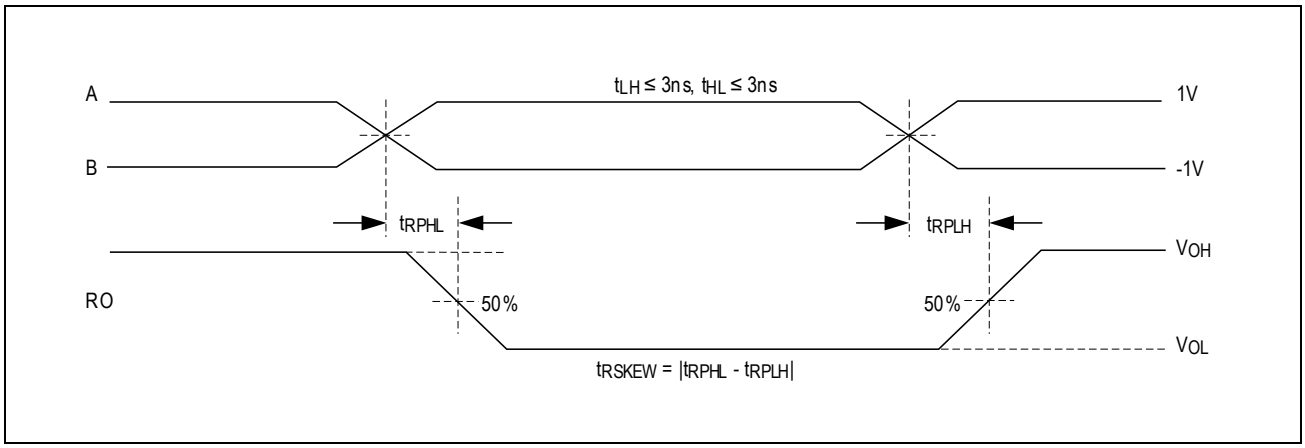


Figure 7. Receiver Propagation Delays

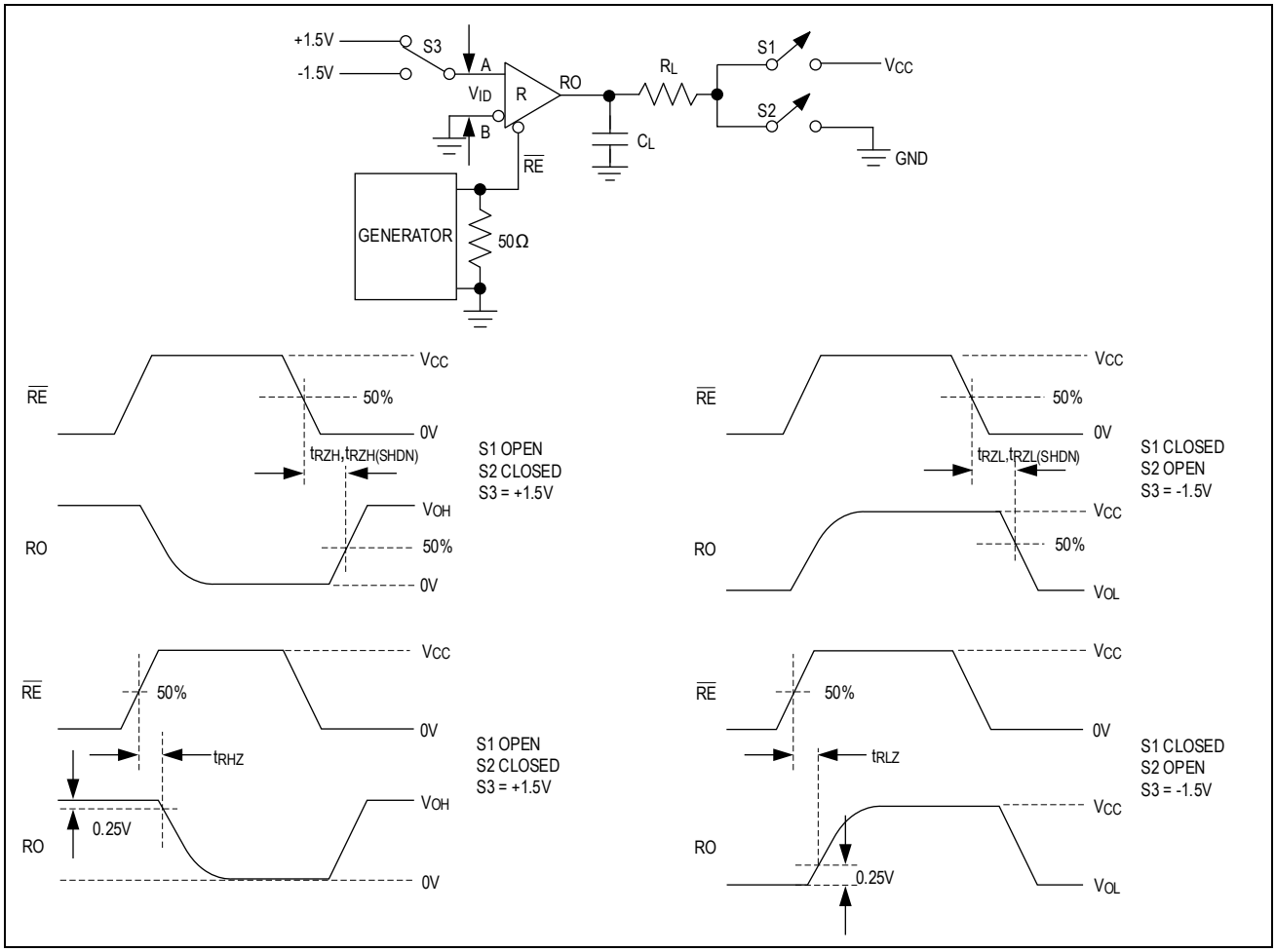
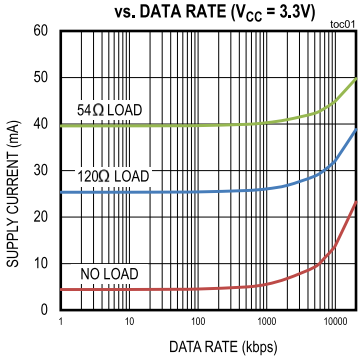


Figure 8. Receiver Enable and Disable Times

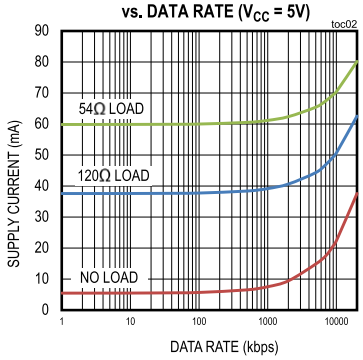
Typical Operating Characteristics

(V_{CC} = +3.3V or +5V and T_A = +25°C, unless otherwise noted.)

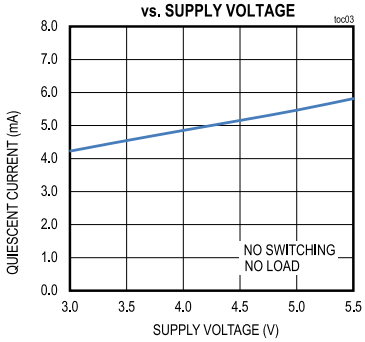
SUPPLY CURRENT vs. DATA RATE (V_{CC} = 3.3V)



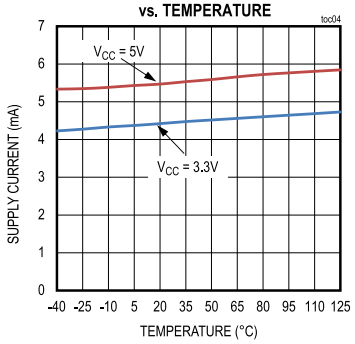
SUPPLY CURRENT vs. DATA RATE (V_{CC} = 5V)



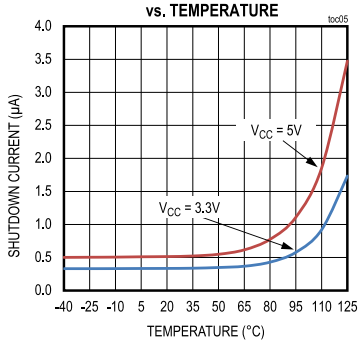
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



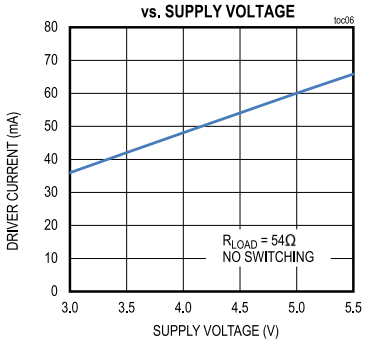
SUPPLY CURRENT vs. TEMPERATURE



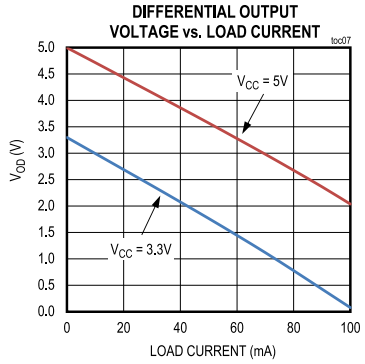
SHUTDOWN CURRENT vs. TEMPERATURE



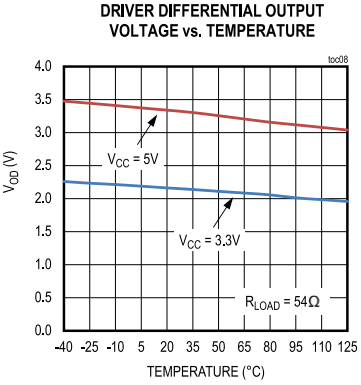
DRIVER CURRENT vs. SUPPLY VOLTAGE



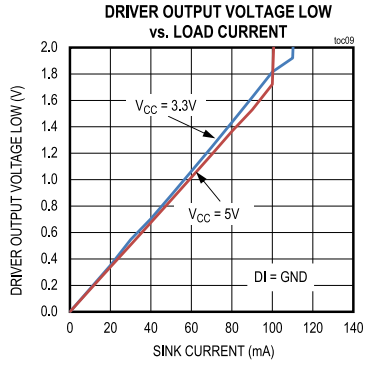
DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD CURRENT

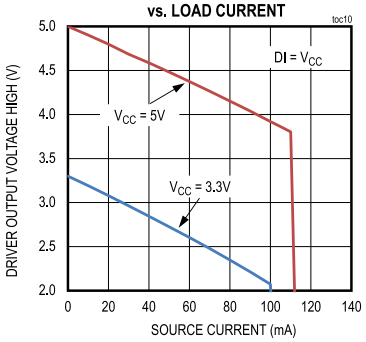


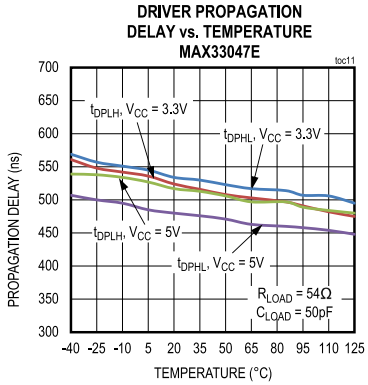
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE

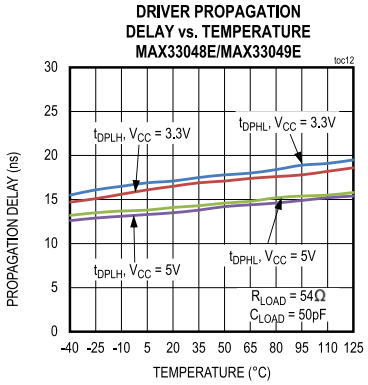


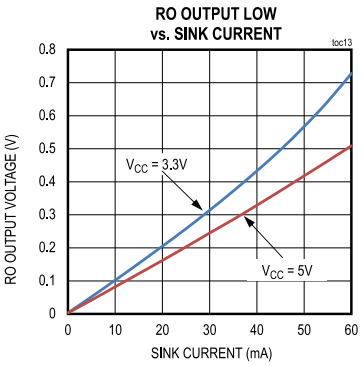
DRIVER OUTPUT VOLTAGE LOW vs. LOAD CURRENT

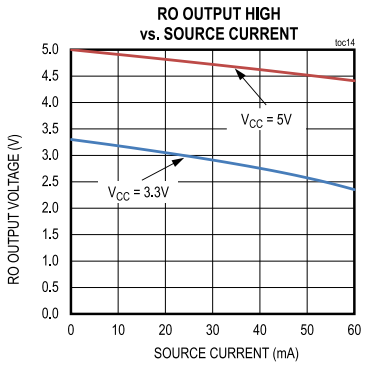


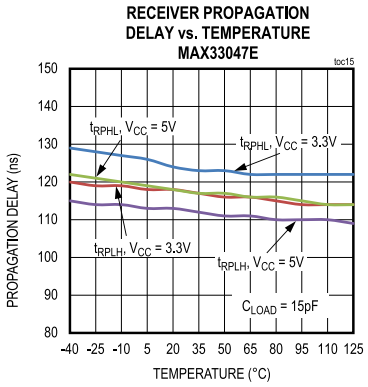

DRIVER OUTPUT VOLTAGE HIGH
vs. LOAD CURRENT
toc10
DI = VCC
VCC = 5V
VCC = 3.3V
DRIVER OUTPUT VOLTAGE HIGH (V)
SOURCE CURRENT (mA)

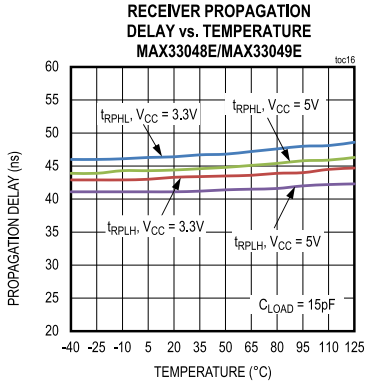

DRIVER PROPAGATION
DELAY vs. TEMPERATURE
MAX33047E
toc11
tDPLH, VCC = 3.3V
tDPHL, VCC = 3.3V
tDPLH, VCC = 5V
tDPHL, VCC = 5V
RLOAD = 54Ω
CLOAD = 50pF
PROPAGATION DELAY (ns)
TEMPERATURE (°C)


DRIVER PROPAGATION
DELAY vs. TEMPERATURE
MAX33048E/MAX33049E
toc12
tDPLH, VCC = 3.3V
tDPHL, VCC = 3.3V
tDPLH, VCC = 5V
tDPHL, VCC = 5V
RLOAD = 54Ω
CLOAD = 50pF
PROPAGATION DELAY (ns)
TEMPERATURE (°C)

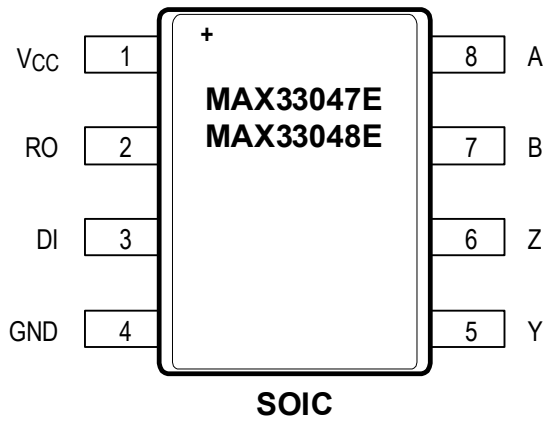

RO OUTPUT LOW
vs. SINK CURRENT
toc13
VCC = 3.3V
VCC = 5V
RO OUTPUT VOLTAGE (V)
SINK CURRENT (mA)

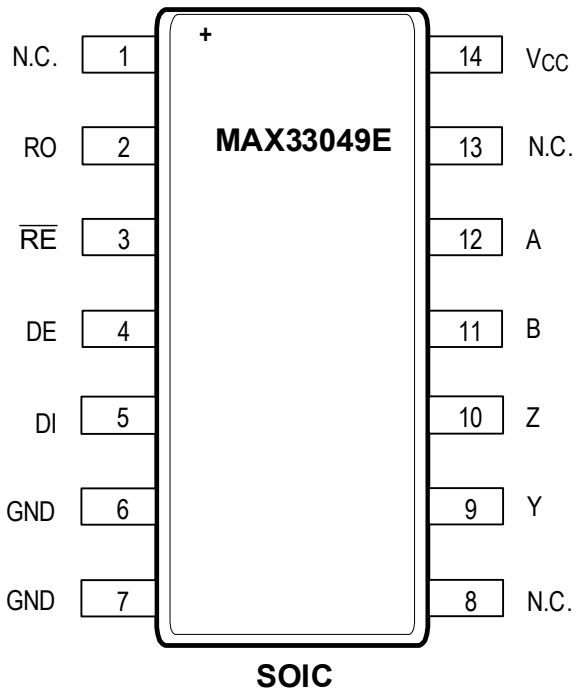

RO OUTPUT HIGH
vs. SOURCE CURRENT
toc14
VCC = 5V
VCC = 3.3V
RO OUTPUT VOLTAGE (V)
SOURCE CURRENT (mA)


RECEIVER PROPAGATION
DELAY vs. TEMPERATURE
MAX33047E
toc15
tRPHL, VCC = 5V
tRPHL, VCC = 3.3V
tRPLH, VCC = 3.3V
tRPLH, VCC = 5V
CLOAD = 15pF
PROPAGATION DELAY (ns)
TEMPERATURE (°C)


RECEIVER PROPAGATION
DELAY vs. TEMPERATURE
MAX33048E/MAX33049E
toc16
tRPHL, VCC = 3.3V
tRPHL, VCC = 5V
tRPLH, VCC = 3.3V
tRPLH, VCC = 5V
CLOAD = 15pF
PROPAGATION DELAY (ns)
TEMPERATURE (°C)

Pin Configurations





Pin Descriptions

PIN		NAME	FUNCTION
MAX33049E	MAX33047E /MAX33048 E		
1, 8, 13	-	N.C.	Not Connected. This pin is not internally connected.
2	2	RO	Receiver Output. For more information, see *Table 3* and *Table 4.*
3	-	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ high to disable the receiver. Drive $\overline{RE}$ low to enable the receiver and tristate RO. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
4	-	DE	Driver Output Enable. Drive DE high to enable the driver outputs. The driver outputs are high-impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode.
5	3	DI	Driver Input. For more information, see *Table 1* and *Table 2.*
6, 7	4	GND	Ground
9	5	Y	Noninverting Driver Output
10	6	Z	Inverting Driver Output
11	7	B	Inverting Receiver Input
12	8	A	Noninverting Receiver Input
14	1	V_{CC}	Power Supply Input. Bypass V_{CC} to ground with a 0.1µF ceramic capacitor as close to the device as possible.

Function Tables

Table 1. MAX33047E/MAX33048E Transmitting Function Table

INPUTS	OUTPUTS	
DI	Y	Z
0	0	1
1	1	0

Table 2. MAX33049E Transmitting Function Table

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Y	Z
X	1	0	0	1
X	1	1	1	0
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown – Driver outputs are high-impedance	

X = Don't Care

Table 3. MAX33047E/MAX33048E Receiving Function Table

INPUTS	OUTPUTS
$(V_A - V_B)$	RO
≥ - 50mV	1
≤ - 200mV	0

Table 4. MAX33049E Receiving Function Table

INPUTS			OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	RO
0	X	≥ - 50mV	1
0	X	≤ - 200mV	0
1	0	X	Shutdown − Receive output is high-impedance
1	1	X	High Impedance

X = Don't Care

Detailed Description

The MAX33047E/MAX33048E/MAX33049E full-duplex transceivers are optimized for RS-485/RS-422 applications. These devices contain one differential driver and one differential receiver. They feature a 1/8-unit load, which allows up to 256 transceivers on a single bus. The MAX33047E supports data rates of up to 500kbps, and the MAX33048E/MAX33049E support data rates of up to 20Mbps.

Driver

The driver accepts a single-ended, logic-level input (DI) and outputs a differential RS-485/RS-422 signal on the Y and Z lines. The MAX33049E features independent enable inputs for the driver and receiver, labeled DE and $\overline{RE}$. Drive the DE high to enable the driver. Set the DE low to disable the driver. Y and Z are in a high-impedance state when the driver is disabled.

Receiver

The receiver accepts a differential RS-485/RS-422 signal at the A and B inputs and outputs a single-ended, logic-level signal at RO. The MAX33049E features independent driver and receiver enable inputs, DE and $\overline{RE}$. Drive $\overline{RE}$ low to enable the receiver. Drive $\overline{RE}$ high to disable the receiver. RO exhibits a high-impedance state when $\overline{RE}$ is elevated.

Fault Protection

These devices provide ±25V of fault protection for the RS-485/RS-422 I/O interfaces. The A/B and Y/Z data lines can withstand a short circuit ranging from -25V to +25V. This extended overvoltage range provides protection in cases where A/B and Y/Z data lines accidentally short to a power line of up to +24V.

Hot-Swap Inputs (MAX33049E)

When circuit boards are inserted into a hot or powered backplane, disturbances on the enable inputs and differential receiver inputs can lead to data errors. Upon the initial insertion of the circuit board, the processor initiates its power-up sequence. During this period, the processor output drivers are in a state of high-impedance and cannot drive the DE and $\overline{RE}$ inputs of the MAX33049E to a defined logic level. Leakage currents of up to 10µA from the high-impedance outputs of a controller can cause the DE and $\overline{RE}$ signals to drift to an incorrect logic state. Additionally, parasitic capacitance on the circuit board can cause coupling of V_{CC} or GND to the DE and $\overline{RE}$ signals. These factors can improperly enable the driver or receiver. The MAX33049E features integrated hot-swap inputs to avoid these potential problems. When V_{CC} rises, an internal pull-down circuit holds DE low and $\overline{RE}$ high. After the initial power-up sequence, the pull-down circuit becomes transparent and resets the hot-swap-tolerable inputs.

The DE and $\overline{RE}$ enable inputs feature hot-swap capability. At the DE input, there are two nMOS devices, M1 and M2 (*Figure 9*). When the V_{CC} voltage increases from 0V, an internal 10µs timer turns on M2 and sets the SR latch, which in turn activates M1. Transistors M2 (a 500µA current sink) and M1 (a 100µA current sink) pull the DE to GND through a 5kΩ (typ) resistor. M2 is designed to pull the DE signal to a disabled state against an external parasitic capacitance of up to 100pF, which can drive the DE signal high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against tristate leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this moment, the SR latch resets, and M1 turns off. When M1 turns off, DE reverts to a standard high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot swap input is reset. A complementary circuit employing two pMOS devices pulls $\overline{RE}$ to V_{CC}.

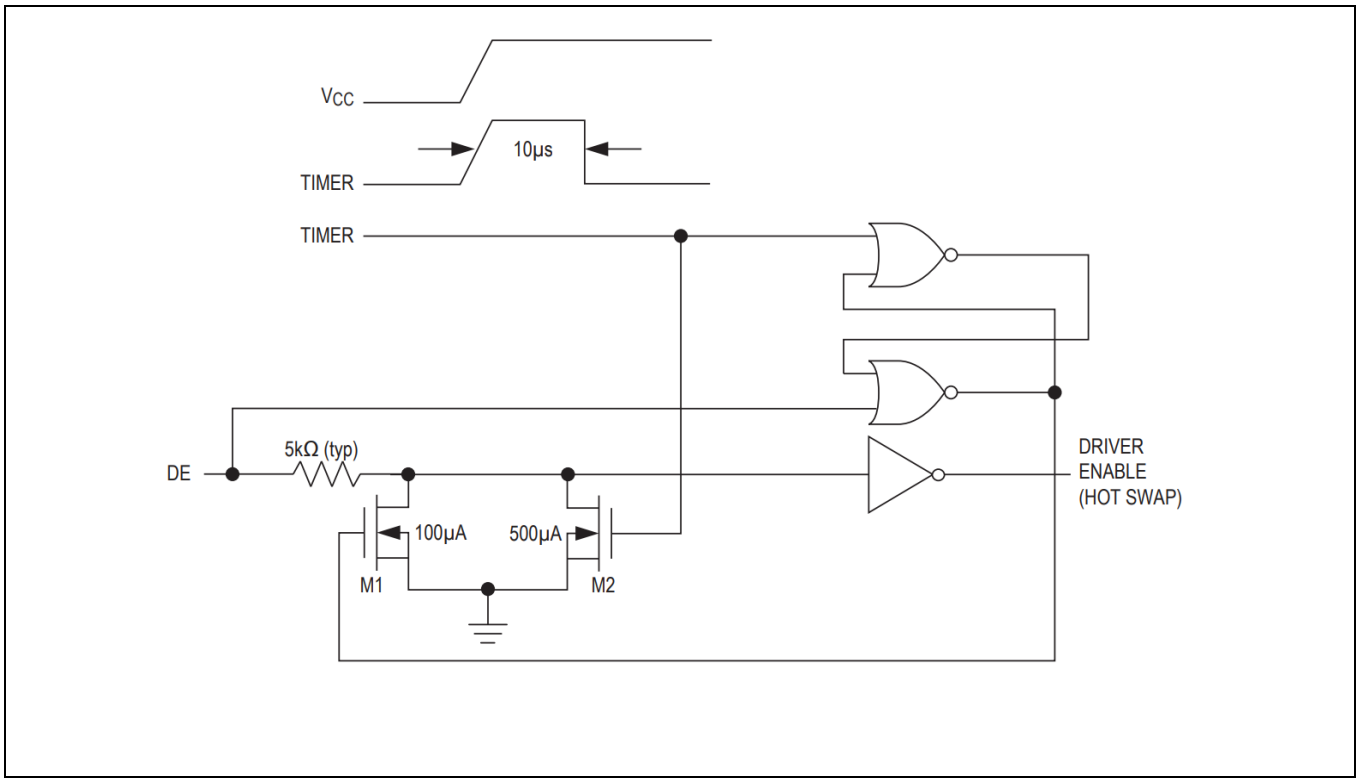


Figure 9. Simplified Structure of the Driver Enable (DE) Pin

True Fail-Safe Receiver

The MAX33047E/MAX33048E/MAX33049E include a true fail-safe feature that ensures the receiver output (RO) remains high when the receiver inputs are either shorted or open, or when they are connected to a differentially terminated transmission line with all drivers disabled. If the differential receiver input voltage (V_A - V_B) is greater than or equal to -50mV, RO is logic high.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus connections. The first, a current limit on the output stage, provides immediate protection against short circuits across the entire common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown (MAX33049E)

Drive DE low and $\overline{RE}$ high for at least 800ns (typ) to put the MAX33049E into low-power shutdown mode. The supply current decreases to 5µA (typ) when the device is in shutdown mode. A glitch protection feature ensures the MAX33049E does not accidentally enter shutdown mode due to logic skews between DE and $\overline{RE}$ when switching between transmitting and receiving modes.

Thermal Shutdown Protection

The MAX33047E/MAX33048E/MAX33049E feature thermal-shutdown protection. When the internal junction temperature exceeds +160°C (typ), the driver outputs are disabled, and RO is high-impedance state. The driver and receiver outputs are re-enabled when the junction temperature falls below +148°C (typ).

Applications Information

The MAX33047E/MAX33038E/MAX33049E full-duplex RS-485/RS-422 transceivers are optimized for robust communication of up to 20Mbps (MAX33048E/MAX33049E) in harsh industrial environments and feature ±40kV human body model (HBM) ESD protection and ±25V fault protection on all bus data pins A, B, Y, and Z.

The MAX33047E/MAX33048E transceivers can be used in bidirectional data communications on point-to-point network with the driver and receiver circuits always enabled, (see *Full Duplex Point-to-Point Network*).

The MAX33049E transceiver is designed for bidirectional data communications on multidrop networks, (see *Full Duplex Multidrop Network*). To minimize reflections on a multidrop network application, terminate the bus line at both ends with its characteristic impedance and keep stub lengths off the main line as short as possible.

Transient Protection on the Bus

For applications requiring high voltage transient protection such as surge transients, external protections are needed on the bus lines. The MAX33047E/MAX33048E/MAX33049E feature absolute maximum voltage ratings of ±30V on pins A, B, Y, and Z, allowing for the use of higher clamping voltage TVS diodes for protection. Choose a TVS diode with a clamping voltage below ±30V and ensure that any external protection added to the bus lines does not distort the signals at the required operating data rate.

Layout Guideline

The MAX33047E/MAX33048E/MAX33049E are designed for robust communication in harsh industrial environments. Use the following guidelines to ensure optimum performance:

- Place the bypass capacitor as close to the V_{CC} pin as possible.
- Use supply and ground planes to reduce trace inductance.
- Place external protection (resistors, capacitors, diodes) as close to the device as possible.
- Design protection components directly in the path of the driver output and receiver input signals.
- For a multipoint bus, keep stub length to a minimum to avoid reflections on the line.

Additionally, separate ground planes from the RS-485/RS-422 data lines when operating at high data rates to minimize capacitive coupling, which can slow down edge rates.

Integrated ESD Protection

ESD protection structures are integrated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX33047E/MAX33048E/MAX33049E have extra protection against static electricity. The ESD structures are designed to withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the devices keep working without experiencing latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs (Y and Z) and receiver inputs (A and B) of the devices are specified for protection against the cable-side ground within the following limits:

- ±40kV HBM
- ±15kV using the Air-Gap Discharge method specified in the IEC 61000-4-2.
- ±10kV using the Contact Discharge method specified in the IEC 61000-4-2.

Human Body Mode (HBM)

Figure 10 shows the HBM test model, and *Figure 11* shows the current waveform generated when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

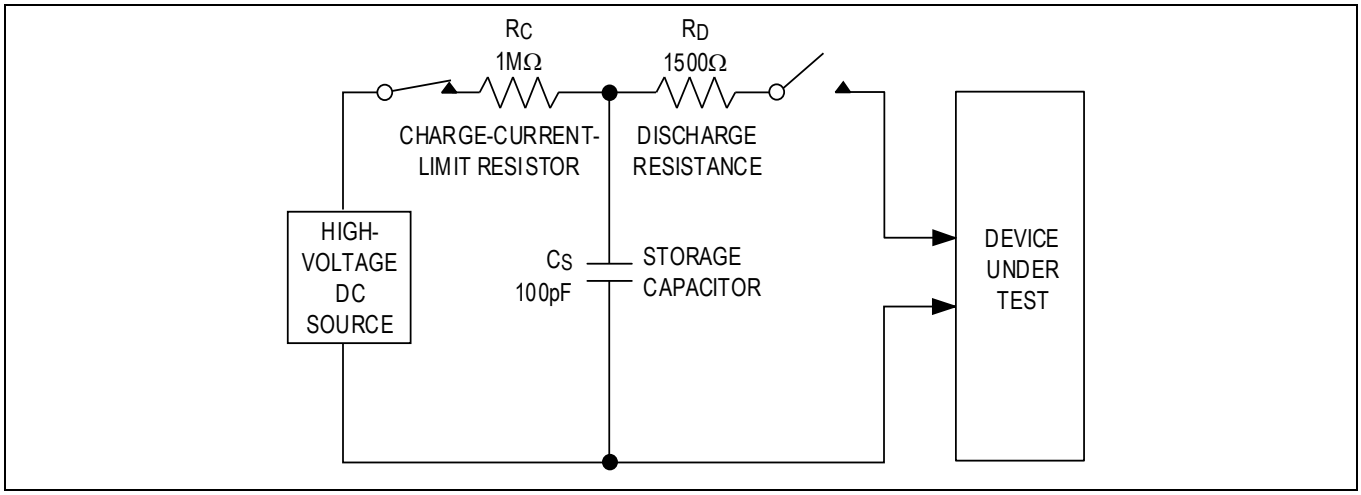


Figure 10. Human Body ESD Test Model

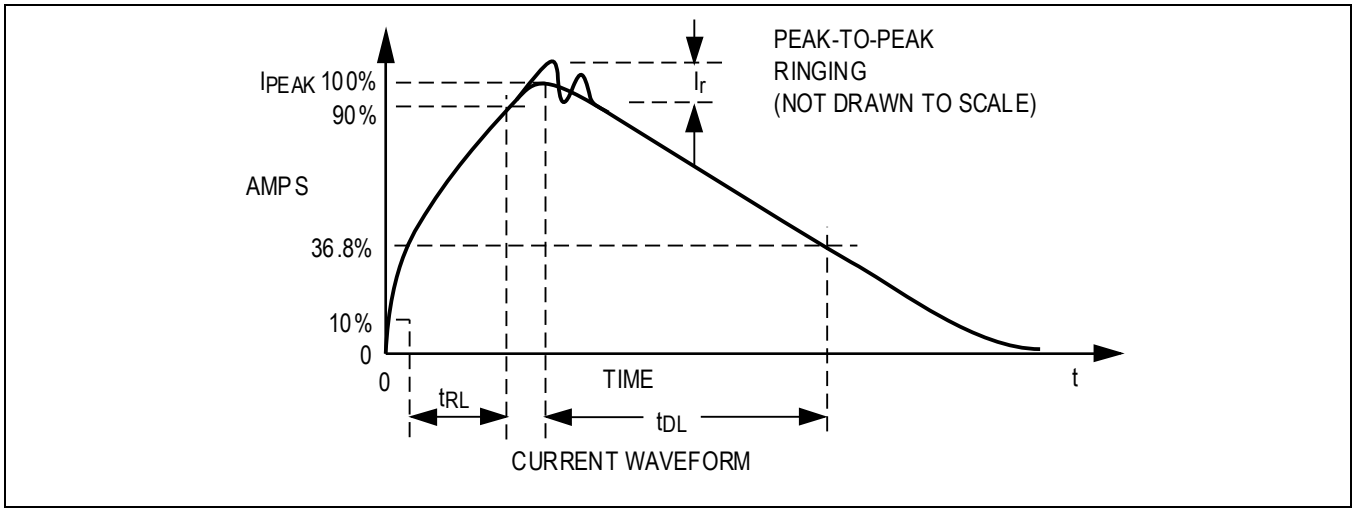


Figure 11. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The Integrated ESD protection circuitry in the MAX33047/MAX33048/MAX33049 facilitates the design of equipment that complies with IEC61000-4-2 standards. The primary difference between tests conducted using the HBM and IEC 61000-4-2 is the higher peak current observed in the IEC 61000-4-2, which is attributed to the lower series resistance in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. *Figure 12* shows the IEC 61000-4-2 test model, and *Figure 13* shows the current waveform for IEC 61000-4-2 ESD Contact Discharge.

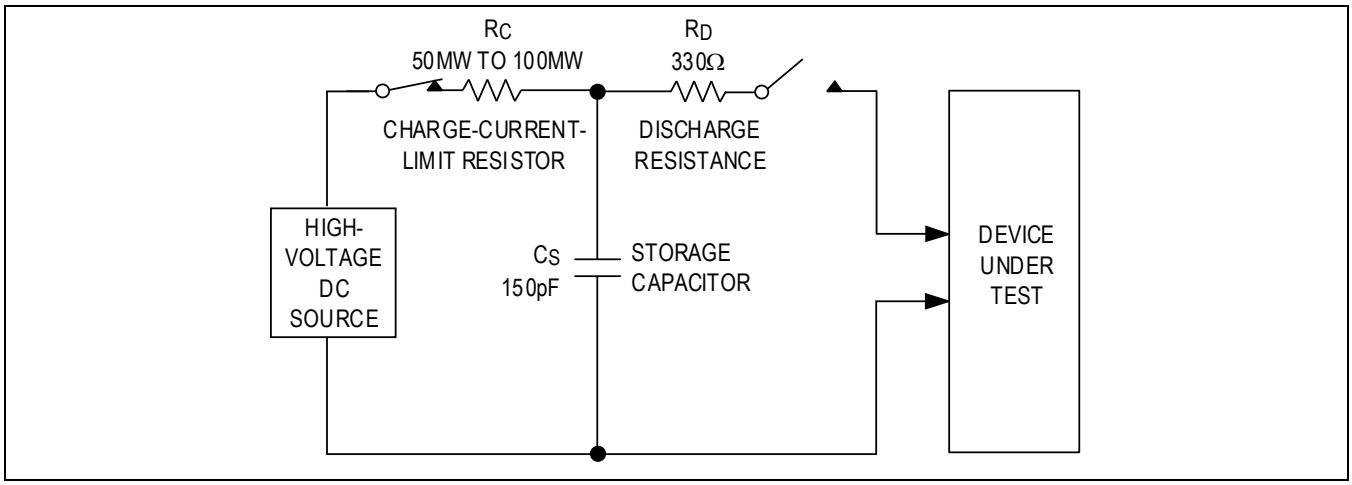


Figure 12. IEC 61000-4-2 ESD Test Model

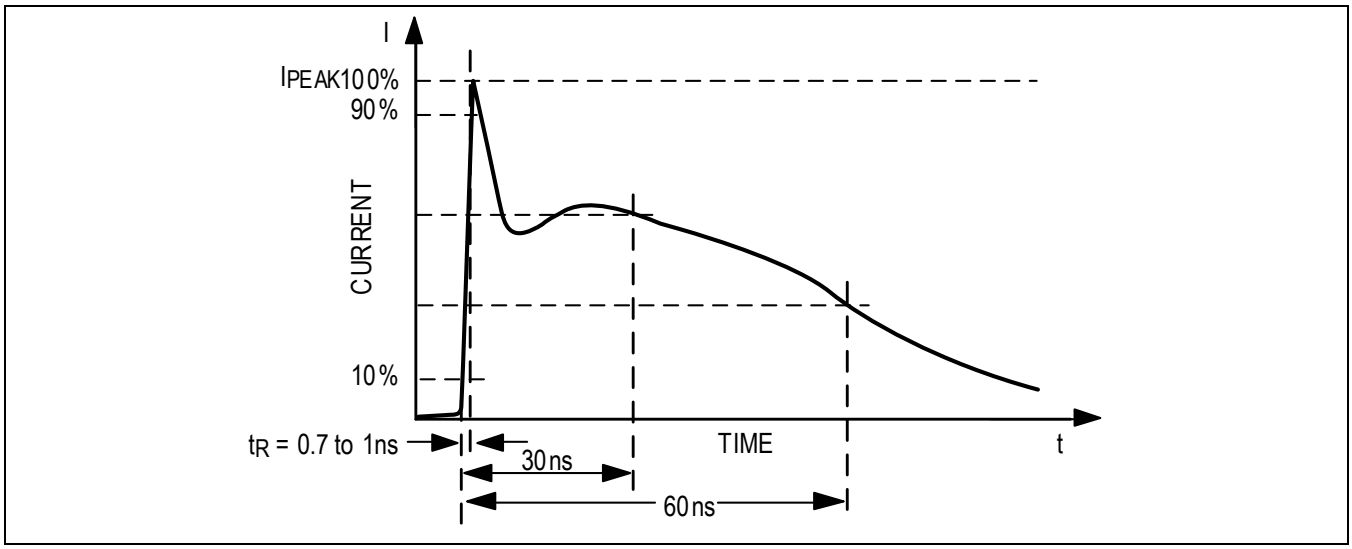
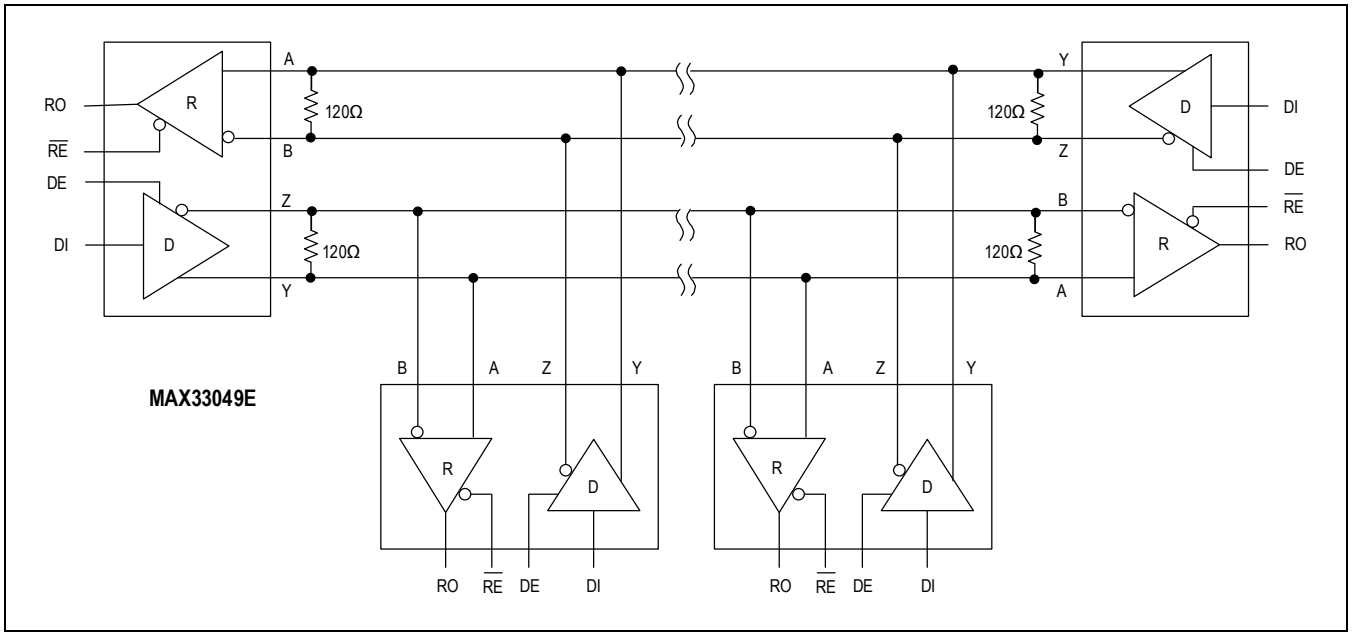


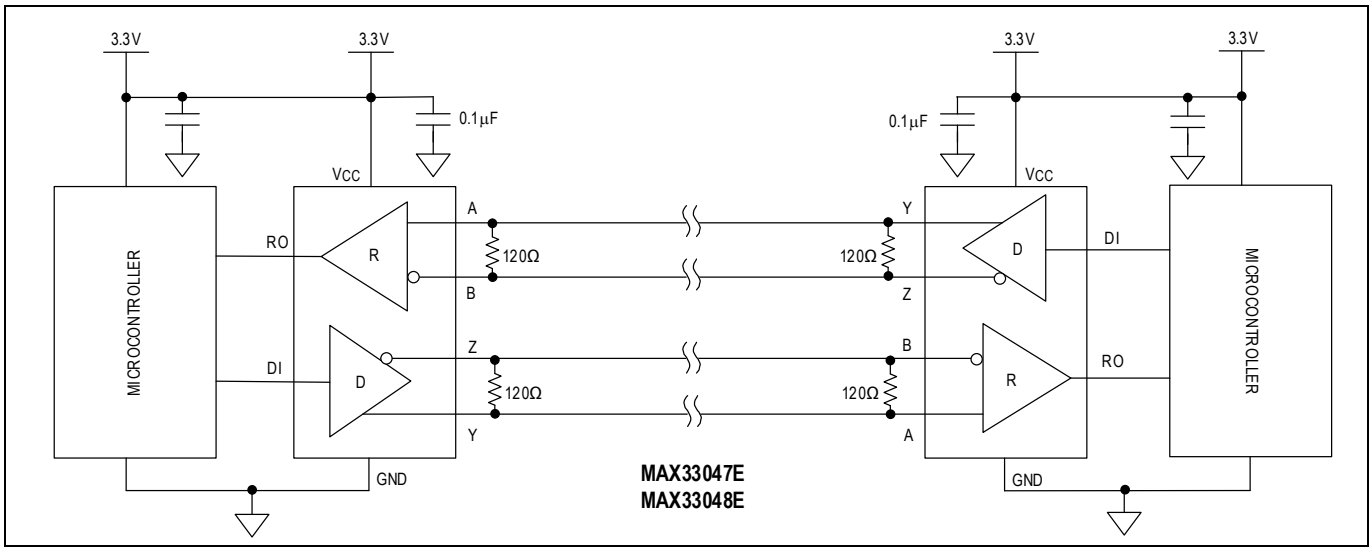
Figure 13. IEC 610004-2 ESD Generator Current Waveform

Typical Application Circuits

Full Duplex Multidrop Network



Full Duplex Point-to-Point Network



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	DATA RATE	DRIVER ENABLE	RECEIVER ENABLE	LOW POWER SHUTDOWN
MAX33047EASA+	-40°C to +125°C	8-pin SOIC	500kbps	NO	NO	NO
MAX33047EASA+T	-40°C to +125°C	8-pin SOIC	500kbps	NO	NO	NO
MAX33048EASA+	-40°C to +125°C	8-pin SOIC	20Mbps	NO	NO	NO
MAX33048EASA+T	-40°C to +125°C	8-pin SOIC	20Mbps	NO	NO	NO
MAX33049EASD+	-40°C to +125°C	14-pin SOIC	20Mbps	YES	YES	YES
MAX33049EASD+T	-40°C to +125°C	14-pin SOIC	20Mbps	YES	YES	YES

+ = Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and Reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	07/22	Release for market intro	—
1	12/24	Added new release information, updated General Description, Applications, Benefits and Features, Simplified Block Diagram, Absolute Maximum Ratings, Package Information, Electrical Characteristics, Test Circuits and Timing Diagrams, Typical Operating Characteristics, Pin Configurations, Pin Descriptions, Function Table, Detailed Description, Applications Information, Typical Application Circuits, and Ordering Information	1–21