MAX32672
ERRATA SHEET

Revision B2 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

This errata sheet only applies to components of this revision. These components are branded on the top side of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the product webpage at www.analog.com/MAX32672.

1) MEMORY MAY BE CORRUPTED DURING POWER-DOWN

Description:

An insufficient decay time of the V_{DD} (V_{DDA} = V_{DD}) supply can corrupt the flash memory contents.

Workaround:

The decay time of the V_{DD} supply from $V_{RST(VDDMIN)}$ to 1.47V must be greater than 100µs.

2) MEMORY MAY BE CORRUPTED DURING POWER-DOWN WHEN OPERATING IN DUAL-SUPPLY MODE

Description:

Incorrect sequencing of the V_{DD} (V_{DDA} = V_{DD}) and V_{CORE} supplies can corrupt the flash memory contents.

Workaround:

1. Control the power supplies so that:
   - $V_{CORE} \geq V_{CORE(MIN)}$ before $V_{DD} > V_{RST(VDDMIN)}$ on power up
   - $V_{DD} < V_{RST(VDDMIN)}$ before $V_{CORE} \leq V_{CORE(MIIN)}$ on power down
2. RSTN is asserted active whenever $V_{CORE} \leq V_{CORE(MIIN)}$.

Workaround #1 can be implemented using an LDO such as the MAX8516 or equivalent, as shown in *Figure 1*. The LDO is guaranteed to regulate its output, which drives V_{CORE} well below $V_{RST(VDDMIIN)}$.

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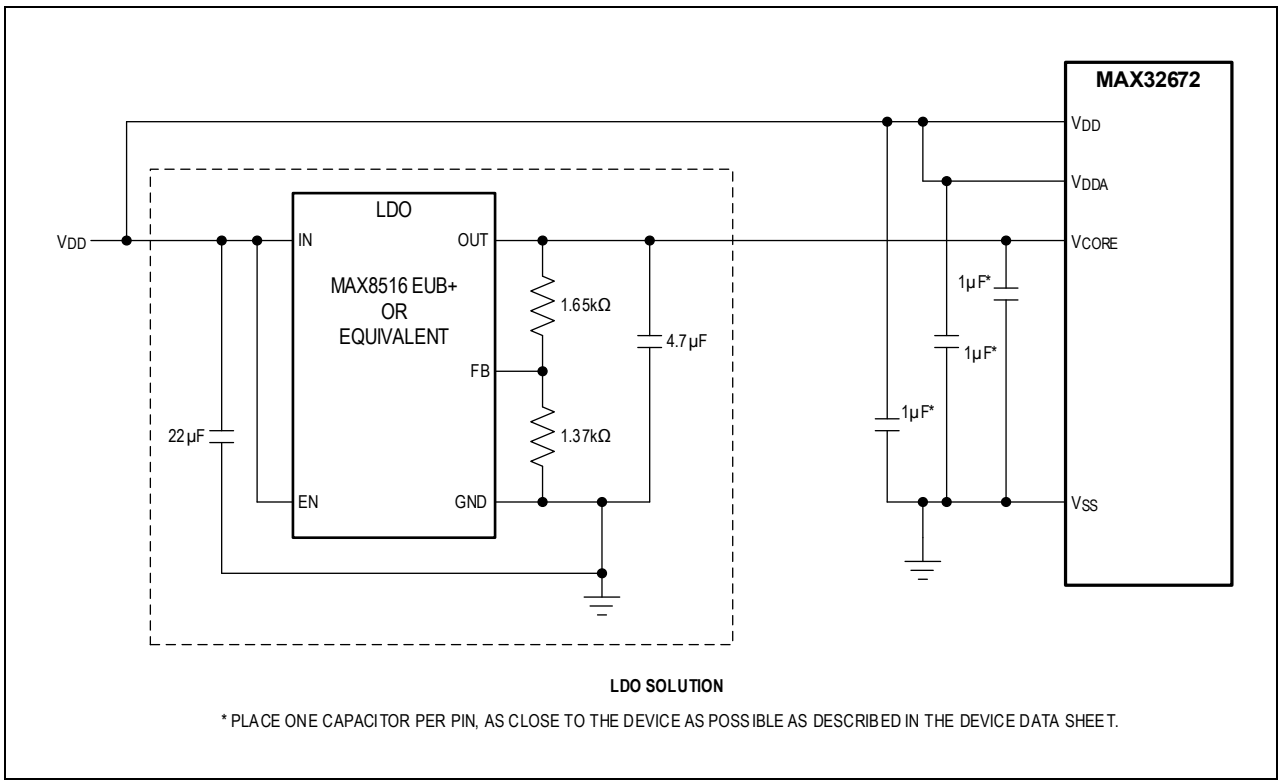

Figure 1. MAX32672 LDO Solution with MAX8516

3) TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18117)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

4) TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18135)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

5) I^2S TRANSMIT FIFO FAILS TO ASSERT HALF-EMPTY INTERRUPT

Description:
The transmit FIFO does not reliably assert the half-empty interrupt. (18118)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

6) I²S TRANSMIT FIFO FAILS TO ASSERT ONE ENTRY REMAINING INTERRUPT

Description:
The transmit FIFO does not reliably assert the one entry remaining interrupt. (18136)

Workaround:
Poll the transmit FIFO level and use software to manage the FIFO contents.

7) DATA IS TRANSMITTED IF AN EMPTY SPI FIFO IS WRITTEN WHILE A TRANSFER IS IN PROGRESS

Description:
In target mode, if data is fed into an empty transmit FIFO while chip select is active and an SPI transfer is in progress (SPI clock is provided by the controller), the first FIFO byte gets transferred immediately and is seen shifted or incomplete in the SPI MISO line. (18101)

Workaround:
Ensure that the target SPI does not let its transmit FIFO become empty.

8) TARGET MODE SPI FIFO TRANSMITS UNEXPECTED DATA WHEN TX FIFO EMPTY

Description:
After an SPI transmit FIFO is empty, the device is expected to transmit 0x00 on subsequent clocks. Instead, when the FIFO empty condition is met, the device continues to loop through the FIFO and transmit its contents. (18102)

Workaround:
None.

9) RECEIVE FIFO FAILS TO ASSERT OVERRUN INTERRUPT

Description:
The receive FIFO does not reliably assert the overrun interrupt. (18125)

Workaround:
Poll the receive FIFO level and use software to manage the FIFO contents.

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REV B2 ERRATA

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/24	Initial release	—