4A, 3MHz, 2.7V to 16V, Step-Down Switching Regulator

MAX20804

General Description

The MAX20804 is a fully integrated, highly efficient, step-down DC-DC switching regulator. It is able to operate from 2.7V to 16V input supplies, and each output can be regulated from 0.5V to 5.8V, delivering up to 4A of load current.

The switching frequency of this device can be configured from 500kHz to 3.0MHz and provides the capability of optimizing the design in terms of solution size and performance.

The MAX20804 utilizes fixed-frequency, current-mode control with internal compensation. The MAX20804 features a selectable advanced modulation scheme (AMS) to provide improved dynamic load-transient performance. The device also features selectable discontinuous current-mode (DCM) operation to improve light load efficiency. Operation settings and configurable features can be selected by connecting pin-strap resistors from the PGM_ pins to ground.

The MAX20804 has an internal 1.8V LDO output to power the gate drives and internal circuitry (V_{CC}).

The MAX20804 integrates multiple protections including positive and negative overcurrent protection, output overvoltage protection, and overtemperature protection to ensure a robust design.

The MAX20804 is available in a compact 3.0mm x 2.5mm FC2QFN package that supports -40°C to +150°C junction temperature operation. It is footprint compatible with the MAX20806 and MAX20807.

Applications

- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load Voltage Regulators

Benefits and Features

- High Power Density with Low Component Count
  - Single-Supply Operation with Integrated LDO for Bias Generation
  - Compact 3.0mm x 2.5mm, 14-Pin, FC2QFN Package
  - Internal Compensation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.5V to 5.8V Output Voltage Range
  - 500kHz to 3MHz Configurable Switching Frequency
  - -40°C to +150°C Junction Temperature Range
  - Two Pin-Strap Programming Pins to Select Different Configurations
- Optimized Performance and Efficiency
  - 91.3% Peak Efficiency with V_{DDH} = 12V, V_{OUT} = 1.8V, and f_{SW} = 1MHz
  - Selectable AMS to Improve Load Transient
  - Selectable DCM to Improve Light Load Efficiency

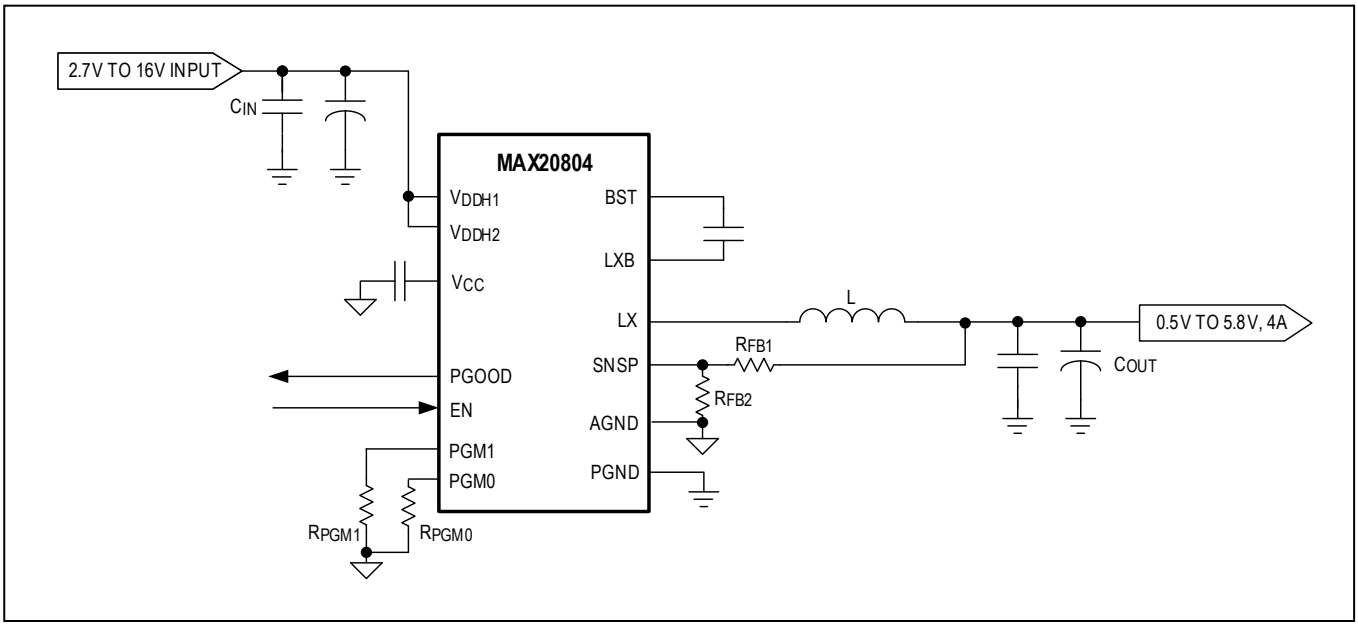
DESCRIPTION	CURRENT RATING (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating	4	2.7 to 16	0.5 to 5.8
Thermal Rating T_A = +85°C, No Air Flow	4	12	1.8
Thermal Rating T_A = +55°C, 200LFM Air Flow	4	12	5.0

**Maximum T_J = +125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the Typical Operating Characteristics.*

***Ordering Information* appears at end of data sheet.**

19-101960; Rev 0; 1/25

Simplified Application Circuit



Absolute Maximum Ratings

V_{DDH1}, V_{DDH2} to PGND (Note 1) ..... -0.3V to +19V
LX, LXB to PGND (DC) ..... -0.3V to +19V
LX, LXB to PGND (AC) (Note 2) ..... -10V to +23V
(AC) (Note 3) ..... -10V to +25V
V_{DDH1}, V_{DDH2} to LX (DC) (Note 1) ..... -0.3V to +19V
V_{DDH1}, V_{DDH2} to LX (AC) (Note 2) ..... -10V to +23V
(AC) (Note 3) ..... -10V to +25V
BST to PGND (DC) ..... -0.3V to +21.5V
BST to PGND (AC) (Note 2) ..... -7V to +25.5V
(AC) (Note 3) ..... -7V to +27.5V
BST to LXB ..... -0.3V to +2.5V
LXB to LX ..... -0.3V to +0.3V
PGND to AGND ..... -0.3V to +0.3V
V_{CC} to AGND ..... -0.3V to +2.5V
EN to AGND ..... -0.3V to +4V
PGOOD to AGND ..... -0.3V to +4V
SNSP to AGND ..... -0.3V to V_{CC}+0.3V
PGM0, PGM1 to AGND ..... -0.3V to V_{CC}+0.3V
Peak LX Current ..... -12A to +19A
Junction Temperature (T_J) (Note 4) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Peak Reflow Temperature Lead-Free ..... +260°C

Note 1: Input HF capacitors placed not more than 40 mils away from the $V_{DDH\_}$ pins are required to keep inductive voltage spikes within Absolute Maximum limits.

Note 2: AC is limited to 25ns.

Note 3: AC is limited to 2ns.

Note 4: The MAX20804 is guaranteed over the full -40°C to +150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than +125°C. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:
$T_J = T_A + (P_D \times \theta_{JA})$
where θ_{JA} (in °C/W) is the package thermal impedance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

14 FC2QFN

Package Code	F142A3F+1
Outline Number	21-100712
Land Pattern Number	90-100247
Thermal Resistance	
Junction to Ambient (θ_{JA}) JEDEC	51.7 °C/W
Junction to Ambient (θ_{JA}) on MAX20804EVKIT#	21.0 °C/W
Junction to Case (θ_{JC})	22.6 °C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(See the *Typical Application Circuit*. V_{DDH1} = V_{DDH2} = 12V, T_A = T_J = -40°C to +150°C, unless otherwise noted. Specifications are production tested at T_A = +25°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{DDH}		2.7		16	V
Input Supply Current	I_{VDDH}	EN = AGND		2		mA
Internal LDO Regulated Output	V_{CC}		1.75		1.95	V
Linear Regulator Current Limit			80			mA
		V_{CC} < 1.6V		20		
V_{CC} Undervoltage Lockout	V_{CC_UVLO}	Rising	1.65	1.67	1.74	V
		Falling		1.62		
V_{CC} Undervoltage Lockout Hysteresis				55		mV
V_{DDH} Undervoltage Lockout	V_{DDH_UVLO}	Rising	2.4	2.5	2.6	V
V_{DDH} Undervoltage Lockout Hysteresis				100		mV
OUTPUT VOLTAGE RANGE AND ACCURACY						
Feedback Voltage		V_{SNSP} = 0.5V, T_A = T_J = -40°C to +150°C	0.497	0.500	0.503	V
Voltage Sense Leakage Current	$I_{SNSP\_}$	T_A = T_J = +25°C	-1		+1	µA
SWITCHING FREQUENCY						
Switching Frequency	$f_{SW\_}$			500		kHz
				750		
				1000		
				1500		
				2000		
				3000		
Switching Frequency Accuracy			-10		+10	%
Minimum Controllable On-Time		I_{OUT} = 0A (*Note 5*)		24	40	ns
		I_{OUT} = 1A (*Note 5*)		22	37	
Minimum Controllable Off-Time		I_{OUT} = 0A (*Note 5*)		100	110	ns
ENABLE AND STARTUP						
Initialization Time	t_{INIT}			800		µs
EN Threshold		Rising	0.9			V
		Falling			0.6	
EN Filtering Delay	$t_{EN\_RISING\_DELAY}$	Rising		200		µs
	$t_{EN\_FALLING\_DELAY}$	Falling		2		
EN Leakage	I_{EN}	EN = 0V			250	nA
		EN = 1.85V			2	µA

(See the *Typical Application Circuit*. V_{DDH1} = V_{DDH2} = 12V, T_A = T_J = -40°C to +150°C, unless otherwise noted. Specifications are production tested at T_A = +25°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		EN = 4V		3.5	8	
Soft-Start Time	t_{SS}			3		ms
POWER-GOOD AND FAULT PROTECTIONS						
PGOOD Output Low		I_{PGOOD} = 4mA			0.4	V
PGOOD Leakage	I_{PGOOD}	PGOOD = 3.6V		0.01	1	µA
Output Undervoltage (UV) Threshold			-16	-13	-10	%
Output UV Deglitch Delay				4		µs
Output Overvoltage Protection (OVP) Threshold			10	13	16	%
Output OVP Threshold Deglitch Delay				2		µs
Positive Overcurrent Protection (POCP) Threshold	POCP	Inductor peak current, POCP = 5.4A	4.7	5.4	6.12	A
		Inductor peak current, POCP = 4A	3.58	4.0	4.5	
POCP Deglitch Delay				36		ns
Fast Positive Overcurrent Protection (FPOCP) Threshold	FPOCP		12.5	14.5	16.5	A
Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio	NOCP	With respect to POCP threshold (typ)		-84		%
NOCP Accuracy			-25		+25	%
BST UVLO Threshold	V_{BST}	Rising	1.47	1.59	1.66	V
		Falling	1.41	1.53	1.6	
Overtemperature Protection (OTP) Rising Threshold	OTP	(*Note 6*)		176		°C
OTP Accuracy				6		%
OTP Hysteresis				20		°C
Hiccup Protection Time	t_{HICCUP}			20		ms
DCM OPERATION MODE						
DCM Comparator Threshold to Enter DCM		POCP = 5.4A, inductor valley current		-290		mA
		POCP = 4A, inductor valley current		-195		
DCM Comparator Threshold to Exit DCM		Inductor valley current		100		mA
PROGRAMMING PINS						
PGM_ Pin Resistor Range	$R_{PGM\_}$	(*Note 7*)	0.095		115	kΩ
PGM_ Resistor Accuracy			-1		+1	%

Note 5: Guaranteed by design.

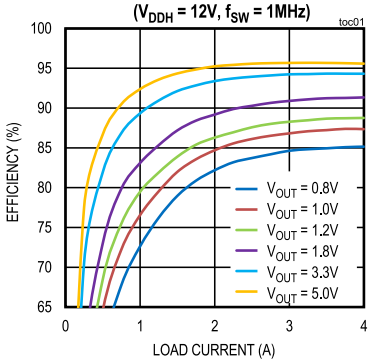
Note 6: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature exceeds +150°C temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature reduces lifetime.

Note 7: The PGM_ pin resistor value is read during startup initialization, and the detection is guaranteed below +125°C.

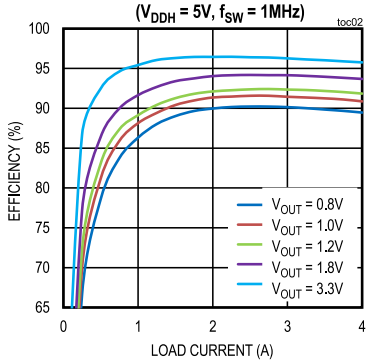
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DDH} = 12V, f_{SW} = 1MHz, tested on MAX20804EVKIT#, T_A = +25°C, unless otherwise noted.)

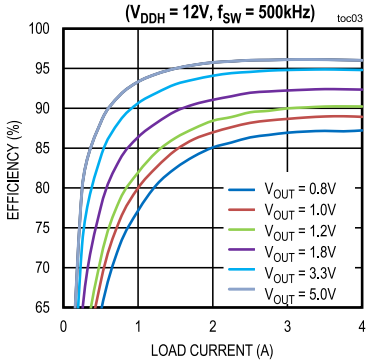
EFFICIENCY
(L = PA5003.XXXNLT)
(V_{DDH} = 12V, f_{SW} = 1MHz)



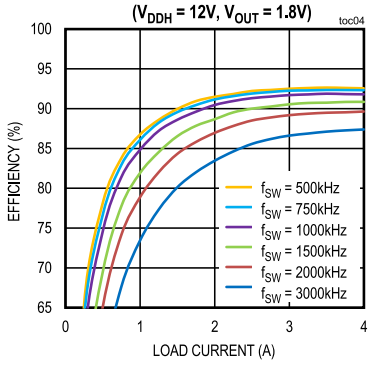
EFFICIENCY
(L = PA5003.XXXNLT)
(V_{DDH} = 5V, f_{SW} = 1MHz)



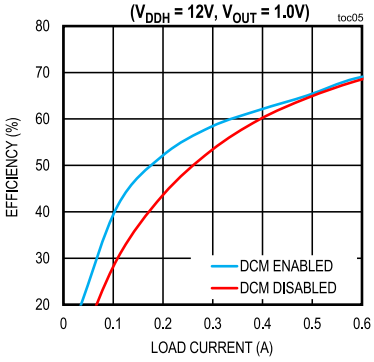
EFFICIENCY
(L = PA5005.XXXNLT)
(V_{DDH} = 12V, f_{SW} = 500kHz)



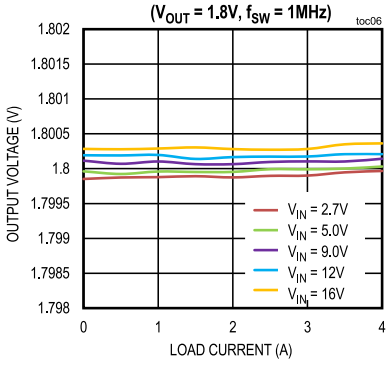
EFFICIENCY
(L = PA5005.152NLT)
(V_{DDH} = 12V, V_{OUT} = 1.8V)



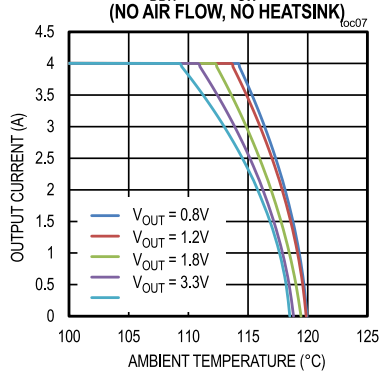
EFFICIENCY
(DCM vs. CCM, L = PA5003.471NLT)
(V_{DDH} = 12V, V_{OUT} = 1.0V)



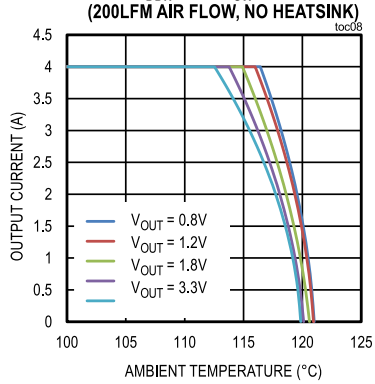
LOAD AND LINE REGULATIONS
(L = PA5003.821NLT)
(V_{OUT} = 1.8V, f_{SW} = 1MHz)



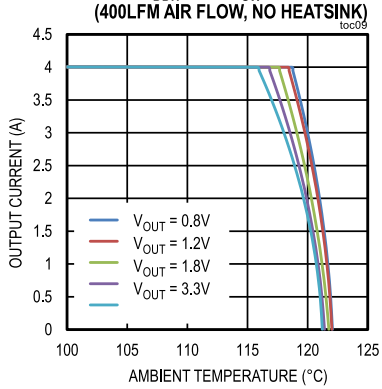
SAFE OPERATING AREA
(V_{DDH} = 12V, f_{SW} = 1MHz)
(NO AIR FLOW, NO HEATSINK)



SAFE OPERATING AREA
(V_{DDH} = 12V, f_{SW} = 1MHz)
(200LFM AIR FLOW, NO HEATSINK)

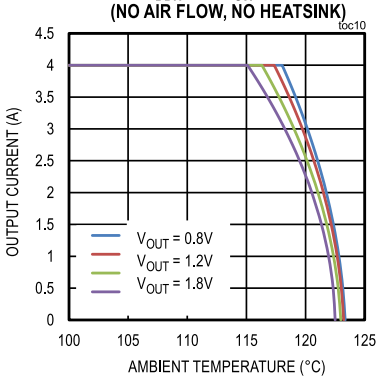


SAFE OPERATING AREA
(V_{DDH} = 12V, f_{SW} = 1MHz)
(400LFM AIR FLOW, NO HEATSINK)

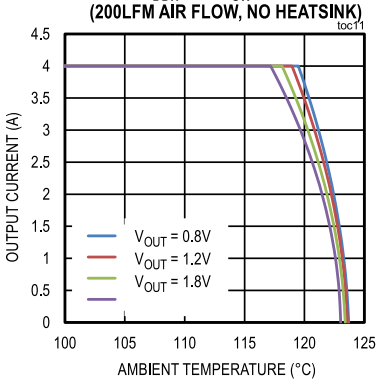


(*Typical Application Circuit*, V_{DDH} = 12V, f_{SW} = 1MHz, tested on MAX20804EVKIT#, T_A = +25°C, unless otherwise noted.)

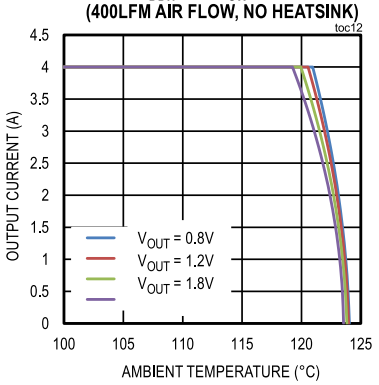
SAFE OPERATING AREA
(V_{DDH} = 5V, f_{SW} = 1MHz)
(NO AIR FLOW, NO HEATSINK)



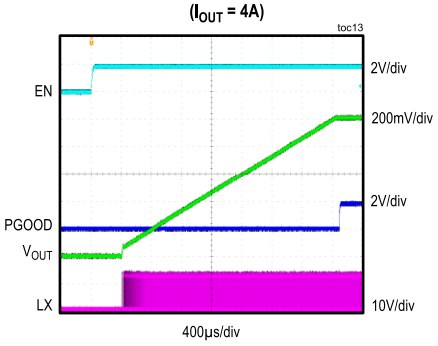
SAFE OPERATING AREA
(V_{DDH} = 5V, f_{SW} = 1MHz)
(200LFM AIR FLOW, NO HEATSINK)



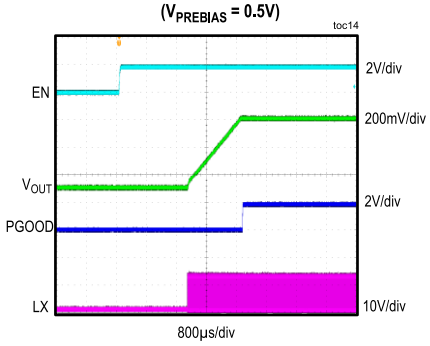
SAFE OPERATING AREA
(V_{DDH} = 5V, f_{SW} = 1MHz)
(400LFM AIR FLOW, NO HEATSINK)



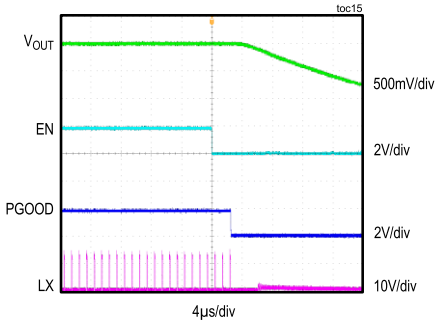
STARTUP
(I_{OUT} = 4A)



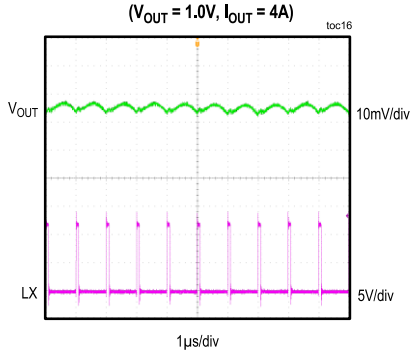
PREBIASED STARTUP
($V_{PREBIAS}$ = 0.5V)



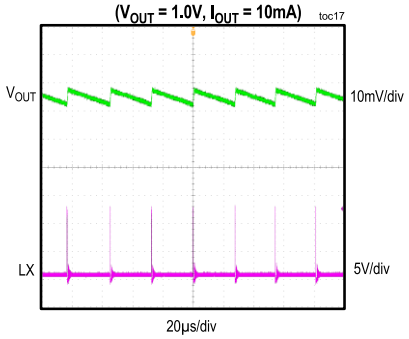
SHUTDOWN
(I_{OUT} = 4A)



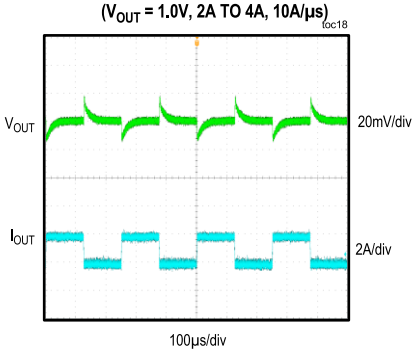
OUTPUT VOLTAGE RIPPLE
(V_{OUT} = 1.0V, I_{OUT} = 4A)



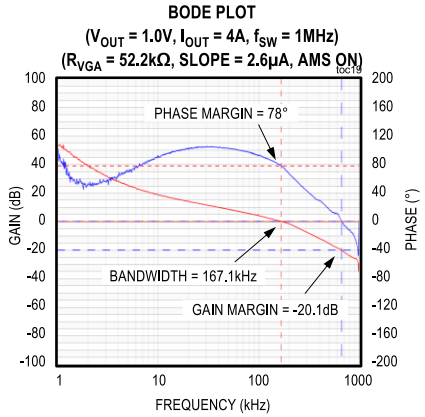
OUTPUT VOLTAGE RIPPLE
(DCM OPERATION)
(V_{OUT} = 1.0V, I_{OUT} = 10mA)

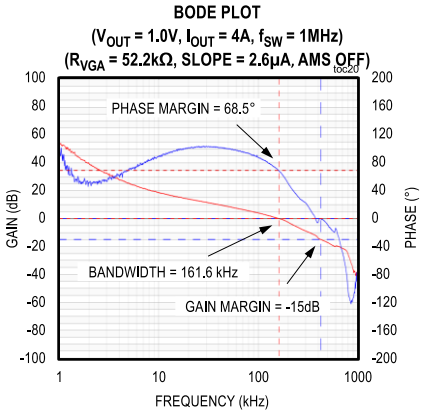


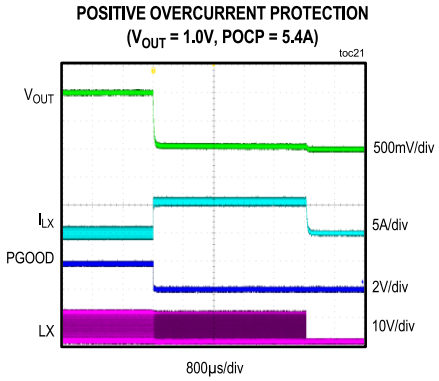
LOAD-TRANSIENT RESPONSE
(V_{OUT} = 1.0V, 2A TO 4A, 10A/µs)

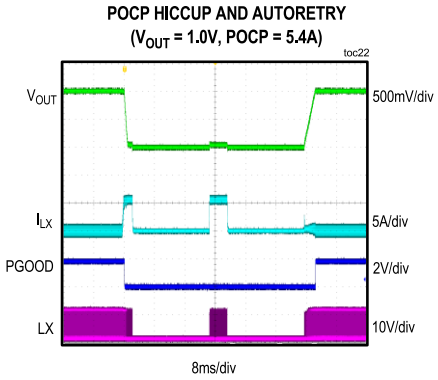


(*Typical Application Circuit*, V_{DDH} = 12V, f_{SW} = 1MHz, tested on MAX20804EVKIT#, T_A = +25°C, unless otherwise noted.)

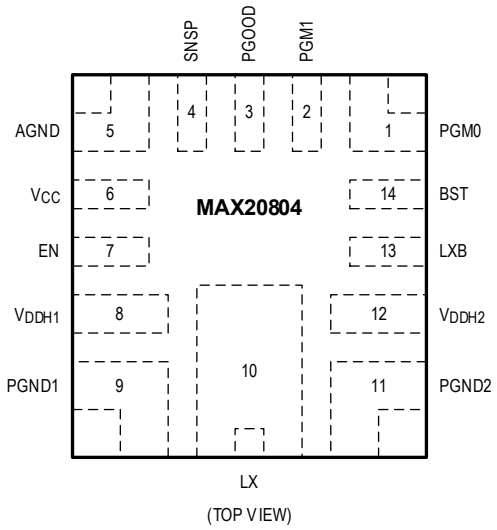








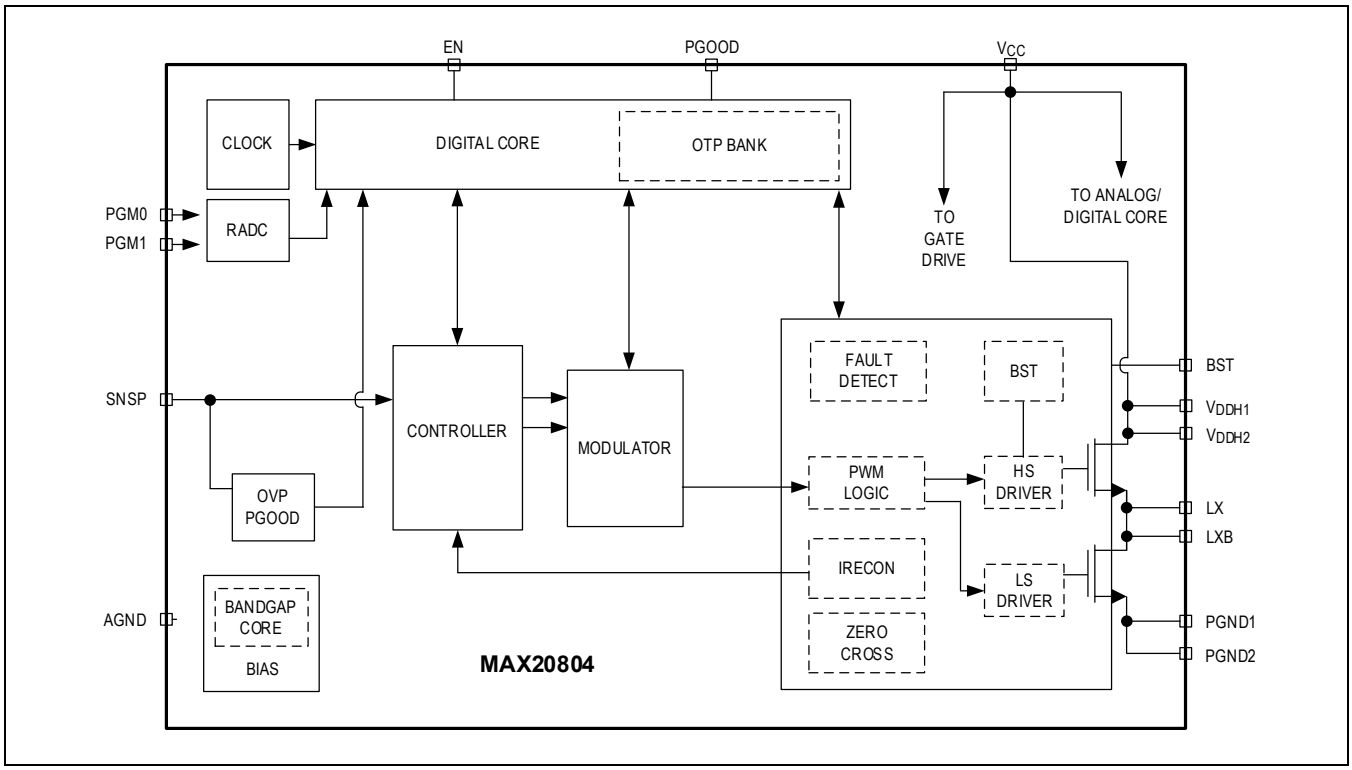
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1	PGM0	Program Input. Connect this pin to ground through a programming resistor.
2	PGM1	Program Input. Connect this pin to ground through a programming resistor.
3	PGOOD	Open-Drain, Power-Good Output
4	SNSP	Output Voltage-Sense Feedback Pin. Connect SNSP to V_{OUT} at the load. A resistive voltage-divider can be inserted between the output and SNSP to regulate the output above the 0.5V fixed reference voltage.
5	AGND	Analog Ground
6	V_{CC}	Internal 1.8V LDO Output. Connect a 2.2µF or greater ceramic capacitor from V_{CC} to AGND.
7	EN	Output Enable
8	V_{DDH1}	Regulator Input Supply. V_{DDH1} and V_{DDH2} should be connected on the PCB.
9	PGND1	Power Ground. PGND1 and PGND2 should be connected on the PCB.
10	LX	Switching Node. Connect LX directly to the output inductor.
11	PGND2	Power Ground. PGND1 and PGND2 should be connected on the PCB.
12	V_{DDH2}	Regulator Input Supply. V_{DDH1} and V_{DDH2} should be connected on the PCB.
13	LXB	Switching Node for Bootstrap Capacitor Connection. LXB and LX are connected internally.
14	BST	Bootstrap Pin. Connect a 0.22µF ceramic capacitor from BST to LXB.

Functional Diagrams



Detailed Description

Control Architecture

The MAX20804 control loop is based on fixed-frequency, peak current-mode control architecture. A simplified control architecture is shown in *Figure 1*. The control loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the pulse-width modulation (PWM) signals to drive high-side and low-side MOSFETs. The device has a fixed 0.5V reference voltage (V_{REF}). The difference between V_{REF} and the sensed output voltage is amplified by the first error amplifier. Its output voltage (V_{ERR}) is used as the input of the voltage loop compensation network. The output of the compensation network (V_{COMP}) is fed to a PWM comparator with the current-sense signal (V_{ISENSE}) and slope compensation (V_{RAMP}). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It can either be a fixed-frequency clock or a phase-shifted clock if AMS is enabled.

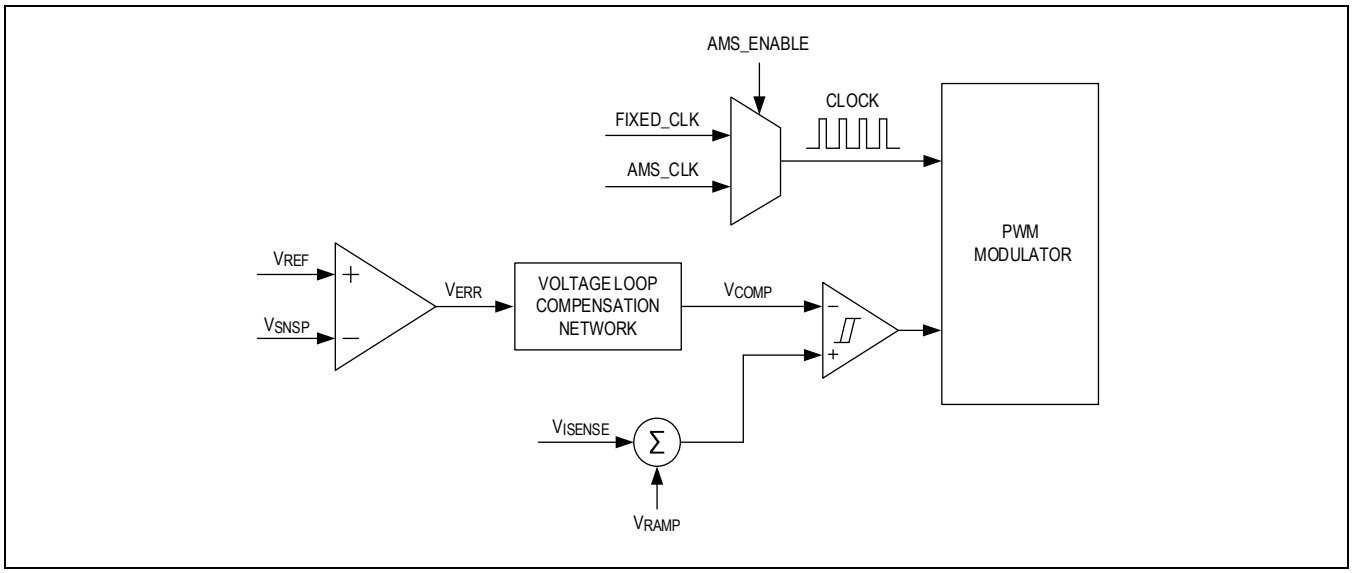


Figure 1. Simplified Control Architecture

Advanced Modulation Scheme (AMS)

The MAX20804 offers a selectable advanced modulation scheme (AMS) to provide improved transient response. AMS provides a significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges, which results a temporary increase or decrease of the switching frequency during large load transients. *Figure 2* shows the scheme to include leading-edge modulation with the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows turn-on and turn-off with minimal delay. Since the total inductor current increases very quickly, thus satisfying the load demand, the current drawn from the output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, output capacitance can be minimized.

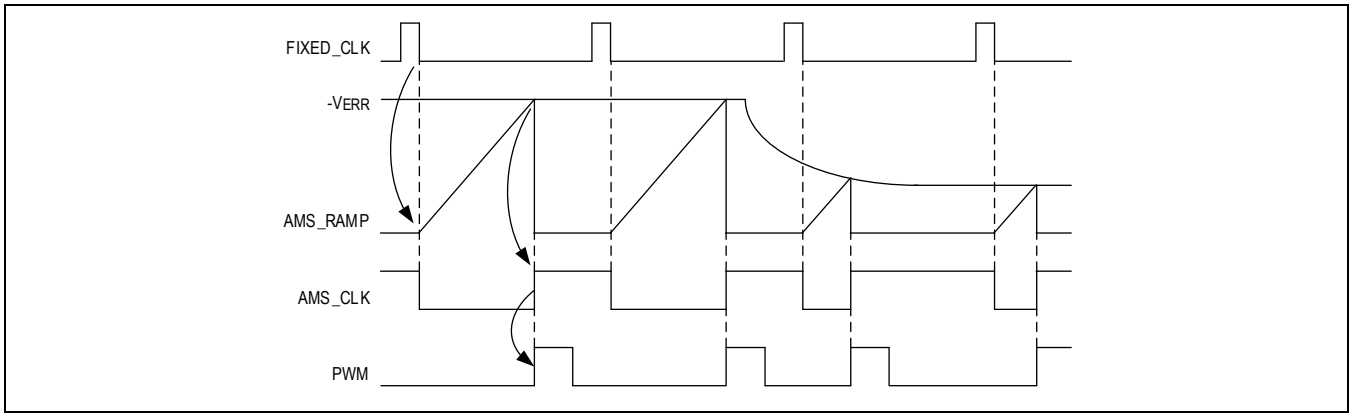


Figure 2. AMS Operation

Discontinuous Current-Mode (DCM) Operation

DCM operation is an optional feature to improve light load efficiency. It is required that V_{DDH} is at least 2V higher than the desired V_{OUT} for the device to operate in DCM. The device has a DCM current-detection comparator to monitor the inductor valley current while operating in CCM. At light load, if the inductor valley current is below the DCM comparator threshold for at least 48 consecutive cycles, the device transitions seamlessly to DCM. Once in DCM, the switching frequency decreases as the load decreases. The device transitions back to CCM operation as soon as the inductor valley current is higher than 100mA.

Internal Linear Regulator

The device contains an internal 1.8V linear regulator (LDO). The 1.8V LDO output voltage on V_{CC} is derived from the V_{DDH} pin by default.

The 1.8V voltage on the V_{CC} pin supplies the current to the MOSFET drivers. A decoupling capacitor of at least 2.2µF must be connected between V_{CC} and AGND.

Startup and Shutdown

The startup and shutdown timing is shown in *Figure 3*. When the V_{CC} pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. Configuration settings on the PGM_ pins are read. Once initialization is complete, the device detects the V_{DDH} UVLO and EN statuses. When both are above their rising thresholds, the soft-start begins and switching is enabled. The output voltage starts to ramp up. The soft-start ramp time is 3ms. If there are no faults, the open-drain PGOOD pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with the output prebiased.

During operation, if either the V_{DDH} UVLO or EN falls below its threshold, switching is stopped immediately. The output voltage is discharged by the load current.

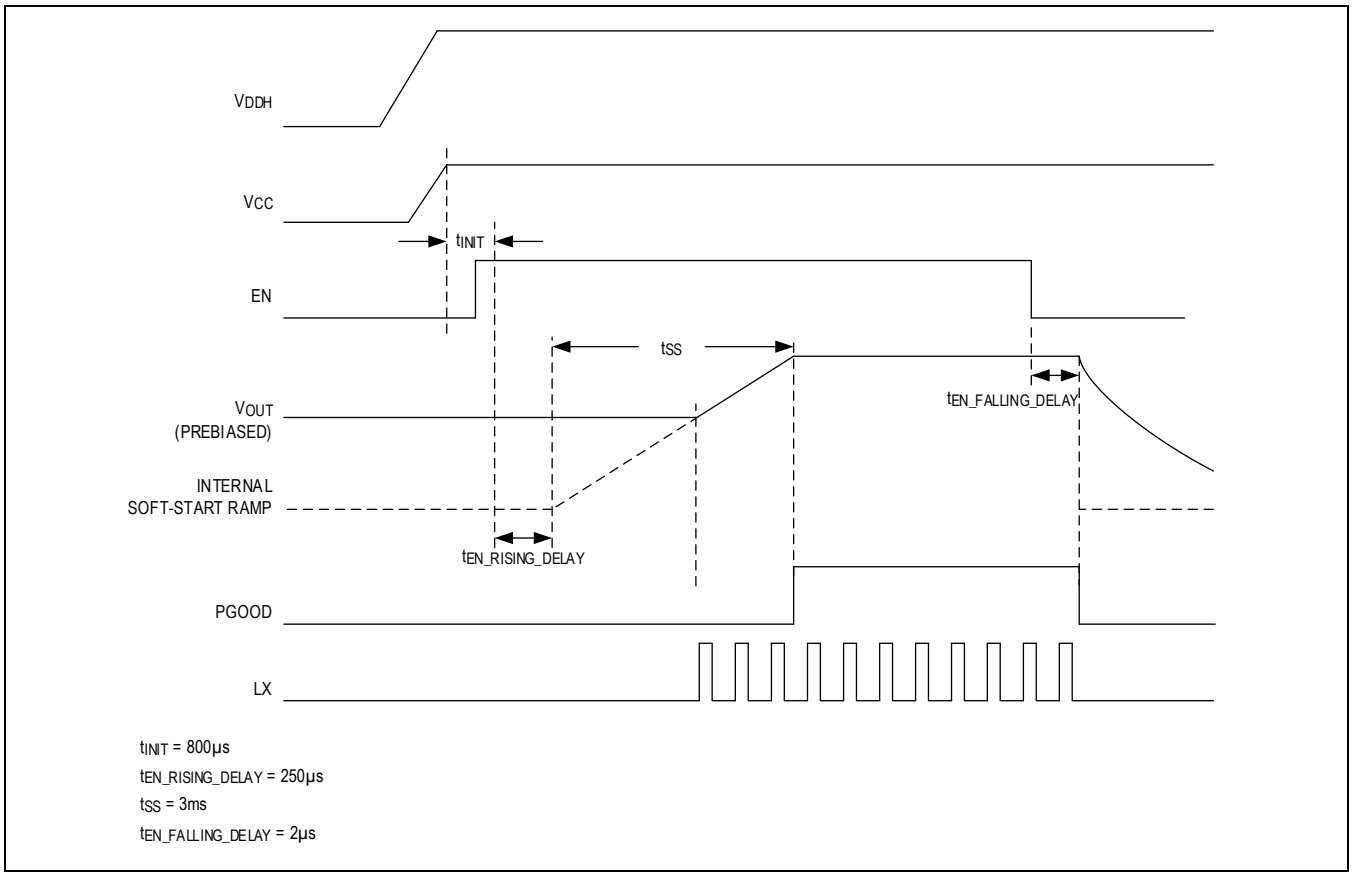


Figure 3. Startup and Shutdown Timing

Fault Handling

Input Undervoltage Lockout (V_{DDH} UVLO)

The MAX20804 internally monitors the V_{DDH} voltage level. When the input supply voltage is below the UVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO status is cleared. See the *Startup and Shutdown* section for the start-up sequence.

Output Overvoltage Protection (OVP)

The feedback voltage of V_{SNSP} – AGND is monitored for output overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OVP status is cleared.

Positive Overcurrent Protection (POCP)

The device's peak current-mode control architecture provides inherent current limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limited on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events in each switching cycle. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. POCP is a hiccup protection, and the device restarts after 20ms.

The MAX20804 offers two POCP thresholds (5.4A and 4A) that can be selected by the PGM1 pin (see the *Pin-Strap Programmability* section). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (see the *Output Inductor Selection* section).

Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -84% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. Similar to that of POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives the PGOOD pin low. NOCP is a hiccup protection, and the device restarts after 20ms.

Overtemperature Protection (OTP)

The overtemperature protection threshold is +176°C with 20°C hysteresis. If the junction temperature reaches the OTP threshold during operation, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OTP status is cleared.

Pin-Strap Programmability

The MAX20804 has two program pins (PGM0 and PGM1) to set some of the key configurations of the device. The PGM_ values are read during start-up initialization, and the detection is guaranteed below +125°C. PGM0 has 18 detection levels, and PGM1 has 32 detection levels. A pin-strap resistor is connected from the PGM_ pin to AGND to select one of the codes. See the *Internal Compensation Selection* section for information about how to select the compensation parameters for optimized control loop performance.

Table 1. PGM0 Switching Frequency, AMS, and DCM Selections

PGM0 CODES	R_{PGM0} (Ω)	AMS	DCM	f_{SW} (kHz)
0	95.3	Disable	Disable	500
1	309			750
2	649			1000
3	909			1500
4	1210			2000
5	1620			3000
6	2150	Enable		500
7	2490			750
8	8060			1000
9	16900			1500
10	26100			2000
11	36500			3000
12	42200		Enable	500
13	56200			750
14	75000			1000
15	86600			1500

16	100000			2000
17	115000			3000

Table 2. PGM1 Configurations for OUTPUT

PGM1 CODES	R_{PGM1} (Ω)	POCP	VOLTAGE LOOP GAIN MULTIPLIER	SLOPE1 (µA)
0	95.3	5.4	0.4	1.5
1	200			2.6
2	309			3.7
3	422			6.0
4	536			7.0
5	649			8.0
6	768		0.7	1.5
7	909			2.6
8	1050			3.7
9	1210			6.0
10	1400			7.0
11	1620			8.0
12	1870		1	1.5
13	2150			2.6
14	2490			3.7
15	2870			6.0
16	3740			7.0
17	8060			8.0
18	12400		1.5	1.5
19	16900			2.6
20	21500			3.7
21	26100			6.0
22	30900			7.0
23	36500	4	0.4	1.5
24	42200			2.6
25	48700			7.0
26	56200		0.7	1.5
27	64900			2.6
28	75000			7.0
29	86600		1	1.5
30	100000			2.6
31	115000			7.0

Reference Design Procedure

Output Voltage Sensing

The MAX20804 has an internal 0.5V reference voltage. When the desired output voltage is higher than 0.5V, it is required to use resistor-dividers R_{FB1} and R_{FB2} to sense the output voltage (see the *Simplified Application Circuit*). It is recommended that the R_{FB2} value does not exceed 5kΩ. The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

V_{OUT} = Output voltage

V_{REF} = 0.5V fixed reference voltage

R_{FB1} = Top resistor-divider

R_{FB2} = Bottom resistor-divider

Switching Frequency Selection

The MAX20804 offers a wide range of selectable switching frequencies from 500kHz to 3MHz. Switching frequency selection can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation due to reduced switching losses. The frequency must be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SWMAX} = MIN\left\{\frac{V_{OUT}}{t_{ONMIN} \times V_{DDHMAX}}, \frac{V_{DDHMIN} - V_{OUT}}{t_{OFFMIN} \times V_{DDHMIN}}\right\}$$

where:

f_{SWMAX} = Maximum selectable switching frequency

V_{DDHMAX} = Maximum input voltage

V_{DDHMIN} = Minimum input voltage

t_{ONMIN} = Minimum controllable on-time

t_{OFFMIN} = Minimum controllable off-time

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency (f_{SW}) should take into consideration the jittering and be lower than f_{SWMAX}. To improve the LX jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize noise sensitivity.

Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance.

To improve current loop noise immunity, typically the output inductor is selected so that the inductor current ripple is at least 1A. The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where:

V_{DDH} = Input voltage

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX20804 offers two POCP thresholds (5.4A and 4A), which can be selected by the PGM1 pin (see the *Pin-Strap Programmability* section). Due to deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage, and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where:

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the *Electrical Characteristics* table

t_{POCP} = POCP deglitch delay (36ns, typ)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$I_{OUTMAX} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

I_{OUTMAX} = Maximum load current

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold

Output Capacitor Selection

One major factor in determining the total required output capacitance is the output-voltage ripple. To meet the output-voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output-voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance can be estimated by the following equation:

$$C_{OUT} \geq MAX\left\{\frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times (V_{DDH}\text{-}V_{OUT})}, \frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times V_{OUT}}\right\}$$

where:

C_{OUT} = Output capacitance

$\triangle I$ = Loading or unloading current step

$\triangle V_{OUT}$ = Maximum allowed output voltage undershoot or overshoot

Input Capacitor Selection

The input capacitance selection is determined by the input voltage ripple requirement. The V_{DDH1} and V_{DDH2} pins of the MAX20804 should be connected on the PCB. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{f_{SW} \times V_{DDH} \times V_{INPP}}$$

where:

C_{IN} = Input capacitance

$I_{OUT(MAX)}$ = Maximum output current of OUTPUT

V_{OUT} = Output voltage of OUTPUT

f_{SW} = Switching frequency of OUTPUT

V_{INPP} = Peak-to-peak input voltage ripple

Besides the minimum required input capacitance, it is also required to place 0.1µF and 1µF high-frequency decoupling capacitors next to each $V_{DDH\_}$ pin to suppress the high-frequency switching noises.

Internal Compensation Selection

Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated using the following equation:

$$BW = \frac{\frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 20m\Omega \times C_{OUT}}$$

where:

R_{VGA} = The voltage loop gain resistance, which is set by the switching frequency, and the voltage loop gain multiplier selected by PGM_ pin resistors, as seen in *Table 3*.

Table 3. Voltage Loop Gain Resistance

SWITCHING FREQUENCY (kHz)	VOLTAGE LOOP GAIN MULTIPLIER	R_{VGA} (kΩ)
500	0.4	15.6
	0.7	27
	1	37
	1.5	52.2
750	0.4	22
	0.7	31
	1	44.5
	1.5	62.3
1000	0.4	22
	0.7	37
	1	52.2
	1.5	74.5
1500	0.4	27
	0.7	44.5
	1	62.3
	1.5	104.4
2000 or 3000	0.4	31
	0.7	52.2
	1	74.5
	1.5	104.4

Slope Compensation

Slope compensation is applied to guarantee current loop stability when the duty cycle is higher than 50%. For applications where the duty cycle is smaller than 50%, it is also recommended to apply slope compensation to improve current loop noise immunity. The minimum and maximum slope compensation values are calculated using the following equation:

$$\frac{V_{OUT}}{L} \times C_{SLOPE} \times \frac{1.6\Omega}{25} \leq SLOPE \leq \frac{V_{IN} \times f_{SW} \times C_{SLOPE}}{V_{OUT}} \left[800mV - \left(I_{OUTMAX} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{25}\right]$$

where:

C_{SLOPE} = 5pF

The slope-compensation options of the MAX20804 can be selected by resistor values on PGM1. A higher slope value is recommended to help reduce duty cycle jittering and improve stability.

Voltage Loop Zero Compensation

The value of the voltage loop zero compensation for the loop stability is dependent on the switching frequency selected by the pinstrap of PGM0 (*Table 4*). The voltage loop zero compensation value cannot be changed by the user once the switching frequency is selected.

Table 4. Voltage Loop Zero Compensation Setting

SWITCHING FREQUENCY (kHz)	ZERO COMPENSATION (kHz)
500	5
750	7.5
1000	8.75
1500	10
2000	12.5
3000	17.5

Typical Reference Designs

See the *Typical Application Circuit* for examples of reference schematics. Reference design examples for some common output voltages are shown in *Table 5*.

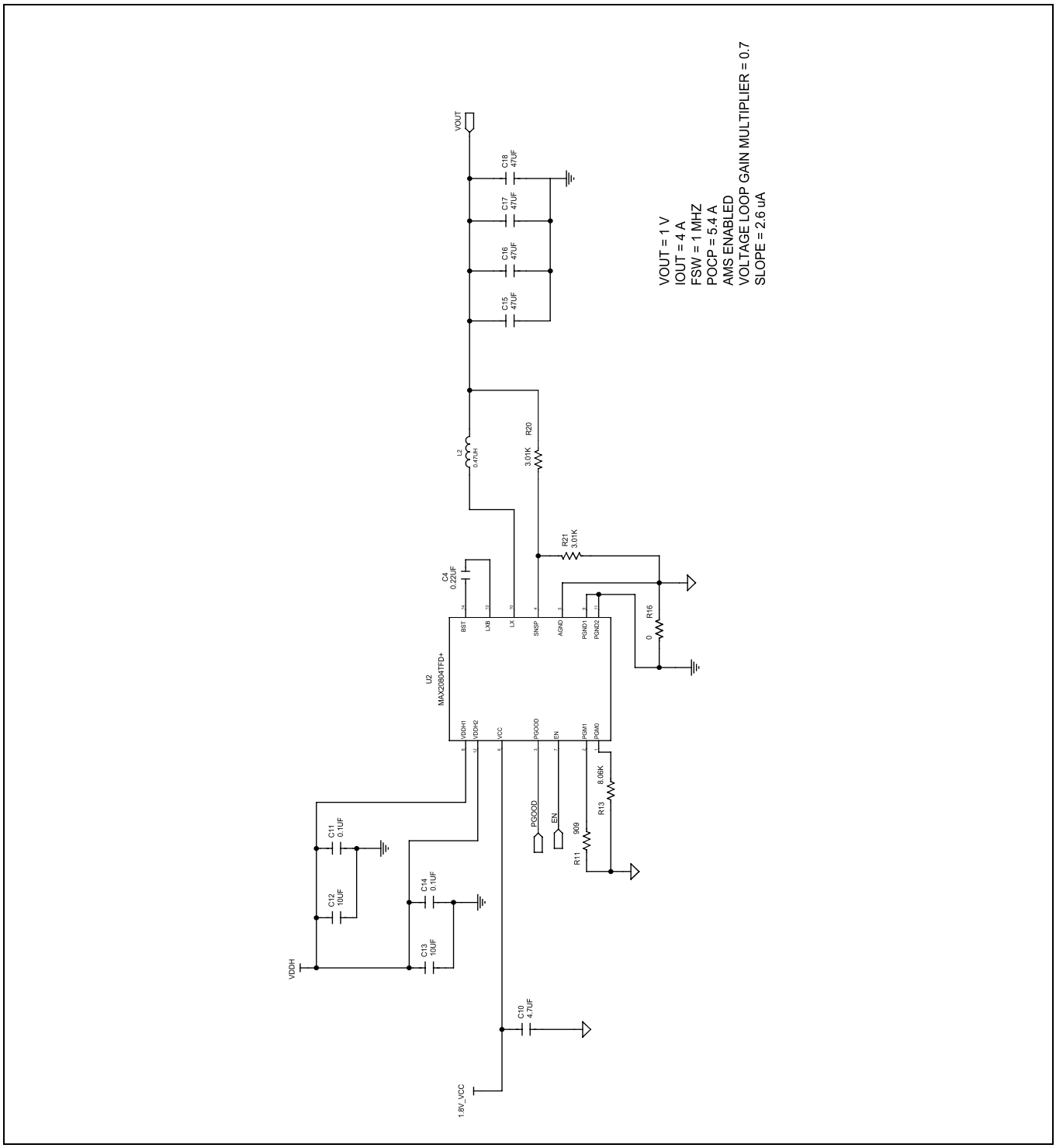
Table 5. Reference Design Examples

V_{OUT} (V)	I_{OUT} (A)	f_{SW} (kHz)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	PGM0 (kΩ)	PGM1 (kΩ)	L (µH)	C_{IN}	C_{OUT}
0.8	4	750	1.82	3.01	2.49	2.49	0.47	10µF+1µF+0.1µF	3x47µF
0.9	4	1000	2.40	3.01	8.06	2.49	0.47	10µF+1µF+0.1µF	3x47µF
1.0	4	1000	3.01	3.01	8.06	2.49	0.47	10µF+1µF+0.1µF	3x47µF
1.2	4	1000	4.22	3.01	8.06	2.49	0.56	10µF+1µF+0.1µF	3x47µF
1.8	4	1500	7.87	3.01	16.9	2.49	0.56	10µF+1µF+0.1µF	2x47µF
3.3	4	2000	16.9	3.01	26.1	2.15	1.0	10µF+1µF+0.1µF	2x47µF
5.0	3	2000	22.6	2.49	26.1	100	2.2	10µF+1µF+0.1µF	1x47µF

PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- The V_{DDH}, PGND, and LX traces must be as wide as possible to reduce trace impedance and improve heat dissipation.
- The high-frequency input decoupling capacitor should be placed on the same side of the PCB as the IC, located the closest to the IC and no more than 40 mils from the $V_{DDH\_}$ pins. The remaining ceramic input capacitors can be placed next to these high-frequency bypass capacitors. These remaining ceramic input capacitors can also be placed on the other side of the PCB, but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Use vias near both of the V_{DDH} pins, and provide a low impedance connection between them through an internal layer.
- The V_{CC} decoupling capacitors should be connected to AGND and placed as close as possible to the V_{CC} pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to the AGND pin. The analog ground can be used as a shield and ground reference for the control signals.
- Do not place vias between the V_{CC} capacitors and AGND pin. These vias conduct switching currents between the V_{CC} capacitors and PGND. Placing the vias near the AGND pin can add noise to the SNSP divider.
- The boost capacitors should be placed as close as possible to LX_ and BST_ pins on the same side of the PCB as the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- The voltage sense line should be shielded by ground plane and kept away from switching node and the inductor.
- Multiple vias are recommended for heat dissipation and for all paths that carry high currents.
- The input capacitors and output inductors should be placed near the IC, and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20804TFD+	-40°C to +150°C	14 FC2QFN
MAX20804TFD+T	-40°C to +150°C	14 FC2QFN

+ Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/25	Initial release	—