

12V Capable, Low- R_{ON} , Beyond-the-Rails™ DPDT Analog Switch

MAX20327

General Description

The MAX20327 ultra-small, low-on-resistance (R_{ON}) double-pole/double-throw (DPDT) analog switches feature Beyond-the-Rails™ capability that allows signals from -5.5V to +12V to pass without distortion, even when the power supply is below the signal range. The low on-resistance (0.2Ω) also makes the devices ideal for low-distortion switching applications, such as audio or video.

The MAX20327 is fully specified to operate from a single +1.6V to +5.5V power supply. Because of the low supply current requirement, V_{CC} can be provided by a GPIO. When power is not applied, the switches go to a high-impedance mode and all analog signal ports can withstand signals from -5.5V to +5.5V. The switches are controlled with a single control bit, CB.

The MAX20327 is available in a 1.6mm x 1.6mm, 0.4mm pitch, 9-bump wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Cell phone
- Tablet
- Portable Audio/Video Equipment
- Portable Navigation Devices

Benefits and Features

- Distortion-Free Beyond-the-Rails Signaling
 - Negative Voltage Audio and Video Signal Capable
 - -5.5V to +12V Analog Signal Range Independent of V_{CC}
 - On-Resistance 0.2Ω (Typ)
 - +1.6V to +5.5V Single-Supply Range
 - Total Harmonic Distortion Plus Noise 0.001% (Typ)
 - On-Resistance Flatness 0.001Ω (Typ)
- Low Supply Current $30\mu A$ (Typ) at 1.6V
 - Can be Powered by GPIO
 - High-Impedance Mode When V_{CC} Not Applied
- ESD Protection on COM_
 - $\pm 15kV$ Human Body Model
 - $\pm 8kV$ IEC 61000-4-2 Air Gap
 - $\pm 6kV$ IEC 61000-4-2 Contact
- Design Flexibility
 - Break-Before-Make Operation
 - 9-Bump WLP (1.6mm x 1.6mm)
 - -40°C to +85°C Operating Temperature Range

[Ordering Information](#) appears at end of data sheet.

Absolute Maximum Ratings

V_{CC} , CB to GND	-0.3V to +6V	Continuous Power Dissipation ($T_A = +70^{\circ}C$, derate 11.91mW/ $^{\circ}C$ above $+70^{\circ}C$.).....	952.8mW
NC_{-} , NO_{-} to GND.....	-6V to +12.5V	Operating Temperature Range.....	$-40^{\circ}C$ to $+85^{\circ}C$
COM_{-} to GND ($V_{CC} < 1.6V$).....	-6V to +6V	Junction Temperature.....	$+150^{\circ}C$
COM_{-} to GND ($V_{CC} \geq 1.6V$).....	-6V to $(+17.5 - V_{NC_{-}}/V_{NO_{-}})V$	Storage Temperature Range.....	$-65^{\circ}C$ to $+150^{\circ}C$
Continuous Current NC_{-} , NO_{-} , COM_{-}	-1.1A to +1.1A	Soldering Temperature (reflow).....	$+260^{\circ}C$
Peak Current NC_{-} , NO_{-} , COM_{-} (50% duty cycle, 10ms pulse)	-1.6A to +1.6A		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

PACKAGE CODE	W91P1+1
Outline Number	21-100195
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	83.98 $^{\circ}C/W$
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/thermal-tutorial.

Electrical Characteristics

($V_{CC} = +1.6V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +2.5V$, $T_A = +25^{\circ}C$, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	V_{CC}		1.6		5.5	V
Power-Supply Rejection Ratio	PSRR	$R_{COM_} = 32\Omega$, $f = 20kHz$		80		dB
Supply Current	I_{CC}	$V_{CC} = +1.6V$, $V_{CB} = 0V$ or V_{CC}		30	50	μA
		$V_{CC} = +4.2V$, $V_{CB} = 0V$ or V_{CC}		55	90	
ANALOG SWITCH (NC_ to COM_, NO_ to COM_)						
Analog Signal Range	$V_{NC_}$, $V_{NO_}$, $V_{COM_}$		-5.5		+12	V
On-Resistance	R_{ON}	$V_{CC} = 2.5V$, $V_{COM_} = 0V$, $I_{COM_} = 100mA$ (Note 2)		0.20	0.35	Ω
		$V_{CC} = 1.8V$, $V_{COM_} = 0V$, $I_{COM_} = 100mA$ (Note 2)		0.25	0.5	
On-Resistance Match Between Channels	ΔR_{ON}	$V_{CC} = 2.5V$, $V_{NC_} = 0V$, $I_{COM_} = 100mA$, between same NC_ and NO_ channel		0.002	0.03	Ω
On-Resistance Flatness	R_{FLAT}	$V_{CC} = 2.5V$, $I_{COM_} = 100mA$, $V_{COM_} = -5.5V$ to $+12V$ (Note 3, Note 4)		0.001	0.05	Ω
NC_ or NO_ Off-Leakage Current	$I_{NO_ (OFF)}$ / $I_{NC_ (OFF)}$	$V_{CC} = 2.5V$, switch open, $V_{NO_}$ or $V_{NC_}$ $= -5.5V$, $+12V$, $V_{COM_} = -5.5V$, $+12V$ unconnected	-250		+250	nA
COM Off-Leakage Current	$I_{COM_ (OFF)}$	$V_{CC} = 0V$, $T_A = 25^{\circ}C$, $V_{COM_} = -5.5V$, $+12V$, $V_{NO_}$ or $V_{NC_} = -5.5V$, $+12V$, unconnected	-1		+1	μA
COM On-Leakage Current	$I_{COM_ (ON)}$	$V_{CC} = 2.5V$, switch closed, $V_{COM_} = V_{NO_} = -5.5V$, $+12V$, unconnected	-250		+250	nA
TIMING CHARACTERISTICS						
Turn-On Time	t_{ON}	$V_{NO_}$ or $V_{NC_} = 0V$, $+R_L = 50\Omega$ (Figure 2)			300	μs
Turn-Off Time	t_{OFF}	$V_{NO_}$ or $V_{NC_} = 0V$, $+R_L = 50\Omega$ (Figure 1)		5	30	μs
Break-Before-Make Time	t_{BBM}	$R_L = 50\Omega$, time for both NC/NO switches are open during transition (Figure 2)	0		300	μs
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	$f = 20Hz$ to $20kHz$, $V_{COM_} = 0.5V_{P-P}$, $R_S = R_L = 600\Omega$, DC bias = 0		0.001		%
Off-Isolation	V_{ISO}	$R_S = R_L = 50\Omega$; $V_{COM_} = 0.5V_{P-P}$, $f = 100kHz$, $V_{CC} = 0V$, DC bias = 0.25V, Figure 3		-60		dB
Crosstalk	V_{CT}	$R_S = R_L = 50\Omega$, $V_{COM_} = 0.5V_{P-P}$, $f = 100kHz$ (Figure 3)		-100		dB
-3dB Bandwidth	BW	$R_S = R_L = 50\Omega$		100		MHz

Electrical Characteristics (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NC_ Off-Capacitance	C_{NC_OFF}	$V_{NC_}/V_{NO_} = 0.5V_{P-P}$, $f = 1MHz$		4		pF
NO_ Off-Capacitance	C_{NO_OFF}	$V_{NC_}/V_{NO_} = 0.5V_{P-P}$, $f = 1MHz$		4		pF
COM_ On-Capacitance	C_{COM_ON}	$V_{NC_}/V_{NO_} = 0.5V_{P-P}$, $f = 1MHz$		6		pF
DIGITAL I/O (CB)						
Input Logic High Voltage	V_{IH}		1.4			V
Input Logic Low Voltage	V_{IL}				0.4	V
Input Leakage Current	I_{IN}	$V_{CB} = 0$ or V_{CC}	-100		+100	nA
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			150		°C
Thermal Hysteresis	T_{HYST}			20		°C
ESD PROTECTION						
COM_		HBM		±15		kV
		IEC61000-4-2 Air-Gap Discharge		±8		
		IEC61000-4-2 Contact Discharge		±6		
All other pins		HBM		±2		kV

Note 1: All specifications are 100% production tested at $T_A = +25°C$, unless otherwise noted. Specifications are over $T_A = -40°C$ to +85°C and are guaranteed by design.

Note 2: The same limits apply for $V_{COM_} = -5.5V$ to +5.5V with NC_ channels and 0V to 12V with NO_ channels. These are guaranteed by design.

Note 3: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.

Note 4: Guaranteed by design; not production tested.

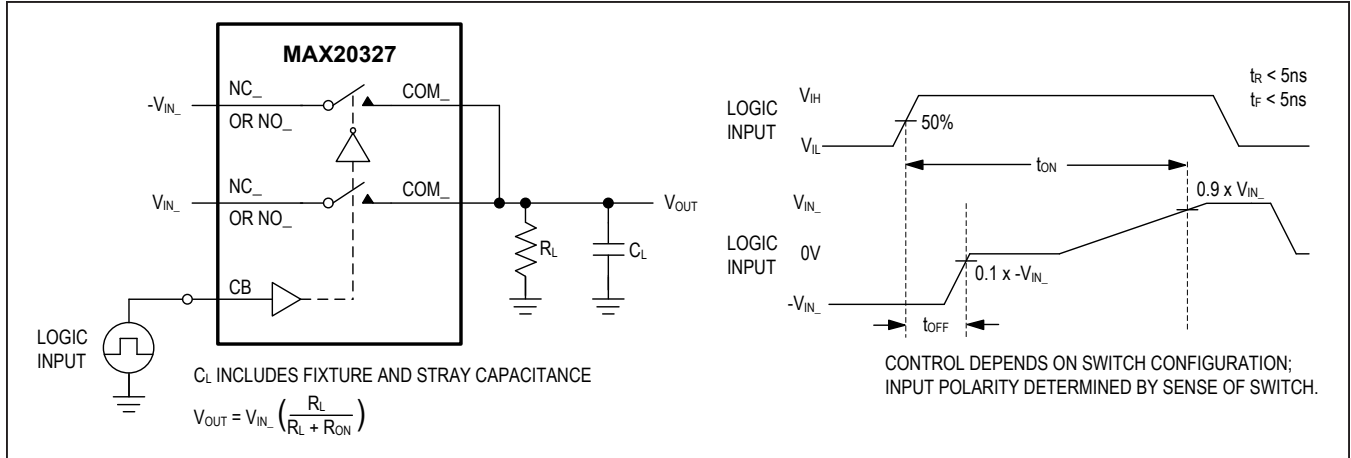


Figure 1. Switching Time

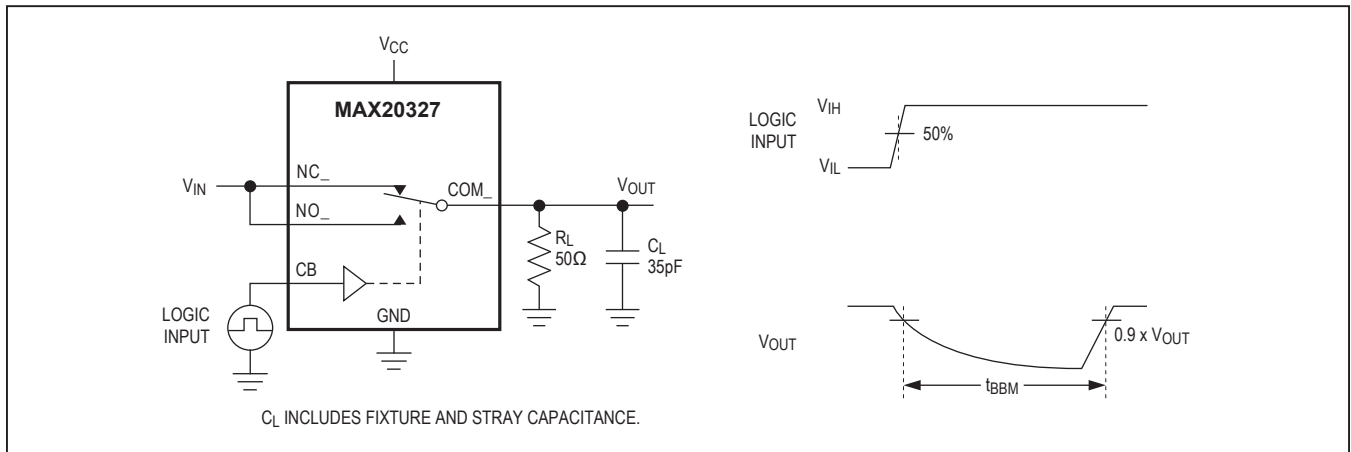


Figure 2. Break-Before-Make Interval

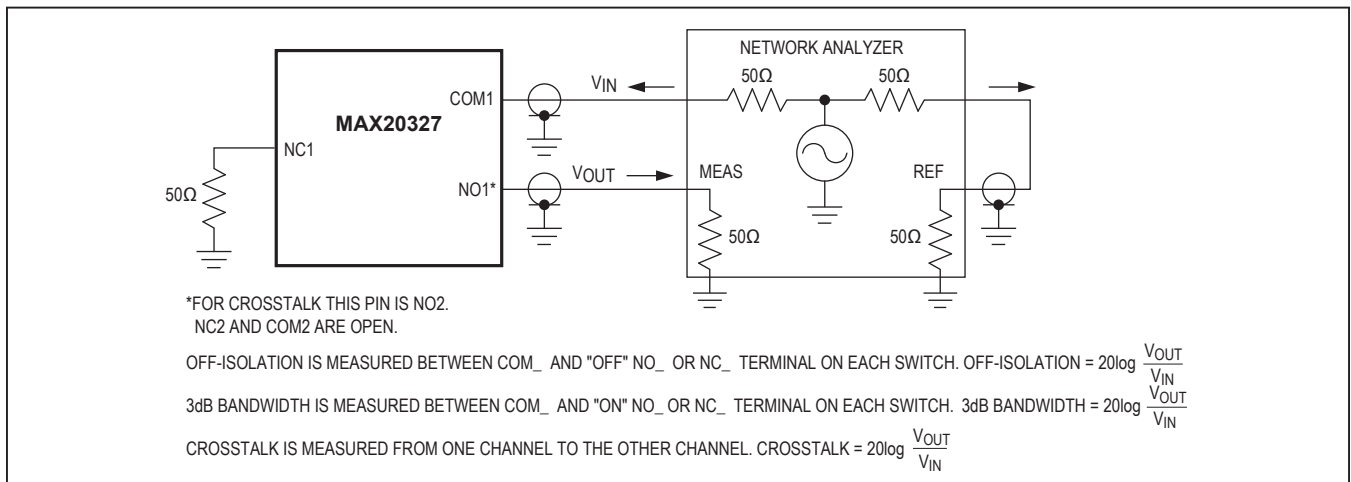
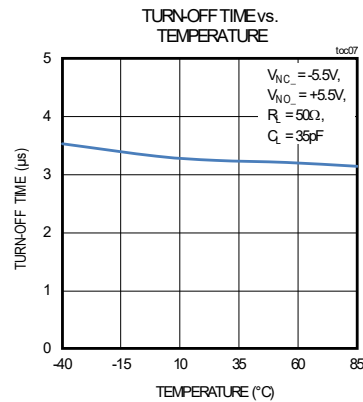
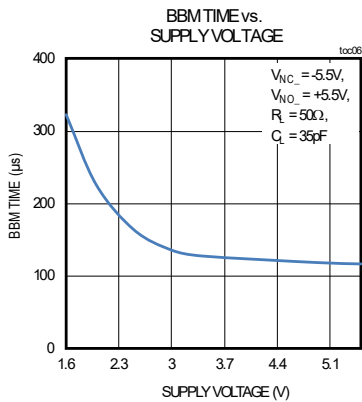
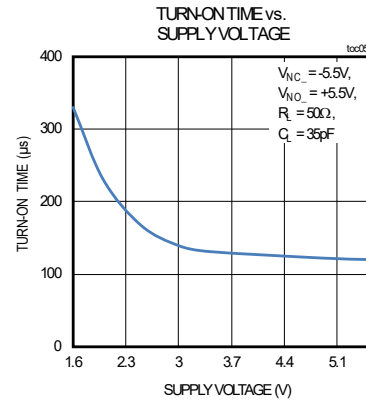
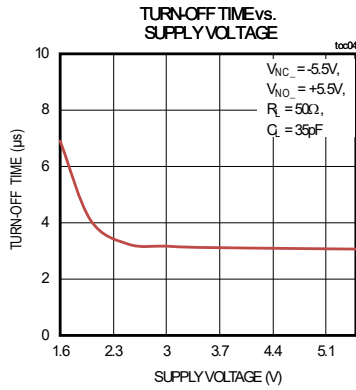
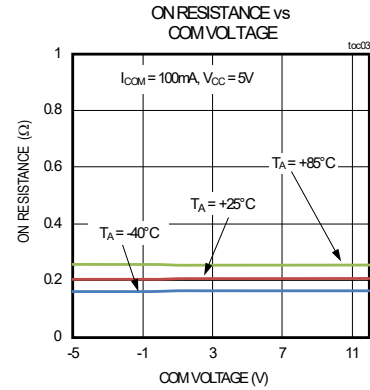
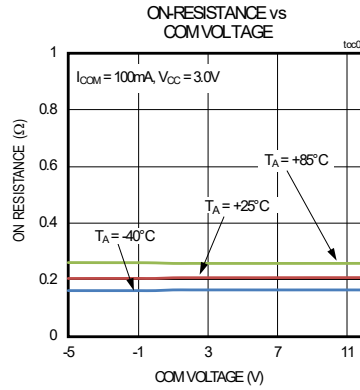
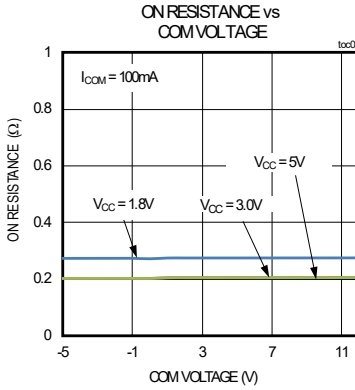


Figure 3. 3dB Bandwidth, Off-Isolation, and Crosstalk

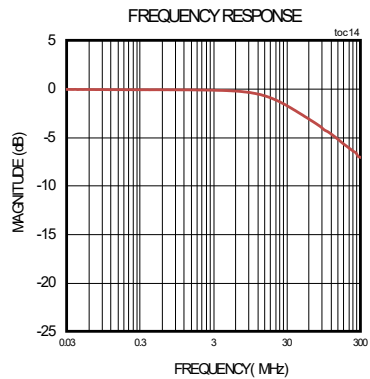
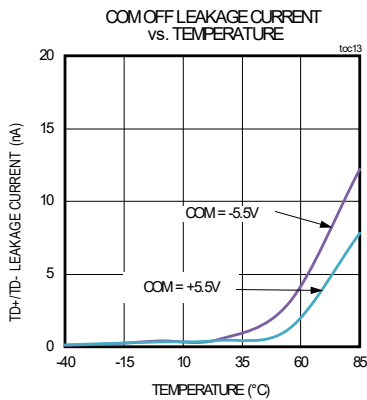
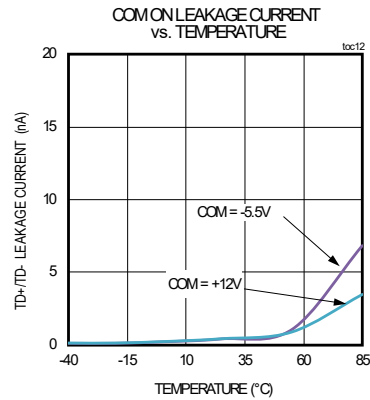
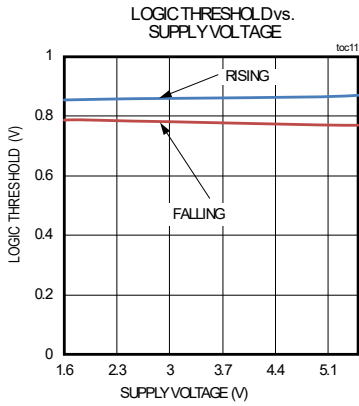
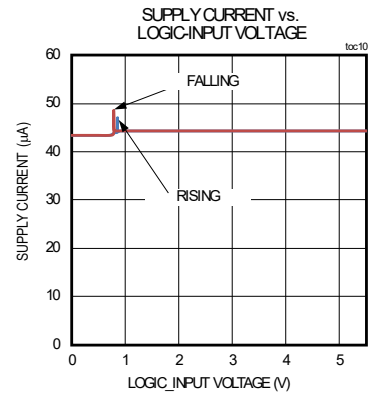
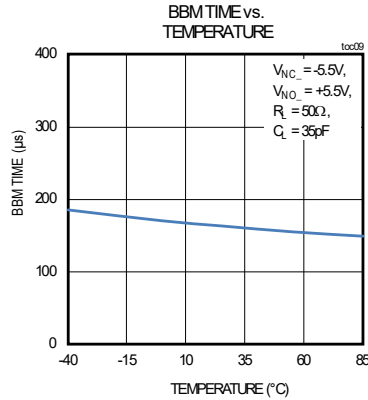
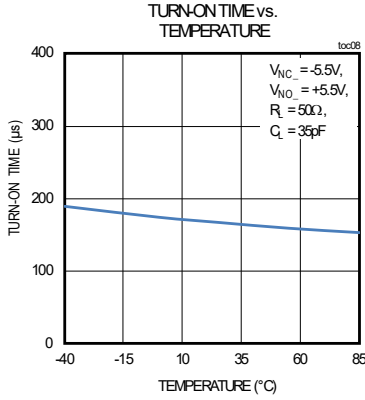
Typical Operating Characteristics

$V_{CC} = +2.5V$, $T_A = +25^\circ C$, unless otherwise noted.



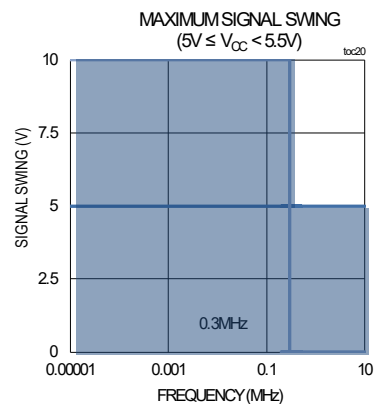
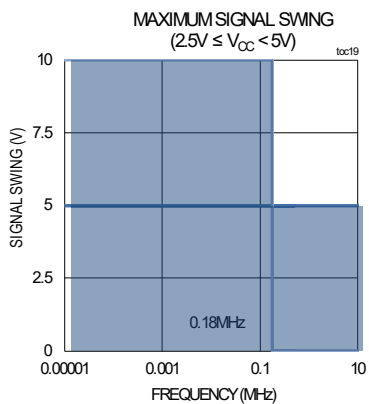
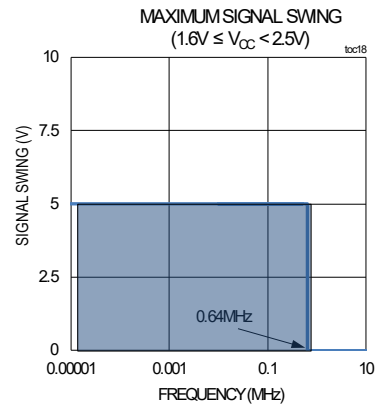
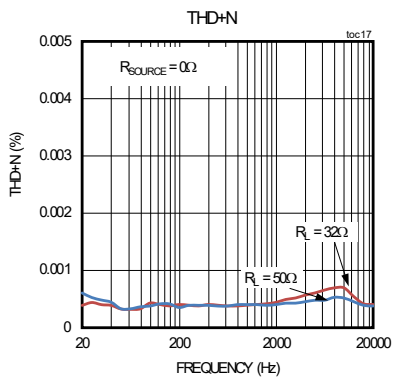
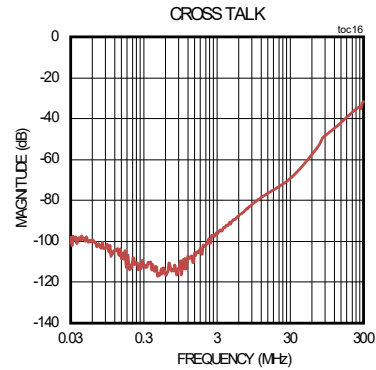
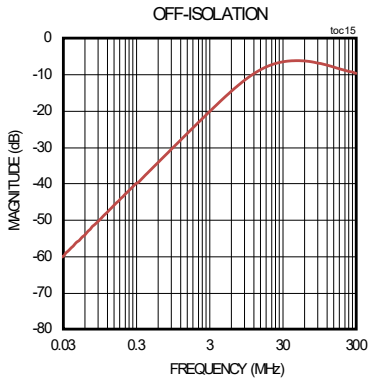
Typical Operating Characteristics (continued)

$V_{CC} = +2.5V$, $T_A = +25^\circ C$, unless otherwise noted.

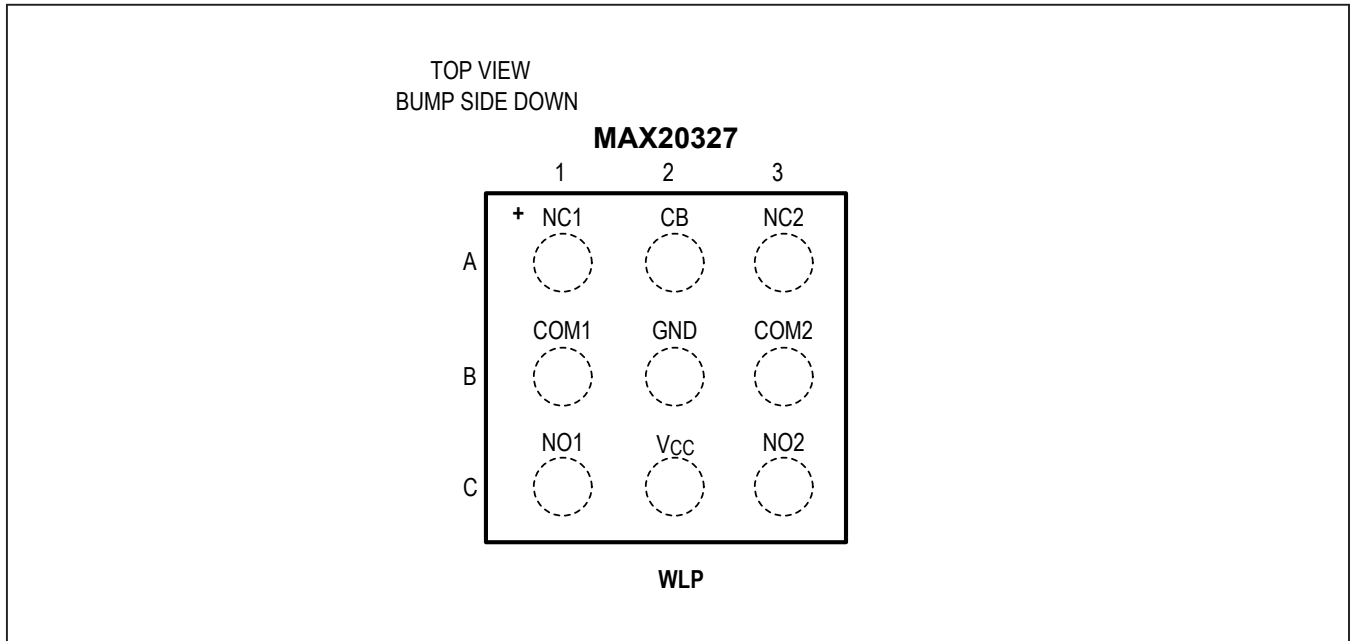


Typical Operating Characteristics (continued)

$V_{CC} = +2.5V$, $T_A = +25^\circ C$, unless otherwise noted.



Bump Configuration



Bump Descriptions

PIN	NAME	FUNCTION
A1	NC1	Normally Closed Terminal for Switch 1
A2	CB	Digital Control Input. Drive CB low to connect COM_ to NC_. Drive CB high to connect COM_ to NO_.
A3	NC2	Normally Closed Terminal for Switch 2
B1	COM1	Common Terminal for Switch 1
B2	GND	Ground
B3	COM2	Common Terminal for Switch 2
C1	NO1	Normally Open Terminal for Switch 1
C2	V _{CC}	Positive Supply Voltage Input. Bypass V _{CC} to GND with a 0.1μF capacitor as close to the device as possible.
C3	NO2	Normally Open Terminal for Switch 2

Detailed Description

The MAX20327 is an ultra-small, low on-resistance, high ESD-protected DPDT switch that operates from a +1.6V to +5.5V supply, and is designed to pass analog signals, such as AC-biased or DC-biased audio and video signals. These switches feature the low on-resistance (R_{ON}) necessary for high-performance switching applications. The Beyond-the-Rails signal capability of the MAX20327 allows signals below ground and above V_{CC} to pass without distortion.

Analog Signal Levels

The MAX20327 is bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs. The topology of the switches allows the signal to drop below ground without the need of an external negative voltage supply.

Digital Control Input

The MAX20327 provides a single-bit control logic input, CB. CB controls the switch position, as shown in the [Typical Application Circuits](#).

Power-Up Sequence

During power-up, it is recommended to apply the CB signal 800µs after V_{CC} rail goes high, as shown in [Figure 4](#).

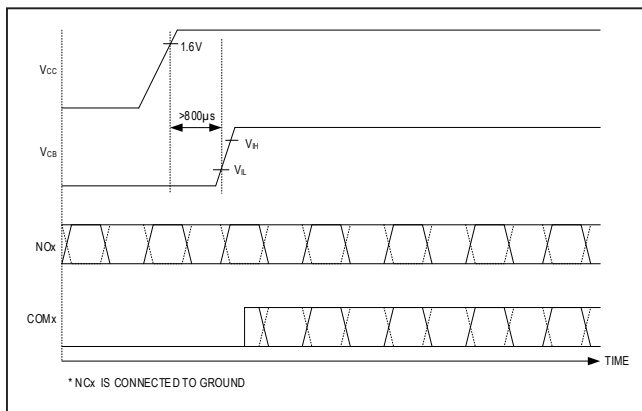


Figure 4. Power-Up Sequence

Applications Information

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. COM1 and COM2 are further protected against ESD up to ±15kV (HBM), ±8kV (Air-Gap Discharge), and ±6kV (Contact Discharge) without damage. NO_ and NC_ are protected against ESD up to ±2kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the devices continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test methodology and test results.

Human Body Model

[Figure 5](#) shows the Human Body Model. [Figure 6](#) shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

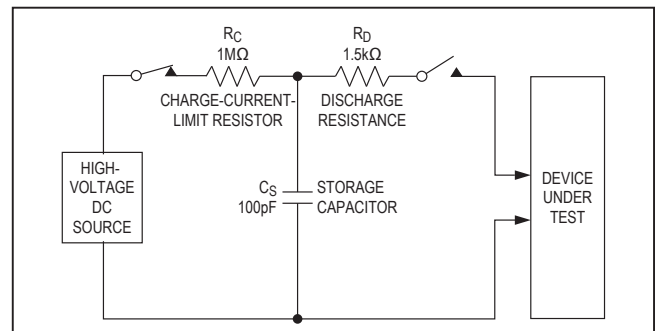


Figure 5. Human Body ESD Test Model

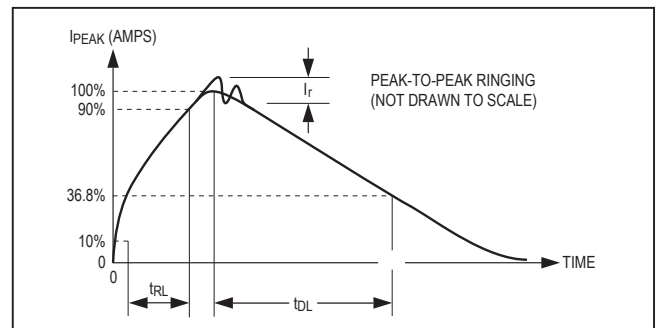


Figure 6. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2,

because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. [Figure 7](#) shows the IEC 61000-4-2 model and [Figure 8](#) shows the current waveform for the $\pm 8kV$, IEC 61000-4-2, Level 4, ESD Contact-Discharge Method.

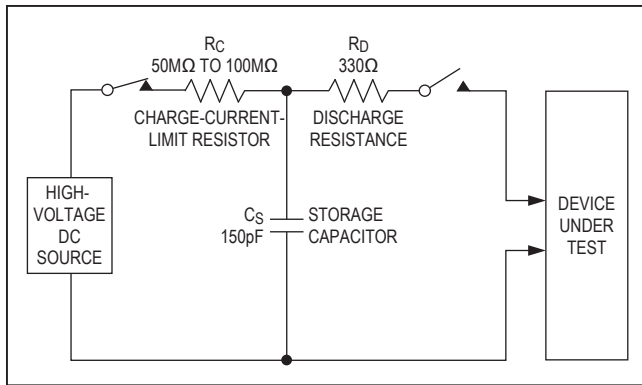


Figure 7. IEC 61000-4-2 ESD Test Model

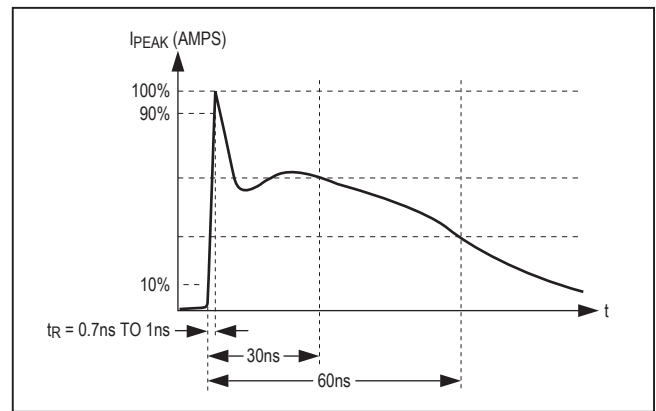
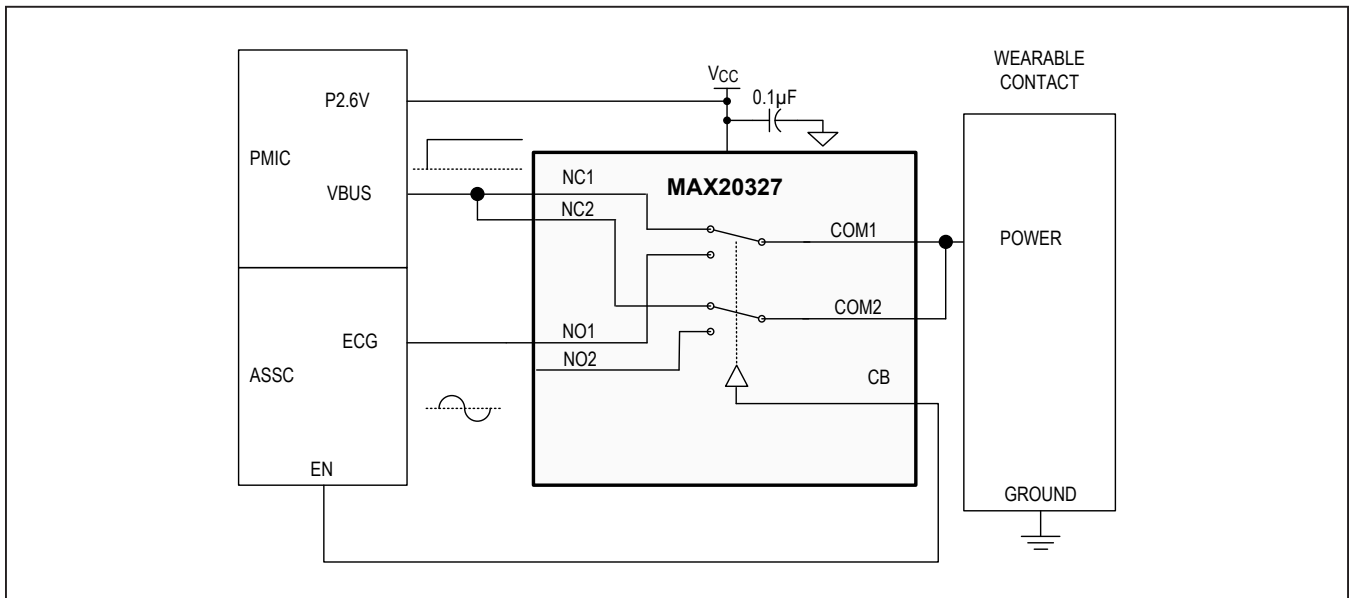
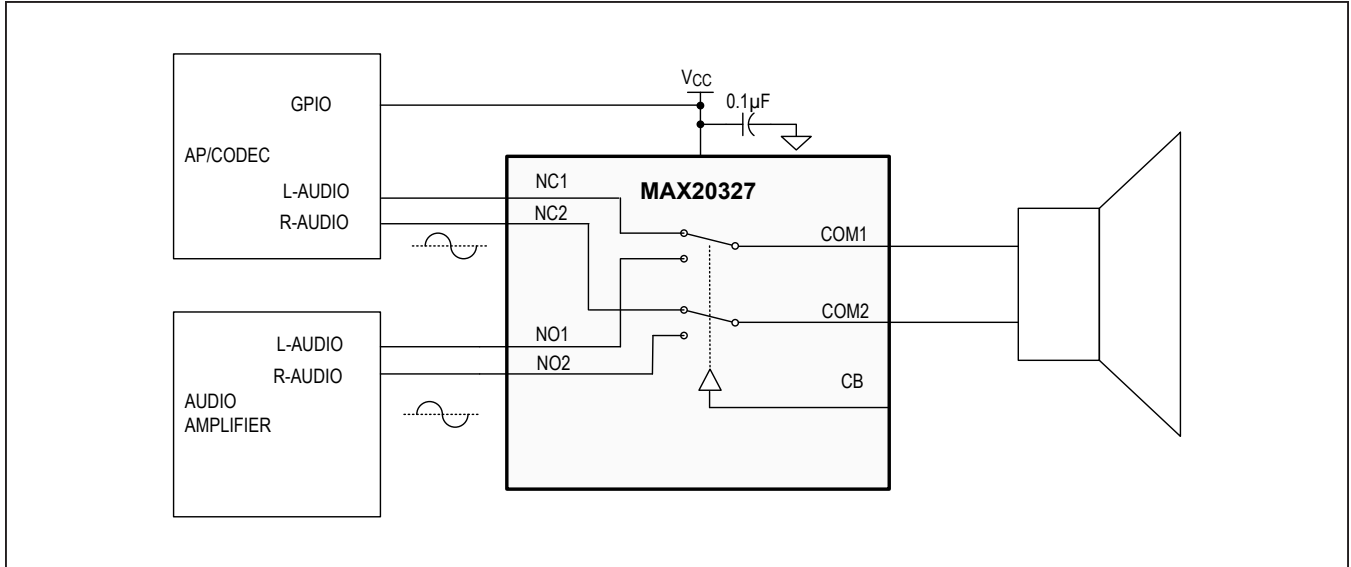


Figure 8. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING	PACKAGE OUTLINE DRAWING
MAX20327EWL+T	-40°C to +85°C	9 WLP	ALA	21-100195

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	2/24	Added <i>Power-Up Sequence</i> section	10



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