# 3V to 80V, 7A, Power-Limiter with OV/Surge, UV, Reverse Polarity and Loss of Ground Protection

**MAX17617/MAX17617A**

## Product Highlights

- Robust Protection Reduces System Downtime
  - Wide Input Supply Range: +3V to +80V (without Reverse Current Protection)
  - Wide Input Supply Range: +3V to +75V (with Reverse Current Protection)
  - ±3% Accurate Programmable Current Limit between 3A to 7A across Full Temperature Range
  - ±4% Accurate Programmable Current Limit between 2A to 3A across Full Temperature Range
  - ±7% Accurate Programmable Current Limit between 0.7A to 2A across Full Temperature Range
  - ±6% Accurate Power Limit at 100W, 24V for Class 2 Applications
  - Input-Voltage Reverse-Polarity Protection (with External nFET)
  - Dual Stage Reverse Current Protection (with External nFET) with Fast 100ns Response Time
  - Low $R_{ON}$ Internal nFET (20mΩ typ)
  - Output-Voltage Reverse-Polarity Tolerant
  - Loss of Ground Protection
  - 200% Short Term Overload capability
  - Programmable Overvoltage Surge Protection (MAX17617A)
- Flexible Design to Maximize Reuse and Minimize Requalification
  - Adjustable UVLO and OVLO/OVFB Thresholds
  - ±2% Accurate Bandwidth Current Monitoring Read-Out, IMON (3A to 7A, up to +85ºC)
  - Programmable Startup Inrush Current Limit
  - Programmable Current Limit Fault Response: Continuous, Autoretry, and Latch-off Modes
  - Logic Level Enable Input (EN)
  - Protected External N-type Field Effect Transistor (nFET) Gate Drive
  - Open Drain Fault Indicator (FLAG)
  - Power Good Output (PGOOD)
  - Programmable Output Under Voltage Sense (OUTUV)
  - Junction Temperature Monitoring ($T_J$)
  - Thermal Foldback Current Limit
- Reduced Solution Footprint
  - 4.5mm x 5.75mm, 23-Pin FCQFN package
  - Integrated nFET for Common-Use Protection Requirements

## Key Applications

- Input Voltage and Output Overcurrent Protections:

The MAX17617/MAX17617A interrupts load current and disconnects the output from the input in input voltage faults and output overcurrent faults.

- Loss of Ground Protection:

The MAX17617/MAX17617A interrupts load current and disconnects the output from the input in a Loss of Ground event, such as when the single-fault safety fuse on its ground path opens up.

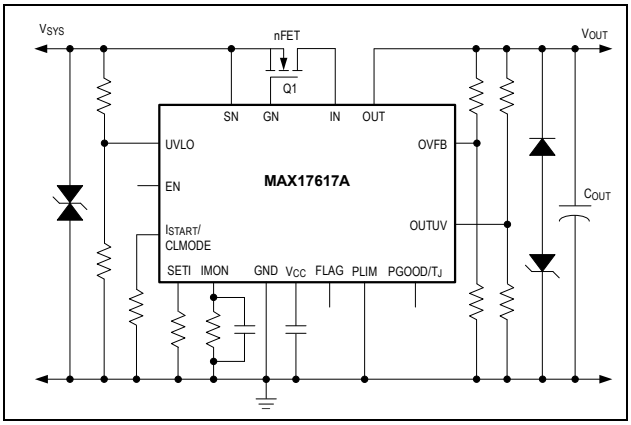
- Surge Protection:

The MAX17617A features an output voltage limiting regulation during transient surges in input voltage to protect connected loads from short-duration input voltage surge events.

- UL1310 Class 2 Power Limiter:

The ±3% accurate current limit between 3A and 7A and ±6% accurate power limit of MAX17617/MAX17617A offer tight protection boundaries in UL1310 Class 2 power supply applications and maximize power delivery to the load.

## Simplified Application Diagram




*Ordering Information* **appears at end of data sheet**

19-101965; Rev 0; 1/25

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## Absolute Maximum Ratings

IN to GND ..... -0.3V to +85V

SN to GND (Reverse Current Protection is used) ..... -85V to +78V

SN to GND (Reverse Current Protection is not used) ..... -85V to +85V

OUT to GND ..... -85V to +85V

IN to OUT (DC) ..... -0.3V to +85V

UVLO, OVLO, OVFB, OUTUV to GND ..... -0.3V to +33V

EN, PGOOD/$T_J$, $I_{START}$/CLMODE, PLIM, FLAG to GND ..... -0.3V to +6V

$V_{CC}$ to GND ..... -0.3V to +2V

SETI, IMON to GND ..... -0.3V to ($V_{CC}$ + 0.3)V

GN to SN ..... -0.3V to +10V

GN to GND ..... -85V to +85V

IN to SN ..... -1V to +85V

IN Current (DC) ..... 8A

Continuous Power Dissipation ($T_A$ = +70°C, derate at 36.5mW/°C above +70°C) ..... 3469.7mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature (Note 1) ..... -40°C to +150°C

Storage Temperature ..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... +300°C

Soldering Temperature (Reflow) ..... +260°C

**Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| | |
|---|---|
| Package Code | F234A5F+1F |
| Outline Number | *21-100606* |
| Land Pattern Number | *90-100213* |
| **THERMAL RESISTANCE, FOUR-LAYER BOARD** | |
| Junction-to-Ambient ($\theta_{JA}$) | 27.38°C/W |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 1.81°C/W |

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

## Electrical Characteristics

($V_{IN}$ = $V_{SN}$ = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON, PGOOD/$T_J$, OUTUV, $I_{START}$/CLMODE, FLAG, PLIM = OPEN, $R_{SETI}$ = 2.13kΩ, $V_{CC}$ = 2.2µF to GND, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical Values are $V_{IN}$ = 48V, $T_A$ = +25°C (See *Note 2*)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Input Section** | | | | | | |
| IN Voltage Range | $V_{IN}$ | Without Reverse Current Protection | 3 | | 80 | V |
| | | With Reverse Current Protection | 3 | | 75 | |
| Shutdown IN Current | $I_{INSHDN}$ | $V_{EN}$ = 0V, $V_{OUT}$ = GND, $T_A$ = +125°C | | 20 | 80 | µA |
| | | $V_{EN}$ = 0V, $V_{OUT}$ = GND, $T_A$ = +85°C | | 20 | 50 | |
| Shutdown SN Current | | $V_{EN}$ = 0V, $V_{SN}$ = -80V | | -53 | -105 | µA |
| Shutdown IN to OUT Current | | $V_{EN}$ = 0V, $V_{IN}$ – $V_{OUT}$ = 80V | | 30 | 110 | µA |
| Shutdown IN, GN, SN shorted | | $V_{EN}$ = 0V, $V_{OUT}$ = GND, $T_A$ = +125°C | | 30 | 90 | µA |
| | | $V_{EN}$ = 0V, $V_{OUT}$ = GND, $T_A$ = +85°C | | 30 | 60 | |
| Supply Current | $I_{IN}$ | | | 2 | 3 | mA |
| Internal IN Undervoltage Trip level | $V_{INUVLOR}$ | $V_{IN}$ Rising | 2.74 | 2.80 | 2.86 | V |
| | $V_{INUVLOF}$ | $V_{IN}$ Falling | 2.64 | 2.70 | 2.76 | |
| **Enable (EN)** | | | | | | |
| EN Input-Logic High | $V_{ENH}$ | | 1.4 | | | V |
| EN Input-Logic Low | $V_{ENL}$ | | | | 0.4 | V |
| EN Internal Pullup Voltage | | 3V < $V_{IN}$ < 80V | 1.3 | | 2.05 | V |
| EN Input Current | | $V_{EN}$ = 5V | | | 20 | µA |
| EN Pullup Current | | $V_{EN}$ = 0V | 2.74 | 5 | 9.56 | µA |
| **$V_{CC}$ (LDO)** | | | | | | |
| $V_{CC}$ Output Voltage Range | $V_{CC}$ | 1mA < $I_{VCC}$ < 10mA | 1.7 | 1.8 | 1.86 | V |
| $V_{CC}$ UVLO | $V_{CC\_UVR}$ | $V_{CC}$ rising | 1.62 | 1.66 | 1.7 | V |
| | $V_{CC\_UVF}$ | $V_{CC}$ falling | 1.54 | 1.58 | 1.62 | |
| $V_{CC}$ current limit | $I_{VCC}$ | | 15 | 29 | 48 | mA |
| **Undervoltage Lockout (UVLO)** | | | | | | |
| UVLO Threshold | | UVLO Rising | 0.911 | 0.93 | 0.948 | V |
| | | UVLO Falling | 0.882 | 0.90 | 0.918 | |
| UVLO Leakage Current | $I_{UVLO\_LEAK}$ | $V_{UVLO}$ = 1V, $T_A$ = +25°C | -100 | | +100 | nA |
| **Overvoltage Lockout (OVLO) (MAX17617 only)** | | | | | | |
| OVLO Threshold | | OVLO Rising | 0.911 | 0.93 | 0.948 | V |
| | | OVLO Falling | 0.882 | 0.90 | 0.918 | |
| OVLO Leakage Current | $I_{OVLO\_LEAK}$ | $V_{OVLO}$ = 1V, $T_A$ = +25°C | -100 | | +100 | nA |

($V_{IN}$ = $V_{SN}$ = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON, PGOOD/$T_J$, OUTUV, $I_{START}$/CLMODE, FLAG, PLIM = OPEN, $R_{SETI}$ = 2.13kΩ, $V_{CC}$ = 2.2µF to GND, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical Values are $V_{IN}$ = 48V, $T_A$ = +25°C (See *Note 2*)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Output Overvoltage Clamp (OVFB) (MAX17617A only)** | | | | | | | |
| Overvoltage Clamp Reference | $OVFB_{REF}$ | | | 0.784 | 0.800 | 0.816 | V |
| Overshoot on OVFB | | IN Slew Rate < 0.1V/µs | $C_{LOAD}$ = 4.7µF, $I_{LIM}$ = 7A, $I_{LOAD}$ = 1A | | 0 | | mV |
| | | IN Slew Rate < 1V/µs | $C_{LOAD}$ = 4.7µF, $I_{LIM}$ = 7A, $I_{LOAD}$ = 1A | | 0 | | |
| **Current Limit and Monitoring (SETI and IMON)** | | | | | | | |
| Current Limit Adjustment Range | $I_{LIM}$ | | | 0.7 | | 7.0 | A |
| Current Limit Threshold Accuracy | $I_{LIM\_ACC}$ | 0.7A < $I_{LIM}$ < 2A | | -7 | | +7 | % |
| | | 2A ≤ $I_{LIM}$ < 3A | | -4 | | +4 | |
| | | 3A ≤ $I_{LIM}$ ≤ 7A | | -3 | | +3 | |
| Overcurrent Response Time | $t_{SOC}$ | $I_{LIM}$ = 1A, $I_{OUT}$ step from 0.5A to 3A, Time to regulate $I_{OUT}$ to Current Limit | | | 20 | | µs |
| Short-Term Over Current Limit | $I_{STLIM}$ | | | | 2 x $I_{LIM}$ | | A |
| Short-Term Over Current Limit Blanking Time | $t_{STOC}$ | | | | 400 | | µs |
| Overcurrent Protection Threshold | $I_{OCP}$ | (See *Figure 16* in the *Short Circuit Protection* Section) | (See *Note 3*) | 22 | 30 | 36 | A |
| Overcurrent Protection Response Time | $t_{OCP}$ | $I_{LIM}$ = 7A, $I_{OUT}$ step from 3.5A to 40A, Time to turn off the switch once $I_{OUT}$ > $I_{OCP}$ | (See *Note 3*) | | 1 | | µs |
| IMON Accuracy | $I_{MON\_ACC}$ | 0.7A < $I_{LIM}$ < 2A | $I_{OUT}$ < $I_{LIM}$ | -6 | | +6 | % |
| | | 2A ≤ $I_{LIM}$ < 3A | $I_{OUT}$ < $I_{LIM}$ | -3 | | +3 | |
| | | 3A ≤ $I_{LIM}$ ≤ 7A | $I_{OUT}$ < $I_{LIM}$, $T_A$ = +125°C | -2.5 | | +2.5 | |
| | | | $I_{OUT}$ < $I_{LIM}$, $T_A$ = +85°C | -2 | | +2 | |
| IMON Range | | | | 0 | | 1.25 | V |
| SETI/IMON Current Ratio | | | | | 21300 | | A/A |
| SETI Clamp | | | | 1.59 | | 1.81 | V |
| IMON Clamp | | | | 1.49 | | 1.69 | V |
| SETI Fault | | | | | 400 | | mV |
| SETI Resistance | | $I_{LIM}$ = 7A | | 2.13 | | | kΩ |
| SETI Regulation Voltage | | | | | 0.7 | | V |
| SETI Range | | | | 0 | | 1.4 | V |

($V_{IN}$ = $V_{SN}$ = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON, PGOOD/$T_J$, OUTUV, $I_{START}$/CLMODE, FLAG, PLIM = OPEN, $R_{SETI}$ = 2.13kΩ, $V_{CC}$ = 2.2µF to GND, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical Values are $V_{IN}$ = 48V, $T_A$ = +25°C (See *Note 2*)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Reverse Current Protection** | | | | | | |
| Slow Reverse Current Blocking Threshold | $V_{RIB\_SLOW}$ | ($V_{IN}$ – $V_{OUT}$) falling | -1 | -5 | -10 | mV |
| Slow Reverse Current Blocking Response Time | $t_{RIB\_SLOW}$ | (See *Figure 1*), CGN-SN = 20nF | | 20 | 30 | µs |
| Fast Reverse Current Blocking Threshold | $V_{RIB\_FAST}$ | ($V_{IN}$ – $V_{OUT}$) falling | -70 | -100 | -130 | mV |
| Fast Reverse Current Blocking Response Time | $t_{RIB\_FAST}$ | (See *Figure 2*), CGN-SN = 20nF | | 100 | 160 | ns |
| Reverse Current Blocking Rising Threshold Voltage | $V_{RIB\_RISING}$ | ($V_{SN}$ – $V_{OUT}$) Rising | 70 | 100 | 130 | mV |
| Reverse Output Current drawn from OUT | $I_{OUT\_REV}$ | $V_{SN}$ = 0V, $V_{OUT}$ = 48V, IN = OPEN | | | 9 | mA |
| **Power Limit** | | | | | | |
| PLIM Threshold | $V_{PLIM\_TH}$ | | | 0.3 | | V |
| PLIM Operating Range | | | $V_{PLIM\_TH}$ | | 3 x $V_{PLIM\_TH}$ | V |
| **Gate Drive (GN, SN)** | | | | | | |
| External Reverse Protection nFET Gate Drive Voltage | $V_{GN\_SN}$ | EN = High, No-Fault Condition, $V_{IN}$ ≥ 10V | 6 | 6.5 | 7 | V |
| Gate Active Pullup Current | | EN = High, $V_{GN}$ = $V_{SN}$, No Reverse Fault Condition | 80 | 100 | 120 | µA |
| Gate Pulldown Resistance | | EN = High, External nFET OFF | | 60 | 120 | Ω |
| | | Always present | | 3 | | MΩ |
| **Internal FET** | | | | | | |
| Internal nFET ON Resistance | $R_{ON}$ | $I_{LOAD}$ = 100mA | | 20 | 40 | mΩ |
| **FLAG Output** | | | | | | |
| Logic-Low Voltage | | $I_{SINK}$ = 1mA | | | 0.4 | V |
| Leakage Current | | $V_{PULLUP}$ = 5V, PGOOD/$T_J$ Open-Drain OFF | | | 1 | µA |
| **Power Good Output (PGOOD/$T_J$)** | | | | | | |
| Logic-Low Voltage | | $I_{SINK}$ = 1mA | | | 0.4 | V |
| Leakage Current | | $V_{PULLUP}$ = 5V, PGOOD/$T_J$ Open-Drain OFF | | | 1 | µA |
| **Output Under Voltage Sensing (OUTUV)** | | | | | | |
| OUTUV Threshold | | OUTUV Rising | 0.911 | 0.93 | 0.948 | V |
| | | OUTUV Falling | 0.882 | 0.90 | 0.918 | |
| **Junction Temperature Monitoring (PGOOD/$T_J$)** | | | | | | |
| Accuracy | | $T_A$ = +25°C | -9 | | 9 | °C |

($V_{IN}$ = $V_{SN}$ = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON, PGOOD/$T_J$, OUTUV, $I_{START}$/CLMODE, FLAG, PLIM = OPEN, $R_{SETI}$ = 2.13kΩ, $V_{CC}$ = 2.2µF to GND, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical Values are $V_{IN}$ = 48V, $T_A$ = +25°C (See *Note 2*)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $T_J$ voltage | | $T_A$ = +25°C, $R_{TJ}$ = 10kΩ to GND | | 652 | | mV |
| | | $T_A$ = +125°C, $R_{TJ}$ = 10kΩ to GND | | 854 | | |
| dV/dTemp | | $T_A$ = +25°C to +125°C | | 2 | | mV/°C |
| $T_J$ Current Limit | | | 100 | | 600 | µA |
| **Timing characteristics** | | | | | | |
| IN Debounce Time | $t_{DEB}$ | Time from $V_{IN}$ > $V_{UVLO\_R}$ and Internal FET turn-on starts | 0.9 | 1 | 1.1 | ms |
| INUVLO Blanking Time | $t_{INUVLOBLANK}$ | Power-up FLAG assertion blanking time | | 0.5 | | ms |
| EN Turn-On Time | | Delay from EN = 1 for the part to turn on Internal FET (provided $V_{IN}$ > $V_{UVLO\_R}$) | | 2.5 | | ms |
| Internal nFET Turn-On Time | $t_{ON\_SWITCH}$ | From No Fault to $I_{OUT}$ = 1A | | 150 | | µs |
| Delay between Internal nFET Turn-On and External nFET Turn-On | $t_{DR}$ | | 90 | 100 | 110 | µs |
| The delay between Internal nFET Turn-OFF and External nFET Turn-OFF | $t_{DF}$ | | 90 | 100 | 110 | µs |
| Undervoltage Lock Out Turn OFF Time | $t_{OFF\_UVLO}$ | $V_{UVLO}$ falling from 1V to 0.8V | | 1 | | µs |
| Overvoltage Lock Out Turn OFF Time | $t_{OFF\_OVLO}$ | $V_{OVLO}$ rising from 0.8V to 1V | | 1 | | µs |
| Undervoltage Lock Out Rising Edge Debounce Time | $t_{DEB\_UVLO}$ | $V_{IN}$ rising | | 10 | | µs |
| Overvoltage Lock Out Falling Edge Debounce Time | $t_{DEB\_OVLO}$ | $V_{IN}$ falling | | 10 | | µs |
| Auto Retry Tme | $t_{RETRY}$ | | | 800 | | ms |
| Blanking Time | $t_{BLANK}$ | | 21.8 | 24.0 | 26.4 | ms |
| Startup Timeout | $t_{STO}$ | | 1080 | 1200 | 1320 | ms |
| Loss of Ground Switch Turn OFF Time | | $C_{VCC}$ = 2.2µF | | 100 | | ms |
| **Thermal Protection** | | | | | | |
| Thermal Foldback | $T_{J(FB)}$ | | | 150 | | °C |
| Thermal Shutdown | $T_J$ | | | 165 | | °C |
| Thermal Shutdown Hysteresis | $T_{J(HYS)}$ | | | 20 | | °C |

**Note 2:** All devices are 100% production-tested at $T_A$ = +25°C. Limits over the operating-temperature range are guaranteed by design, not production tested.

**Note 3:** Guaranteed by design, not production tested.

## Timing Diagrams

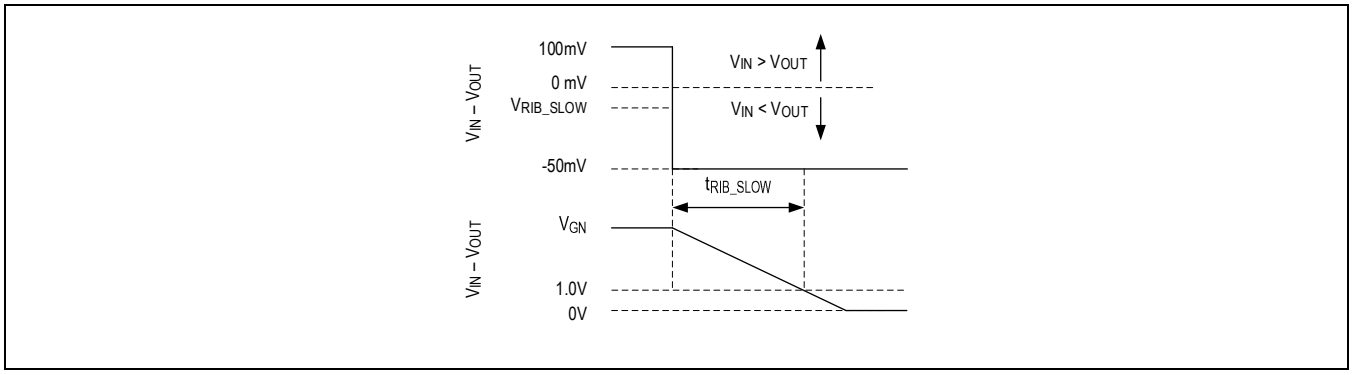



*Figure 1. Slow Reverse Current Blocking Response Time*

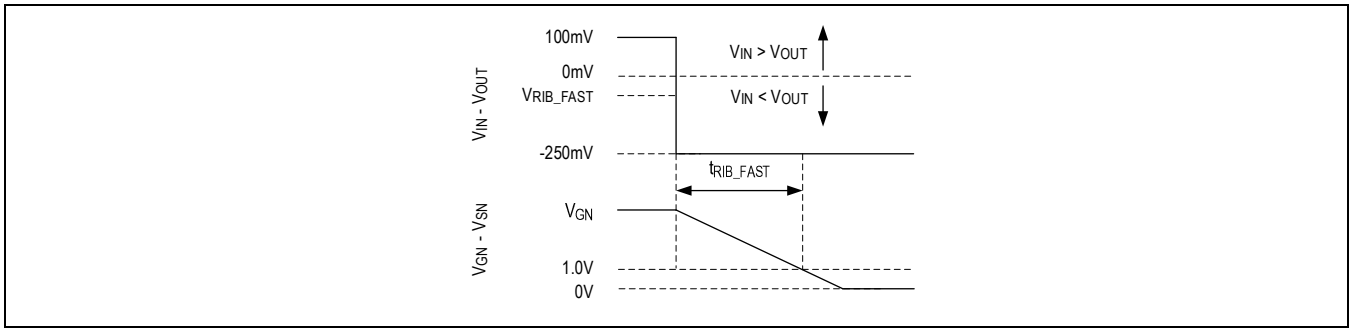
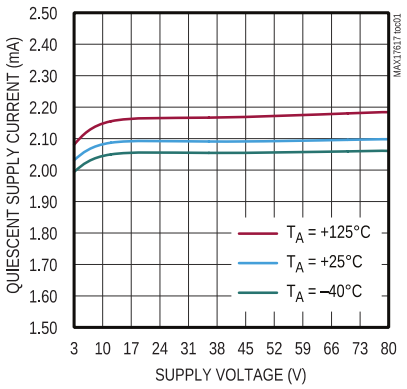


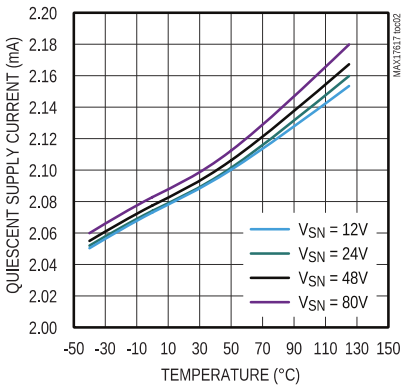

*Figure 2. Fast Reverse Current Blocking Response Time*

## Typical Operating Characteristics

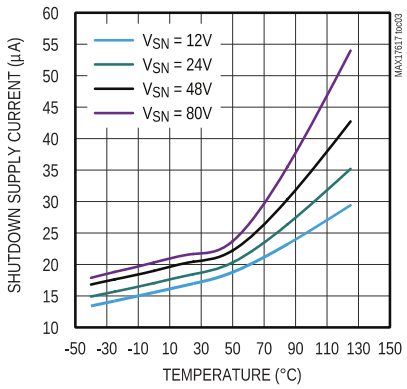
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



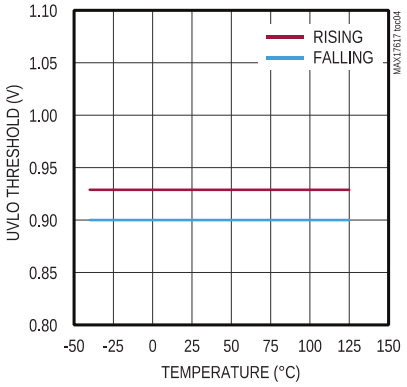

QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



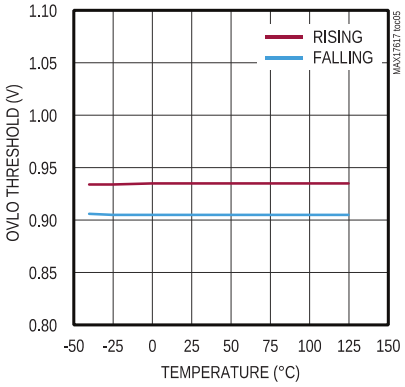

SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



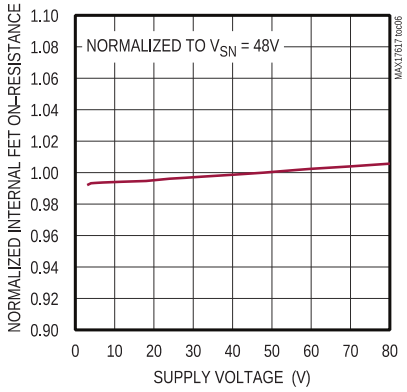

UVLO THRESHOLD vs. TEMPERATURE



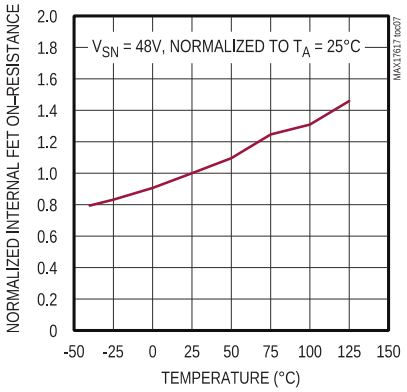

OVLO THRESHOLD vs. TEMPERATURE



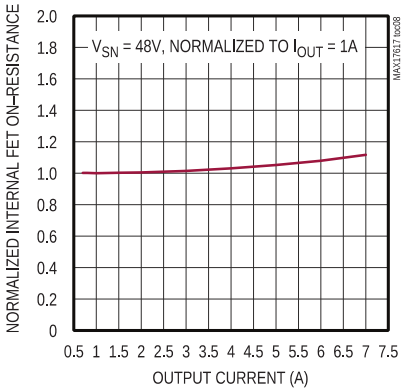

NORMALIZED INTERNAL FET ON–RESISTANCE vs. SUPPLY VOLTAGE



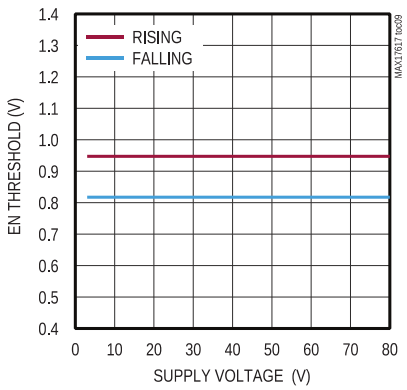

NORMALIZED INTERNAL FET ON–RESISTANCE vs. TEMPERATURE



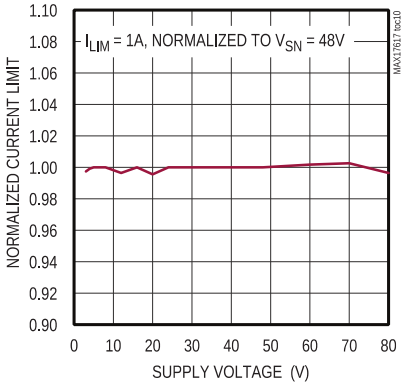

NORMALIZED INTERNAL FET ON–RESISTANCE vs. OUTPUT CURRENT



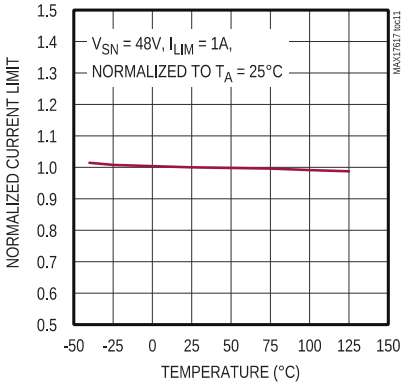

EN THRESHOLD vs. SUPPLY VOLTAGE



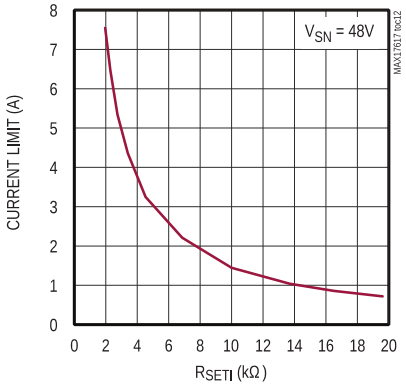
**NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE**



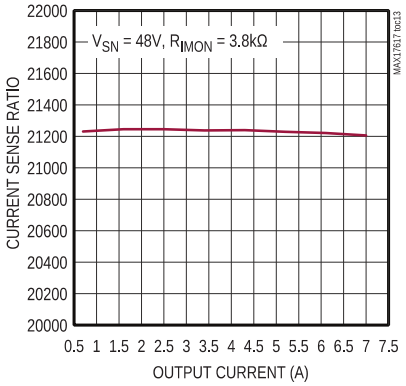

**NORMALIZED CURRENT LIMIT vs. TEMPERATURE**



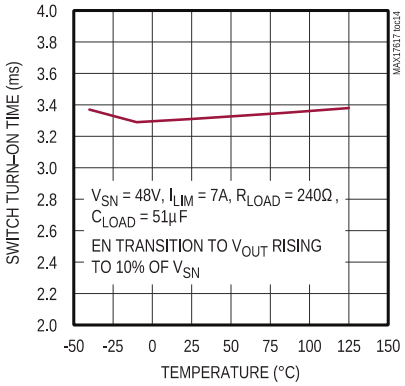

**CURRENT LIMIT vs. $R_{SETI}$**



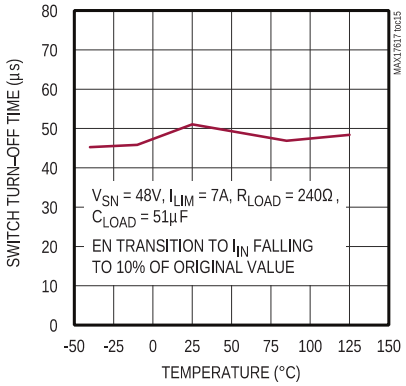

**CURRENT SENSE RATIO vs. OUTPUT CURRENT**



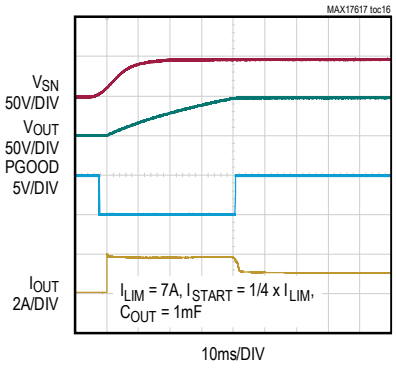

**SWITCH TURN–ON TIME vs. TEMPERATURE**



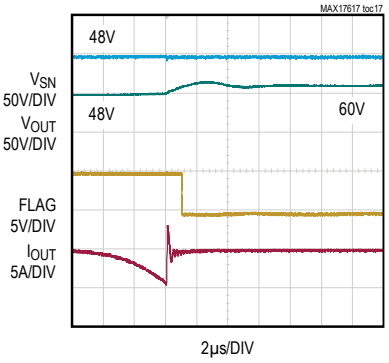

**SWITCH TURN–OFF TIME vs. TEMPERATURE**



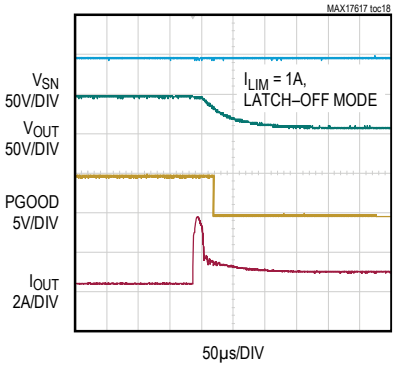

**POWER–UP RESPONSE**



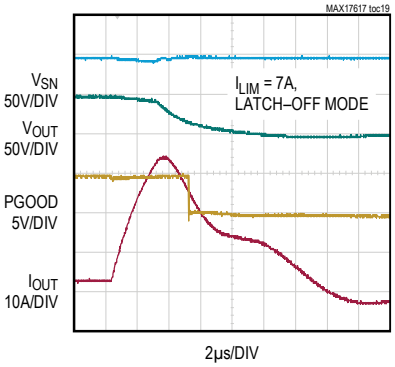

**REVERSE–BLOCKING RESPONSE**



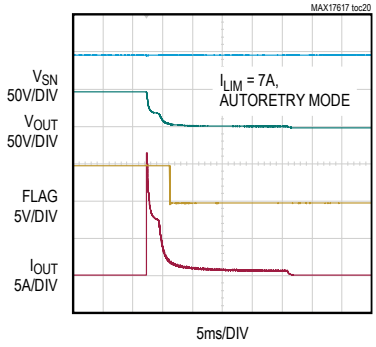
**CURRENT LIMIT RESPONSE**



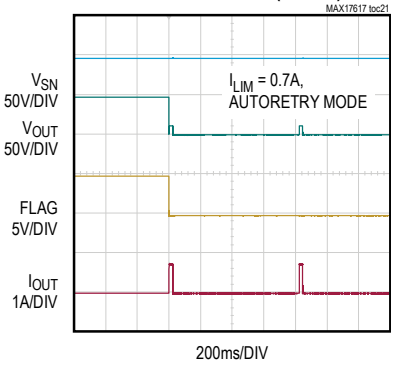

**OUTPUT SHORT–CIRCUIT RESPONSE**



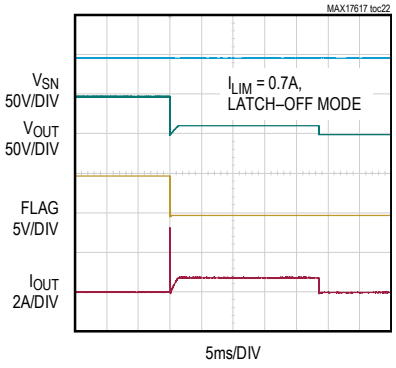

**THERMAL FOLDBACK DUE TO OUTPUT SHORT–CIRCUIT**



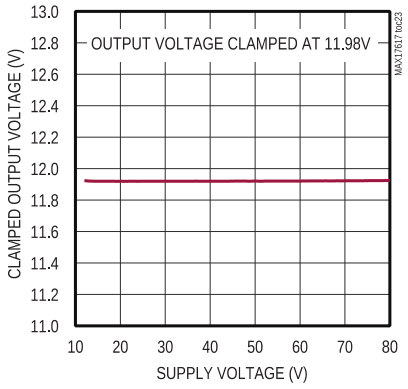

**AUTORETRY TIME ($t_{RETRY}$)**



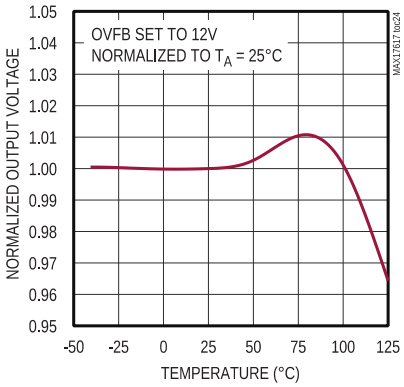

**LATCH–OFF CURRENT LIMIT**



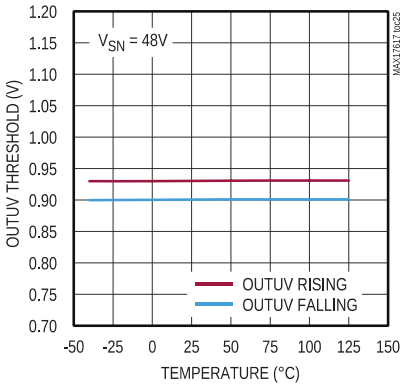

**CLAMPED OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**



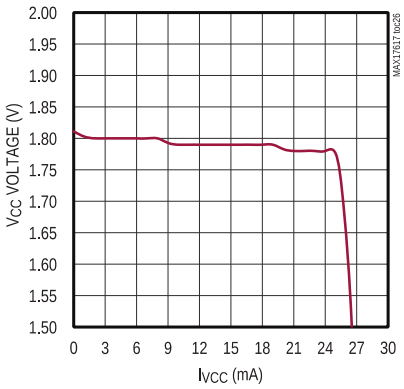
NORMALIZED CLAMPED OUTPUT VOLTAGE vs. TEMPERATURE



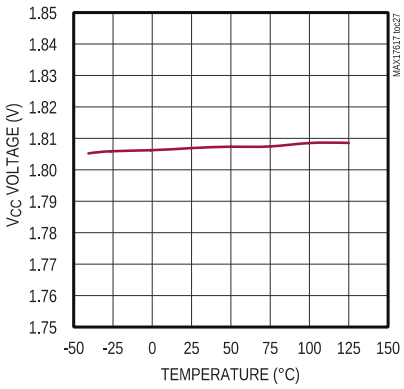

OUTUV THRESHOLD vs. TEMPERATURE



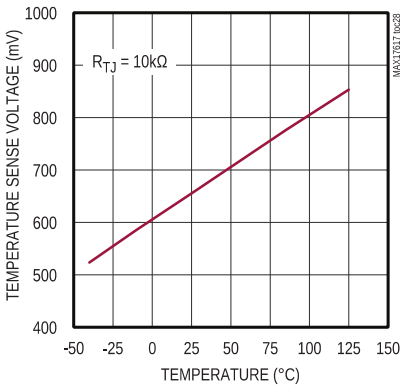

$V_{CC}$ VOLTAGE vs. $I_{VCC}$



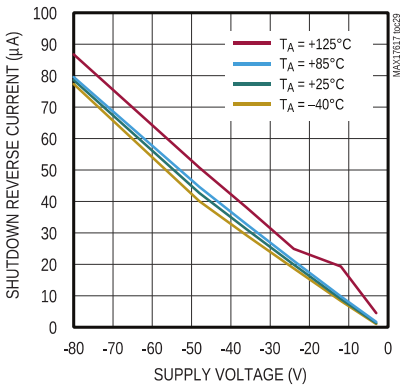

$V_{CC}$ VOLTAGE vs. TEMPERATURE



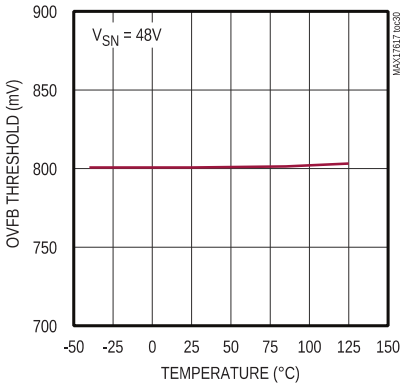

TEMPERATURE SENSE VOLTAGE vs. TEMPERATURE



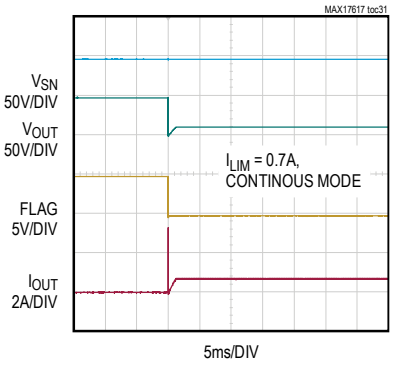

SHUTDOWN REVERSE CURRENT INTO SUPPLY vs. SUPPLY VOLTAGE



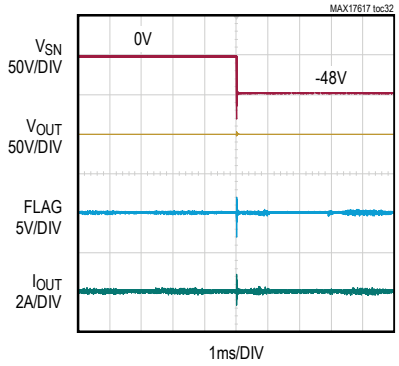
**OVFB THRESHOLD vs. TEMPERATURE**



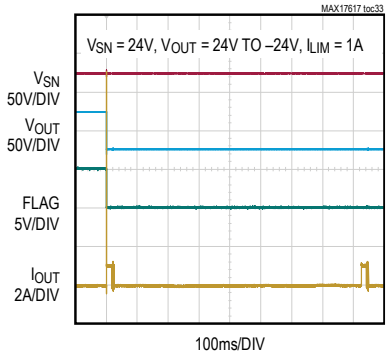

**CONTINOUS CURRENT LIMIT**



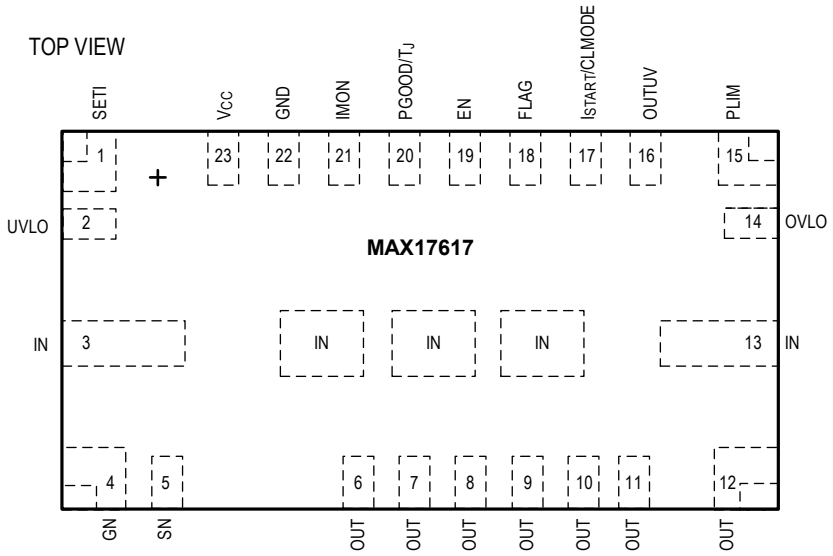

**REVERSE INPUT SUPPLY PROTECTION**



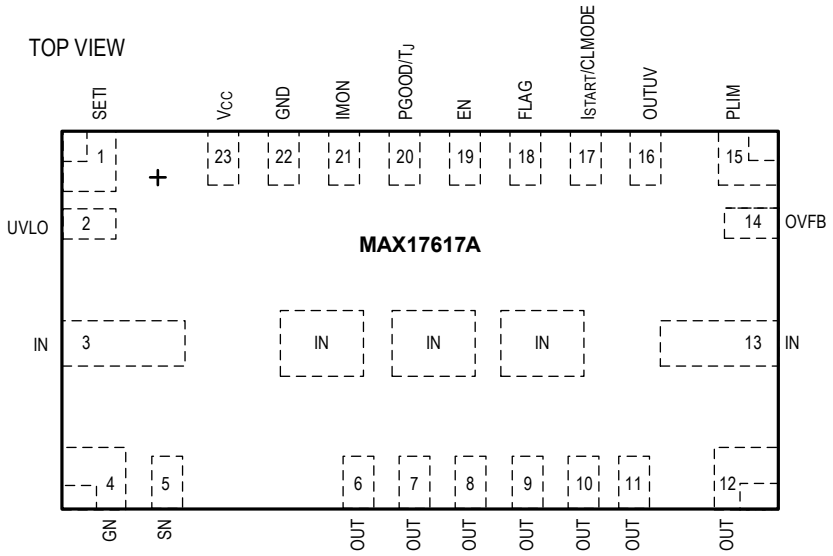

**OUTPUT REVERSE POLARITY PROTECTION**



## Pin Configurations




**23-PIN FCQFN**
**(4.5mm x 5.75mm)**

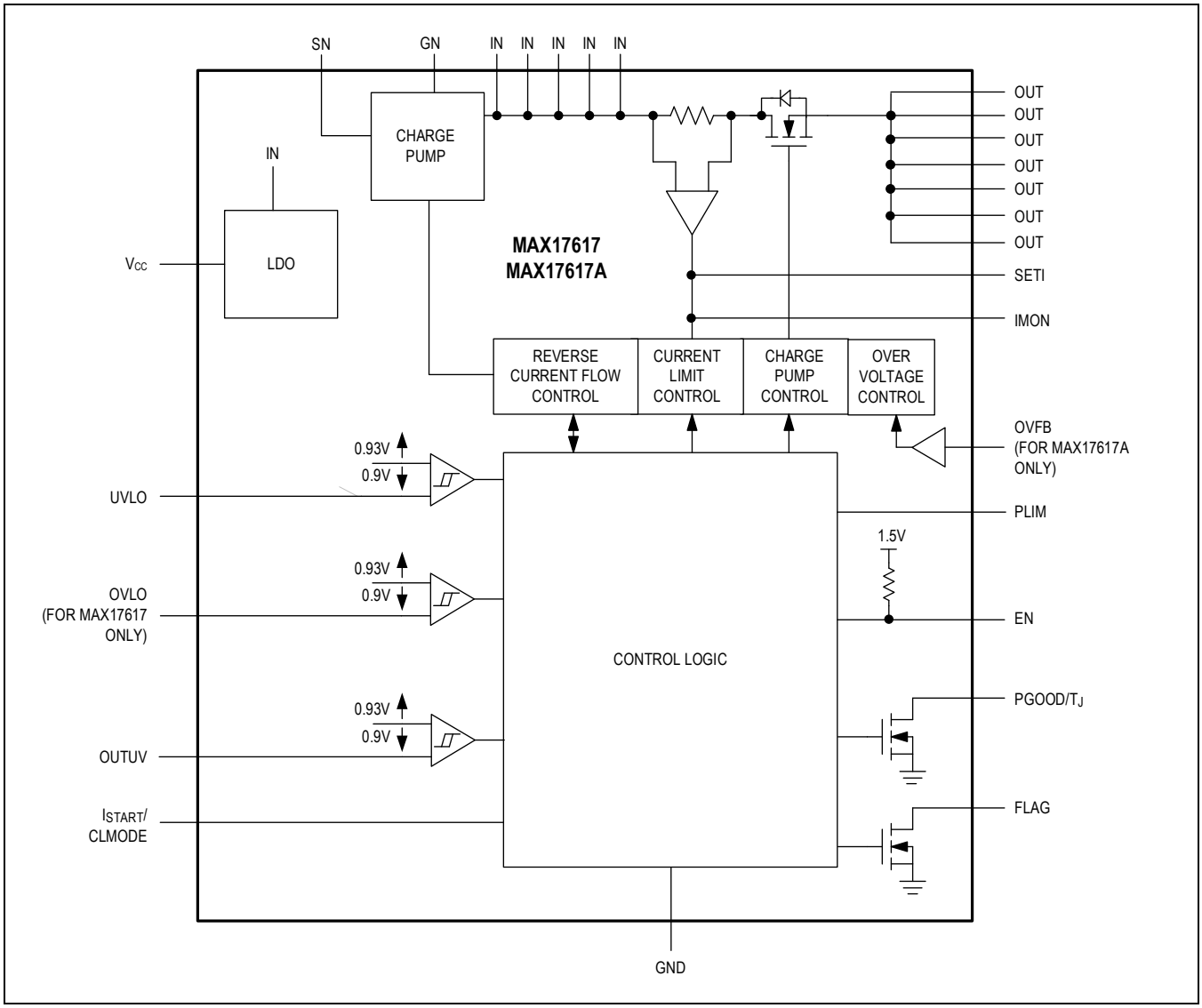



**23-PIN FCQFN**
**(4.5mm x 5.75mm)**

## Pin Descriptions

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX17617 | MAX17617A | | |
| 1 | 1 | SETI | Current Limit Adjustment Pin. Connect a resistor from SETI to GND to set the current limit. See *Setting the Current-Limit Threshold* section. Do not connect more than 30pF to SETI. |
| 2 | 2 | UVLO | Input Under Voltage Lockout (UVLO) Adjustment Pin. Connect resistive potential divider from SN/IN to GND pin to set the UVLO threshold. Tie UVLO to a voltage higher than the UVLO threshold if the UVLO function is not used. |
| 3, 13 | 3, 13 | IN | Input Pins. For Hot Plug-In applications, see the *Applications Information* section. |
| 4 | 4 | GN | Gate Driver Output for External Reverse Protection nFET. Connect SN and GN terminals to IN, if external nFET is not used. |
| 5 | 5 | SN | Return for External Reverse Protection nFET and Input Voltage Sense Pin. Connect to the source of external nFET as shown in the *Typical Application Circuits*. Connect SN and GN terminals to IN, if external nFET is not used. |
| 6–12 | 6–12 | OUT | Output Pins. For a long output cable or inductive load, see the *Applications Information* section. |
| 14 | – | OVLO | OVLO Adjustment Pin. Connect resistive potential divider from SN/IN to GND pin to set the OVLO threshold. Connect OVLO to GND to disable the OVLO function. |
| – | 14 | OVFB | Output Voltage feedback pin for Over Voltage Clamp function. Connect the resistive potential divider from OUT to GND to set the output voltage clamp threshold. Connect OVFB to GND when not used. See the *Input Voltage Surge Stopping and Output Overvoltage Feedback Regulation (OVFB)* section. |
| 15 | 15 | PLIM | Power Limit Adjustment Pin. Connect PLIM to an external resistive potential divider to define a threshold at which the power limit feature starts reducing the current-limit threshold. Connect PLIM to GND to disable this feature and have the current limit set only by the resistor placed on SETI. |
| 16 | 16 | OUTUV | Output Undervoltage Sensing for PGOOD Comparator Input. Connect resistive potential divider from OUT to GND pin to set the OUTUV threshold. |
| 17 | 17 | $I_{START}$/ CLMODE | Startup Inrush Current limit/Current Limit Mode Selection and Reverse Protection nFET presence programming pin. Connect a resistor from the $I_{START}$/CLMODE pin to GND to program the startup current limit and current limit mode. See the *Startup Inrush Current Limit ($I_{START}$)* section. |
| 18 | 18 | FLAG | Open-Drain Fault Indicator Output. Pull the FLAG to an external bias voltage for the FLAG function. See the *Fault Output (FLAG)* section for FLAG functionality. |
| 19 | 19 | EN | Active-High Enable Input. Internally pulled up to 1.5V. Leave unconnected for always-on the operation. |
| 20 | 20 | PGOOD/ $T_J$ | Open-Drain Power Good Output or Die Temperature Monitor Output.<br>Pull the PGOOD/$T_J$ to an external bias voltage for the PGOOD function.<br>PGOOD is pulled high when:<br>• $V_{OUT}$ exceeds OUTUV rising threshold and ($V_{IN}$ –$V_{OUT}$) satisfies < $V_{FA}$ condition.<br>PGOOD is pulled low when:<br>• $V_{OUT}$ falls below OUTUV falling threshold.<br>This pin can also be used to monitor the die temperature. Connect a 10kΩ–20kΩ resistor from PGOOD/$T_J$ to GND to measure device temperature. See the *Die Temperature Monitoring (PGOOD/$T_J$)* for more details. |
| 21 | 21 | IMON | Output Pin for Current Monitoring. Connect a resistor from IMON to GND to program the current monitor readout. See the *Current Monitoring (IMON)* section. |
| 22 | 22 | GND | Ground Pin. Reference pin for all control signals. |
| 23 | 23 | $V_{CC}$ | Internal LDO Output. Connect a minimum of 2.2µF/0603, low-ESR ceramic capacitor from $V_{CC}$ to GND. |

## Functional Diagram



## Detailed Description

The MAX17617/MAX17617A offers highly versatile and programmable protection boundaries for systems against input voltage faults and output overcurrent faults. In addition, MAX17617/MAX17617A offers a programmable power limiting function. Input-voltage faults (with positive polarity) are protected up to +80V (without Reverse Current Protection)/+75V (with Reverse Current Protection), by an internal nFET featuring low ON-resistance (20mΩ typ). The devices feature a programmable undervoltage-lockout (UVLO) thresholds by using external voltage-dividers. The MAX17617 features a programmable overvoltage-lockout (OVLO) while MAX17617A offers a programmable output voltage clamp function through the OVFB pin that features an output voltage limiting regulation during input transient surge events. Input undervoltage and overvoltage protection (MAX17617)/output voltage clamp function (MAX17617A) can be programmed across the entire 3V to 80V operating range.

Input reverse-polarity protection is realized using an external nFET that is controlled by the devices. The magnitude of reverse-polarity voltage protection is dependent on the operating load-bus voltage ($V_{OUT}$) and the voltage-blocking capability of the external nFET. For example, for protection down to a -55V input range with $V_{OUT}$ = 30V, an external nFET rated at 85V is needed. The external nFET is also needed for the optional reverse-current protection. When used with a Reverse Protection external nFET (Q1), the devices prevent reverse current flow from load to source by turning off Q1. The reverse current thresholds and forward bias characteristics of the reverse current protection feature are tuned to achieve an ideal diode function suited for OR-ing and Power Multiplexer applications. If reverse polarity protection and reverse-current protection are not needed, SN and GN pins must be connected to IN. The devices are tolerant against accidental output reverse-polarity application due to incorrect wiring across the output terminals.

The current limit of the devices is programmed by connecting a resistor from the SETI pin to GND. The current limit can be programmed from 0.7A to 7.0A. When the current through the devices reaches or exceeds the set current limit, the resistance of the internal nFET is modulated to limit the current. The devices offer three current-limit behavioral modes: Continuous, Auto-retry, and Latch-off modes. In addition, the devices allow programmable startup inrush current limit during startup events, to prevent inrush current from limited power sources flowing into capacitive or negative impedance output loads.

The IMON pin presents a current proportional to the device current under normal operation. Together with the IMON resistor (between IMON and GND), the IMON pin presents a voltage that is proportional to the device current. This voltage can be read by a monitoring system to record the instantaneous current of the device. Place an optional 100nF ceramic capacitor from IMON to GND to limit the bandwidth of the measured current.

The device can be turned ON or OFF by enabling input EN by a controller supervisory system. This allows the controller supervisory system to Turn ON or OFF the power delivery to connected loads.

The devices offer loss-of-ground protection where it safely turns OFF the device operation during a loss-of-ground fault event, i.e., when the safety ground fuse opens in a redundant safety application.

The devices offer a status announcement signal (FLAG) to indicate operational and fault signals. The devices also offer a Power Good Signal (PGOOD/$T_J$) that may be used by a supervisory system to enable/disable the downstream loads. FLAG and PGOOD/$T_J$ are open drain pins and require an external pullup resistor to the appropriate system interface.

The devices offer a programmable output undervoltage sense threshold that governs the restart response after the output voltage drops below the OUTUV rising threshold. The device also offers internal thermal shutdown protection against excessive power dissipation.

### Input Undervoltage Lockout (UVLO)

The devices have a UVLO adjustment range from 3V to 79V. Connect an external resistive potential divider to the UVLO pin, as shown in *Figure 3*, to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. For low-bias current applications, such as a battery supply, the recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{UVLO\_RISING}\, x\, \left(1 + \frac{R_1}{R_2}\right)$$

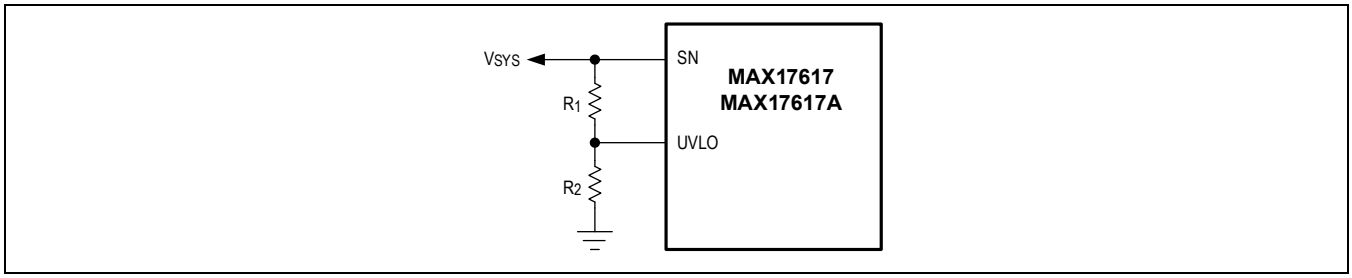



*Figure 3. Adjustable Input UVLO*

A 30mV (typ) hysteresis is provided on the UVLO pin, thus causing the devices to enter and exit undervoltage conditions in a deterministic manner. When the UVLO pin voltage falls below 0.9V (typ), the internal nFET turns OFF, and FLAG is asserted low. The external nFET, if used, turns OFF after a delay time ($t_{DF}$) of 100µs. When the Undervoltage condition is removed, and the UVLO pin voltage rises above 0.93V (typ), the devices take undervoltage lockout rising to debounce time ($t_{DEB\_UVLO}$) to start the switch turn ON process. The internal nFET turns ON, and the external nFET turns ON after a delay time ($t_{DR}$) of 100µs, and FLAG is de-asserted. The UVLO pin must not be left unconnected.

A typical undervoltage turn-on and turn-off sequence when the voltage on the UVLO pin increases above the rising threshold and decreases below the falling threshold. See *Figure 4* for more details.

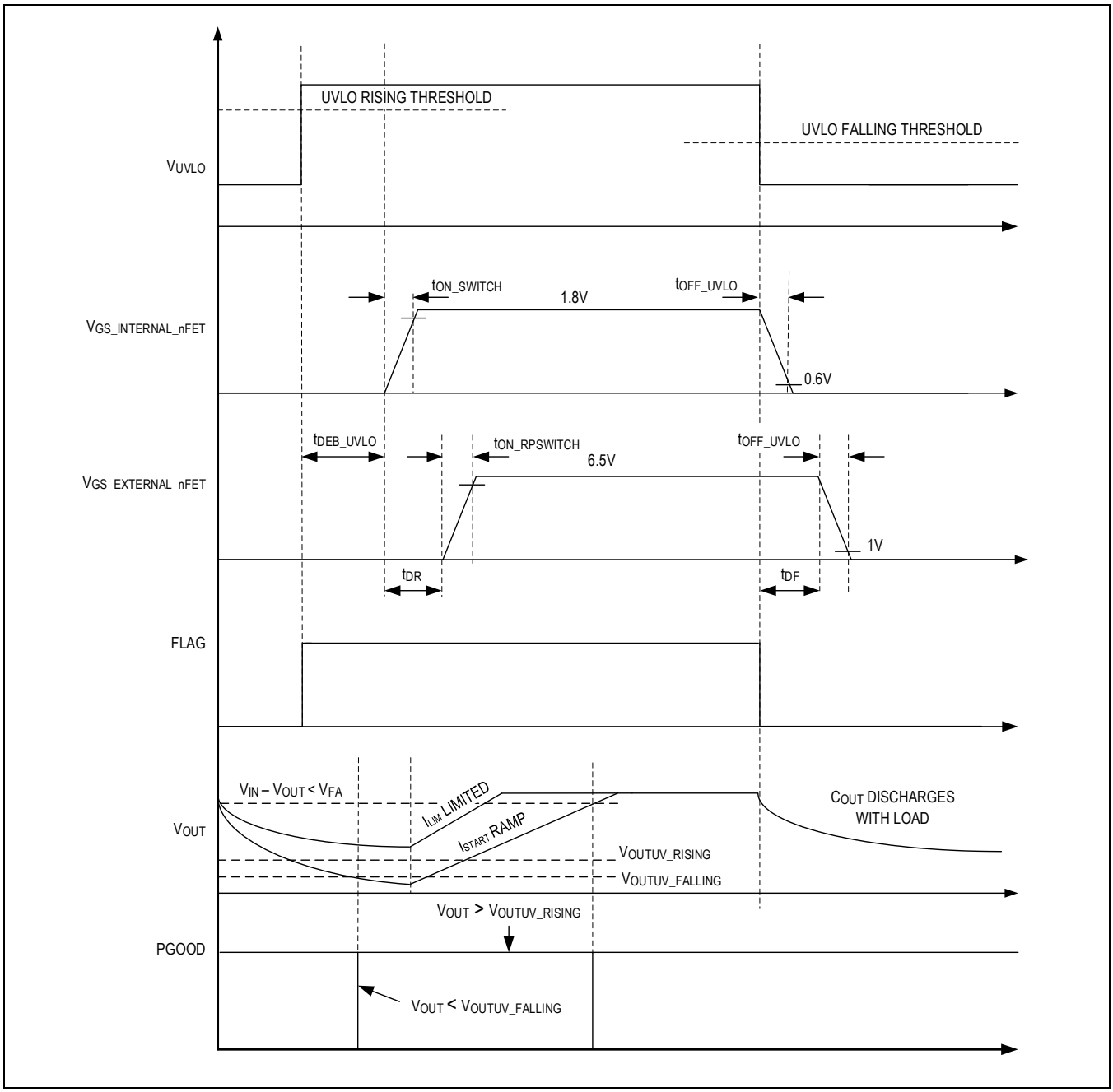



*Figure 4. Input Undervoltage Fault Timing Diagram*

### Input Overvoltage Lockout (OVLO)

The MAX17617 has an OVLO adjustment range from 3.5V to 80V. Connect an external resistive potential divider to the OVLO pin, as shown in *Figure 5*, to adjust the OVLO threshold voltage. Use the following equation to adjust the OVLO threshold. For low-bias current applications, such as a battery supply, the recommended value of R3 is 2.2MΩ.

$$V_{OVLO} = V_{OVLO\_RISING}\, x\, \left(1 + \frac{R_3}{R_4}\right)$$

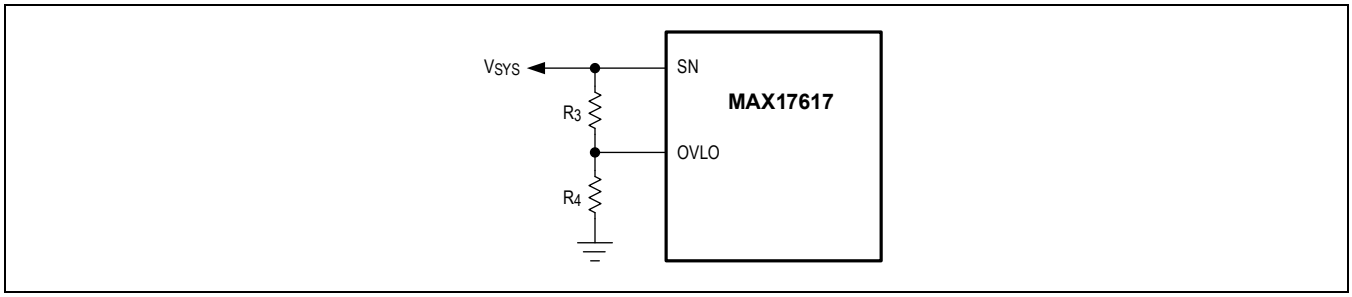



*Figure 5. Adjustable Input OVLO*

A 30mV (typ) hysteresis is provided on the OVLO pin, thus causing the devices to enter and exit overvoltage conditions in a deterministic manner. When the OVLO pin voltage rises above 0.93V (typ), the internal nFET turns OFF, and FLAG is asserted low. The external nFET, if used, turns OFF after a delay time ($t_{DF}$) of 100µs. When the overvoltage condition is removed, and the OVLO pin voltage falls below 0.9V (typ), the MAX17617 takes overvoltage lockout rising debounce time ($t_{DEB\_OVLO}$) to start the switch turn-on process. The internal nFET turns ON, and the external nFET turns ON after a delay time ($t_{DR}$) of 100µs, and FLAG is de-asserted. If the OVLO function is not used, the OVLO pin must be connected to GND. The OVLO pin must not be left unconnected.

A typical overvoltage turn-off and turn-on sequence when the voltage on the OVLO pin increases above the rising threshold and decreases below the falling threshold as shown in *Figure 6*.

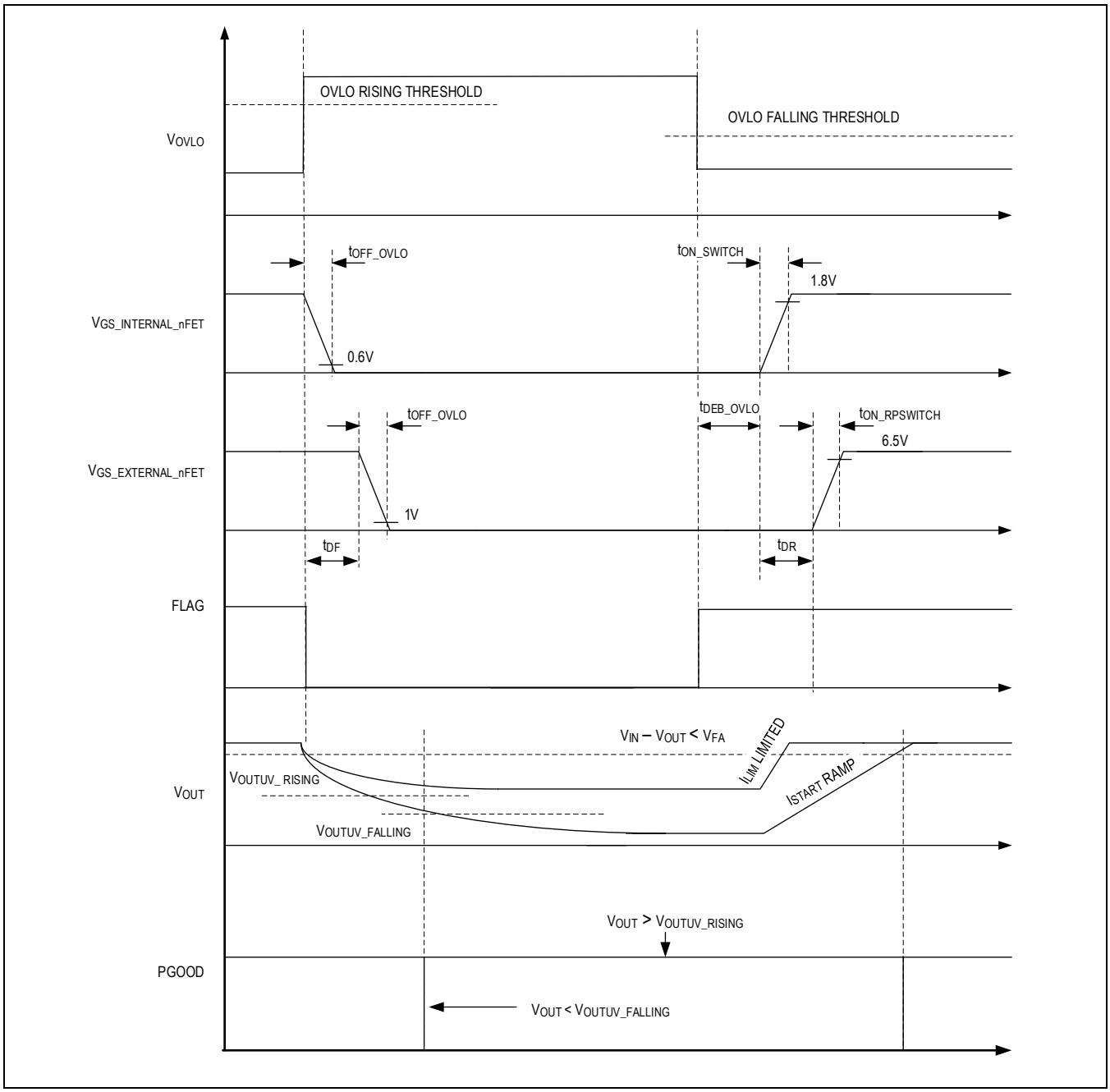



*Figure 6. Input Overvoltage Fault Timing Diagram*

### Input Debounce Protection

The devices provide input debounce protection. The devices start operation (by turning on the nFETs) only if the IN pin voltage is higher than the $V_{IN\_UVLO(R)}$ rising threshold for a period greater than the debounce time ($t_{DEB}$). If the voltage at the IN pin falls below the $V_{IN\_UVLO(F)}$ falling threshold before $t_{DEB}$ has elapsed, the devices remain off. When the devices are turned ON through EN, $t_{DEB}$ + EN turn-on time is always present. *Figure 7* shows a typical Input power-up timing sequence.

During initial power up (either hot plug-in, controlled input voltage slew rate, or otherwise), when the input voltage crosses INUVLOR (2.86V Max), if the input voltage does not reach the UVLO pin programmed voltage until INUVLO_Blanking_Time ($t_{INUVLOBLANK}$) = 500µs(typ), then the part shall declare UVLO fault by pulling FLAG low.

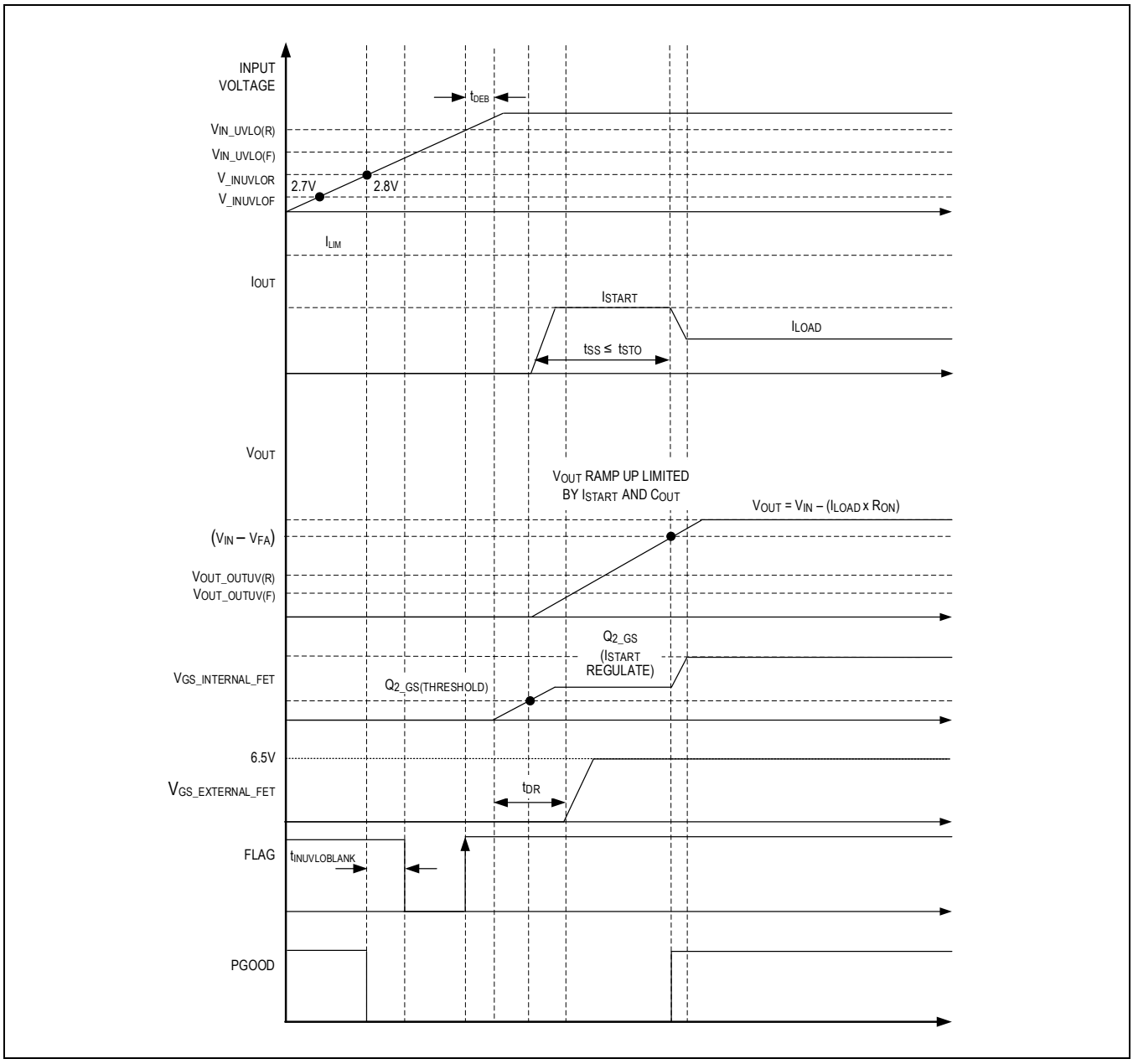



*Figure 7. Input Power-up Timing Diagram*

### Enable

The MAX17617/MAX17617A can be turned ON or OFF using the enable input pin (EN) to control the power delivery to connected loads. In Latch-Off Mode, the EN pin must be pulled low below 0.4V for at least 10µs to reset the fault condition and the devices resume operation. The EN pin is internally pulled up to 1.5V to have an always-on option when it is left open.

*Figure 8* and *Figure 9* show turn-on and turn-off control with EN.

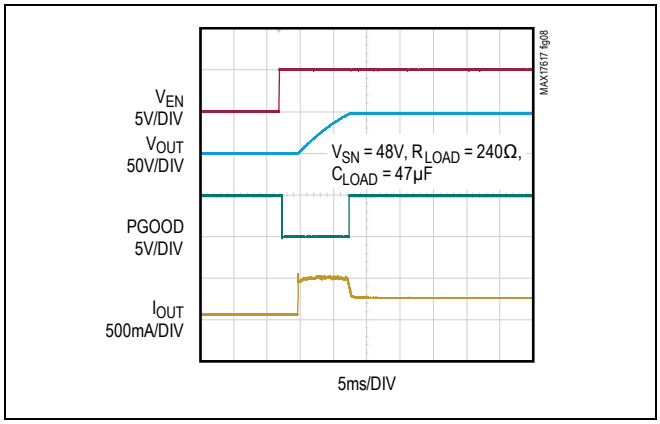



*Figure 8. Turn-on Control through EN Pin*

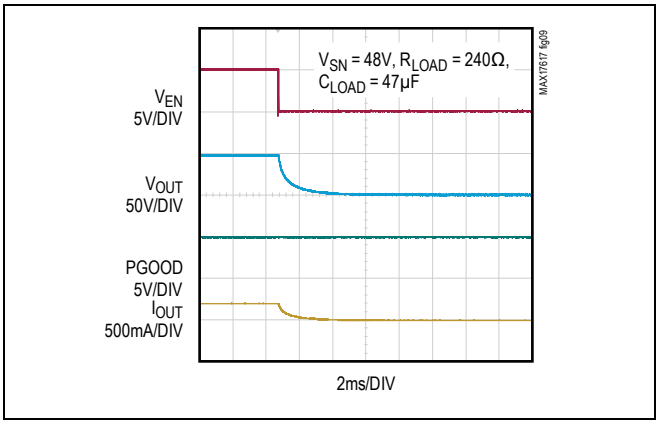



*Figure 9. Turn-off Control through EN Pin*

### Startup Inrush Current Limit ($I_{START}$)

The devices offer a programmable startup inrush current limit feature to limit the inrush current drawn from the power source and delivered to large capacitive loads. During the startup timeout period ($t_{STO}$), the current delivered to the output is limited to $I_{START}$ when $V_{OUT} < V_{IN} - V_{FA}$. The $t_{STO}$ timeout period is applied when there is a restart after a turn-off event caused by POR, EN, UVLO, or OVLO. If the output is not charged to ($V_{IN} – V_{FA}$) level within $t_{STO}$, the devices turn off, and IN or EN must be toggled to resume normal device operation, irrespective of CLMODE selected.

$I_{START}$ is programmed by connecting a resistor from the $I_{START}$/CLMODE pin to GND. The $R_{ISTART/CLMODE}$ is read immediately after POR to program the $I_{START\_RATIO}$ ($I_{START}/I_{LIM}$). Select the value of $R_{ISTART/CLMODE}$ from *Table 1* to program $I_{START\_RATIO}$ = (1/16, 1/8, 1/4, 1/2, 1). The $I_{START}$/CLMODE pin is also used to configure Current Limit Mode and Reverse Protection Feature.

## Table 1. $I_{START}$/CLMODE Configurations

| $R_{ISTART/CLMODE}$ (Ω) | $I_{START}/I_{LIM}$ ($I_{START\_RATIO}$) | CLMODE | PRESENCE OF EXTERNAL nFET/ REVERSE PROTECTION FEATURE |
|---|---|---|---|
| 24.3 | 1 | Auto-retry | No |
| 78.7 | 1 | Continuous | No |
| 147.0 | 1 | Latch-off | No |
| 226.0 | 1 | Auto-retry | Yes |
| 309.0 | 1 | Continuous | Yes |
| 402.0 | 1 | Latch-off | Yes |
| 499.0 | 0.5 | Auto-retry | No |
| 604.0 | 0.5 | Continuous | No |
| 732.0 | 0.5 | Latch-off | No |

| $R_{ISTART/CLMODE}$ (Ω) | $I_{START}/I_{LIM}$ ($I_{START\_RATIO}$) | CLMODE | PRESENCE OF EXTERNAL nFET/ REVERSE PROTECTION FEATURE |
|---|---|---|---|
| 866.0 | 0.5 | Auto-retry | Yes |
| 1000 | 0.5 | Continuous | Yes |
| 1210 | 0.5 | Latch-off | Yes |
| 1400 | 0.25 | Auto-retry | No |
| 1620 | 0.25 | Continuous | No |
| 1870 | 0.25 | Latch-off | No |
| 3160 | 0.25 | Auto-retry | Yes |
| 5760 | 0.25 | Continuous | Yes |
| 9090 | 0.25 | Latch-off | Yes |
| 12400 | 0.125 | Auto-retry | No |
| 16200 | 0.125 | Continuous | No |
| 20000 | 0.125 | Latch-off | No |
| 24300 | 0.125 | Auto-retry | Yes |
| 28700 | 0.125 | Continuous | Yes |
| 34800 | 0.125 | Latch-off | Yes |
| 41200 | 0.0625 | Auto-retry | No |
| 48700 | 0.0625 | Continuous | No |
| 56200 | 0.0625 | Latch-off | No |
| 64900 | 0.0625 | Auto-retry | Yes |
| 75000 | 0.0625 | Continuous | Yes |
| 86600 | 0.0625 | Latch-off | Yes |

The startup time for large capacitive loads may be calculated using the following equation:

$$t_{SS} = \frac{V_{IN}\ x\ C_{OUT}}{I_{START}}$$

where $t_{SS}$ is the required startup charging time in seconds.

*Figure 10* shows a typical Startup Timing Sequence during powerup.

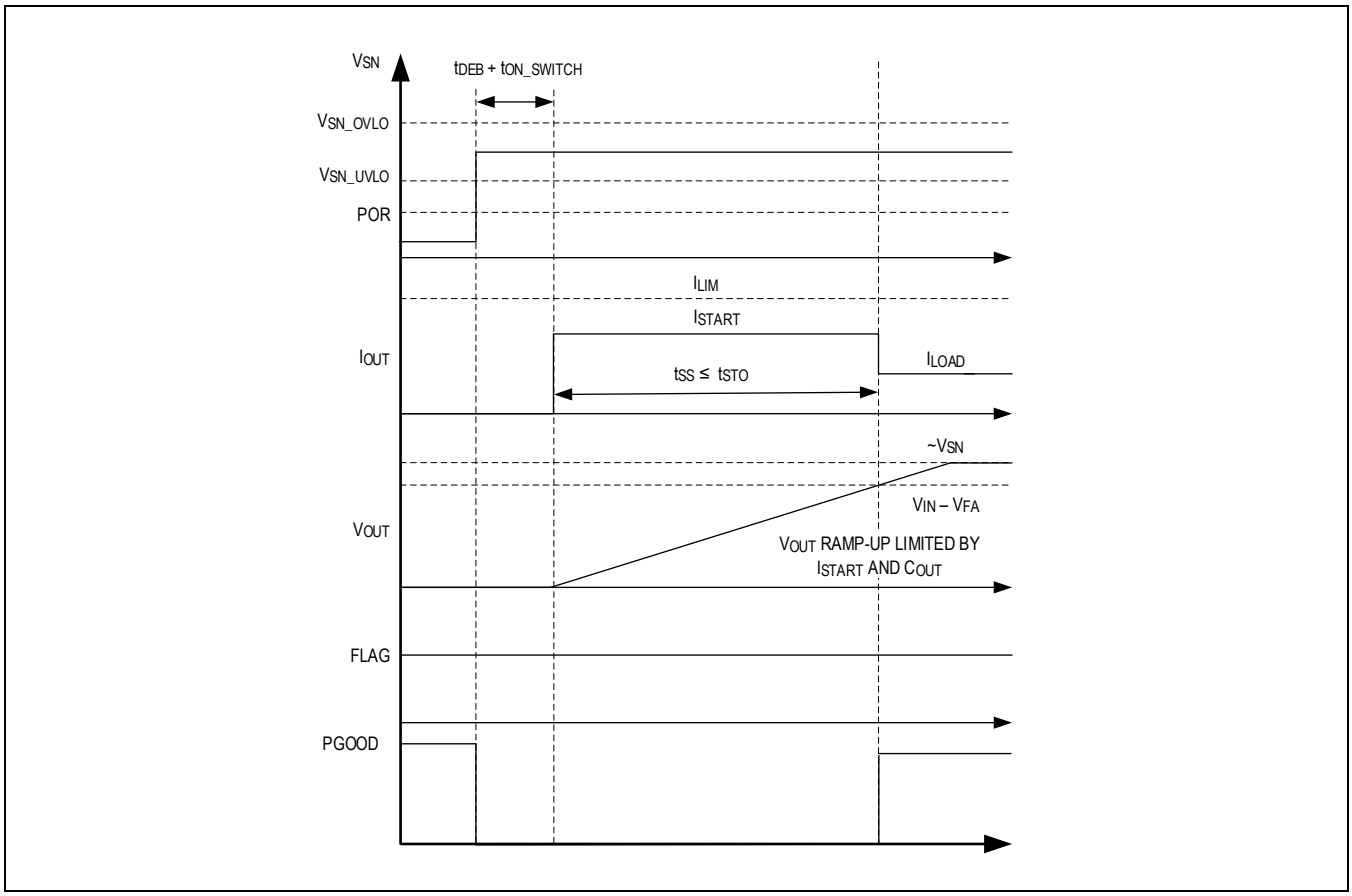



*Figure 10. $I_{START}$ Timing Diagram*

PGOOD remains asserted low during the soft start period. As the output voltage increases, when the voltage drop across the internal nFET (measured across IN and OUT pins) falls below an internal threshold $V_{FA}$, PGOOD is de-asserted.

### Setting the Current-Limit Threshold ($I_{LIM}$)

Connect a resistor between SETI and GND to program the current-limit threshold in the device. Use the following equation to calculate the current limit-setting resistor:

$$R_{SETI}(k\Omega) = \frac{14910}{I_{LIM}(mA)}$$

where $I_{LIM}$ is the desired current limit in mA.

Do not use an $R_{SETI}$ smaller than 1.86kΩ. *Table 2* shows current-limit thresholds for different resistor values.

## Table 2. Current-Limit Threshold vs. Resistor Values

| $R_{SETI}$ (kΩ) | CURRENT LIMIT $I_{LIM}$ (A) |
|---|---|
| 21.0 | 0.7 |
| 14.7 | 1 |
| 7.32 | 2 |
| 4.87 | 3 |
| 3.65 | 4 |
| 2.94 | 5 |
| 2.43 | 6 |
| 2.10 | 7 |

If SETI is left unconnected, $V_{SETI} \geq 1.5V$, and the current regulator does not allow any current to flow. The devices perform a check on the SETI pin for the first time it exits a shutdown condition. If the resistor placed on SETI is below 1kΩ, the switch remains off, and the FLAG asserts. *Figure 11* shows the SETI response during a load step event.

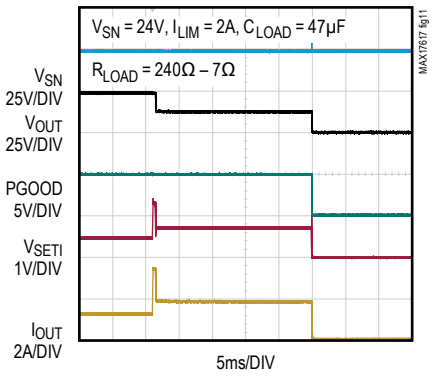



*Figure 11. SETI Response during a Load Step Event*

## Current Monitoring (IMON)

The devices offer a dedicated IMON pin to monitor the load current flowing through the internal nFET.

Connect a resistor ($R_{IMON}$) between IMON and GND to monitor the device current. Use the following equation to calculate the monitoring resistor $R_{IMON}$:

$$R_{IMON} = \frac{26625}{I_{LIM}(mA)}$$

where $R_{IMON}$ is the resistance from IMON to GND in kΩ.

An optional ceramic capacitor may be used from the IMON pin to GND to limit the bandwidth of the measured current. Use the following formula to select the required capacitor.

$$C_{IMON} = \frac{1}{2\pi \times R_{IMON} \times f_{CIMON}}$$

where $f_{CIMON}$ is the desired current monitor bandwidth in Hz, and $C_{IMON}$ is the required capacitance in F.

The voltage on the IMON pin ($V_{IMON}$) is calculated using the following formula:

$$V_{IMON} = \frac{I_{nFET}}{21300} \times R_{IMON}$$

where $I_{nFET}$ is the load current through the internal FET.

## Current-Limit and Short-Term Over Current features

The devices feature Short-Term Over Current Loading Capability ($I_{STLIM}$) to support load current profiles that contain short-term overload currents during normal operation. The $I_{STLIM}$ is set to two times the programmed current limit ($I_{LIM}$) on the SETI pin, and the short-term over the current duration ($t_{STOC}$) is set to 400µs.

1) If the load current exceeds $I_{LIM}$ but stays lower than $I_{STLIM}$ for a duration < $t_{STOC}$, the devices do not limit the current, and normal operation continues.
2) If the load current exceeds $I_{LIM}$ but stays lower than $I_{STLIM}$ for duration > $t_{STOC}$, or If the load current exceeds $I_{STLIM}$ but stays lower than $I_{OCP}$, the devices limit the current to the programmed current limit ($I_{LIM}$) within ~100µs.

Once the devices enter the current limit (ILIM), the devices' operation is decided by the current limit mode as described in the *Current-Limit Type Select* section.

*Figure 12* shows the current limit and short-term overcurrent timing diagram.

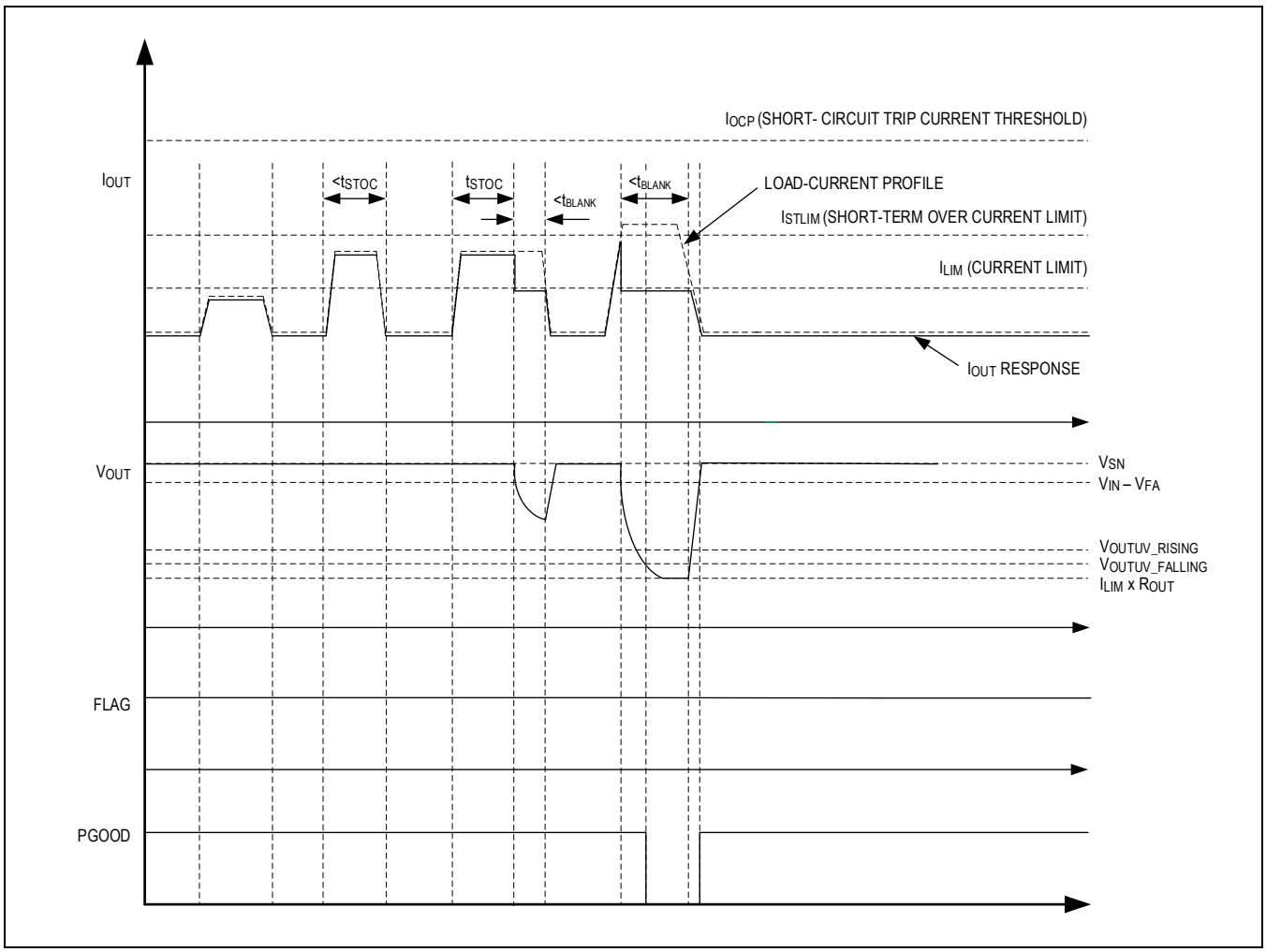



*Figure 12. Current Limit and Short-Term Overcurrent Timing Diagram*

## Current-Limit Type Select

The MAX17617/MAX17617A features three selectable current limit modes: Continuous, Auto-Retry, and Latch-Off modes. The current limit mode is programmed through the $I_{START}$/CLMODE pin, as shown in *Table 1*. If the ($V_{IN} - V_{OUT} < V_{FA}$) condition is not met within $t_{STO}$, the devices enter a latch-off state, irrespective of the CLMODE selected.

### Continuous Current Limit

In continuous current-limit mode, the devices limit the current continuously. The FLAG pin asserts when the current limit exceeds $t_{BLANK}$ duration and deasserts when voltage drops across the internal switch falls below $V_{FA}$. *Figure 13* depicts typical behavior in continuous current-limit mode.

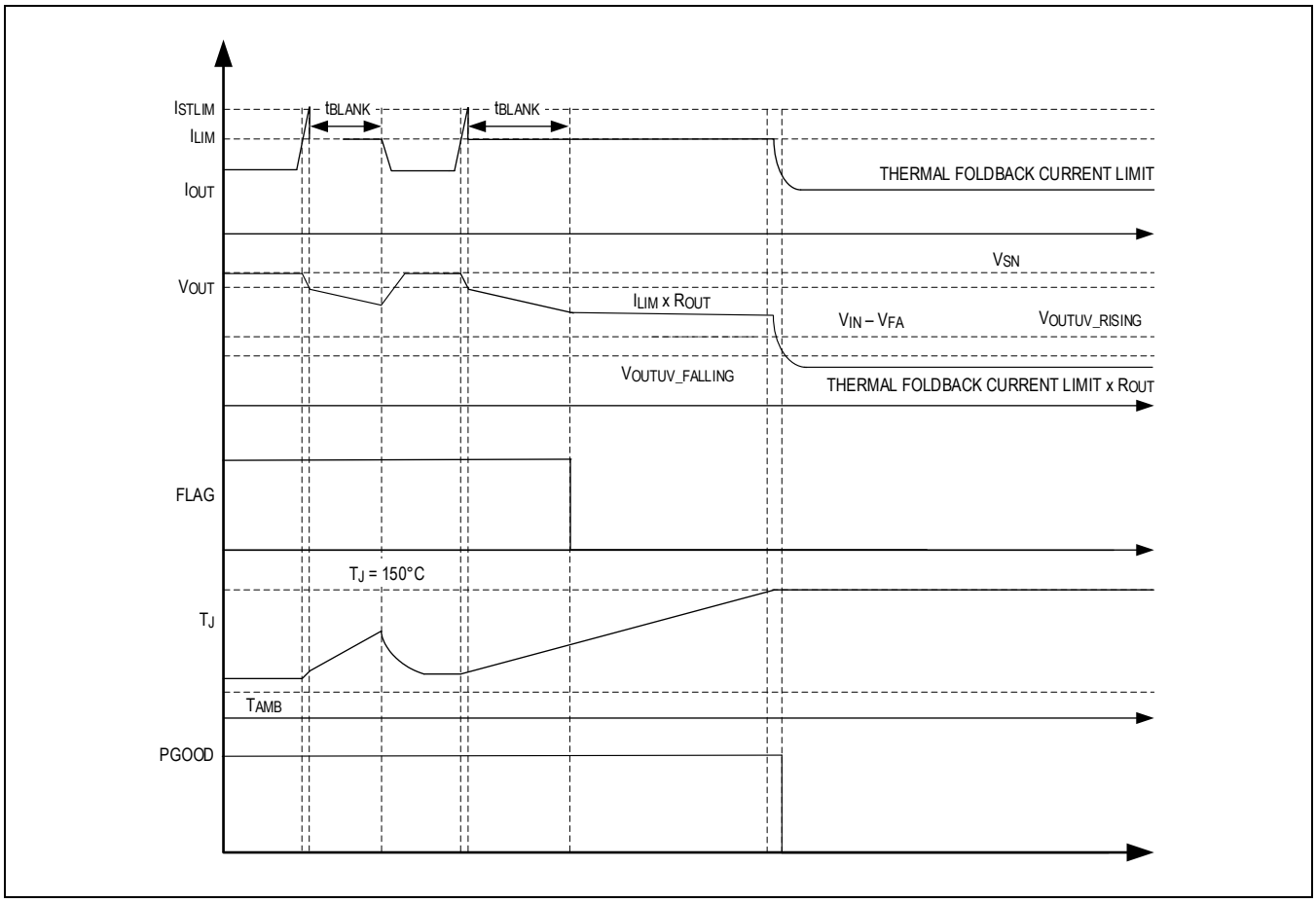



*Figure 13. Continuous-Fault Timing Diagram*

### Autoretry Current Limit

In Autoretry current limit mode, the devices attempt to restart operation after an internally fixed Autoretry period ($t_{RETRY}$). The internal Autoretry timer is activated when an overcurrent event condition remains for the blanking timer period ($t_{BLANK}$). The blanking timer resets if the overcurrent condition resolves before $t_{BLANK}$ has elapsed. During the $t_{RETRY}$ period, the switch remains OFF. Once $t_{RETRY}$ has elapsed, the device restarts with $I_{LIM}$. If the fault exists, the cycle repeats, and the FLAG pin remains asserted. If the overcurrent condition is resolved, the switch stays ON. The FLAG pin asserts when the current limit exceeds $t_{BLANK}$ duration and desserts when the voltage drop across the internal switch falls below $V_{FA}$.

The Autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is ON during $t_{BLANK}$ time, the supply current is held at the current limit. During $t_{RETRY}$ time, there is no current through the switch. Thus, the average output current is much less than the programmed current limit. The average output current can be calculated using the following equation:

$$I_{LOAD} = I_{LIM} \times \frac{t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

With a 24ms (typ) $t_{BLANK}$ and 800ms (typ) $t_{RETRY}$, the duty cycle is 2.9%, resulting in a 97.1% power reduction when compared to the switch being on the entire time. *Figure 14* shows typical behavior in the Autoretry Current-Limit mode.

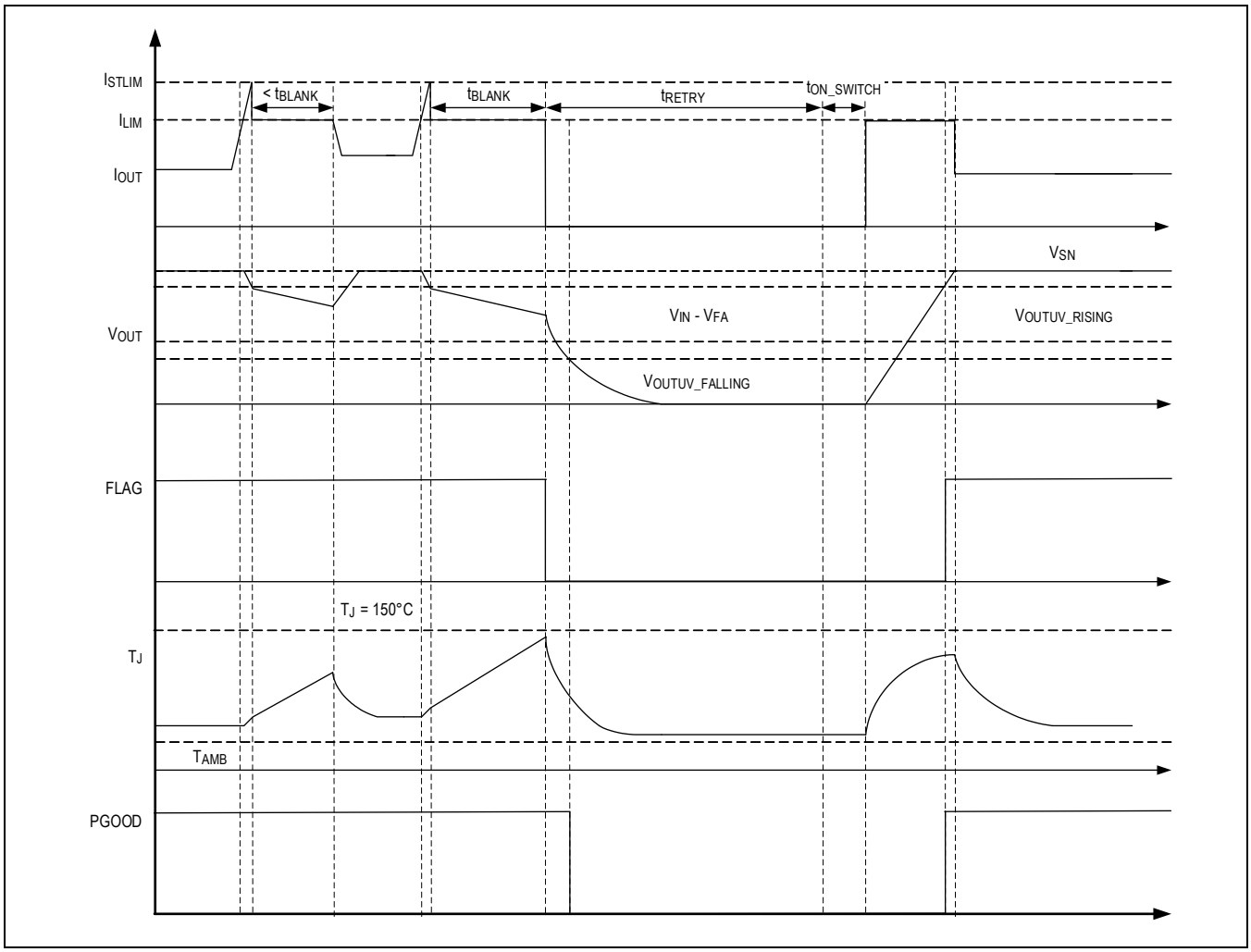



*Figure 14. Autoretry Fault Timing Diagram*

### Latch-Off Current Limit

In Latch-Off current limit mode, the devices remain OFF and latched, if an overcurrent event remains for the blanking timer period ($t_{BLANK}$). The blanking timer resets if the overcurrent condition resolves before $t_{BLANK}$ has elapsed. To reset the switch, either by holding the control logic (EN) low for at least 10µs (typ) or cycle the input power.
*Figure 15* shows typical behavior in latch-off current-limit mode.

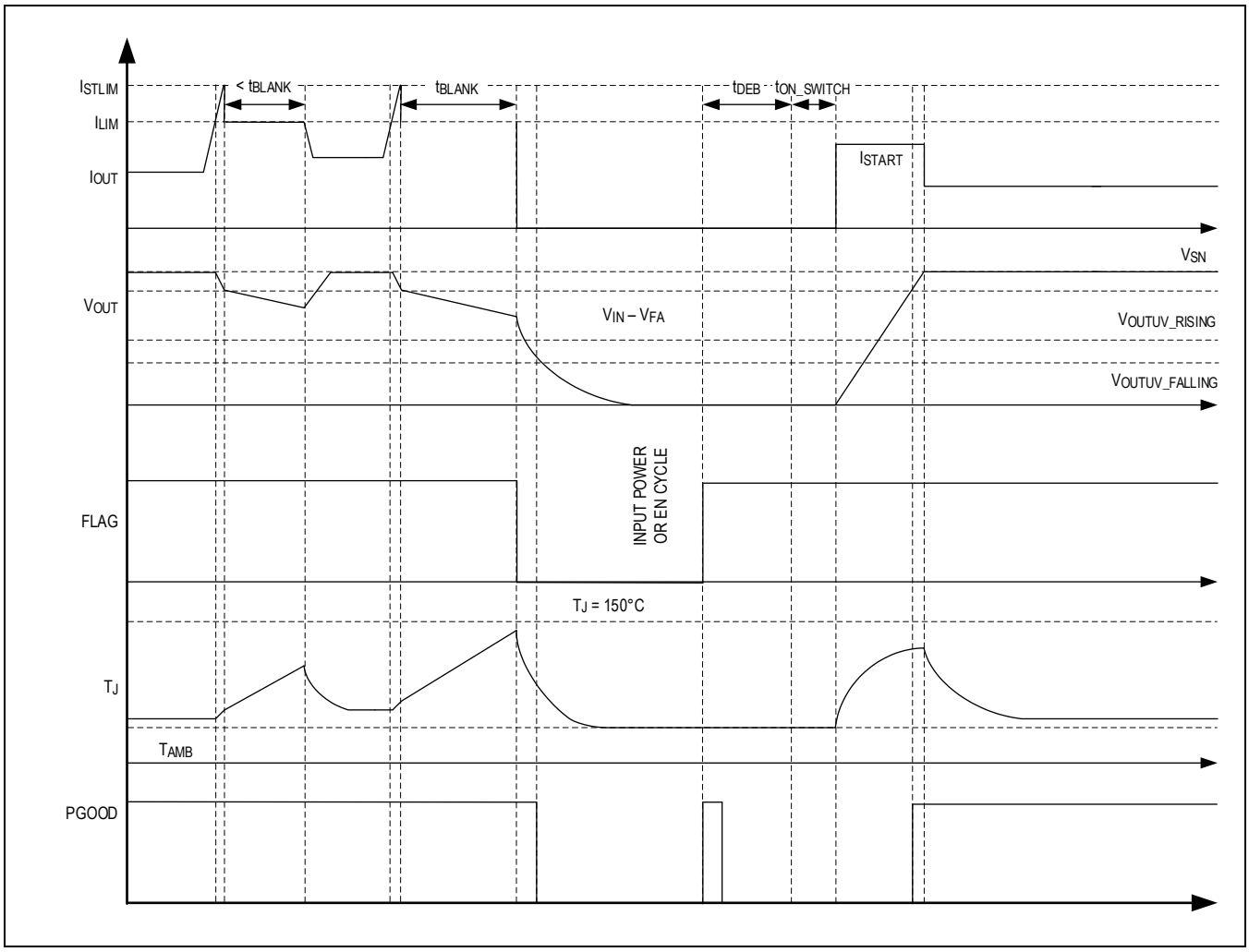



*Figure 15. Latch-off Fault Timing Diagram*

### Short Circuit Protection

During an output short circuit event, the current through the device increases very rapidly. The devices incorporate a fast-trip current comparator to limit the output short circuit peak current. The fast-trip current comparator turns off the internal nFET within 1µs ($t_{DELAY1}$) when the current through the internal FET exceeds $I_{OCP}$. The $I_{OCP}$ is internally set to 30A (typ). After a time delay of 200µs ($t_{DELAY2}$), the device turns back ON and limits the output current to the programmed current limit, and operates as described in earlier current limit mode sections. *Figure 16* illustrates the behavior of the system when the current exceeds the $I_{OCP}$ threshold.

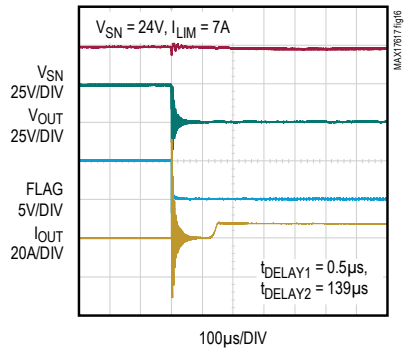



*Figure 16. Short Circuit Response*

## Reverse Current Protection

The reverse current protection feature is enabled when used with external nFET. The devices prevent reverse current flow from OUT to IN pins.

If a reverse current condition is detected ($V_{IN}$ - $V_{OUT}$) < $V_{RIB\_}$), the external nFET is turned OFF. When the reverse current condition no longer exists ($V_{SN}$ - $V_{OUT}$) > $V_{RIB\_RISING}$), the external nFET is turned back ON after $t_{ON\_RPSWITCH}$. If the reverse-current condition is the only fault (no UVLO, no OVLO, no thermal fault, no forward overcurrent fault), then the internal nFET is kept ON. Otherwise, the internal nFET is also turned OFF. *Figure 17* shows typical behavior in a slow- or fast-reverse-current condition.

The device contains two reverse-current thresholds with slow (20µs typ) and fast (100ns typ) response times for reverse-current protection. The threshold value for slow reverse is -5mV (typ), whereas for fast reverse, it is -100mV (typ). This feature results in robust operation in a noisy environment while still delivering fast protection for a severe fault, such as input short-circuit or hot plug-in at the OUT pins. The FLAG pin asserts during a reverse current condition.

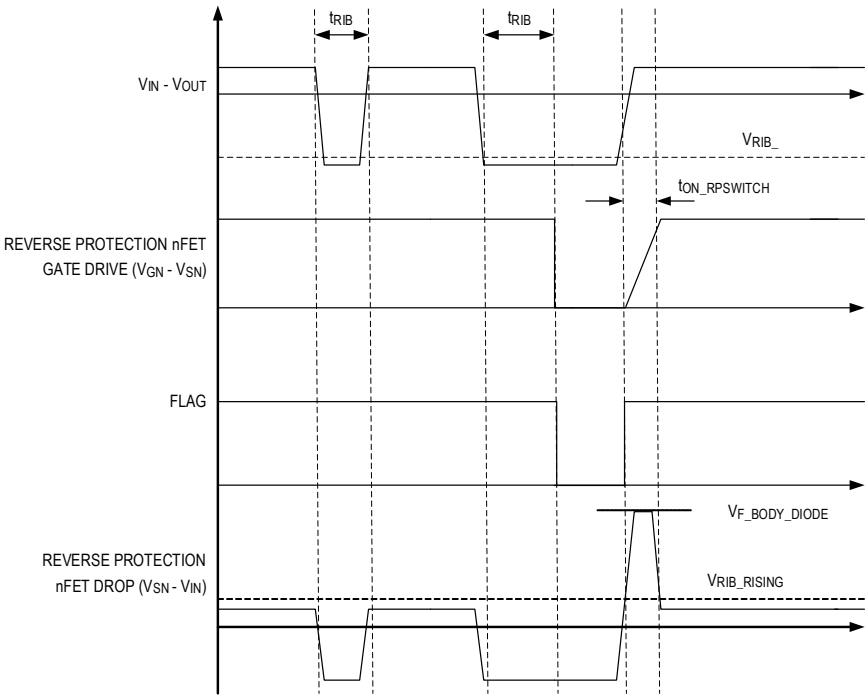



*Figure 17. Reverse Current Fault Timing Diagram*

### Input Voltage Surge Stopping and Output Overvoltage Feedback Regulation (OVFB)

The MAX17617A offers a surge protection feature whereby the output voltage is limited to a programmable voltage level during input voltage surge events. When the input voltage surges above a set threshold, the output overvoltage feedback loop (OVFB) modulates the drain to source resistance of the internal Control nFET and limits the output voltage. A simplified internal block diagram of the overvoltage clamp function is shown in *Figure 18*.

There is no timer for the OVFB condition. The part can regulate OUT to be below IN indefinitely, depending on load conditions.

1. Part shall operate in OVFB mode as long as no other condition (overcurrent, thermal foldback, and much more) kicks in. This is true even if ($V_{IN}$ - $V_{OUT}$) exceeds $V_{FA}$, provided only the OVFB condition is present. FLAG pin is not asserted in this case.

2. The OVFB condition may trigger $t_{BLANK}$ (when a consequential thermal foldback condition kicks in), and the part needs to follow programmed CLMODE after $t_{BLANK}$. At the end of the $t_{BLANK}$ period, the FLAG pin is asserted.

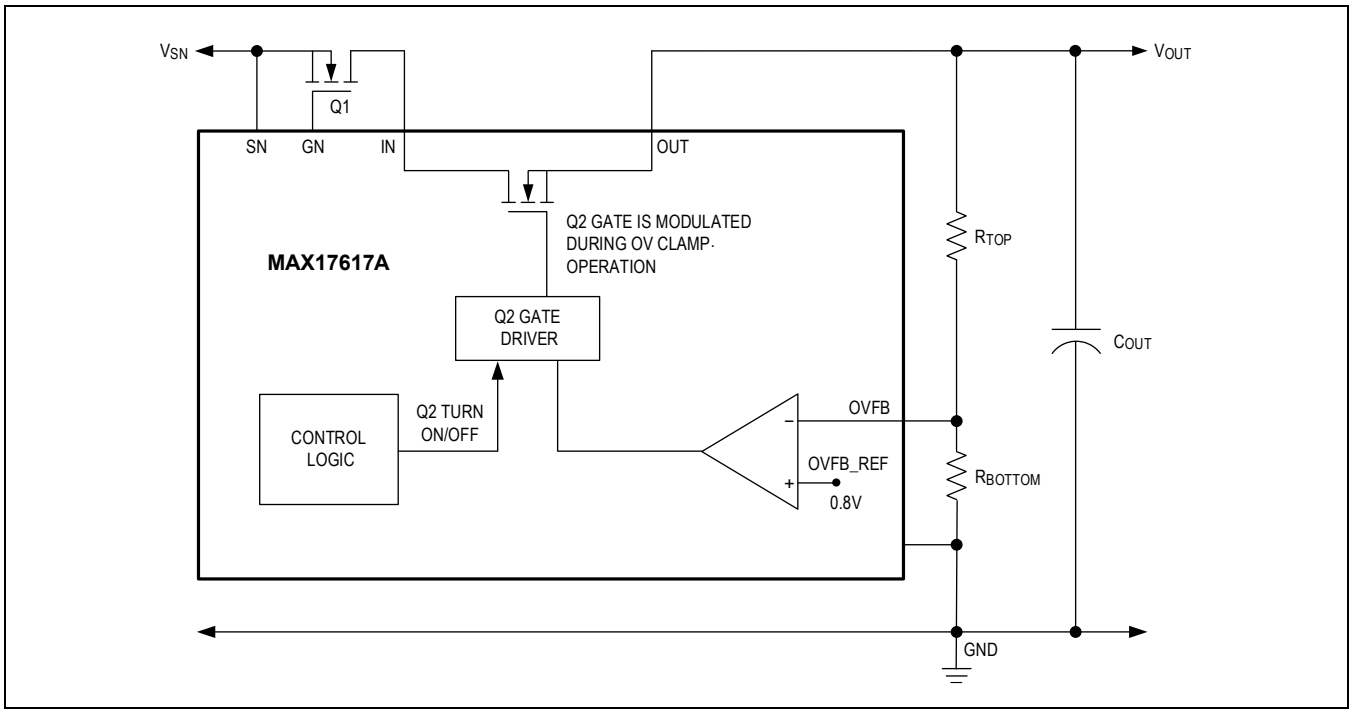



*Figure 18. Overvoltage Clamp through OVFB*

A typical overvoltage clamp operation and recovery sequence are shown in *Figure 19* and *Figure 20* shows overvoltage clamp response for MAX17617A during an input surge event.

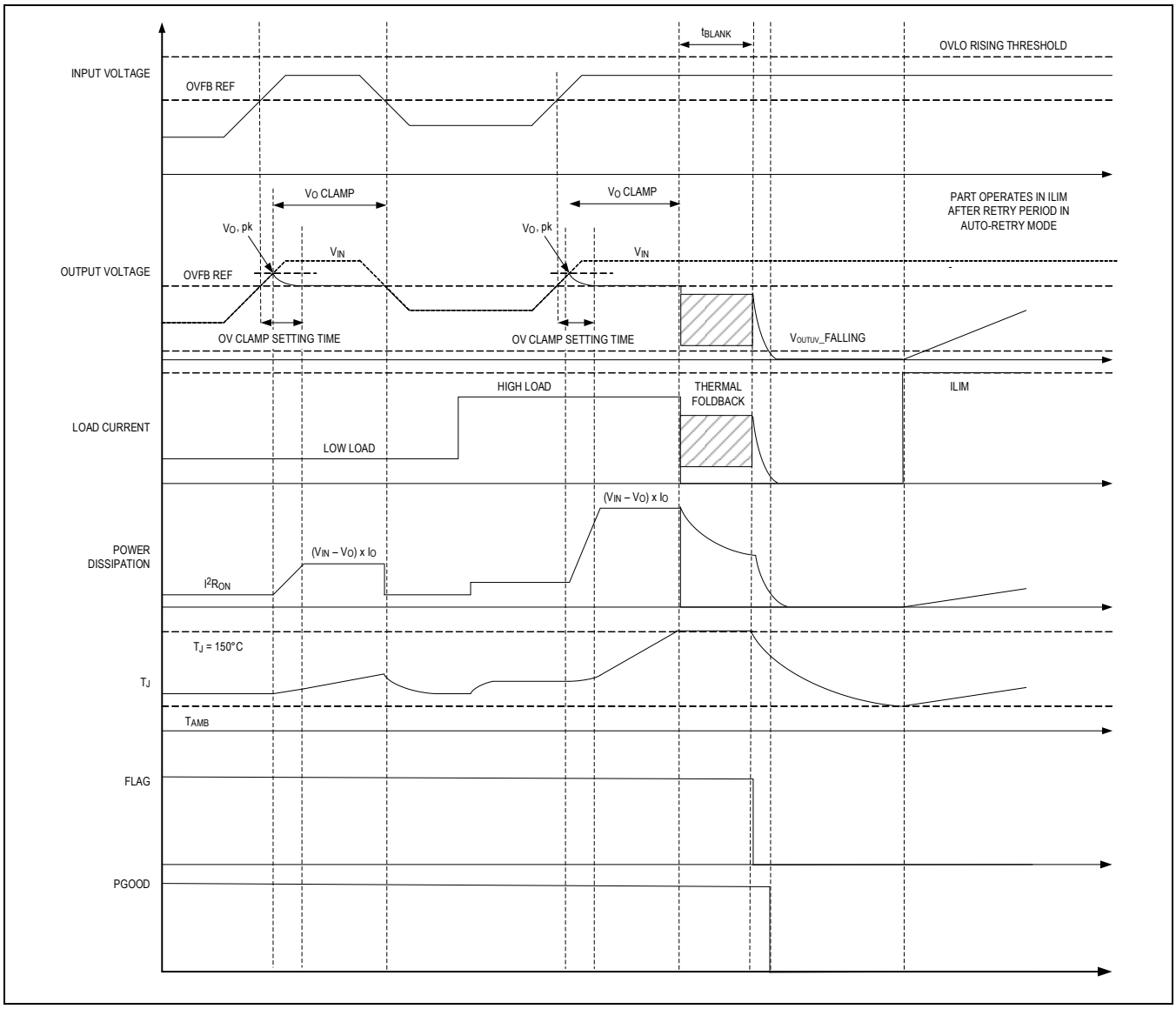



*Figure 19. Overvoltage Clamp Operation and Recovery*

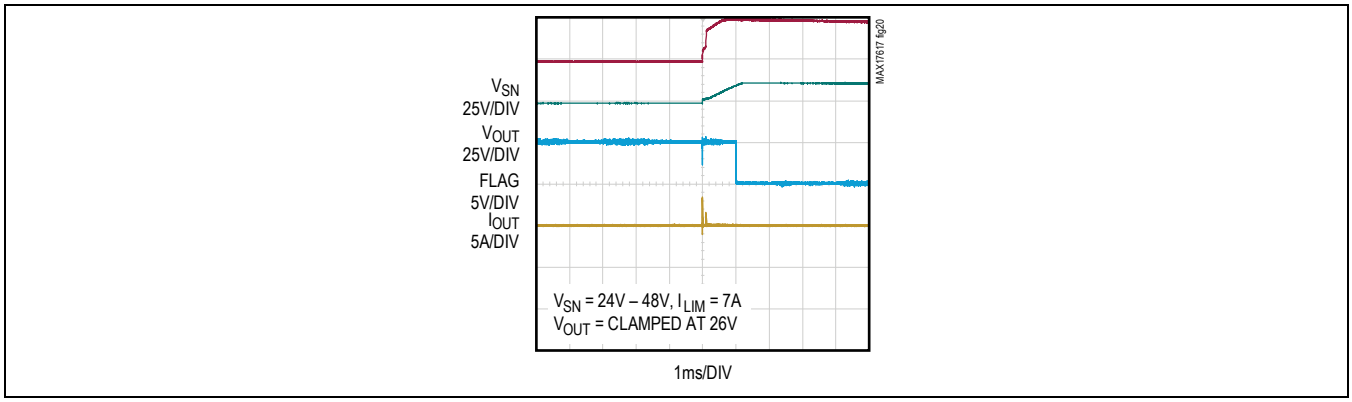



*Figure 20. Overvoltage Clamp Response*

## Input Reverse-Polarity Protection

Input reverse-polarity protection is realized using an external nFET that is controlled by MAX17617/MAX17617A. Due to incorrect wiring on the input power supply terminals, a negative supply can appear on the devices' input pins. Connect an external nFET (Q1) with the source connected to the SN pin, drain to the IN pin, and gate to the GN pin, as shown in the *Typical Application Circuits*. During an input reverse polarity voltage fault, this external nFET turns OFF and protects the load. The external nFET is also needed for the optional reverse-current protection. If reverse polarity protection and reverse-current protection are not needed, the SN and GN pins must be connected to the IN pin.

The magnitude of reverse-polarity voltage protection is dependent on the operating load bus voltage ($V_{OUT}$) and the voltage-blocking capability of the external nFET. For example, for protection down to a -55V input voltage with $V_{OUT}$ = 30V, an external nFET rated for 85V is needed. The devices provide a gate drive (GN) of 6.5V (typ). *Figure 21* shows the reverse-polarity protection of MAX17617 with $V_{OUT}$ = 0V and $V_{SN}$ = -24V. *Figure 22* shows the reverse-polarity protection of MAX17617 with $V_{OUT}$ = +24V and $V_{SN}$ = -24V.

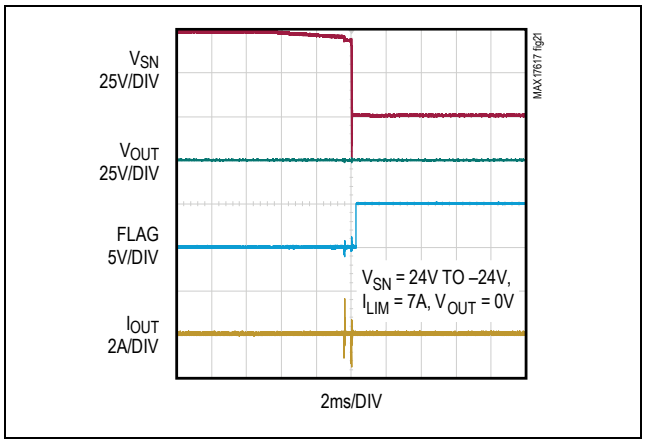



*Figure 21. Input Reverse-Polarity Protection at $V_{OUT}$ = 0V and $V_{SN}$ = -24V*

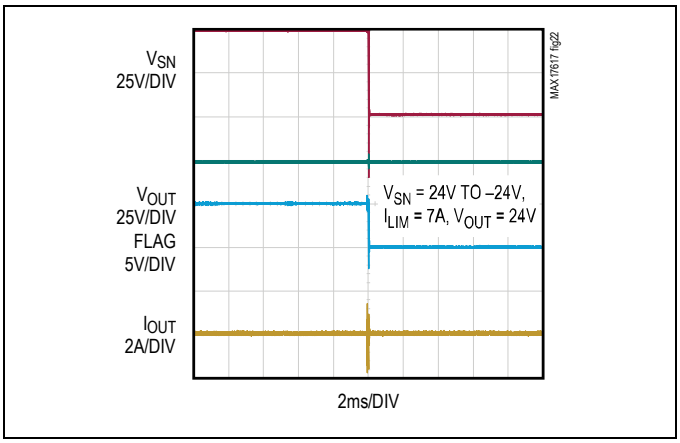



*Figure 22. Input Reverse-Polarity Protection at $V_{OUT}$ = +24V and $V_{SN}$ = -24V*

## Output Reverse-Polarity Protection

MAX17617/MAX17617A protects itself and the input-power connections from accidental reverse output-voltage polarity connections. Reverse output voltage can appear across the OUT and GND pins due to inductive loads or incorrect wiring connections of live loads across the output terminals.

*Figure 23* shows the output reverse-polarity protection of the MAX17617 with $V_{OUT}$ = -24V and $V_{SN}$ = 24V and *Figure 24* shows the response with $V_{OUT}$ = -24V, and $V_{SN}$ = 0V. The devices can protect the circuit's negative output voltage up to – (85 – $V_{IN}$) V. *Figure 25* shows the recovery performance from an output reverse polarity fault condition.

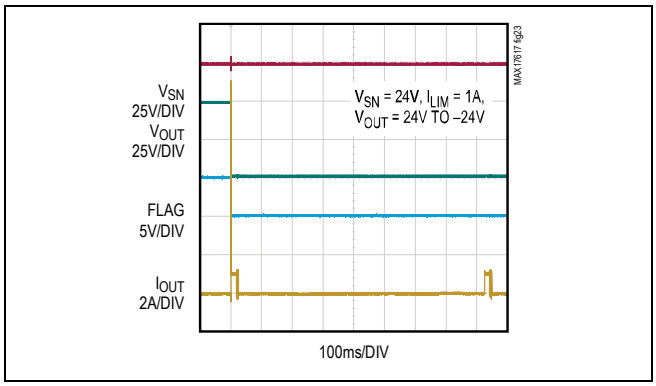



*Figure 23. Output Reverse-Polarity Protection with Auto-Retry Mode with $V_{OUT}$ = -24V and $V_{SN}$ = 24V*

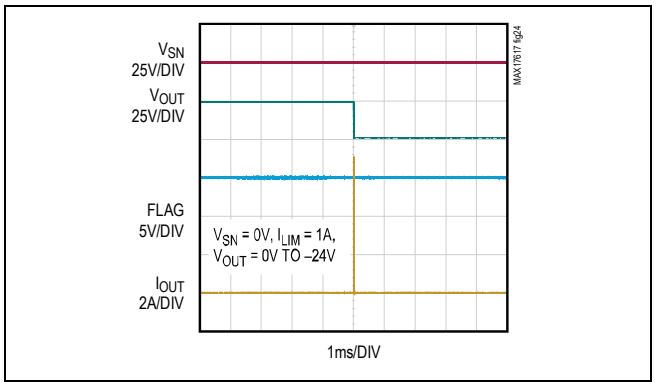



*Figure 24. Output Reverse-Polarity Protection with Auto-Retry Mode with $V_{OUT}$ = -24V and $V_{SN}$ = 0V*

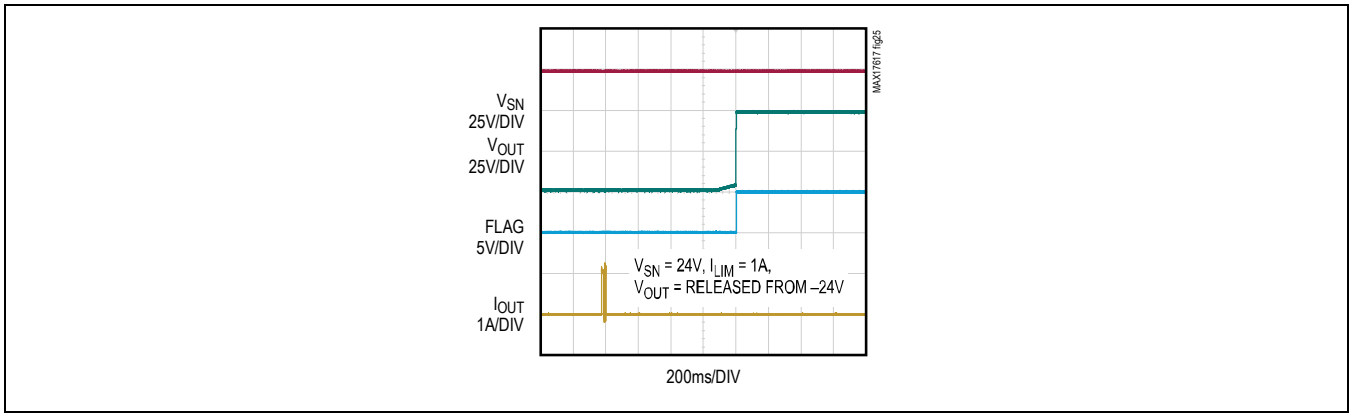



*Figure 25. Recovery Performance from an Output Reverse-Polarity Fault with $V_{OUT}$ = -24V Initial Condition and $V_{SN}$ = 24V*

## Loss of Ground Protection

The devices protect loads by turning OFF the internal and external nFETs in a loss-of-ground event. A loss-of-ground event can be caused by a break in connectivity between the ground reference of the system control and the IC ground net around MAX17617/MAX17617A. This feature eliminates the requirement for additional external circuits to protect from loss-of-ground events. Additional components are required to protect signal pins (EN, IMON, FLAG, PGOOD), as shown in the *Typical Application Circuits*. *Figure 26* shows the typical behavior during a loss-of-ground event.

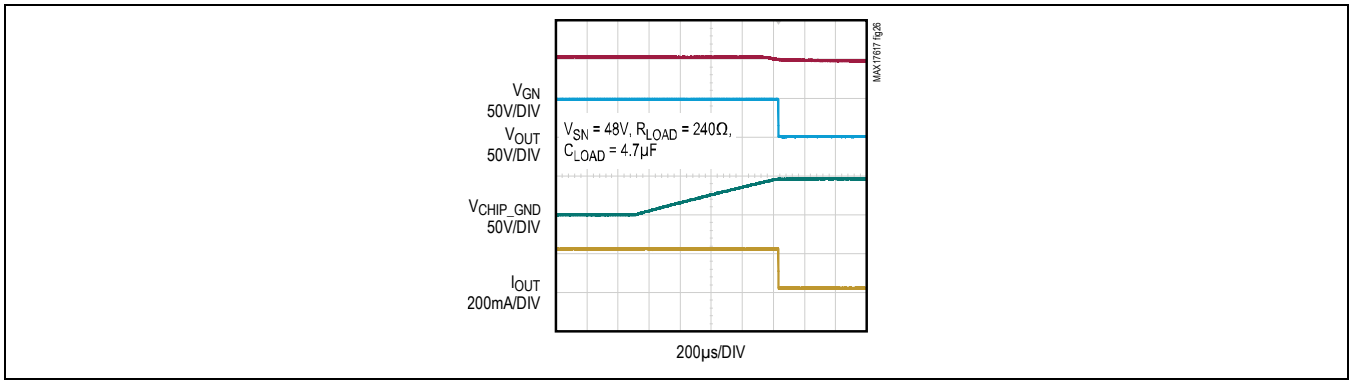



*Figure 26. Load Current Interruption During a Loss of Ground Event*

### Output Undervoltage Sensing (OUTUV)

The devices offer a programmable output undervoltage sensing threshold (OUTUV). When the voltage on the OUT pin falls below the OUTUV falling threshold due to any fault condition, the internal control logic affects a restart cycle with a soft start. If, during any fault condition, the output voltage does not fall below the OUTUV falling threshold, then the restart cycle is affected without soft-start. This is particularly useful during transient input source fault conditions that do not discharge the output voltage below the programmed OUTUV threshold, where the devices recover without going through a soft-start cycle.

Connect an external resistive potential divider to the OUTUV pin, as shown in *Figure 27* to adjust the OUTUV threshold voltage. Use the following equation to adjust the OUTUV threshold. For low-bias current applications, such as a battery supply, the recommended value of R7 is 2.2MΩ.

$$V_{OUTUV} = V_{OUTUV\_RISING} \times (1 + R7/R8)$$

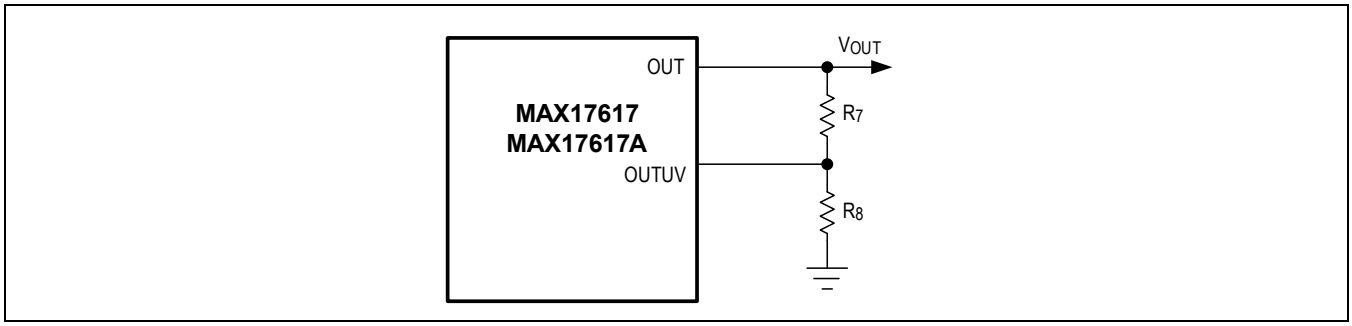



*Figure 27. Adjustable Output Undervoltage Sensing*

### Power Good Output (PGOOD/$T_J$)

The devices include a PGOOD comparator to monitor the status of output voltage and to enable/disable the downstream loads. The power good open-drain output requires an external pullup resistor and bias supply. The functionality of PGOOD is explained as follows.

1) PGOOD goes high when the output voltage exceeds the OUTUV rising threshold and the ($V_{IN}$ - $V_{OUT}$) < $V_{FA}$ condition is satisfied.
2) PGOOD goes low when the output voltage falls below the OUTUV falling threshold.
3) At system power-up, PGOOD remains high if $V_{OUT}$ > $V_{OUTUV}$ and ($V_{IN}$ - $V_{OUT}$) < $V_{FA}$; otherwise, it is low.

### Fault Output (FLAG)

The devices offer an open drain fault signal FLAG. The fault signal requires an external pullup resistor and bias supply. The FLAG pin is asserted low during the following fault conditions:

- Soft Start, when ($V_{IN}$ – $V_{OUT}$) > $V_{FA}$ at the end of $t_{STO}$.
- Overcurrent and short circuit conditions once the current limit exceeds $t_{BLANK}$ duration.
- Reverse current condition when Reverse Protection external nFET is turned OFF.
- Thermal Shutdown.
- Input UVLO.
- Input OVLO.

The FLAG will be deasserted once the above fault conditions observed by the device are cleared.

*Table 3* shows the status of the nFETs and the status of the fault signal under various operating conditions.

## Table 3. FETs Status During Faults

| CONDITION | EXTERNAL nFET STATUS | INTERNAL nFET STATUS | FLAG STATUS |
|---|---|---|---|
| EN Disabled | OFF | OFF | High |
| Normal Operation (No Fault) | ON | ON | High |
| Input UVLO | OFF | OFF | Low |
| Input OVLO | OFF | OFF | Low |
| Soft Start (During $I_{START}/t_{STO}$ period) | ON | ON | High |
| Output Overcurrent | ON | Regulate | Low (After $t_{BLANK}$) |
| Short Circuit | OFF | OFF | Low |
| Reverse current with No Other Fault | OFF | ON | Low |
| Over Voltage Clamp | ON | Regulate | High |
| Power Limit | ON | Regulate | High (Automatically low after $t_{BLANK}$ due to current regulation) |
| Loss of Ground | OFF | OFF | High |
| Output Undervoltage | ON | ON | High |
| Thermal Regulation | ON | Regulate | High (Automatically low after $t_{BLANK}$ due to current regulation) |
| Thermal Shutdown | OFF | OFF | Low |
| SETI Grounded (First Power ON) | OFF | OFF | Low |
| $(V_{IN}-V_{OUT}) > V_{FA}$ at the end of $t_{STO}$ (during startup) | OFF | OFF | Low |

### Linear Regulator ($V_{CC}$)

The MAX17617/MAX17617A has an internal low dropout (LDO) regulator that powers $V_{CC}$ from $V_{IN}$. This LDO is enabled during power-up or when EN is cycled. The typical $V_{CC}$ output voltage is 1.8V. Bypass $V_{CC}$ to GND with a 2.2µF low-ESR ceramic capacitor.

### Gate Driver for Reverse Protection External nFET

The devices offer an integrated gate driver circuit to drive the Reverse Protection external nFET. The gate drive is protected internally from accidental short circuits between the gate and source terminals. Connect a resistor from the $I_{START}$/CLMODE pin to GND to provide information about the presence of external nFET. The devices provide a gate drive (GN) of 6.5V (typ). The gate drive has passive resistive behavior across the gate and source terminals of external nFET when the device's operation is disabled by de-asserting the EN pin.

If the reverse protection function is not used, and the external nFET is not installed, connect SN and GN terminals to IN pins.

### Die Temperature Monitoring (PGOOD/$T_J$)

The devices offer a die temperature monitoring feature. Connect a 10kΩ ~ 20kΩ resistor from PGOOD/$T_J$ to GND to monitor the internal die temperature on the PGOOD/$T_J$ pin.

The PGOOD/$T_J$ pin provides 652mV at 25°C and 854mV at +125°C of die (hot spot) temperature, with a temperature slope of 2mV/°C. The die (hot spot) temperature is expressed using the following equation:

$$V_{TJ} = (T_{DIE} - 25℃) \times 2mV + 652mV$$

$$T_{DIE} = \frac{V_{TJ} - 652mV}{2mV} + 25℃$$

where,

$T_{DIE}$ is the die temperature,

$V_{TJ}$ is the voltage at the pin PGOOD/$T_J$.

### Thermal Shutdown Protection

The devices have a thermal-shutdown feature to protect against overheating, and a thermal foldback current limit control. When the junction temperature reaches 150°C (typ), the current limit is internally lowered to reduce the power dissipation on the internal nFET, and regulate the junction temperature at around 150°C. In extreme conditions, the devices turn off and assert the FLAG pin when the junction temperature exceeds +165°C (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools by 20°C (typ), except when in a latch-off mode, where the devices remain latched off.

### Power Limit

The devices feature a unique Power Limit feature that allows the set current limit to be modified automatically based on an external voltage ($V_{EXT}$). The devices monitor a fraction of this external voltage on the PLIM pin through a potential divider connected from $V_{EXT}$ to GND, and dynamically adjust the current limit based on the following relationship:

When $V_{PLIM} \leq V_{PLIMTH}$, the output current is limited to the $I_{LIM}$ value set by $R_{SETI}$.

When $V_{PLIM} > V_{PLIMTH}$, the output current limit is limited to = $\frac{I_{LIM} \times V_{PLIMTH}}{V_{PLIM}}$.

For a given external potential divider of ratio K formed by R5 and R6 in the *Typical Application Circuits*, the power delivered by the external voltage is given by the following expressions:

$$V_{PLIM} = V_{EXT} \times K$$

$$P = \frac{V_{EXT} \times I_{LIM} \times V_{PLIMTH}}{V_{PLIM}}$$

$$\text{Hence, } P = \frac{I_{LIM} \times V_{PLIMTH}}{K}$$

where, $I_{LIM}$, K, and $V_{PLIM\_TH}$ are essentially constants with tolerances dictated by the design.

The devices offer ±6% power limit accuracy for the range $V_{PLIMTH} < V_{PLIM} < 3 \times V_{PLIMTH}$, which covers a 3x variation of the external voltage ($V_{EXT}$).

Let's assume the design requirement of the output power limit (P) is 100W, and the current limit is 4A.

The resistor-divider ratio K is calculated as: $k = \frac{R_6}{R_6+R_5} = \frac{I_{LIM} \times V_{PLIM\_TH}}{P}$

Where, $V_{PLIM\_TH}$ = 0.3. Assuming R6 is 10kΩ, R5 is calculated to be 825kΩ.

In an input Power Limit application, $V_{SN}$ is equal to $V_{EXT}$, and the PLIM resistor divider is set to determine the Input voltage at which the current limit starts decreasing. By setting this voltage and setting the maximum current limit, the maximum "input-power limit" for the application is set. The current limit can also be dynamically modified based on the

output voltage by using $V_{OUT}$ equal to $V_{EXT}$. This feature implements an output-power limit function that potentially allows larger output currents to be delivered to charge the output reservoir capacitors at low output voltage conditions experienced after input power returns after an "outage," provided there are no thermal limitations due to excessive power dissipation. The power-limit feature is disabled by connecting the PLIM pin to GND. A simplified block diagram of the PLIM feature is shown in *Figure 28*. *Figure 29* shows the 100W Class 2 output-power limit response.

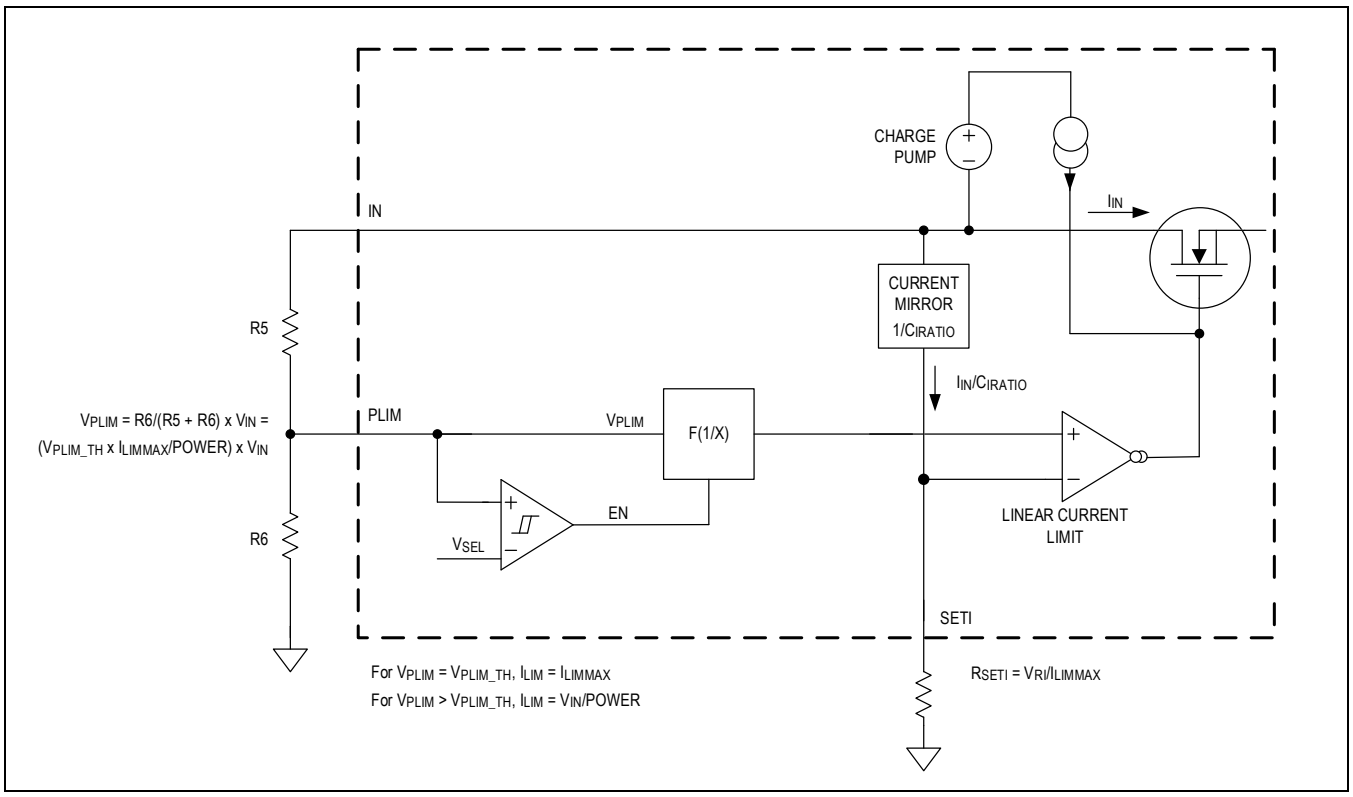



*Figure 28. Power Limit Circuit*

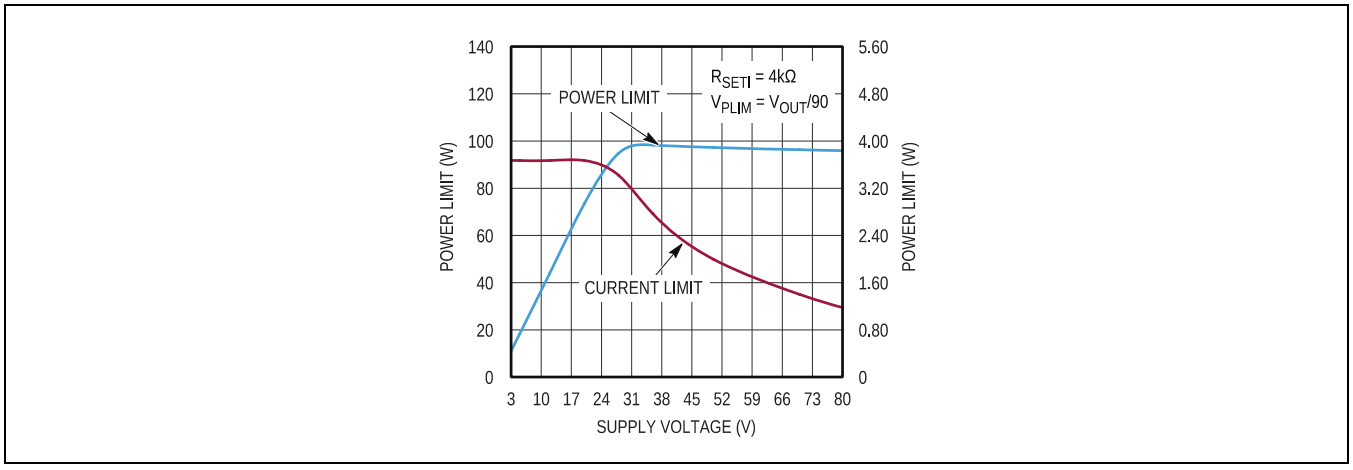



*Figure 29. 100W Class 2 Output Power Limit*

## Applications Information

### IN Capacitor

A 1µF capacitor from the IN pin to GND is recommended to hold input voltage during sudden load-current changes.

### Hot Plug-In at IN Terminal

In many powering applications, an input-filtering capacitor is required to lower the radiated emission and enhance the ESD capability. In hot plug-in applications, parasitic cable inductance, and the input capacitor cause overshooting and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that can limit surge voltage to a maximum of 80V shall be placed close to the input terminals for enhanced protection.

### Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The device detects reverse current entering at the OUT pin and flowing out of the IN pin, and turns off the external nFET. The magnitude of the reverse current depends on the inductance of the input circuitry and any capacitance installed near the IN pins.

### Voltage Interruption Response

MAX17617/MAX17617A features fast recovery after voltage interruption during input-supply brownout tests. The device takes 150µs (typ) to turn on the internal nFET and 100µs (typ) to start turning on the external nFET when recovering from a brownout fault. *Figure 30* illustrates the performance of voltage interruption and recovery response.

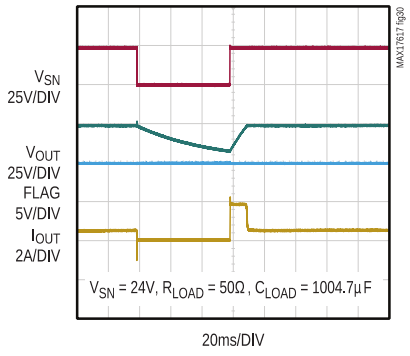



*Figure 30. Voltage Interruption Response*

### OUT Capacitor

The maximum capacitive load ($C_{MAX}$) that can be connected is a function of the current-limit setting ($I_{LIM}$ in A), the startup timeout ($t_{STO}$ in ms), and the input voltage ($V_{SN}$). The $C_{MAX}$ is calculated using the following equation:

$$C_{MAX}\ (mF) = \frac{I_{LIM} \times t_{STO}}{V_{SN}}$$

For example, for $V_{SN}$ = 24V, $t_{STO}$ (typ) = 1200ms, and $I_{LIM}$ = 1A, $C_{MAX}$ is 50mF.

Output capacitor values over $C_{MAX}$ can trigger false overcurrent conditions. Note that the above equation assumes that no-load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current, resulting in a large charging period and, hence, the possibility of a false overcurrent condition.

In practical applications, the $C_{MAX}$ value is limited by the thermal performance of the Printed Circuit Board (PCB). Poor thermal design can cause the thermal foldback current-limiting function of the device to kick in too early, which can further limit the maximum capacitance that can be charged. Therefore, a good thermal PCB design is imperative for charging large capacitor banks.

### Hot Plug-In at OUT Terminal

In some applications, an external voltage at the OUT terminal of the devices can be applied with or without the presence of an input voltage. During these conditions, the devices detect any reverse current entering the OUT pin, flowing out of the IN pin, and turn off the external nFET. Parasitic cable inductance, along with input and output capacitors, causes overshooting and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the *Absolute Maximum Ratings*.

### OUT Clamping Diode for inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, an output clamp is recommended. This clamp can be implemented with a TVS, and a diode, as shown in the *Typical Application Circuits*. This is required to clamp the negative spike on the OUT pin due to the inductive kickback during an output short-circuit event within the safe operating region. The maximum negative clamping voltage of the TVS for a maximum input voltage of $V_{INMAX}$ is limited to (80 – $V_{INMAX}$) V to ensure IN to OUT pin voltage does not exceed 80V.

### Layout and Thermal Dissipation

Place input and output capacitors as close as possible to the device. The IN and OUT pins must be connected with wide, short traces to the power bus. During normal operation, the power dissipation is small, and the package temperature change is minimal.

Power dissipation under steady-state normal operation may be calculated as:

$$P_{SS} = I_{OUT}^2 \times R_{ON}$$

See the *Electrical Characteristics Table* and *Typical Operating Characteristics* for $R_{ON}$ values at various operating temperatures. Thermal vias from the exposed pad to the ground plane should be used to provide adequate heatsinking to internal ground planes.

### ESD Protection

No capacitor is required for ±2kV (type) (HBM) ESD on IN. All pins have ±2kV (HBM) ESD protection. In applications in which an external nFET is used, see the IN Capacitor section.

*Figure 31* shows the Human Body Model and *Figure 32* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

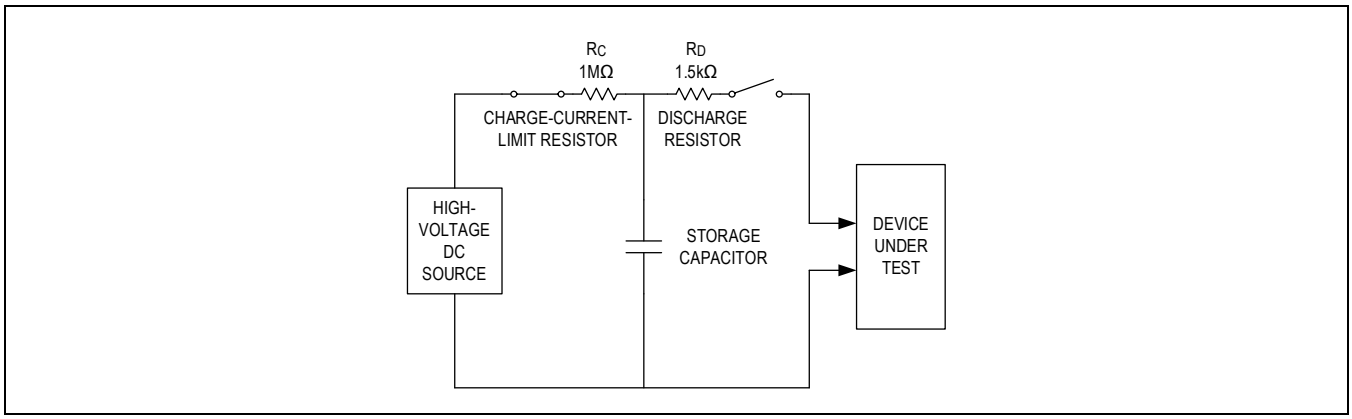



*Figure 31. Human Body ESD Test Model*

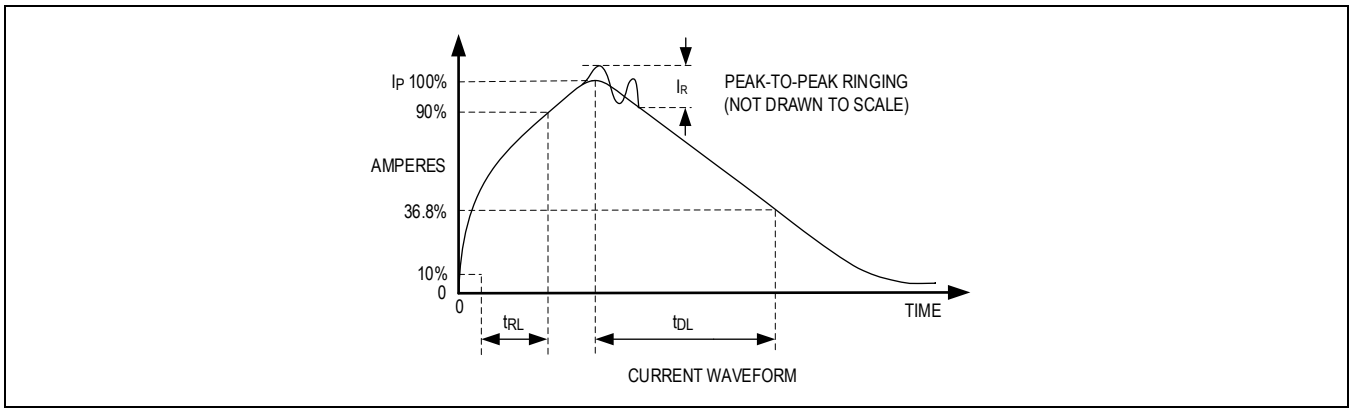
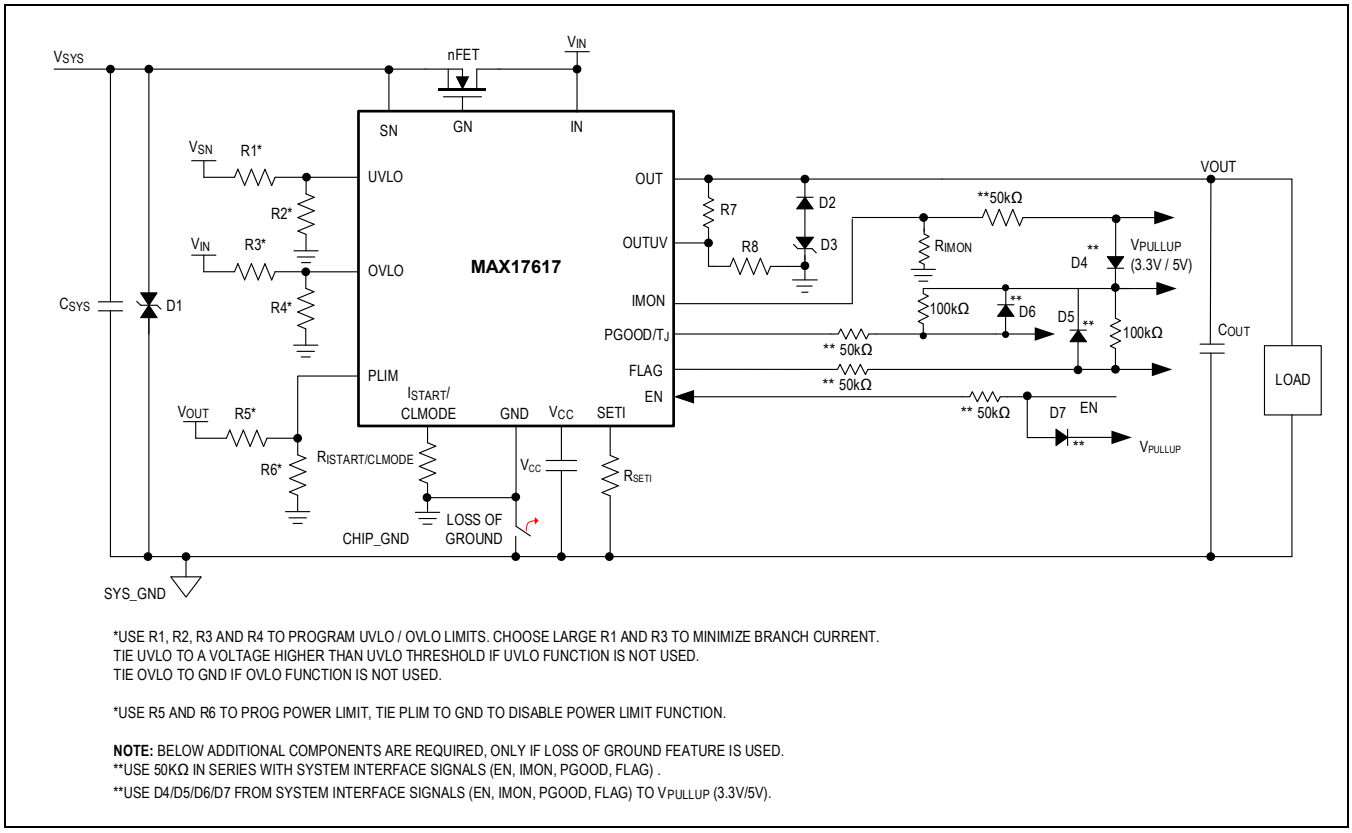



*Figure 32. Human Body Current Waveform*

## Typical Application Circuits

### MAX17617 Application Circuit




*USE R1, R2, R3 AND R4 TO PROGRAM UVLO / OVLO LIMITS. CHOOSE LARGE R1 AND R3 TO MINIMIZE BRANCH CURRENT.
TIE UVLO TO A VOLTAGE HIGHER THAN UVLO THRESHOLD IF UVLO FUNCTION IS NOT USED.
TIE OVLO TO GND IF OVLO FUNCTION IS NOT USED.

*USE R5 AND R6 TO PROG POWER LIMIT, TIE PLIM TO GND TO DISABLE POWER LIMIT FUNCTION.

**NOTE:** BELOW ADDITIONAL COMPONENTS ARE REQUIRED, ONLY IF LOSS OF GROUND FEATURE IS USED.
**USE 50KΩ IN SERIES WITH SYSTEM INTERFACE SIGNALS (EN, IMON, PGOOD, FLAG) .
**USE D4/D5/D6/D7 FROM SYSTEM INTERFACE SIGNALS (EN, IMON, PGOOD, FLAG) TO $V_{PULLUP}$ (3.3V/5V).

## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE | FEATURES |
|---|---|---|---|
| MAX17617AFD+ | -40°C to +125°C | 23-Pin FCQFN | OVLO |
| MAX17617AFD+T | -40°C to +125°C | 23-Pin FCQFN | OVLO |
| MAX17617AAFD+ | -40°C to +125°C | 23-Pin FCQFN | OVFB |
| MAX17617AAFD+T | -40°C to +125°C | 23-Pin FCQFN | OVFB |

*+Denotes a lead (Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/25 | Initial release | — |