42V Dual Input, Low Noise 150mA Step-Down µModule Regulator with I²C Battery Health Monitor

FEATURES

- Seamless and Automatic Transition between Two Input Power Sources
- Integrated Battery Health Monitor
- Wide Voltage Range for Dual Inputs: 2.4V to 42V
- Battery Health Monitor Input Voltage: 1.8V to 5.5V
- Adjustable Output Range: 1V to 4.2V
- Up to 150mA Continuous Output Current
- Integrated Low-Dropout Linear Regulator: 195mV at 150mA Load for Low Output Noise
- 200kHz to 2.2MHz Switching Frequency
- Synchronization to an External Clock
- Current Mode Control With 60ns Minimum On-time
- Burst Mode® Operation, I_Q = 18.5µA
- Programmable Input UVLO Thresholds and Discharge Alarm with Interrupt Output
- Input Valid, Priority Channel, and PG Indicators
- Available in a Compact *64-Pin BGA, 7mm × 7mm × 1.85mm* Package

APPLICATIONS

- Portable Battery-Powered Devices
- Radio, Healthcare, and Industrial Test Equipment
- Uninterruptible Power Supplies

GENERAL DESCRIPTION

The *LTM4719* is a 42V dual input, 150mA synchronous buck power µModule® (micromodule) regulator with an integrated battery health monitor interfaced through I²C. The ultralow quiescent current post-regulation linear regulator draws 560nA (typical) at no load and a 42µA (typical) at full load, which is ideal for battery-operated portable equipment.

The LTM4719 supports seamless transition between two separate input power sources if one of the inputs is lost. The automatic switchover eliminates the need for holdup capacitors and minimizes disturbances on the output rail. The 18.5µA Burst Mode operation quiescent current makes the LTM4719 compatible with many applications.

The LTM4719 has a built-in precision coulomb counter (Q) accessible through an I²C interface. A discharge alarm threshold can be programmed. When the threshold is reached, an interrupt signal is generated at the $\overline{IRQ}$ pin. Battery voltage (V), battery impedance (Z), and temperature (T) are accessible through I²C. Fault protection features include input undervoltage lockout (UVLO), power good (PG), current limit, and overtemperature (OV) protection.

TYPICAL APPLICATION

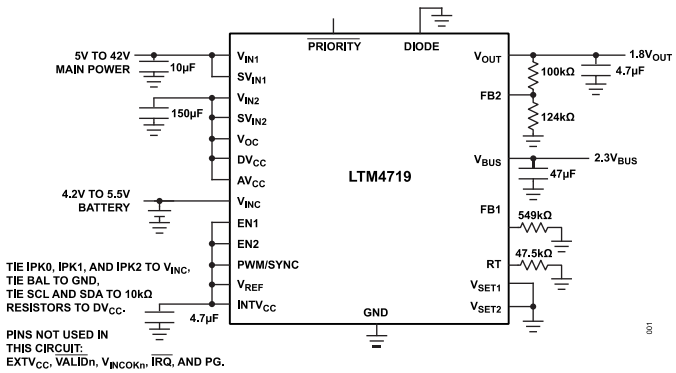

Figure 1. 700kHz, 1.8V, 150mA Supply from Main Power and Backup Battery

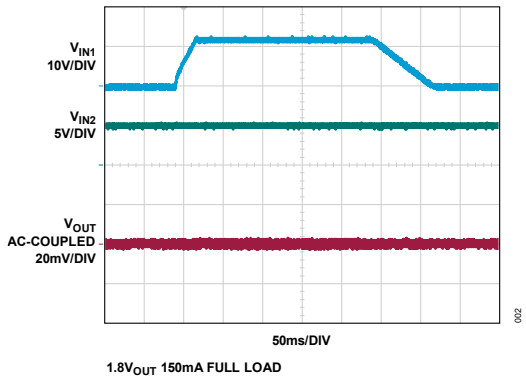

Figure 2. Switchover to Battery Power

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REVISION HISTORY

01/2025 - Rev. 0, Initial Release.

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Dual Input Buck Switching Regulator							
Input voltage of power source	V_{IN}	After startup	–40°C ≤ T_J ≤ 125°C	2.4		42	V
V_{IN1}, V_{IN2} UVLO threshold	V_{UVLO}	Rising	–40°C ≤ T_J ≤ 125°C		2.4	2.6	V
		Falling	–40°C ≤ T_J ≤ 125°C	1.85	2.0	2.4	
SV_{IN1} current in disable	$I_{SVIN1(SD)}$	EN1/EN2 low, V_{IN1} = 24V, V_{IN2} = 12V[5]			1.35		µA
		EN1/EN2 low, V_{IN1} = 12V, V_{IN2} = 24V[5]			0.55		
SV_{IN2} current in disable	$I_{SVIN2(SD)}$	EN1/EN2 low, V_{IN2} = 24V, V_{IN1} = 12V[5]			1.35		µA
		EN1/EN2 low, V_{IN2} = 12V, V_{IN1} = 24V[5]			0.55		
SV_{IN1} current, operating from SV_{IN2}		EN1/EN2 high, buck operating, V_{IN1} = 24V, V_{IN2} = 27V[5]			0.7		µA
SV_{IN2} current, operating from SV_{IN1}		EN1/EN2 high, buck operating, V_{IN2} = 24V, V_{IN1} = 27V[5]			0.7		µA
Burst Mode operation quiescent current from SV_{IN1}	I_{Q_BURST}	EN1/EN2 is high, PWM/SYNC is low[5]			18.5		µA
Oscillator frequency	f_{OSC}	Programmable frequency		200		2200	kHz
		R_T resistor = 33.2kΩ	–40°C ≤ T_J ≤ 125°C	900	1000	1100	
PWM/SYNC applied clock frequency	f_{SYNC}			200		2200	kHz
Logic input threshold (EN1, diode)		V_{IN1} = SV_{IN1} = 12V, V_{IN2} = SV_{IN2} = 24V	–40°C ≤ T_J ≤ 125°C	0.3	0.8	1.1	V
V_{BUS} voltage accuracy	V_{BUS}	No load	–40°C ≤ T_J ≤ 125°C	2.262	2.3	2.350	V
V_{BUS} line regulation	$V_{LINEREG\_BUS}$	V_{IN1}, V_{IN2} = 2.4V to 42V, no load			0.05		%
V_{BUS} load regulation	$V_{LOADREG\_BUS}$	I_{BUS} = 0A to 150mA, apply load from V_{BUS} to GND			0.1		%
Feedback voltage	V_{FB1}	–40°C ≤ T_J ≤ 125°C		804	818	832	mV
Soft start duration	t_{SS}				5.5		ms
PG threshold		V_{FB1} overvoltage rising			10		%
		V_{FB1} undervoltage falling			–9		

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{REF} voltage	V_{REF}			0.995	1	1.005	V
		–40°C ≤ T_J ≤ 125°C		0.982	1	1.018	
V_{IN1}, V_{IN2} input valid threshold, rising	V_{IH}	V_{SET1} = V_{SET2} = 1000mV	–40°C ≤ T_J ≤ 125°C	20.0	20.15	20.4	V
		V_{SET1} = V_{SET2} = 500mV	–40°C ≤ T_J ≤ 125°C	10.0	10.15	10.3	
		V_{SET1} = V_{SET2} = 250mV	–40°C ≤ T_J ≤ 125°C	5.0	5.1	5.3	
		V_{SET1} = V_{SET2} = 150mV	–40°C ≤ T_J ≤ 125°C	3.0	3.1	3.2	
V_{IN1}, V_{IN2} input valid threshold, falling	V_{IL}	V_{SET1} = V_{SET2} = 1000mV	–40°C ≤ T_J ≤ 125°C	17.4	17.6	17.8	V
		V_{SET1} = V_{SET2} = 500mV	–40°C ≤ T_J ≤ 125°C	8.6	8.75	8.8	
		V_{SET1} = V_{SET2} = 250mV	–40°C ≤ T_J ≤ 125°C	4.2	4.3	4.4	
		V_{SET1} = V_{SET2} = 150mV	–40°C ≤ T_J ≤ 125°C	2.45	2.55	2.65	
V_{IN1}, V_{IN2} input valid threshold hysteresis		As a percentage of the rising threshold		12		20	%
Open-drain leakage	$I_{LEAKAGE}$	PG, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$				1	µA
$INTV_{CC}$ voltage	V_{INTVCC}			4.12	4.22	4.32	V
$INTV_{CC}$ dropout voltage	V_{DO_INTVCC}	Powered from V_{IN1} or V_{IN2}, V_{IN} = 2.4V, I_{LOAD} = 5mA			70		mV
		Powered from $EXTV_{CC}$, $EXTV_{CC}$ = 3.3V, I_{LOAD} = 5mA			100		
$INTV_{CC}$ load regulation	V_{LR_INTVCC}	I_{LOAD} = 1mA to 15mA			1.1		%
$EXTV_{CC}$ applied voltage range	V_{EXTVCC}			3.15		42	V
$EXTV_{CC}$ valid, rising threshold		-40°C ≤ T_J ≤ 125°C		2.95	3.05	3.15	V
$EXTV_{CC}$ valid, hysteresis					220		mV
SW minimum on-time	$t_{ON(MIN)}$	V_{IN} = 24V, 0.15A load, $EXTV_{CC}$ = open[5]			46		ns

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
SW minimum off-time	$t_{OFF(MIN)}$	[5]			100		ns
Post Regulation LDO Regulator							
V_{BUS} input voltage range	V_{BUS}	–40°C ≤ T_J ≤ 125°C		2.2		5.5	V
V_{OUT} output voltage accuracy	V_{OUT}	100µA < I_{OUT} < 150mA, V_{BUS} = 2.2V to 5.5V		1.764	1.8	1.83	V
			–40°C ≤ T_J ≤ 125°C	1.730		1.863	
Feedback voltage FB2	V_{FB2}	100µA < I_{OUT} < 150mA, V_{BUS} = 2.2V to 5.5V		0.98		1.02	V
			–40°C ≤ T_J ≤ 125°C	0.97		1.03	
Line regulation	$V_{LINEREG}$	V_{BUS} = 2.2V to 5.5V, I_{OUT} = 10mA	–40°C ≤ T_J ≤ 125°C	–0.1		0.1	%/V
Load regulation	$V_{LOADREG}$	I_{OUT} = 100µA to 150mA	–40°C ≤ T_J ≤ 125°C		0.6	1.5	%
Dropout voltage	V_{DO}	V_{OUT} = 3.3V, I_{OUT} = 10mA			8	10	mV
		V_{OUT} = 3.3V, I_{OUT} = 150mA	–40°C ≤ T_J ≤ 125°C		120	225	
Start-up time	$t_{START-UP}$	V_{OUT} = 3.3V			1100		µs
Current limit threshold	I_{LIM}			220	320	500	mA
Thermal shutdown threshold		Temperature rising			150		°C
Thermal shutdown hysteresis		Temperature rising			15		°C
EN2 input logic high	V_{IH_EN2}	2.2V ≤ V_{BUS} ≤ 5.5V		0.88		1.28	V
EN2 input logic low	V_{IL_EN2}	2.2V ≤ V_{BUS} ≤ 5.5V		0.34		0.76	V
EN2 input leakage current	$I_{LEAKAGE\_EN2}$	EN2 = 2.3V	–40°C ≤ T_J ≤ 125°C		0.1	1	µA
V_{BUS} input voltage UVLO	V_{UVLO_BUS}	Rising				2.19	V
		Falling		1.65			
		Hysteresis			300		mV

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Output noise	$V_{RMS(OUT)}$	10Hz to 100kHz RMS noise, V_{BUS} = 5V, V_{OUT} = 3.3V			105		µV
		10Hz to 100kHz RMS noise, V_{BUS} = 5V, V_{OUT} = 2.5V			100		
		10Hz to 100kHz RMS noise, V_{BUS}= 5V, V_{OUT} = 1.2V			80		
Battery Health Monitor Section							
Input voltage range (V_{INC})	V_{INC}	[2]	–40°C ≤ T_J ≤ 125°C	2.0		5.5	V
AV_{CC} voltage range	V_{AVCC}	–40°C ≤ T_J ≤ 125°C		1.8		5.5	V
Coulomb Counter							
Input current into V_{INC}	I_{INC}	V_{INC} – V_{OC} = 50mV			0		nA
		V_{INC} – V_{OC} = 175mV (current source turned on), 100mA I_{PEAK} setting		90	100	110	mA
			–40°C ≤ T_J ≤ 125°C	85	100	115	
		V_{INC} – V_{OC} = 175mV (current source turned on), 75mA I_{PEAK} setting		67.5	75	82.5	
			–40°C ≤ T_J ≤ 125°C	65	75	85	
		V_{INC} – V_{OC} = 175mV (current source turned on), 50mA I_{PEAK} setting		45	50	55	
			–40°C ≤ T_J ≤ 125°C	43	50	57	
		V_{INC} – V_{OC} = 175mV (current source turned on), 25mA I_{PEAK} setting		22.5	25	27.5	
			–40°C ≤ T_J ≤ 125°C	21.5	25	28.5	

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
		V_{INC} – V_{OC} = 175mV (current source turned on), 20mA I_{PEAK} setting		18	20	22	
			–40°C ≤ T_J ≤ 125°C	17	20	23	
		V_{INC} – V_{OC} = 175mV (current source turned on), 15mA I_{PEAK} setting		13.5	15	16.5	
			–40°C ≤ T_J ≤ 125°C	13	15	17	
		V_{INC} – V_{OC} = 175mV (current source turned on), 10mA I_{PEAK} setting		9	10	11	
			–40°C ≤ T_J ≤ 125°C	8.5	10	11.5	
		V_{INC} – V_{OC} = 175mV (current source turned on), 5mA I_{PEAK} setting		4.5	5	5.5	
			–40°C ≤ T_J ≤ 125°C	4.2	5	5.8	
		Startup: V_{OC} = 0V, 25mA/50mA/75mA/100mA I_{PEAK} setting			25		
		Startup: V_{OC} = 0V, 5mA to 20mA I_{PEAK} setting			5		
AV_{CC} pin input quiescent current	I_{Q_AVCC}	V_{INC} – V_{OC} = 50mV, I_{PEAK} = 100mA			100	160	nA
q_{LSB} (for prescaler setting M = 0)[3, 4]	Q_{LSB}	100mA I_{PEAK} setting			14.91		mA × hr
		75mA I_{PEAK} setting			11.18		
		50mA I_{PEAK} setting			7.457		
		25mA I I_{PEAK} setting			3.728		
		20mA I_{PEAK} setting			2.983		
		15mA I_{PEAK} setting			2.237		
		10mA I_{PEAK} setting			1.491		
		5mA I_{PEAK} setting			745.7		µA × hr

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Full-scale coulomb count (battery capacity)		5mA I_{PEAK} setting, M = 15 (smallest battery)			1.491		mA × hr
		100mA I_{PEAK} setting, M = 0 (largest battery)	-40°C ≤ T_J ≤ 125°C	928.5	977.3	1026	A × hr
Total coulomb counter error[4]				–3		3	%
		-40°C ≤ T_J ≤ 125°C		–5		5	
Coulomb counter turn-on threshold		(V_{INC} – V_{OC}), V_{OC} rising			0.6		V
Coulomb counter turn-off threshold		(V_{INC} – V_{OC}), V_{OC} falling			1.2		V
V_{INCOK} Threshold	V_{INCOK}	(V_{INC} – V_{OC}), V_{OC} rising	–40°C ≤ T_J ≤ 125°C	90	120	170	mV
		(V_{INC} – V_{OC}), V_{OC} falling	–40°C ≤ T_J ≤ 125°C	375	400	425	
I_{PEAK} turn-off threshold (V_{OC_HIGH})		(V_{INC} – V_{OC}), V_{OC} rising	–40°C ≤ T_J ≤ 125°C	90	120	170	mV
I_{PEAK} turn-on threshold (V_{OC_LOW})		(V_{INC} – V_{OC}), V_{OC} falling	–40°C ≤ T_J ≤ 125°C	140	160	250	mV
V_{OC} hysteresis	V_{HYST_OC}	V_{HYST_OC} = V_{OC_LOW} – V_{OC_HIGH}			70		mV
Voltage Monitor							
V_{LSB}	V_{LSB}				1.465		mV
Total voltage error		BATT = 2V		–1.5		1.5	%
			–40°C ≤ T_J ≤ 125°C	–2.5		2.5	
Full-scale voltage (111111111111 code)					6		V
Zero voltage (000000000000 code)					0		V
Temperature Monitor							
T_{LSB}					0.784		°C
Code for room temperature 25°C				–5LSB	010101 01	5LSB	
Full-scale temperature (11111111 code)					159		°C

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Zero-scale temperature (00000000 code)					–41		°C
Hot die temperature warning threshold (die temperature that causes $\overline{IRQ}$ = 0)		00000000 code for register bits H[15:8]			–41		°C
		11111111 code for register bits H[15:8] (default)			159		
Cold die temperature warning threshold (die temperature that causes $\overline{IRQ}$ = 0)		00000000 code for register bits H[7:0] (default)			–41		°C
		11111111 code for register bits H[7:0]			159		
Supercapacitor Balancer							
V_{SCAP} (V_{OC} pin)	V_{SCAP}	Supercapacitor balancer input range	–40°C ≤ T_J ≤ 125°C	2.5		5.5	V
I_{SCAP} (V_{OC} pin)	I_{SCAP}	Supercapacitor balancer quiescent current, V_{OC} = 5V, I_{BAL} = 0			200	400	nA
Supercapacitor balancer max source current		V_{OC} = 5V, V_{BAL} = 2.4V		10			mA
Supercapacitor balancer max sink current		V_{OC} = 5V, V_{BAL} = 2.6V				–10	mA
Supercapacitor balance point (V_{BAL})	V_{BAL}	Percentage of V_{OC} voltage	–40°C ≤ T_J ≤ 125°C	49	50	51	%
Digital Inputs and Outputs							
DV_{CC} voltage range	DV_{CC}	–40°C ≤ T_J ≤ 125°C		1.8		5.5	V
Digital input high voltage	DV_{IH}	For pins IPK[2:0]	–40°C ≤ T_J ≤ 125°C	V_{INC} – 0.5			V
		For pins SDA, SCL	–40°C ≤ T_J ≤ 125°C	70			%DV_{CC}
Digital input low voltage	DV_{IL}	For pins IPK[2:0]	–40°C ≤ T_J ≤ 125°C			0.5	V
		For pins SDA, SCL	–40°C ≤ T_J ≤ 125°C			30	%DV_{CC}

(T_A = 25°C, V_{IN1} = SV_{IN1} = 24V, V_{IN2} = SV_{IN2} = 12V, V_{INC} = V_{OC} = AV_{CC} = DV_{CC} = 3.6V, V_{SET1} = V_{SET2} = GND, V_{BUS} = 2.3V, V_{OUT} = 1.8V, EN2 = V_{BUS}, C_{OUT} = 1µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Digital input high current	DI_{IH}	For pins IPK[2:0]			10	nA
		For pins SDA, SCL			10	
Digital input low current	DI_{IL}	For pins IPK[2:0]			10	nA
		For pins SDA, SCL			10	
Digital output high voltage	DV_{OH}	For pins $\overline{IRQ}$, V_{INCOK}; 1µA out of pin	DV_{CC} – 0.5			V
Digital output low voltage	DV_{OL}	For pins $\overline{IRQ}$, V_{INCOK}; 1µA into pin			0.5	V
		For pin SDA; 3mA into pin			0.4	
I^2C Timing Characteristics (See *Figure 3*)						
I^2C read address				110010 01		
I^2C write address				110010 00		
Clock operating frequency	f_{SCL}				400	kHz
Bus free time between STOP/START	t_{BUF}		1.3			µs
Repeated START setup time	$t_{SU(STA)}$		600			ns
Hold time (repeated) START condition	$t_{HD(STA)}$		600			ns
Setup time for STOP condition	$t_{SU(STO)}$		600			ns
Data setup time (input)	$t_{SU(DAT)}$		100			ns
Data hold time (input)	$t_{HD(DATI)}$		0			µs
Data hold time (output)	$t_{HD(DAT0)}$		0		0.9	µs
Clock/data fall time	t_f		20		300	ns
Clock/data rise time	t_r		20		300	ns
Clock low period	t_{LOW}		1.3			µs
Clock high period	t_{HIGH}		0.6			µs
Spike suppression time	t_{SP}				50	ns

[1] The LTM4719 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4719E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specification over the –40°C to 125°C operation junction temperature range is assured by design, characterization, and correlation with statistical process controls. The LTM4719I specifications are guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by the specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

[2] Coulomb counter and peak current limit accuracy is at its best for V_{INC} voltages above 2V. The voltage and temperature monitor accuracy are at their best down to 1.8V.

[3] The equivalent charge of a least-significant bit (LSB) in the accumulated charge register depends on the I_{PEAK} setting and the internal pre-scaling factor M. Note that 1mA × hr = 3.6A × s = 3.6C

[4] The specified accuracy of q_{LSB} in percent is better than that of the corresponding I_{PEAK} because the time base used for calculating coulombs is internally adjusted to compensate for errors in the actual I_{PEAK} value. The total coulomb counter error specified includes any inaccuracy in q_{LSB}.

[5] Data tested on the bench.

Timing Diagram

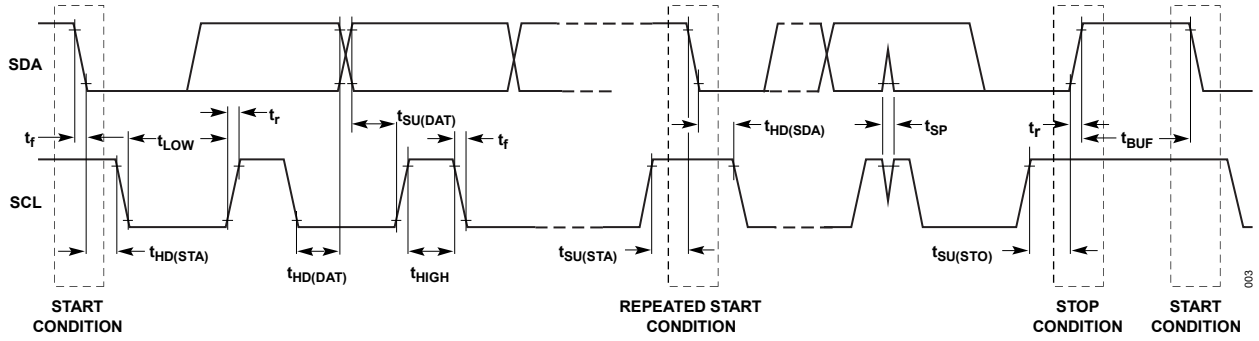


Figure 3. Definition of Timing on I²C Bus

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN1}, V_{IN2}, SV_{IN1}, SV_{IN2}, SW	–0.3V to 42V
$EXTV_{CC}$	–0.3V to 42V
$INTV_{CC}$	–0.3V to 6V
V_{REF}, V_{SET1}, V_{SET2}, FB1, RT	–0.3V to 6V
PWM/SYNC, DIODE, EN1	–0.3V to 6V
$\overline{VALID1}$, $\overline{VALID2}$, PG, $\overline{PRIORITY}$	–0.3V to 6V
V_{INC}, V_{OC}, AV_{CC}	–0.3V to 6V
(V_{INC} – V_{OC})	0.3V
SDA, SCL, DV_{CC}	–0.3V to 6V
IPK[2:0]	–0.3 to [lesser of (V_{INC} + 0.3V) or 6V]
V_{BAL}	–0.3 to [lesser of (V_{OC} + 0.3V) or 6V]
V_{BUS}	–0.3V to 6V
V_{OUT}, EN2, FB2	–0.3 to V_{BUS} (V)
$\overline{IRQ}$, V_{INCOK} current	±1mA
Operating junction temperature (I-grade)	–40°C to 125°C
Storage temperature range	–55°C to 125°C
Maximum reflow (package body) temperature	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD-protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 3. LTM4719 ESD Ratings

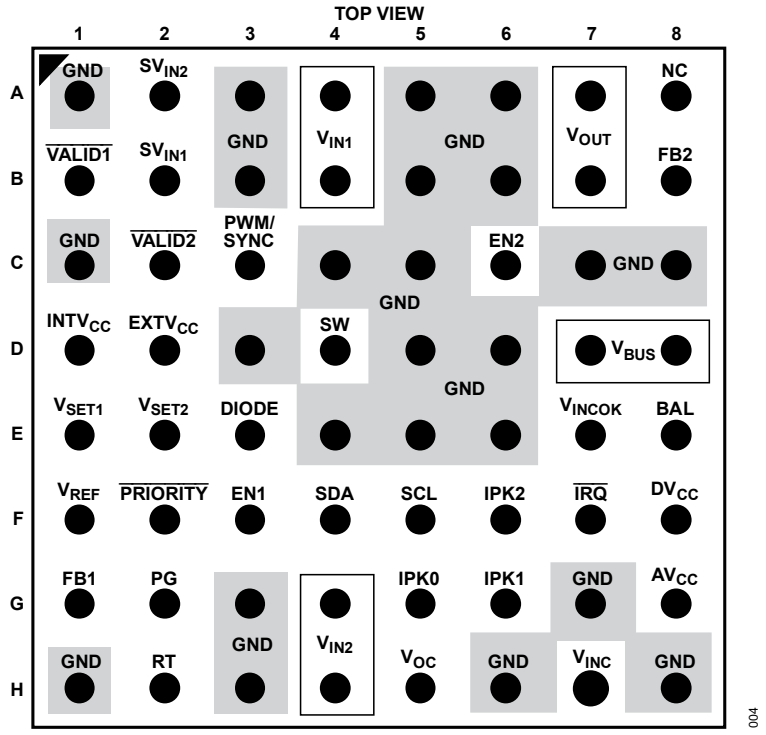
ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Pin Configuration



BGA PACKAGE
64-PIN (7mm × 7mm × 1.85mm)
T_{JMAX} = 125°C, θ_{JCtop} = 22.1°C/W, $\theta_{JCbottom}$ = 6.2°C/W, θ_{JA} = 17.1°C/W,
θ VALUES DEFINED PER JESD5112, WEIGHT = 210mg (TYPICAL)

θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
SEE THE APPLICATIONS INFORMATION SECTION FOR LAB MEASUREMENT DERATING INFORMATION.

Figure 4. 64-Pin BGA Pin Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Functions

Table 4. Pin Functions Description

PIN	NAME	DESCRIPTION
A1, C1, H1, A3, B3, D3, G3, H3, C4, E4, A5-E5, A6, B6, D6, E6, H6, C7, G7, C8, H8	GND	Power Ground Connections. These pins must be connected to ground in the application.
A2	SV_{IN2}	Secondary Power Source Kelvin Connection. This pin has been internally bypassed with a 0.1µF ceramic capacitor to ground. The SV_{IN2} pin must be connected to V_{IN2} in the application.
A4, B4	V_{IN1}	Priority Power Source Input for the Buck Converter. In priority mode (DIODE pin low), the buck converter will preferentially operate from this input if both input power sources are valid (above their respective UVLO thresholds). This pin must be bypassed with a 4.7µF or larger ceramic capacitor to ground. If the V_{IN1} input is subjected to inductive shorts to ground, then a power Schottky diode must be added from ground to V_{IN1} to prevent this pin from being driven below ground.
A7, B7	V_{OUT}	Regulated Output Voltage. These pins supply power to the load. Bypass V_{OUT} to GND with a capacitor, at least 1µF.
A8	NC	Do Not Connect. Leave this pin floating.
B1, C2	$\overline{VALID1}$ and $\overline{VALID2}$	Open-drain outputs indicating whether the V_{IN1} and V_{IN2} Inputs are valid. When the part is enabled (EN1 is high), $\overline{VALID1}$ and $\overline{VALID2}$ are driven low if the voltage at the V_{IN1} or V_{IN2} input is above the UVLO threshold set by the respective V_{SET1} or V_{SET2} pin. When the part is disabled (EN1 is low) the $\overline{VALID1}$ and $\overline{VALID2}$ pull-downs are disabled allowing the pins to float. The maximum voltage that can be applied to the $\overline{VALID1}$ and $\overline{VALID2}$ pins is 5.5V.
B2	SV_{IN1}	Priority Power Source Kelvin Connection. This pin has been internally bypassed with a 0.1µF ceramic capacitor to ground. The SV_{IN1} pin must be connected to V_{IN1} in the application.
B8	FB2	Feedback Voltage Input of the Post-Regulation Linear Regulator. Connect this pin to the midpoint of the voltage divider from V_{OUT} to GND to set the output voltage.
C3	PWM/SYNC	Pulse-width modulation (PWM)/Burst Mode Operation Control and External Synchronization Clock Input. Forcing this pin high causes the buck converter to operate in PWM mode. In PWM mode, the converter maintains fixed frequency operation at heavy load, leaving fixed frequency operation only at extremely light loads where the converter skips pulses to maintain regulation. Forcing the PWM/SYNC pin low causes the IC to utilize Burst Mode operation at light loads and automatically

		transition to PWM mode at higher load current. Burst Mode operation improves light load efficiency and significantly reduces no-load input quiescent current at the expense of modestly increased output voltage ripple. In addition, an external clock can be applied to the PWM/ SYNC pin for synchronization purposes. When synchronized to an external clock, the buck converter operates in PWM mode (Burst Mode operation is disabled).
C6	EN2	Enable Input of Post-Regulation Linear Regulator. Drive EN2 high to turn on the linear regulator; drive EN2 low to turn off the linear regulator. For automatic startup, connect EN2 to $INTV_{CC}$.
D1	$INTV_{CC}$	Internal Linear Regulator Output and Power Supply for the Low Voltage Control Circuitry in the IC. Internal linear regulators generate a regulated voltage on these pins from either SV_{IN1}, SV_{IN2}, or $EXTV_{CC}$. A 4.7µF or larger bypass capacitor must be connected between these pins and ground. The $INTV_{CC}$ rail remains powered in shutdown and can be used to supply up to 1mA to external loads.
D2	$EXTV_{CC}$	$INTV_{CC}$ Regulator Bootstrapping Pin. If this pin is forced to 3.15V or greater then $EXTV_{CC}$ will be used to power the internal $INTV_{CC}$ rail. Typically, the $EXTV_{CC}$ input is connected to the buck converter output voltage. Bootstrapping the $INTV_{CC}$ rail in this fashion provides a significant efficiency advantage and reduced quiescent current especially in applications with high input voltage and low output voltage. If the $EXTV_{CC}$ pin is left open, then the $INTV_{CC}$ rail will be powered from the SV_{IN1} and SV_{IN2} pins.
D4	SW	Switching Node. This pin is used for testing purposes.
D7, D8	V_{BUS}	Bus Voltage. This is the output of the dual-input Buck and the input of the post-regulation linear regulator. Bypass V_{BUS} to GND with at least 22µF capacitor.
E1, E2	V_{SET1}, V_{SET2}	Programming Pins for the UVLO thresholds on V_{IN1} and V_{IN2}. The voltage on the V_{SET1} and V_{SET2} pins programs the UVLO threshold for the power source inputs V_{IN1} and V_{IN2}, respectively. A voltage between 0V and 1V programs a corresponding UVLO threshold between 0V and 20V. However, there is also a fixed internal UVLO threshold (typically 2.34V) on each input which is always in effect. The voltage on V_{SET1} and V_{SET2} can be set using a resistor divider from the accurate reference output, V_{REF}. Grounding V_{SET1} and V_{SET2} will allow the respective inputs V_{IN1} and V_{IN2} to be used down to the fixed, internal UVLO threshold.
E3	DIODE	Logic Input Used to Select Between Ideal Diode-OR and Priority Modes. The integrated power path allows operation from either of two input power sources, V_{IN1} or V_{IN2}. An input is considered valid for use only if its voltage is above the UVLO threshold for that input as programmed by the respective voltage at the V_{SET1} or V_{SET2} pin. If DIODE is high, then the part operates in ideal-diode mode, and the buck converter will operate from the highest voltage valid input (V_{IN1} or V_{IN2}). If DIODE is low, then the part operates in priority mode, and the buck converter will operate from V_{IN1} whenever it is valid and will switch to V_{IN2} only if V_{IN1} becomes invalid. In either mode, if both inputs are under voltage, then the buck converter will be disabled.
E7	V_{INCOK}	V_{INCOK} Comparator Output. Logic level output referenced to DV_{CC}. This pin is logic high when the V_{OC} pin is high and in its normal operating range where the coulomb counter operates properly.

E8	BAL	Supercapacitor Balance Point. The common node of a stack of two supercapacitors (optional) connected to V_{OC}. A source/sink balancing current of up to ±10mA is available. Tie BAL to GND to disable the balancer and its associated quiescent current.
F1	V_{REF}	Voltage Reference Output for Powering Resistor Dividers to Set the V_{SET1} and V_{SET2} Inputs. The voltage at this pin is regulated by the IC to maintain a high precision, temperature-stable 1.0V output. Resistive dividers from the V_{REF} pin can be used to set the voltage at the V_{SET1} and V_{SET2} pins and thereby program the UVLO threshold for each input. The V_{REF} output may also be used as a general-purpose voltage reference in the application, providing a temperature-stable reference for comparators, DACs, or other functions. The total current drawn from this pin must be limited to 1mA, and the total capacitive load should be limited to 470pF. If this pin is not used in the application (i.e., if there is no resistor from V_{REF} to ground) then the V_{REF} pin must be connected to $INTV_{CC}$.
F2	$\overline{\text{PRIORITY}}$	Open-Drain Output Indicating that the Priority Input (V_{IN1}) Is Being Utilized. The $\overline{\text{PRIORITY}}$ pin is driven low if the part is enabled and the buck converter operates from the priority input, V_{IN1}. In disable (EN1 low), the $\overline{\text{PRIORITY}}$ pull-down is disabled, allowing the pin to float. The maximum voltage that can be applied to the $\overline{\text{PRIORITY}}$ pin is 5.5V.
F3	EN1	Enable Input of the Buck. Forcing the EN1 pin low disables the input voltage comparators, the V_{REF} pin driver, and the buck converter. The $INTV_{CC}$ rail remains powered in disable, and therefore, EN1 can be connected to $INTV_{CC}$ to continuously enable the part. The maximum voltage that can be applied to the EN1 pin is 5.5V.
F4	SDA	Serial Data Input/Output for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float this pin.
F5	SCL	Serial Clock Input for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC} for I^2C compliance. Do not float this pin.
F6	IPK2	Input Current Limit Select Bit of Battery Health Monitor (with IPK0 and IPK1). See IPK0. Do not float this pin.
F7	$\overline{\text{IRQ}}$	Interrupt Output. Logic level output referenced to DV_{CC}. Active low. This pin is normally logic high but will transition low when either the coulomb counter alarm level or one of the temperature warning levels is reached.
F8	DV_{CC}	Supply Rail for the I^2C Serial Bus and for the $\overline{\text{IRQ}}$ and V_{INCOK} Outputs. DV_{CC} sets the reference level of the SDA and SCL pins for I^2C compliance. The external I^2C pull-up resistors on SDA and SCL should connect to DV_{CC}. Depending on the application, DV_{CC} can be connected to AV_{CC} or to a separate external supply between 1.8V and 5.5V.
G1	FB1	Feedback Voltage Input of the Buck. Inside the module, a 1MΩ ±1% resistor has been internally connected between this pin and the output of the buck, which is V_{BUS}. A resistor connected between this pin and GND is needed to establish the desired V_{BUS}. Care should be taken in the routing to minimize switching noise coupled to this pin.
G2	PG	Open-Drain Power Good Indicator for the Buck Converter Output Voltage. This output is driven low if the buck converter output voltage is more than 9% below the regulation voltage or more than 10% above the regulation voltage. The PG pin is also

		driven low whenever the buck converter is disabled. The maximum voltage that can be applied to the PG pin is 5.5V.
G4, H4	V_{IN2}	Secondary Power Source Input for the Buck Converter. In priority mode (DIODE pin low), the buck converter will only operate from this input if the priority input power source is under voltage. This pin must be bypassed with a 4.7µF or larger ceramic capacitor to ground. If the V_{IN2} input is subjected to inductive shorts to ground, then a power Schottky diode must be added from ground to V_{IN2} to prevent this pin from being driven below ground.
G5	IPK0	Input Current Limit Select Bit of Battery Health Monitor (with IPK1 and IPK2). IPK0 should be tied to V_{INC} to select high or to GND to select low to program the desired I_{PEAK} (see *Table 7* in the *Theory of Operation* section). Do not float this pin.
G6	IPK1	Input Current Limit Select Bit of Battery Health Monitor (with IPK0 and IPK2). See IPK0. Do not float this pin.
G8	AV_{CC}	Supply Rail for the Coulomb Counter and Battery Health Monitor Circuit. AV_{CC} is normally connected to V_{OC}, but some applications may connect to V_{INC} (see the *Applications Information* section).
H2	RT	Switching Frequency Programming Pin. A resistor placed from this pin to ground sets the switching frequency of the buck converter.
H5	V_{OC}	Battery Health Monitor Output Voltage. Connect V_{IN2} or load to this pin.
H7	V_{INC}	Battery Health Monitor Input Voltage. Connect the battery as close as possible to this pin.

Pin Configuration Description

Table 5. LTM4719 Component BGA Pinout (Sorted by Pin Number)

PIN ID	PIN NAME	PIN ID	PIN NAME	PIN ID	PIN NAME	PIN ID	PIN NAME
A1–D8							
A1	GND	B1	$\overline{\text{VALID1}}$	C1	GND	D1	$INTV_{CC}$
A2	SV_{IN2}	B2	SV_{IN1}	C2	$\overline{\text{VALID2}}$	D2	$EXTV_{CC}$
A3	GND	B3	GND	C3	PWM/SYNC	D3	GND
A4	V_{IN1}	B4	V_{IN1}	C4	GND	D4	SW
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	GND	C6	EN2	D6	GND
A7	V_{OUT}	B7	V_{OUT}	C7	GND	D7	V_{BUS}
A8	NC	B8	FB2	C8	GND	D8	V_{BUS}
E1–H8							
E1	V_{SET1}	F1	V_{REF}	G1	FB1	H1	GND
E2	V_{SET2}	F2	$\overline{\text{PRIORITY}}$	G2	PG	H2	RT
E3	DIODE	F3	EN1	G3	GND	H3	GND
E4	GND	F4	SDA	G4	V_{IN2}	H4	V_{IN2}
E5	GND	F5	SCL	G5	IPK0	H5	V_{OC}
E6	GND	F6	IPK2	G6	IPK1	H6	GND
E7	V_{INCOK}	F7	$\overline{\text{IRQ}}$	G7	GND	H7	V_{INC}
E8	BAL	F8	DV_{CC}	G8	AV_{CC}	H8	GND

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

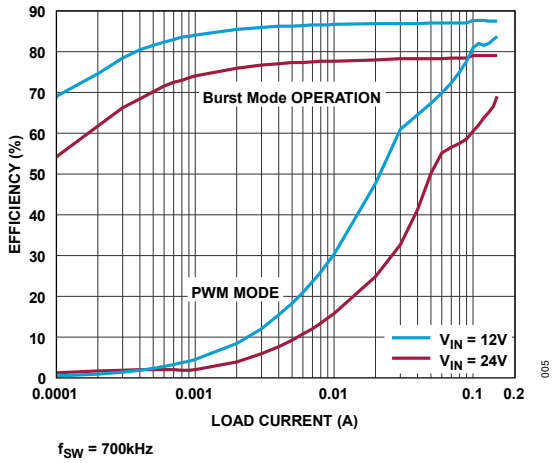


Figure 5. Efficiency from V_{IN} to V_{BUS}, V_{BUS} = 5.5V

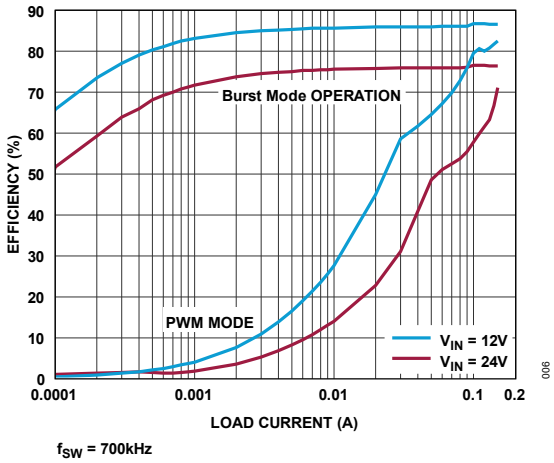


Figure 6. Efficiency from V_{IN} to V_{BUS}, V_{BUS} = 5V

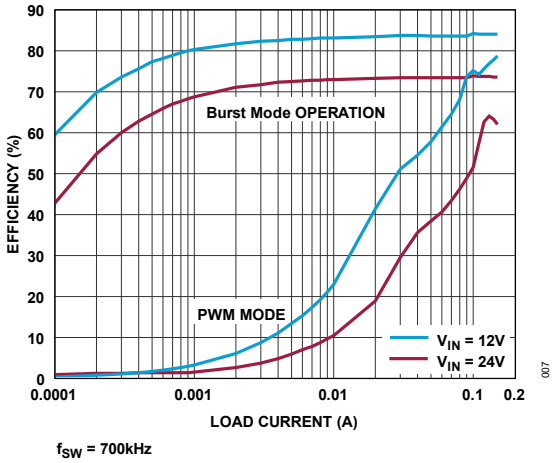


Figure 7. Efficiency from V_{IN} to V_{BUS}, V_{BUS} = 3.8V

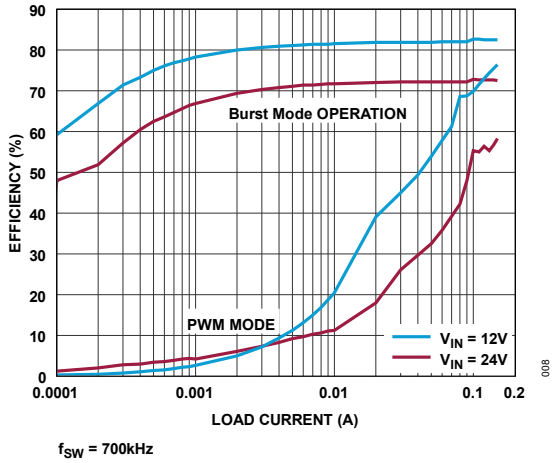


Figure 8. Efficiency from V_{IN} to V_{BUS}, V_{BUS} = 3.3V

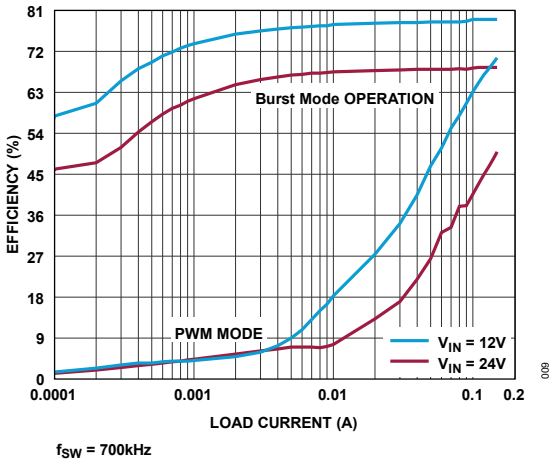
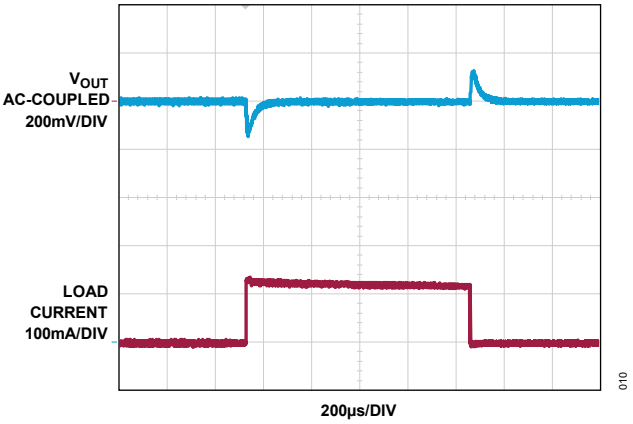
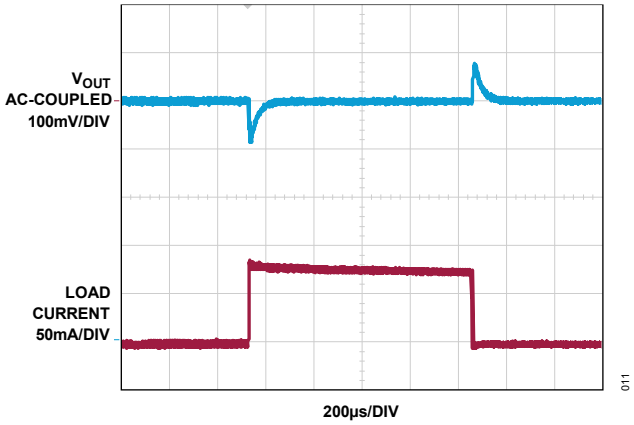


Figure 9. Efficiency from V_{IN} to V_{BUS}, V_{BUS} = 2.3V



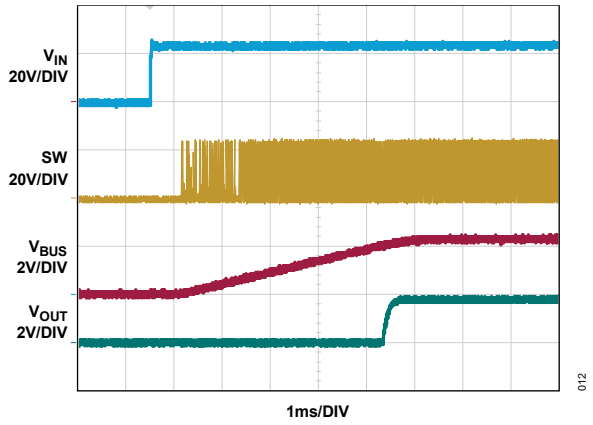
V_{IN} = 24V, V_{BUS} = 2.3V, V_{OUT} = 1.8V,
C_{OUT} = 4.7µF, f_{SW} = 700kHz,
1µs RISE/FALL TIME,
10% TO 90%, 15mA TO 135mA

Figure 10. Load Transient Response



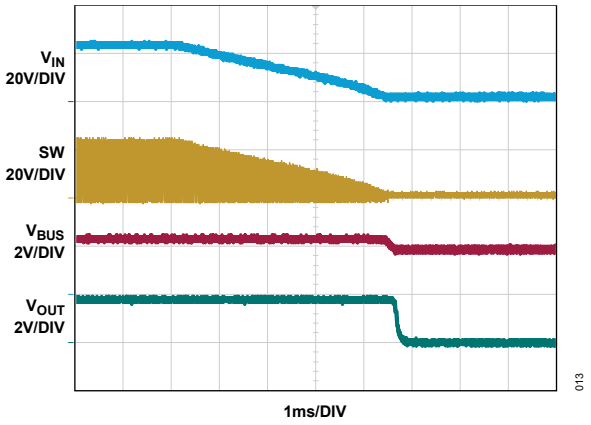
V_{IN} = 24V, V_{BUS} = 2.3V, V_{OUT} = 1.8V,
C_{OUT} = 4.7µF, f_{SW} = 700kHz,
1µs RISE/FALL TIME,
25% TO 75%, 37.5mA TO 112.5mA

Figure 11. Load Transient Response



V_{IN} = 24V, V_{BUS} = 2.3V, V_{OUT} = 1.8V,
C_{OUT} = 4.7µF, f_{SW} = 700kHz,
LOAD 150mA

Figure 12. Startup Waveforms



V_{IN} = 24V, V_{BUS} = 2.3V, V_{OUT} = 1.8V,
C_{OUT} = 4.7µF, f_{SW} = 700kHz,
LOAD 150mA

Figure 13. Shutdown Waveforms

THEORY OF OPERATION

The LTM4719 is a 42V dual input, 150mA synchronous buck µModule regulator with a battery health monitor interfaced through I²C and an integrated linear regulator for a low noise output. It can support a seamless transition between two separate input power sources when one input is lost. The fast, automatic switchover eliminates the need for holdup capacitors and minimizes disturbances on the output rail. The LTM4719 can be used in a wide variety of applications, including portable battery-powered devices, backup power, radio, healthcare, industrial automated test equipment (ATE), and uninterruptible power supply. The LTM4719 has a built-in precision coulomb counter accessible through an I²C interface. A discharge alarm threshold can be programmed. When the threshold voltage is reached, an interrupt signal is generated at the $\overline{IRQ}$ pin. Battery voltage, battery impedance, and temperature can be monitored and are accessible through I²C. The integrated ultralow quiescent current post-regulation linear regulator in the LTM4719 draws only 560nA (typical) at no load and a 42µA of quiescent current (typical) at full load, which makes LTM4719 ideal for battery-operated portable equipment. Fault protection features include input UVLO, PG, current limit, and OV protection.

Block Diagram

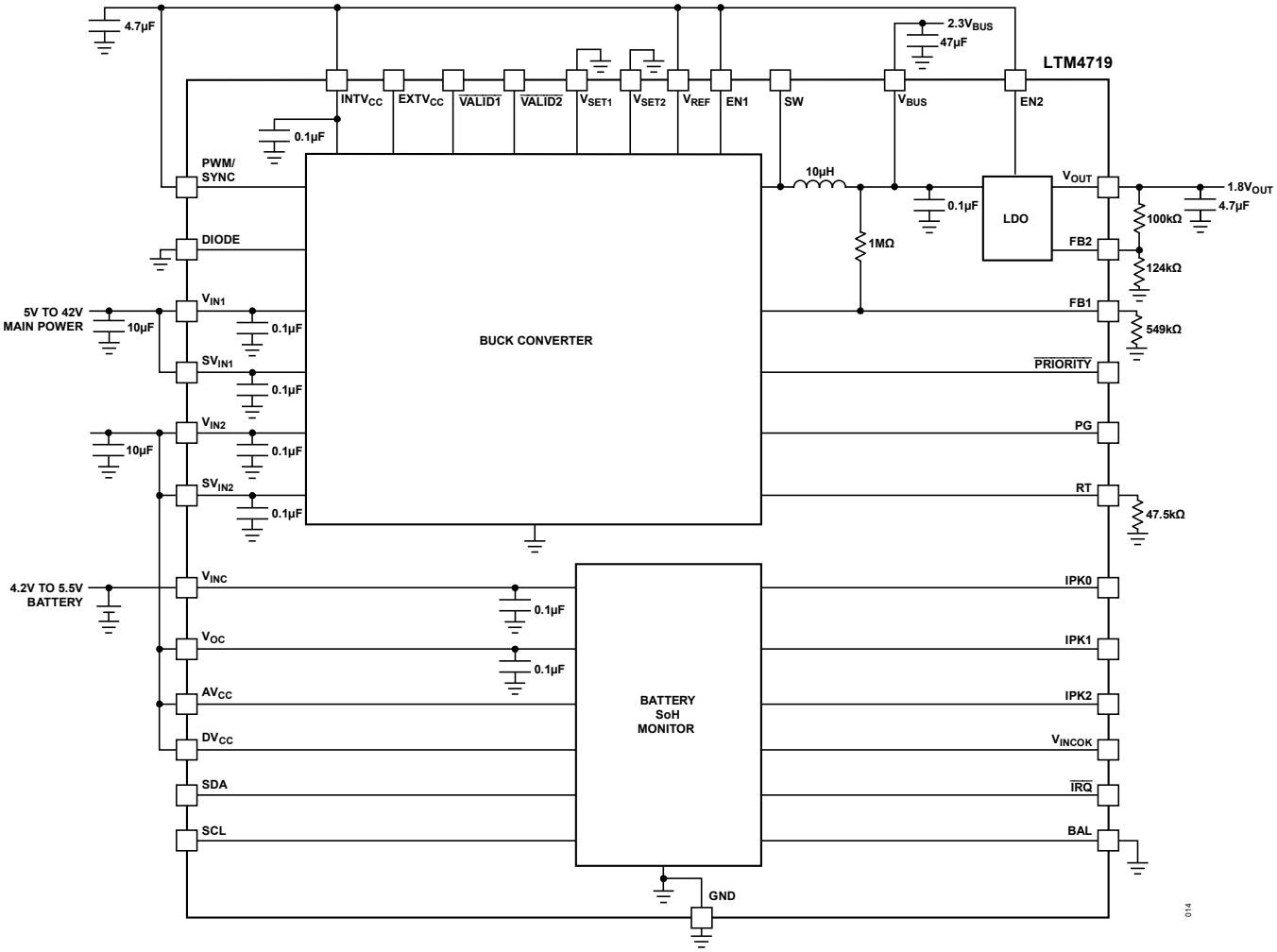


Figure 14. LTM4719 Simplified Block Diagram

PowerPath Operation

The PowerPath™ controls whether the LTM4719 operates from the V_{IN1} or V_{IN2} based on programmable UVLO thresholds for each input. The UVLO architecture used by the LTM4719 eliminates the need to connect external resistor dividers directly to the input voltages, thereby providing a substantial reduction in quiescent current.

The V_{SET1} and V_{SET2} pins are used to set the UVLO thresholds for the two power source inputs, V_{IN1} and V_{IN2}, respectively. The UVLO threshold for each input can be independently set to any voltage from 20V down to the internal fixed UVLO threshold of 2.34V using an external resistor divider, as shown in *Figure 15*. The V_{REF} pin is regulated to a fixed, temperature-stable, 1V. An external resistor divider from the V_{REF} pin establishes the voltage at the V_{SET1} and V_{SET2} pins. The programmed voltage at the V_{SET1} and V_{SET2} pins is compared to the respective input voltage (V_{IN1} or V_{IN2}) scaled down through an internal resistor divider with a ratio of 20:1 to determine if that input is undervoltage. As a result, a voltage range of 0V to 1V on the V_{SET1} and V_{SET2} corresponds to a UVLO threshold of 0V to 20V on the V_{IN1} and V_{IN2}. In addition, there is a fixed internal minimum UVLO threshold of 2.34V, which is always enforced independently of the programmed voltage on the V_{SET1} and V_{SET2} pins. To use this minimum UVLO threshold, the respective V_{SET1} and V_{SET2} pins can be connected to ground.

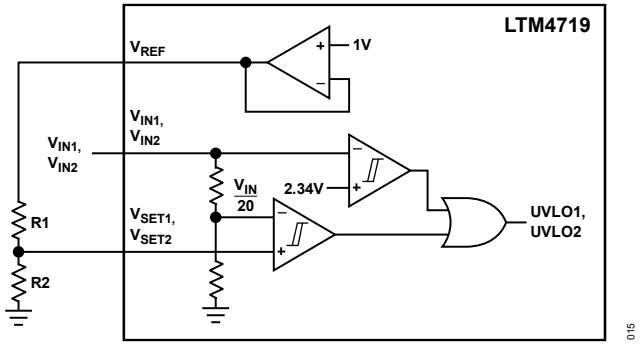


Figure 15. Programming the UVLO Thresholds on V_{IN1} and V_{IN2}

The LTM4719 PowerPath has two operational modes as determined by the state of the DIODE logic input. With DIODE high, the IC utilizes the ideal diode-OR mode and operates from the input that has the higher voltage (assuming both inputs are above their respective UVLO thresholds). If one input is in UVLO, then the other input is utilized. If both inputs are in UVLO, then the buck converter is disabled. With the DIODE input low, the IC operates in priority mode, whereby V_{IN1} is always given priority and is utilized if it is above its UVLO threshold. If V_{IN1} is in UVLO, then V_{IN2} is utilized if it is not in UVLO. If both V_{IN1} and V_{IN2} are in UVLO, then the buck converter is disabled.

All current drawn from the V_{REF} pin is supplied by one of the inputs, V_{IN1} or V_{IN2}. If neither input is above its respective UVLO threshold, then this current is drawn from the input with the higher voltage. Otherwise, this current is drawn by the active channel as determined by the PowerPath. The V_{REF} pin current is supplied by the $EXTV_{CC}$ pin if that pin is utilized and a valid voltage is present.

The $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, and $\overline{\text{VALID2}}$ open-drain outputs provide feedback on the state of the PowerPath. The $\overline{\text{VALID1}}$ and $\overline{\text{VALID2}}$ outputs indicate that the respective input is present and above its UVLO threshold. Specifically, the $\overline{\text{VALID1}}$ pin is driven low if the IC is enabled (EN1 is high) and V_{IN1} is above its UVLO threshold. The $\overline{\text{VALID2}}$ pin is driven low if the IC is enabled and V_{IN2} is above its UVLO threshold. The $\overline{\text{PRIORITY}}$ pin is driven low if the IC is enabled and the buck converter is operating from the priority channel, V_{IN1}. The $\overline{\text{PRIORITY}}$ pin provides the ability to determine which input is being utilized in ideal-diode mode when both inputs are valid.

The $INTV_{CC}$ rail stays powered even when the LTM4719 is disabled (EN1 is low) as long as either V_{IN1} or V_{IN2} is powered. In this disabled state, the $INTV_{CC}$ output is powered from whichever input (V_{IN1} or V_{IN2}) is higher in voltage

independent of the state of the DIODE pin. Given that the $INTV_{CC}$ output remains powered in shutdown, the EN1 pin can be connected to $INTV_{CC}$ to continuously enable the part.

Buck Converter Operation

The LTM4719's front-end switching regulator utilizes constant frequency switching with peak current mode control. The switching frequency can be set from 200kHz to 2.2MHz by the appropriate choice of the RT pin resistor. In addition, the buck converter can be synchronized to an external clock applied to the PWM/SYNC pin.

The buck converter always operates from a single input power source (V_{IN1} or V_{IN2}) at any time. The input that is used is determined by the state of the DIODE input, the programmed UVLO thresholds, and the voltage of each input, as described previously in the *PowerPath Operation* in this section. Each switching cycle begins with the high-side switch of the active input turning on. The high-side switch remains on until the inductor current reaches the current level set by the output of the internally compensated error amplifier. At that point, the low-side synchronous rectifier turns on and remains on for the remainder of the cycle or until the inductor current falls to zero. The error amplifier continuously adjusts the commanded current level to regulate the FB1 pin voltage.

If PWM/SYNC is forced high or has an external clock applied, then the buck converter operates in PWM mode. In PWM mode operation, the buck converter maintains fixed frequency switching at most load currents, switching to pulse-skipping mode only at very light load currents when the minimum on-time of the SW is reached. The PWM mode provides low noise, fixed frequency operation and low output voltage ripple over the widest possible range of load currents and should be used when it is necessary to maintain the lowest possible noise levels. With PWM/SYNC forced low, the converter automatically transitions to Burst Mode operation at light loads to increase efficiency and reduce no-load quiescent current.

The buck converter is current limit-protected to prevent damage to the IC during output overload and short-circuit conditions. If the inductor current exceeds the high-side switch current limit threshold then the high-side switch is turned off for the remainder of the cycle. If the inductor current exceeds the low-side current limit threshold, then the high-side switch remains off during the next cycle to prevent increasing the inductor current further during the high-side switch minimum on-time. In addition, the switching frequency is reduced by a factor of 16 if the FB1 voltage is below 200mV to ensure control of the inductor current is maintained during output overcurrent conditions.

The internal circuitry of the buck converter, including the gate drivers, is powered from $INTV_{CC}$. Internal dropouts (LDOs) generate the $INTV_{CC}$ rail from the active input, V_{IN1} or V_{IN2}. In applications where the buck converter output is 3.3V or greater, the $INTV_{CC}$ rail can be bootstrapped by connecting the $EXTV_{CC}$ pin to the buck converter output, V_{BUS}. This allows a third LDO to generate the $INTV_{CC}$ rail directly from $EXTV_{CC}$. Given that the buck converter has much greater efficiency than the LDOs, bootstrapping through the $EXTV_{CC}$ pin increases the efficiency of the converter and reduces its quiescent current. This is particularly the case for applications with high input voltage, low output voltage, and high switching frequencies.

V_{IN1}, V_{IN2} UVLO Thresholds

The V_{IN1} and V_{IN2} UVLO thresholds are set by the voltage on the V_{SET1} and V_{SET2} pins, respectively. Each UVLO threshold can be set from a maximum of 20V down to the internal fixed UVLO threshold of 2.34V using a resistor divider from the V_{REF} output as shown in *Figure 16*. The rising UVLO threshold is given by the Equation *1*.

$$V_{UVLO1}, V_{UVLO2} = 20V_{SET1,2} = 20V\frac{R2}{R1+R2} \quad (1)$$

Grounding the V_{SET1} and V_{SET2} pins defines the respective input as valid down to the fixed internal UVLO threshold of 2.34V.

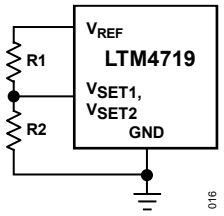


Figure 16. Input UVLO Threshold Divider

Switching Frequency

The buck converter switching frequency, f_{SW}, is set by the value of R_T resistor connected between the RT pin and ground according to Equation *2*. The values are given in *Table 6*.

$$R_T = \frac{33.2MHz}{f_{SW}}k\Omega \quad (2)$$

Table 6. R_T Value for Common Switching Frequencies

f_{SW} (Hz)	R_T (kΩ)
300k	110
500k	66.5
750k	44.2
1M	33.2
1.2M	27.4
1.5M	22.1
2M	16.5

External Synchronization Clock Frequency

The buck converter can be synchronized to an external clock applied to the PWM/SYNC pin. The frequency of the external clock must be higher than the internal oscillator frequency as set by the RT pin. To accommodate the ±10% possible variation in the oscillator frequency, the R_T resistor should be chosen to set the internal oscillator frequency at least 10% below the lowest synchronization frequency. For example, to synchronize to an external 1MHz clock, R_T should be picked to set the internal oscillator at 900kHz or lower.

Bus Voltage

The buck converter output voltage (V_{BUS}) is set through a resistor divider connected to the FB1 pin, as shown in *Figure 17*.

The upper voltage divider R_{TOP} equals to 1MΩ, and it is integrated inside the LTM4719 for ease of use. The R_{BOT} can be determined by Equation *3*, where V_{BUS} is the desired bus voltage.

$$V_{BUS} = 0.818V\left(\frac{1M\Omega}{R_{BOT}} + 1\right) \quad (3)$$

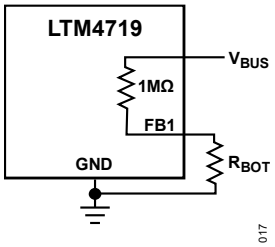


Figure 17. FB1 Resistor Divider

Bus Capacitor

The recommended minimum bus capacitor, C_{MIN}, is given in Equation *4* as a function of the bus voltage.

$$C_{MIN} = \frac{1V}{V_{BUS}}150\mu F \quad (4)$$

Feedforward Capacitor

The feedforward capacitor, C_{FF}, as shown in *Figure 18*, improves the noise robustness of the FB pin and adds a zero to the loop at the frequency f_{ZERO} which is given by Equation *5*.

$$f_{ZERO} = \frac{1}{2\pi \times R_{TOP} \times C_{FF}} \quad (5)$$

In most applications, performance is optimized if the zero frequency is set at approximately 16kHz. In applications with large bus capacitance, a larger feedforward capacitor can be utilized to reduce the zero frequency and improve the transient response and phase margin. As shown in *Figure 18*, a 10kΩ feedforward resistor, R_{FF}, can be added to improve noise immunity in applications with high output voltage ripple or a long distance between the resistor divider and V_{BUS}.

Feedforward Resistor

In applications where there is a long connection between the feedback resistor divider and the point at which the bus voltage is sensed, it is recommended that a 10kΩ feedforward resistor (R_{FF}) be added in series with the feedforward capacitor, as shown in *Figure 18*. The feedforward resistor prevents high-frequency noise on the V_{BUS} trace from coupling into the sensitive FB1 node. The addition of a 10kΩ feedforward resistor has little impact on the frequency response of the control loop since the divider pole location is dominated by the values of resistors R_{TOP} = 1MΩ and R_{BOT}.

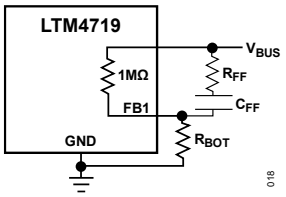


Figure 18. Feedforward Resistor (R_{FF}) for Improved Noise Robustness

Open-Drain Outputs

The open-drain outputs (PG, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, and $\overline{\text{VALID2}}$) are low-voltage pins and cannot be pulled up to a voltage higher than 5.5V. The PG pin is forced low in disabled mode.

Logic Inputs

The logic input pins (DIODE, EN1, PWM/SYNC) are low voltage pins and cannot be forced above 5.5V. To force any of these pins continuously high, the pin can be connected to $INTV_{CC}$.

Important Usage Notes

1. V_{IN1} and SV_{IN1} must be connected in the application. V_{IN2} and SV_{IN2} must be connected in the application. V_{IN1} and V_{IN2} must each have a 4.7µF or larger bypass capacitor installed and placed as close to the µModule as possible. In addition, SV_{IN1} and SV_{IN2} have separate 0.1µF bypass capacitors installed internally.
2. $INTV_{CC}$ should be bypassed with a 4.7µF or larger capacitor.
3. If the V_{REF} pin is not used in the application (i.e., there is no resistor from V_{REF} to GND), then the V_{REF} pin must be connected to $INTV_{CC}$.
4. If V_{IN1} or V_{IN2} can be driven below ground in the application, for example, due to large inductive ringing at the input, then Schottky diodes must be installed from ground to V_{IN1}/V_{IN2} to protect the LTM4719.

Linear Regulator Operation

The LTM4719's back-end linear regulator is an ultralow quiescent current, low dropout linear regulator that operates from 2.2V to 5.5V and can provide up to 150mA of output current. Drawing only 560nA (typical) at no load and a low 42µA of quiescent current (typical) at full load makes this linear regulator ideal for battery-operated portable equipment. Shutdown current consumption is typically 50nA.

Using new innovative design techniques, the linear regulator provides ultralow quiescent current and superior transient performance for digital and RF applications. The linear regulator is also optimized for use with small 1µF ceramic capacitors.

The linear regulator includes an output discharge resistor to force the output voltage to zero when the LDO is disabled. This ensures that the output of the LDO is always in a well-defined state, whether it is enabled or not.

Output Voltage

The linear regulator has an output voltage range of 1V to 4.2V. The output voltage is set by the ratio of two external resistors, as shown in *Figure 19*. The device servos the output to maintain the voltage at the FB2 pin at 1V referenced to ground. The current in R2 is then equal to 1V/R2, and the current in R1 is the current in R2 plus the FB2 pin bias current. The FB2 pin bias current, IBIAS_FB2, 10nA at 25°C, flows through R1 into the FB2 pin. The output voltage can be calculated using Equation *6*.

$$V_{OUT} = 1V\left(1 + \frac{R1}{R2}\right) + \text{IBIAS\_FB2} \times R1 \qquad (6)$$

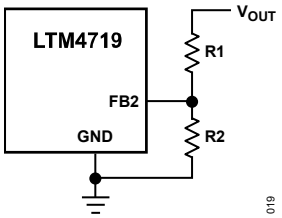


Figure 19. FB2 Resistor Divider

The value of R1 should be less than 200kΩ to minimize errors in the output voltage caused by the FB2 pin bias current. For example, when R1 and R2 each equal 200kΩ, the output voltage is 2.0V. The output voltage error introduced by the IBIAS_FB2 is 2mV or 0.05%, assuming a typical IBIAS_FB2 of 10nA at 25°C.

To minimize quiescent current in the linear regulator, Analog Devices recommends using high values of resistance for R1 and R2. Using a value of 1MΩ for R2 keeps the total, no-load quiescent current below 2µA. Note, however, that a high value of resistance introduces a small output voltage error. For example, assuming R1 and R2 are 1MΩ, the output voltage is 2V. Considering the nominal IBIAS_FB2 of 10nA, the output voltage error is 0.25%. Note that during shutdown, the output is turned off and the divider current is zero.

Battery Health Monitor

The LTM4719's battery state of health (SoH) monitor integrates a precision coulomb counter, which monitors the accumulated charge that is transferred from a primary battery connected to its V_{INC} pin to an output load connected to its V_{OC} pin. The I_{PEAK} is a low dropout current source between V_{INC} and V_{OC}. The current source value can be set through the input current limit select pins IPK[2:0] (see *Table 7*).

Table 7. IPEAK Selection

IPK2	IPK1	IPK0	I_{PEAK} (mA)
0	0	0	5
0	0	1	10
0	1	0	15
0	1	1	20
1	0	0	25
1	0	1	50
1	1	0	75
1	1	1	100

As shown in *Figure 20*, if V_{OC} is less than V_{INC} – V_{OC_LOW} (where V_{OC_LOW} is nominally 160mV), the current source is turned on, and the charge is delivered from V_{INC} to V_{OC}. After V_{OC} charges up to V_{INC} – V_{OC_HIGH} (where V_{OC_HIGH} is nominally 110mV), the current source is turned off.

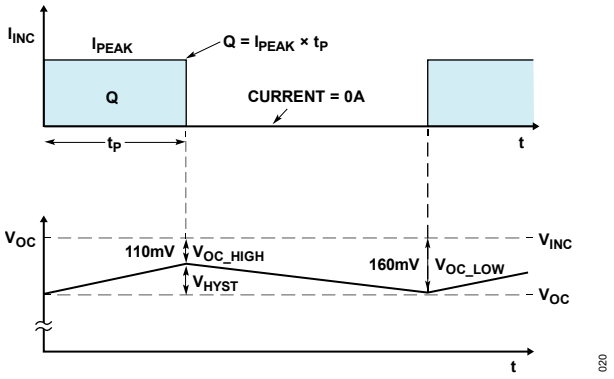


Figure 20. Coulomb Counter Operation

The capacitor connected between V_{OC} and ground supports the load while the current source is off and should have a minimum value of 100µF for the 100mA I_{PEAK} setting. See *Table 17* in the *Applications Information* section.

A hysteretic comparator senses both thresholds and controls the current source timing. The output of the comparator in one state represents the time (t_P) during which the battery is delivering a current equal to I_{PEAK}. This output enables an oscillator to have a period T (500ns typical) which is used to increment a counter. The counter output bits represent a precise count of the battery coulombs. The last 2 bytes can be read through I^2C.

The amount of charge represented by the least significant bit (qLSB) of the accumulated charge register is given in the *Electrical Characteristics* table for all eight I_{PEAK} settings for the case of the default prescaler setting (M = 0). This default prescaler setting uses the full length of the internal counter. See Equation *7*.

$$q_{LSB\ (M=0)} = \frac{2^{46} - 1 \times I_{PEAK} \times T}{65535} \qquad (7)$$

Choosing the Coulomb Counter Prescaler M

To preserve adequate digital resolution for a wide range of battery capacities and I_{PEAK} current values, the LTM4719's battery SoH monitor includes a programmable prescaler. The user can set the prescaler value from 0 to 15 by writing bits A[3:0] (see *Table 9*). Note that the default value for the prescaler is 0.

To use most of the range of accumulated charge Register B, the prescaler value (M) should be chosen for a given battery capacity Q_{BAT} based on Equation *8*.

$$M = \log_2\left(\frac{q_{LSB} \times 65535}{Q_{BAT}}\right) \qquad (8)$$

where Q_{BAT} is the battery capacity, and q_{LSB} is the typical value (for M = 0) from the *Electrical Characteristics* table for the selected I_{PEAK}. The M must be an integer, so the result of Equation *8* must be rounded down to the nearest integer value. The M has a maximum value of 15.

A smaller capacity battery will require a higher prescaler value M than a larger capacity battery for the same I_{PEAK}. Likewise, a lower I_{PEAK} will require a lower prescaler value M, than a higher I_{PEAK} for the same capacity battery.

The amount of charge represented by the least significant bit (q_{LSB}_M) of the accumulated charge register is given by Equation 9.

$$q_{LSB\_M} = \frac{q_{LSB}}{2^M} \quad (9)$$

where q_{LSB} is the typical (M = 0) value in the *Electrical Characteristics* table for the selected I_{PEAK}.

AV_{CC} Pin Connection

The AV_{CC} pin serves as the power supply for all internal LTM4719's battery SoH monitor circuits and can be connected to V_{INC} or to V_{OC}. With AV_{CC} connected to V_{OC}, the coulomb counter counts all coulombs coming out of the battery, including those associated with the battery SoH monitor's own quiescent current, which effectively parallels the output load at V_{OC}. When connecting AV_{CC} to V_{INC}, the battery SoH monitor's own quiescent current represents an error on coulombs out of the battery. However, coulombs associated purely with the output load are now more accurately counted, and this may be beneficial in output power metering applications. In this second option, a scaling factor of minus 1.6% needs to be applied to all coulomb counter measurements.

Battery Voltage (V) and Battery Impedance (Z) Monitors

The LTM4719's battery SoH monitor includes a 12-bit analog-to-digital converter (ADC), which is used to measure the battery voltage at the V_{INC} pin, the V_{OC} pin, and the monitor's die temperature.

The V_{INC} pin voltage is sampled when the coulomb counter is delivering a known I_{PEAK} pulse ($V_{INC(ON)}$). The ADC converts this sampled value to a 12-bit value with an LSB = 1.465mV. The conversion time is typically 3.5ms. The V_{INC} voltage is then sampled a second time when the coulomb counter is delivering zero current, ($V_{INC(OFF)}$). After a second conversion time, the last stored value is readable from Register D (for $V_{INC(ON)}$) and Register E (for $V_{INC(OFF)}$). See *Table 8*, *Table 12*, and *Table 13*.

The voltage measurement is performed only every 1024 on-cycles to minimize the AV_{CC} quiescent current.

Battery impedance can be calculated from the previous two conversion values: $Z = (V_{BAT\_IN(OFF)} - V_{BAT\_IN(ON)})/I_{PEAK}$ based on the last stored values in Registers D and E.

The V_{OC} voltage is also sampled when the I_{PEAK} current source turns on ($V_{OC(ON)}$) and sampled a second time when the I_{PEAK} current source turns off ($V_{OC(OFF)}$). Again, after two conversion times, the last stored values are readable from Register F (for $V_{OC(ON)}$) and Register G (for $V_{OC(OFF)}$). See *Table 8*, *Table 14*, and *Table 15*. Just like for the V_{INC} voltages, these voltage measurements are performed only every 1024 on-cycles to minimize the AV_{CC} quiescent current.

Temperature Monitor (T)

The LTM4719's battery SoH monitor also measures its own die temperature and stores it in an 8-bit register. This temperature measurement is also taken only every 1024 on-cycles. The last stored value can be read from the 8MSBs in Register C. See *Table 8* and *Table 11*.

I²C Interface

The LTM4719's battery state of health (SoH) monitor communicates with the main bus using the standard I²C 2-wire serial interface. The timing diagram in *Figure 3* shows the relationship of the signals on the bus. The two bus lines, serial data access (SDA) and serial clock line (SCL), must be high when the bus is not in use. External pull-up resistors are required on these lines. The I²C control signals, SDA and SCL, are referenced internally to the DV_{CC} supply. The DV_{CC} should be connected to the same power supply as the bus pull-up resistors. The DV_{CC} can be connected to AV_{CC} or to a separate external supply between 1.8V and 5.5V.

The 7-bit hard wired I²C address of the LTM4719's battery SoH monitor is 1100100[R/$\overline{W}$]. The LTM4719's battery SoH monitor is a subordinate-only device, meaning that the serial clock line (SCL) is only an input while the serial data line (SDA) is bidirectional.

Internal Registers

The LTM4719's battery SoH monitor has eight internal sub-addressed I²C registers, as shown in *Table 8*. Registers A and H are write-only registers, Register B is read/write, and Registers C, D, E, F, and G are read-only, as shown in *Table 8* through *Table 16*.

Table 8. Register Map

SUB-ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	R/W	DEFAULT
01h	A	Prescaler selection, clear interrupt, coulomb counter shutdown, gross test, and coulomb counter alarm threshold.	W	FF00h
02h	B	Accumulated charge, 16 bits (read), 8 bits (write).	R/W	0000h
03h	C	Status register, die temperature.	R	0000h
04h	D	V_{INC} voltage when I_{PEAK} is on.	R	0000h
05h	E	V_{INC} voltage when I_{PEAK} is off.	R	0000h
06h	F	V_{OC} voltage when I_{PEAK} is on.	R	0000h
07h	G	V_{OC} voltage when I_{PEAK} is off.	R	0000h
08h	H	Cold and hot die temperature alarms.	W	00FFh

Table 9. Write Register A (Address 01h)

BIT	NAME	OPERATION	DEFAULT
A[3:0]	Prescaler bits	Set coulomb counter prescaling factor M from 0 to 15.	0000
A[4]	Clear_Int	Clear interrupt (alarm reset).	0
A[5]	Counter check	Counter-check using $\overline{IRQ}$ pin.	0
A[6]	Coulomb counter shutdown	Extend battery range.	0
A[7]	Set ADC conversion when the coulomb counter is turned off	Start ADC conversion of battery measurement and temperature when A[6] = 1. This bit self-resets when the ADC measurements/conversions are finished.	0
A[15:8]	Alarm level	The coulomb counter alarm level threshold is calculated by the user based on battery capacity and I_{PEAK} current.	FFh

Table 10. Read/Write Register B (Address 02h)

BIT	NAME	OPERATION	DEFAULT
B[15:0]	Accumulated charge	Readback 16MSBs of counter data, only 8MSBs B[15:8] are writable.	0000h

Table 11. Read Register C (Address 03h)

BIT	NAME	OPERATION	DEFAULT
C[0]	Coulomb counter overflow	Coulomb counter operating fault due to an improperly chosen prescaler causing the ripple counter to overflow.	0
C[1]	Alarm trip	Accumulator Register B value has met or exceeded the alarm threshold set in Register A.	0
C[2]	Alarm minimum die temperature	The die temperature has reached the minimum die temperature set with bits H[7:0].	0
C[3]	Alarm maximum die temperature	The die temperature has reached the maximum die temperature set with bits H[15:8].	0
C[4]	ADC measurements ready	Indicates when the ADC measurements are ready after a read request with the coulomb counter turned off (Bit A[7] = 1 and Bit A[6] = 1) after this bit is read through I2C, it self-resets.	0
C[7:5]	Pin-strapped I_{PK} pin	Readback of IPK[2:0] pins (setting latched at startup).	000
C[15:8]	DIE_TEMP	Readback 8MSBs of die temperature measurement.	00h

The die temperature DIE_TEMP can be calculated by Equation *10*.

$$DIE_{TEMP} = T_{LSB} \times COUNT_C - 41°C \qquad (10)$$

where T_{LSB} is the typical value in the *Electrical Characteristics* table and $COUNT_C$ are the 8MSBs of Register C.

Table 12. Read Register D (Address 04h)

BIT	NAME	OPERATION	DEFAULT
D[11:0]	$V_{INC(ON)}$	Readback V_{INC} pin voltage measurement when I_{PEAK} turns on.	000000 000000
D[15:12]		Not used.	0000

The battery voltage $V_{INC(ON)}$ can be obtained from the count in Register D ($COUNT_D$) by Equation *11*.

$$V_{INC(ON)} = V_{LSB} \times COUNT_D \qquad (11)$$

where V_{LSB} is the typical value in the *Electrical Characteristics* table.

Table 13. Read Register E (Address 05h)

BIT	NAME	OPERATION	DEFAULT
E[11:0]	$V_{INC(OFF)}$	Readback V_{INC} pin voltage measurement when I_{PEAK} turns off.	000000 000000
E[15:12]		Not used.	0000

The battery voltage $V_{INC(OFF)}$ can be obtained from the count in Register E ($COUNT_E$) by using Equation *12*.

$$V_{INC(OFF)} = V_{LSB} \times COUNT_E \quad (12)$$

where V_{LSB} is the typical value in the *Electrical Characteristics* table.

Battery impedance can be calculated from the above two conversion values: $Z = (V_{INC(OFF)} - V_{INC(ON)})/I_{PEAK}$.

Table 14. Read Register F (Address 06h)

BIT	NAME	OPERATION	DEFAULT
F[11:0]	$V_{OC(ON)}$	Readback V_{OC} pin voltage measurement when I_{PEAK} turns on.	000000 000000
F[15:12]		Not used.	0000

The V_{OC} voltage $V_{OC(ON)}$ can be obtained from the count in Register F ($COUNT_F$) by using Equation *13*.

$$V_{OC(ON)} = V_{LSB} \times COUNT_F \quad (13)$$

where V_{LSB} is the typical value in the *Electrical Characteristics* table.

Table 15. Read Register G (Address 07h)

BIT	NAME	OPERATION	DEFAULT
G[11:0]	$V_{OC(OFF)}$	Readback V_{OC} pin voltage measurement when I_{PEAK} turns off.	000000 000000
G[15:12]		Not used.	0000

The V_{OC} voltage $V_{OC(OFF)}$ can be obtained from the count in Register G ($COUNT_G$) by using Equation *14*.

$$V_{OC(OFF)} = V_{LSB} \times COUNT_G \quad (14)$$

where V_{LSB} is the typical value in the *Electrical Characteristics* table.

Table 16. Write Register H (Address 08h)

BIT	NAME	OPERATION	DEFAULT
H[7:0]	Cold die temperature alarm level	Minimum temperature threshold.	00h
H[15:8]	Hot die temperature alarm level	Maximum temperature threshold.	FFh

Counter Check Test

Setting bit A[5] = 1 allows the user to verify that the coulomb counter is operating correctly without having to wait for the accumulated charge register to increment from 0000h. In this mode, the input clock of the ripple counter is output to the $\overline{IRQ}$ pin. The coulombs represented by each transition on the $\overline{IRQ}$ pin (time between two consecutive rising edges) is: $q_{LSB\_M}/2^{(24-M)}$, where q_{LSB} is given in the *Electrical Characteristics* for each I_{PEAK} setting.

Alarms

Alarms cause the $\overline{IRQ}$ pin to be pulled low. The user can read Register C to determine what caused the alarm. The alarm can then be cleared by writing a 1 to bit A[4]. The clear interrupt bit itself is self-clearing after the action is taken on the $\overline{IRQ}$ pin. If another alarm occurs while clearing a previous alarm, the $\overline{IRQ}$ pin will go high for 1µs (typical) before returning low again. At this time, the clear interrupt bit A[4] is also reset to zero.

The following are the four different fault/alarm conditions:

1. A coulomb counter overflow (C[0] is high) due to an improperly chosen prescaler (M), value causing the ripple counter to overflow. After the alarm is cleared, the $\overline{IRQ}$ pin is released for 1µs and later pulled low again unless Register C is overwritten with a lower value.
2. The preset alarm level is reached (C[1] is high) when the 8MSBs of the ripple counter are equal to or higher than the 8MSBs in Register A (coulomb counter alarm threshold). The user should increase the alarm threshold in A[15:8] bits and write bit A[4] to 1 to clear the alarm. The alarm threshold is only checked when the LSB of the accumulator register changes or when a write to Register B or Register A is done through I^2C. Therefore, if bit A[4] is set to 1 to clear an alarm interrupt without also changing the contents of Register A and/or B, and this occurs during a long I_{PEAK} source off time, the $\overline{IRQ}$ pin is cleared and will not go back high again until the LSB bit of Register B again changes. This could require several I_{PEAK} cycles.
3. The cold threshold of the die temperature alarm is reached (C[2] is high) due to the measured die temperature in C[15:8] being equal to or lower than the cold temperature threshold set in Register H.
4. The hot threshold of the die temperature alarm is reached (C[3] is high) due to the measured die temperature in C[15:8] being equal to or higher than the hot temperature threshold set in Register H.

Extended Battery Range Below 2V

When the coulomb counter operates, the V_{OC} voltage is lower than the V_{INC} voltage by a controlled amount (typically 110mV to 160mV). The coulomb counter works properly for V_{INC} voltages down to 2V and for V_{OC} voltages down to 1.8V. The V_{INC} range can be somewhat extended down below 2.0V by setting bit A[6] = 1. This action disables the coulomb counter and the peak current limit I_{PEAK} and creates a low-impedance connection between V_{INC} and V_{OC}. Because the current limit circuitry is disabled in this mode, care must be taken not to exceed the *Absolute Maximum Ratings* of the V_{OC} pin. Although this mode can be entered at any V_{INC} voltage, it is only intended (and recommended) for "last gasp" end-of-life 2V and below operation.

The temperature monitor and the V_{INC} voltage monitor are still functional down to 1.8V on V_{INC}. These values can still be read on request by issuing a read command through I^2C.

Supercapacitor Balancer (Optional)

An integrated supercapacitor balancer with 62nA of quiescent current from the V_{OC} pin is available to balance a stack of two supercapacitors at the V_{OC} pin. The BAL pin is tied to the middle of the stack and can source or sink 10mA to regulate the BAL pin's voltage to half that of the V_{OC} pin's voltage. To disable the balancer and its associated quiescent current, tie the BAL pin to ground.

Advantages of Supercapacitors

Supercapacitors are used in many power-management applications requiring many rapid charge/discharge cycles for short-term power needs. Supercapacitors have many advantages. For instance, they maintain a long cycle lifetime and thanks to their low equivalent series resistance, supercapacitors provide high power density and high load currents to achieve almost instant charge in seconds.

One disadvantage of supercapacitors is their low energy density. Thus, they cannot be used as a continuous power source. Also, the maximum voltage of a single cell is typically only 2.7V. If higher voltage is needed, a second cell must be connected in series.

APPLICATIONS INFORMATION

Input UVLO Thresholds on V_{IN1}, V_{IN2}

The undervoltage lockout (UVLO) threshold for each input, V_{IN1} and V_{IN2}, is set by the voltage on the V_{SET1} and V_{SET2} pins, respectively. A voltage between 0V and 1V on V_{SET1} and V_{SET2} linearly programs a corresponding UVLO threshold of zero to 20V. There is also an additional internal minimum UVLO threshold of 2.34V on each input which is always in effect independent of the voltage at the V_{SET1} and V_{SET2} pins. To allow input to operate fully down to the internal minimum UVLO threshold, the respective V_{SET1} and V_{SET2} pins can be connected to ground.

In most applications, the voltage at the V_{SET1} and V_{SET2} pins is established using a resistor divider from the V_{REF} pin, as shown in *Figure 21*. The corresponding rising UVLO threshold is given by the Equation *15*.

$$V_{UVLO1}, V_{UVLO2} = 20V_{SET1}, V_{SET2} = 20V\frac{R2}{R1+R2} \quad (15)$$

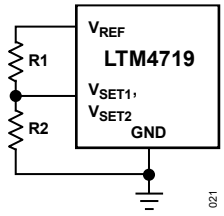


Figure 21.Setting the Input UVLO Thresholds

When neither input is valid (above its respective UVLO threshold), the current drawn from the V_{REF} pin adds directly to the quiescent current of the higher voltage input (V_{IN1} or V_{IN2}). Therefore, the use of large value resistors in the V_{SET1} and V_{SET2} divider string reduces the quiescent current. However, larger value resistors also result in lower immunity to noise and leakage currents. A reasonable compromise in most applications is to utilize a total resistor string impedance of 1MΩ.

To minimize quiescent current and eliminate an external resistor, it is also possible to set both UVLO thresholds through a single resistor string, as shown in *Figure 22*.

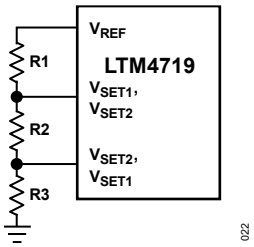


Figure 22. Setting Both Input UVLO Thresholds Using a Single Resistor String

Resistor R3 can be chosen independently, and selecting R3 equal to 200kΩ is a reasonable starting choice for most applications. The value of R2 and R1 can then be determined using Equation *16* and Equation *17* where V_{UVLOH} is the UVLO threshold on the higher voltage channel, and V_{UVLOL} is the UVLO threshold on the lower voltage channel.

$$R2 = R3\left(\frac{V_{UVLOH}}{V_{UVLOL}} - 1\right) \quad (16)$$

$$R1 = (R2 + R3)\left(\frac{20}{V_{UVLOH}} - 1\right) \quad (17)$$

If the resulting total resistance through the resistor chain (R1 + R2 + R3) is larger or smaller than desired, the choice of R3 can be adjusted in the appropriate direction, and the calculation for R2 and R1 can be repeated.

Input Hold-Up Capacitance

The LTM4719 features internal micropower UVLO comparators that minimize the quiescent current required by the application. However, due to their low operating current, the UVLO comparators exhibit a significant delay when responding to an undervoltage condition. Sufficient input hold-up capacitance must be provided to ensure the voltage on the utilized channel remains sufficient to power the buck converter until the transition to the secondary channel is completed.

Consider the example illustrated in *Figure 23* where the LTM4719 is being powered by the priority input (V_{IN1}) at 12.8V and the UVLO threshold on the V_{IN1} channel is programmed to 10V. At time t_1, the priority input is unplugged, and the buck converter begins discharging the input capacitor. At time t_2, the UVLO threshold is reached, but the buck converter remains operating from the priority channel due to the comparator delay. At time t_3, after comparator delay t_{DELAY}, the buck converter switches over to the secondary input (V_{IN2}), and the input capacitor on V_{IN1} maintains its voltage since there is no longer any current being drawn on that channel. In this example, the input capacitor on V_{IN1} must be large enough that V_{IN1} remains at sufficient voltage to maintain the output voltage in regulation until time t_3. If V_{IN1} is allowed to drop lower than the regulated output voltage, then the buck converter output temporarily loses regulation during the transition.

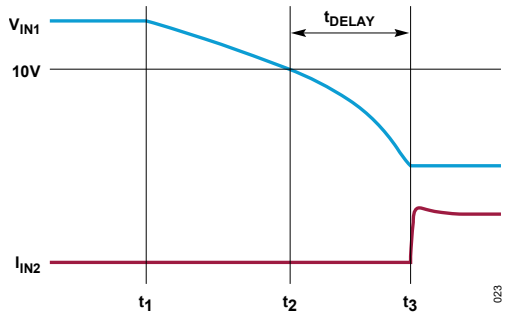


Figure 23. Waveforms During Transition from V_{IN1} to V_{IN2}

Soft Start

The LTM4719 incorporates an internal soft start circuit with a nominal duration of 7.5ms. The soft start is implemented by a linearly increasing ramp of the error amplifier reference voltage during the soft start duration. As a result, the duration of the soft start period is largely unaffected by the size of the bus capacitor or the bus regulation voltage. Given the closed-loop nature of the soft start implementation, the converter can respond to load transients that occur during the soft start interval. The soft start period is reset by thermal shutdown, when the buck converter is disabled through the EN1 pin, and when both inputs are in UVLO.

V_{REF} Output

The V_{REF} output is a regulated, temperature-stable, 1V voltage reference. It is intended primarily to be used to establish the V_{SET1} and V_{SET2} pin voltages. However, it can also be used for other functions if the total current drawn from the pin is limited to 1mA or less. In addition to that restriction, there is also a maximum amount of capacitance that can be placed on the V_{REF} pin to maintain a suitable phase margin in the internal pin driver. The maximum recommended capacitance on the V_{REF} pin is 470pF or less. If the V_{REF} pin is not being used in the application (i.e., there is no resistor from V_{REF} to GND) then the V_{REF} pin should be connected to $INTV_{CC}$.

The V_{REF} pin cannot be left floating. The V_{REF} pin is only powered when the front-end switching regulator IC is enabled (EN1 is high).

Buck Converter Switching Frequency

The LTM4719's buck converter utilizes fixed-frequency PWM to achieve low output ripple and low noise operation. The switching frequency can be set from 200kHz to 2.2MHz by the appropriate selection of the RT resistor placed between the RT pin and ground. See the *Theory of Operation* section for details on selecting the value for RT.

The on-time of the buck converter SW pin decreases as the step-down ratio from V_{IN} to V_{BUS} increases and as the switching frequency is increased. The minimum switch on-time, $t_{ON(MIN)}$, is the shortest duration on-time that the SW pin can generate. If the required on-time is shorter than the minimum on-time, then the IC pulse skips to maintain regulation. Although regulation of the output is maintained, pulse-skipping results in lower frequency switching and increased output voltage ripple. To avoid a pulse-skipping operation, the switching frequency should be selected to be less than $f_{SW(MAX)}$ as given by Equation *18*, where $t_{ON(MIN)}$ is the minimum SW pin on time with a typical value of 60ns.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN} \times t_{ON(MIN)}} \quad (18)$$

Input Capacitor

To ensure the proper functioning of the buck converter, minimize electromagnetic interference (EMI), and reduce input ripple, the V_{IN1} and V_{IN2} pins must each be connected to a low ESR bypass capacitor with a value of at least 4.7µF. Ceramic capacitors with X5R or X7R dielectric are recommended. Each bypass capacitor must be located as close as possible to the respective pin and should connect to the ground plane through the shortest route possible.

When powered through an inductive connection such as a long cable, the inductance of the power source and the input bypass capacitor form a High-Q resonant LC filter. In such applications, hot plugging into a powered source can lead to a significant voltage overshoot, even up to twice the nominal input source voltage. Care must be taken in such situations to ensure that the absolute maximum input voltage rating of the LTM4719 is not violated. Refer to the Analog Devices *Application Note 88* for solutions to increase damping in the input filter and minimize this voltage overshoot.

The V_{IN1} and V_{IN2} pins provide power to the $INTV_{CC}$ regulator and other internal circuitry. Each of these pins should be connected to a 0.1µF bypass capacitor located as close to the pin as possible.

Bus Capacitor

A low ESR capacitor should be utilized at the output of the buck converter to minimize bus voltage ripple. For most applications, a ceramic capacitor with X5R or X7R dielectric is the optimal choice. The crossover frequency of the voltage control loop increases with lower bus capacitance; therefore, a minimum capacitance value is required to limit the bandwidth and ensure stability of the voltage feedback loop. Given that the loop gain is dependent on the voltage divider ratio, the minimum required bus capacitor is a function of the bus voltage as well. At lower bus voltages, the loop gain is higher, and a larger bus capacitor is required to maintain a fixed loop crossover frequency. The larger recommended bus capacitance at low bus voltages also helps to reduce the magnitude of voltage steps on load transients in proportion to the reduced bus voltage rail to maintain a constant percentage deviation.

Increasing the value of the buck converter output capacitor decreases the bandwidth of the feedback loop. If the bus capacitor gets too large, the crossover frequency may decrease too far below the compensation zero, leading to a degraded phase margin and an underdamped transient response. In such cases, the phase margin and transient

performance can be improved by increasing the size of the feedforward capacitor in parallel with the upper resistor divider resistor to restore the full bandwidth of the feedback loop.

Output Capacitor

The back-end linear regulator is designed for operation with small, space-saving ceramic capacitors, but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1µF capacitance with an ESR of 1Ω or less is recommended to ensure stability of the LDO. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the linear regulator to large changes in load current.

PG Output

The open-drain PG output is driven low whenever FB1 is more than +9.8%/–8.7% (typical) from the FB1 reference voltage. The PG output is also driven low whenever the buck converter is disabled. The maximum voltage that can be applied to the PG output is 5.5V. The PG comparator has a deglitching delay of approximately 200µs.

$INTV_{cc}$ Regulators and Bootstrapping with $EXTV_{cc}$

The $INTV_{CC}$ rail powers the internal control circuitry and power device gate drivers of the LTM4719. Two internal low dropout linear regulators provide the ability to generate this rail from either V_{IN1} or V_{IN2}. When the IC is disabled (EN1 low), the $INTV_{CC}$ rail is powered by the higher voltage input, V_{IN1} or V_{IN2}, regardless of the state of the V_{SET1}, V_{SET2}, and DIODE pins. When the IC is enabled, the input voltage comparators on the V_{SET1} and V_{SET2} pins become active, and the $INTV_{CC}$ rail is powered by the active channel. In ideal diode mode (DIODE high) the active channel is the valid input with the higher voltage. In priority mode (DIODE low), the active channel is V_{IN1} if V_{IN1} is valid or V_{IN2} otherwise (assuming it is valid). If both V_{IN1} and V_{IN2} are in UVLO, then the higher voltage input is utilized to power the $INTV_{CC}$ rail.

A third linear regulator allows the $INTV_{CC}$ rail to be powered through the $EXTV_{CC}$ pin, which can be connected to the buck converter output (V_{BUS}) or an auxiliary rail with a voltage above 3.15V. When operating at high input voltages, the losses in the $INTV_{CC}$ regulator powered from the input voltage can become a significant factor in conversion efficiency and can even become a substantial source of power dissipation. A significant performance improvement can be obtained by connecting the $EXTV_{CC}$ input to the buck converter output so that the gate drive current is provided through the high-efficiency buck converter rather than the less-efficient linear regulator. This is of particular benefit at higher input voltages, lower output voltages, and higher switching frequencies. The $EXTV_{CC}$ pin is only utilized to power the $INTV_{CC}$ rail when the buck converter is operating.

EN1 and EN2 Feature

The LTM4719 uses the EN1 and EN2 pins to enable and disable the V_{BUS} and the V_{OUT} pins under normal operating conditions. When a rising voltage on EN2 crosses the active threshold, V_{OUT} turns on. When a voltage higher or lower than the threshold voltage of EN1 is applied, the V_{BUS} is turned on or off. When a falling voltage on EN2 crosses the inactive threshold, V_{OUT} turns off. The EN2 pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN2 pin as it passes through the threshold points.

Current Limit and Thermal Overload Protection

The LTM4719 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The LTM4719 is designed to the current limit when the output load reaches 320mA (typical). When the output load exceeds 320mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and the output current is restored to its nominal value.

V_{OC} Capacitor Selection

A minimum value of capacitance (C_{OC}) is required between V_{OC} and ground. This capacitor determines the I_{PEAK} pulse on and off durations. Its value should be selected based on the maximum current load at the V_{OC} pin and the I_{PEAK} setting. For best coulomb counter accuracy, it is recommended to have 50µs minimum I_{PEAK} on/off durations (see Equation *19*).

$$I_{PEAK\_ON}\ time(\min) = \frac{C_{OC} \times V_{HYST\_OC}}{I_{PEAK}}$$
$$I_{PEAK\_OFF}\ time(\min) = \frac{C_{OC} \times V_{HYST\_OC}}{I_{LOAD(MAX)}} \quad (19)$$

where V_{HYST_OC} is the voltage ripple value between V_{OC_HIGH} and V_{OC_LOW}. See *Figure 20*. The hysteresis is nominally set to 50mV.

For the 100mA I_{PEAK} setting and a maximum load current of 100mA, a 100µF C_{OC} capacitor is recommended. See *Table 17* for recommended C_{OC} values for the other I_{PEAK} settings.

Table 17.Recommended Minimum C_{OC} Values for Each I_{PEAK} Selection

IPK2	IPK1	IPK0	I_{PEAK} (mA)	RECOMMENDED C_{OC} (µF)
0	0	0	5	4.7
0	0	1	10	10
0	1	0	15	15
0	1	1	20	22
1	0	0	25	33
1	0	1	50	47
1	1	0	75	82
1	1	1	100	100

The V_{OC_HIGH} and V_{OC_LOW} thresholds are DC levels. The actual AC values seen in application will be outside of these levels due to finite delay in the hysteretic comparator.

Battery ESR and Voltage Ripple

The ripple voltage between V_{INC} and V_{OC} is also affected by the battery effective series resistance (ESR) value. For maximum coulomb counter accuracy, it is recommended to choose a battery such that ESR × I_{PEAK} is much smaller than the hysteresis. ESR × I_{PEAK} larger than the hysteresis generates very short I_{PEAK} pulses. If the duration is shorter than 3µs, the analog-to-digital converter (ADC) cannot correctly measure the V_{INC} and V_{OC} voltages. An alternative is to increase the V_{INC} capacitor to a minimum of 10µF. The input capacitor helps in increasing the I_{PEAK} pulse duration. If the V_{INC} capacitor is too big, the battery impedance measurement accuracy will suffer because it slows down V_{INC} voltage movement when I_{PEAK} turns on/off.

Maximum Load at V_{OC}

The maximum continuous load at V_{OC} cannot exceed I_{PEAK} or it will lose regulation. The maximum instantaneous load, however, can exceed I_{PEAK} for short durations, provided that the overall average load does not. During the “bursts”, the extra current is provided by the V_{OC} capacitor, and the V_{OC} voltage discharges slightly. The length of the burst and the amount of acceptable V_{OC} voltage droop will determine the required size of the V_{OC} capacitor.

For low voltage (V_{INC}~2V) operation with bit A[6] = 1, the maximum load is no longer limited by I_{PEAK}, but rather by the *Absolute Maximum Ratings* of the V_{OC} pin itself.

Bus Speed

The I^2C port is designed to operate at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I^2C compliant main device. It also contains input filters designed to suppress glitches.

START and STOP Conditions

A main bus signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from high to low while SCL is high. The main bus may transmit either the subordinate write address, or the subordinate read address. Once data is written to the LTM4719, the main bus may transmit a STOP condition which commands the LTM4719 to act upon its new command set. A STOP condition is sent by the main bus by transitioning SDA from low to high while SCL is high.

Byte Format

Each frame sent to or received from the LTM4719 must be eight bits long. The most significant bit (MSB) must be sent first. The eight bits are followed by an extra clock cycle for the acknowledge bit. The read or written data is always 2 bytes. The least significant byte is sent before the most significant byte.

Main and Subordinate Transmitters and Receivers

Devices connected to an I^2C bus may be classified as either the main or the subordinate device. A typical bus is composed of one or more main devices and several subordinate devices.

Some devices can act as either a main or a subordinate, but they may not change roles while a transaction is in progress.

The transmitter/receiver relationship is distinct from that of the main and subordinate. The transmitter is responsible for control of the SDA line during the eight-bit data portion of each frame. The receiver is responsible for control of the SDA line during the ninth and final acknowledge clock cycle of each frame.

All transactions are initiated by the main with a START or repeat START condition. The main controls the active (falling) edge of each clock pulse on SCL, regardless of its status as transmitter or receiver. The subordinate device never brings SCL low.

The LTM4719 does not clock stretch and will never hold SCL low under any circumstance.

The main device begins each I²C transaction as the transmitter and the subordinate device begins each transaction as the receiver. For bus write operations, the main device acts as a transmitter, and the subordinate device acts as a receiver for the duration of the transaction. For bus read operations, the main and subordinate devices exchange transmit/receive roles following the address frame for the remainder of the transaction.

Acknowledge

The acknowledge signal (ACK) is used for handshaking between the transmitter and receiver. When the LTM4719 is written to, it acknowledges its write address as well as the subsequent data bytes as a subordinate receiver. When it is read from, the LTM4719 acknowledges its read address as a subordinate receiver. The LTM4719 then changes to a subordinate transmitter, and the main receiver may optionally acknowledge receipt of the following data byte from the LTM4719.

The acknowledge-related clock pulse is always generated by the main bus. The transmitter (main or subordinate) releases the SDA line (high) during the acknowledge clock cycle.

The receiver (subordinate or main) pulls down the SDA line during the acknowledge clock pulse so that it is a stable low during the high period of this clock pulse.

When the LTM4719 is read from, it releases the SDA line after the eighth data bit so that the main device may acknowledge receipt of the data. The I²C specification calls for a not acknowledge (NACK) by the main receiver following the last data byte during a read transaction. Upon receipt of the NACK, the subordinate transmitter is instructed to release control of the bus. Because the LTM4719 transmits two bytes of data under all circumstances, a main acknowledging or not acknowledging the data sent by the LTM4719 has no consequence. The LTM4719 will release the bus after 2 bytes in either case.

Subordinate Address

The LTM4719 responds to a 7-bit address, which has been factory-programmed to 1100100[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTM4719, and 1 when reading data from it. Considering the address is an 8-bit word, then the write address is 0xC8, and the read address is 0xC9.

The LTM4719 will acknowledge both its read and write addresses.

Sub-Addressed Access

The LTM4719 has five read registers, two write registers, and one read/write register. They are accessed by the I²C port through a sub-addressed pointer system where each sub-address value points to one of the eight registers within the LTM4719. See *Table 8* for sub-address information.

The sub-address pointer is always the first byte written immediately following the LTM4719 write address during bus write operations. The sub-address pointer value persists after the bus write operation and will determine which data byte is returned by the LTM4719 during any subsequent bus read operations. See *Figure 24*.

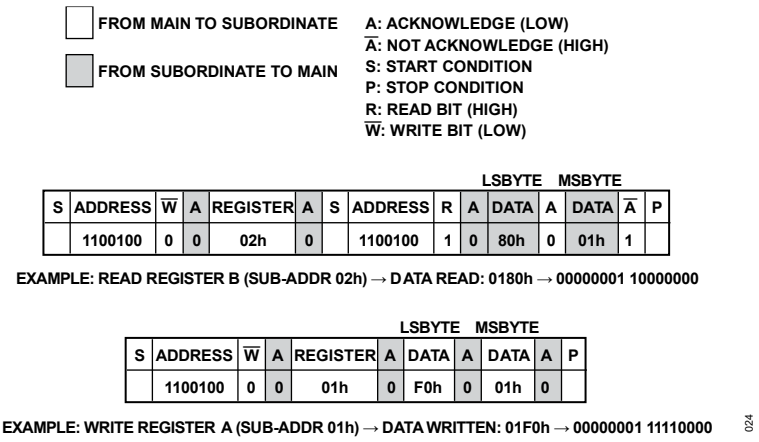


Figure 24. I²C Reading and Writing Protocol

Bus Write Operation

The main bus initiates communication with the LTM4719 with a START condition and the LTM4719's write address. If the address matches that of the LTM4719, the LTM4719 returns an acknowledge. The main bus should then deliver the sub-address. The sub-address value is transferred to a special pointer register within the LTM4719 upon the return of the sub-address acknowledge bit by the LTM4719.

If the main bus wishes to continue the write transaction, it may then deliver the 2 data bytes. The data bytes are transferred to an internal pending data register at the location of the sub-address pointer when the LTM4719 acknowledges both data bytes. The acknowledge bit is sent at the end of each byte. The LTM4719 is then ready to receive a new sub-address, optionally repeating the [SUB-ADDRESS] [DATA-byte1] [DATA-byte2] cycle indefinitely. The main bus may terminate communication with the LTM4719 with either a repeat START or a STOP condition. If a repeat START condition is initiated by the main bus, the LTM4719, or any other chip on the I²C bus, can then be addressed.

The LTM4719 will remember, but not act on, the last input of valid data that it received at each sub-address location.

This cycle can also continue indefinitely. Once all chips on the bus have been addressed, and sent valid data, a global STOP can be sent, and the LTM4719 will immediately update all its command registers with the most recent pending data that it had previously received.

Bus Read Operation

Only one sub-addressed data register is accessible during each bus read operation. The data returned by the LTM4719 is from the data register pointed to by the contents of the sub-address pointer register. The pointer register contents are determined by the previous bus write operation. In preparation for a bus read operation, it may be advantageous for a main bus to prematurely terminate a write transaction with a STOP or repeat START condition. The last transmitted byte then represents a pointer to the register of interest for the subsequent bus read operation.

The main bus reads status data from the LTM4719 with a START or repeat START condition followed by the LTM4719 read address. If the read address matches that of the LTM4719, the LTM4719 returns an acknowledge.

Following the acknowledgment of its read address, the LTM4719 returns one bit of status information for each of the next eight clock cycles from the register selected by the sub-address pointer (LSB first data byte). The SDA line stays high for a 1-clock cycle after the first 8 bits and after LTM4719 returns the second data byte (MSB). Additional clock cycles from the main bus after the 2 data bytes have been read will leave the SDA line high. The LTM4719 will never acknowledge any bytes during a bus read operation except for its read address.

To read a different register, a write transaction must be initiated with a START or repeat START followed by the LTM4719 write address and sub-address pointer byte before the read transaction may be repeated.

When the contents of the sub-address pointer register point to write-only Registers (A, H), the data returned in a bus read operation is the pending command data at that location if it had been modified since the last STOP condition. After a STOP condition, all pending data is copied to the command registers for immediate effect.

When the contents of the sub-address pointer register point to the writable and readable Register B, the data returned in a bus read operation is data at that location, not the pending command data from the previous write operation. After a STOP condition, all pending data is copied to the command registers for immediate effect, and a subsequent read operation can read the effect.

When the contents of the sub-address pointer register point to the read-only Registers (C, D, E, F, G), the data returned is a snapshot of the state of the LTM4719 at a particular instant in time. If no interrupt requests are pending, the status data is sampled when the LTM4719 acknowledges its read address, just before the LTM4719 begins data transmission during a bus read operation. If the read address is acknowledged during an ADC conversion or IPEAK pulse the status data reported is the one from the previous ADC conversion or the end of the last I_{PEAK} pulse.

When an alarm/fault occurs, the $\overline{IRQ}$ pin is driven low and data is latched in bits C[3:0] of status Register C at that moment. Any subsequent read operation from Register C will return these frozen C[3:0] bits to facilitate the determination of the cause of the interrupt request.

After the main bus clears the LTM4719 interrupt request, bits C[3:0] of the status latches are cleared. Bus read operations will then again return either a snapshot of the data at the time of the read address acknowledges, after an ADC conversion, after the I_{PEAK} pulse, or at the time of the next interrupt assertion, whichever comes first.

Derating Curves

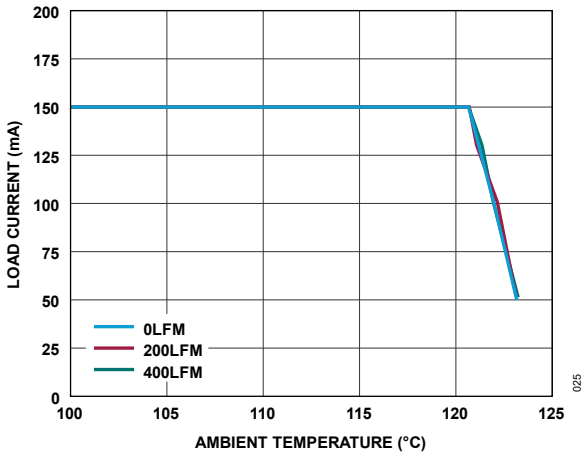


Figure 25. Derating Curve, 12V to 1.8V

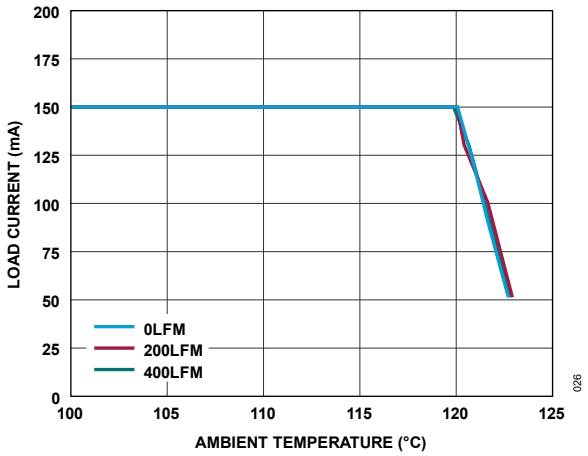


Figure 26. Derating Curve, 12V to 3.3V

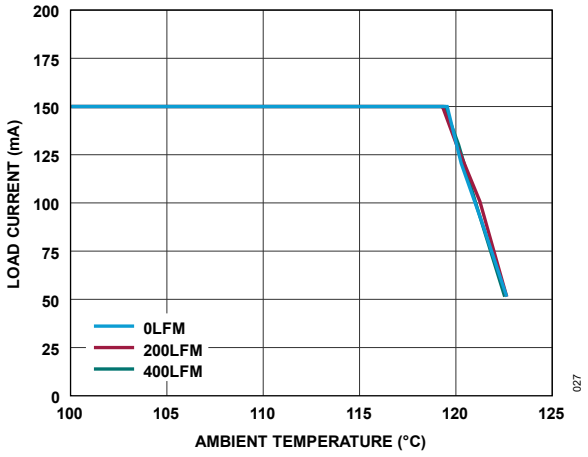


Figure 27. Derating Curve, 12V to 5V

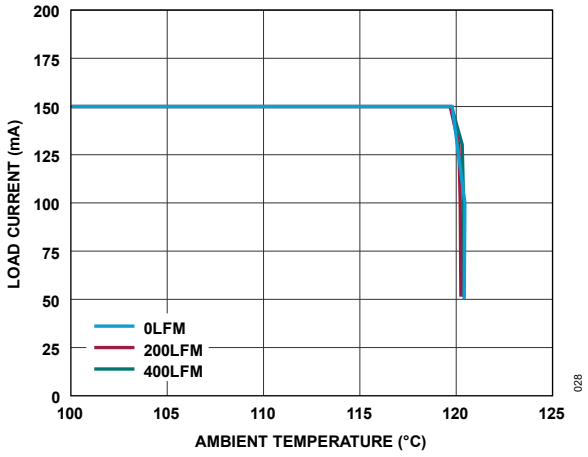


Figure 28. Derating Curve, 24V to 1.8V

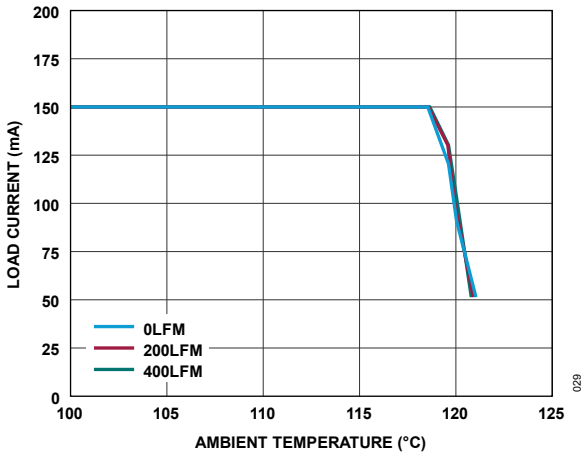


Figure 29. Derating Curve, 24V to 3.3V

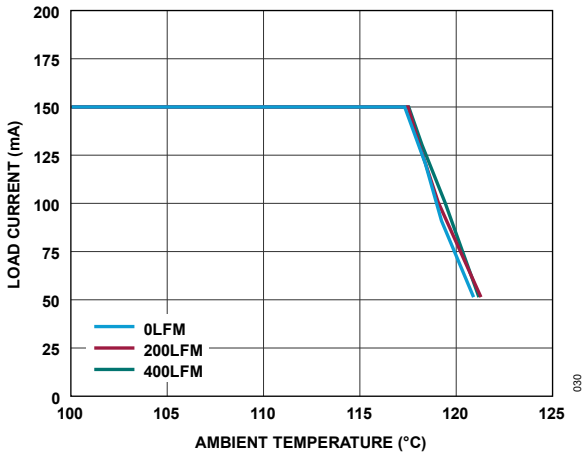


Figure 30. Derating Curve, 24V to 5V

PCB Layout Guidelines

Special attention must be paid to the Printed circuit board (PCB) layout to ensure a stable, noise-free, and efficient application circuit. *Figure 31* shows a representative PCB layout to outline some of the primary considerations. A few key guidelines are as follows.

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes to the inductor, bus capacitor, output capacitor, and V_{IN1}/V_{IN2} bypass capacitors as short and as wide as possible. Capacitor ground connections should be through down the ground plane by way of the shortest route possible. The bypass capacitors on $INTV_{CC}$ should be placed as close to the µModule as possible and should have the shortest possible return paths to ground.
2. Connections to the V_{IN1}, V_{IN2}, and SW pins should be made as wide as possible to reduce the series impedance. This improves efficiency and reduces the thermal resistance.
3. Keep the routes connecting to the high-impedance noise-sensitive inputs (FB1, RT, V_{SET1}, V_{SET2}) as short as possible to minimize noise pickup.
4. The connection to the SV_{IN1}, SV_{IN2} should be separate from the connection to the V_{IN1} and V_{IN2}. SV_{IN1} and SV_{IN2} have separate 0.1µF bypass capacitors installed inside the µModule. This prevents noise from the V_{IN1} and V_{IN2} traces from being coupled into the sensitive SV_{IN1} and SV_{IN2} pins.

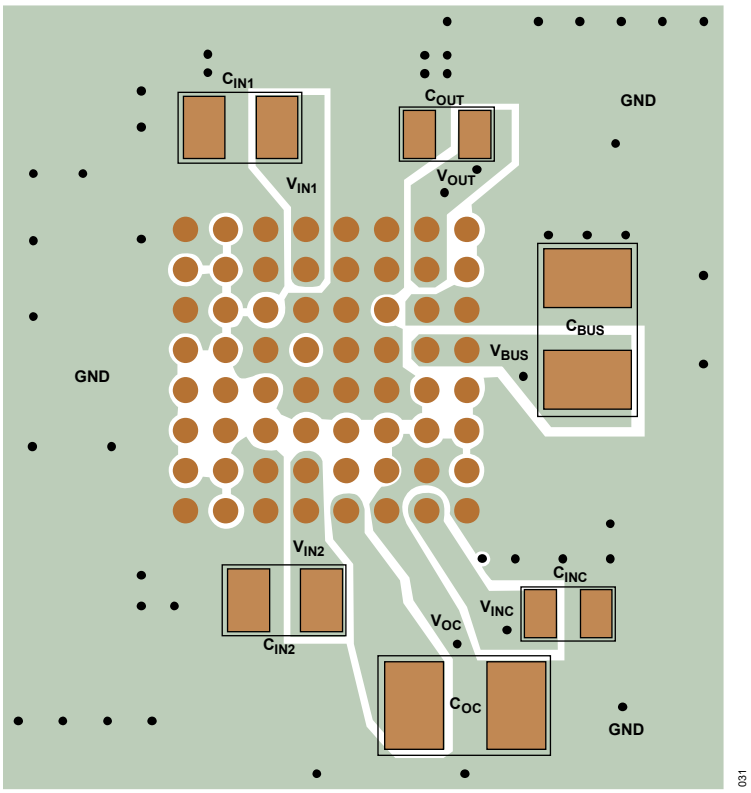


Figure 31. Recommended PCB Layout

Typical Applications

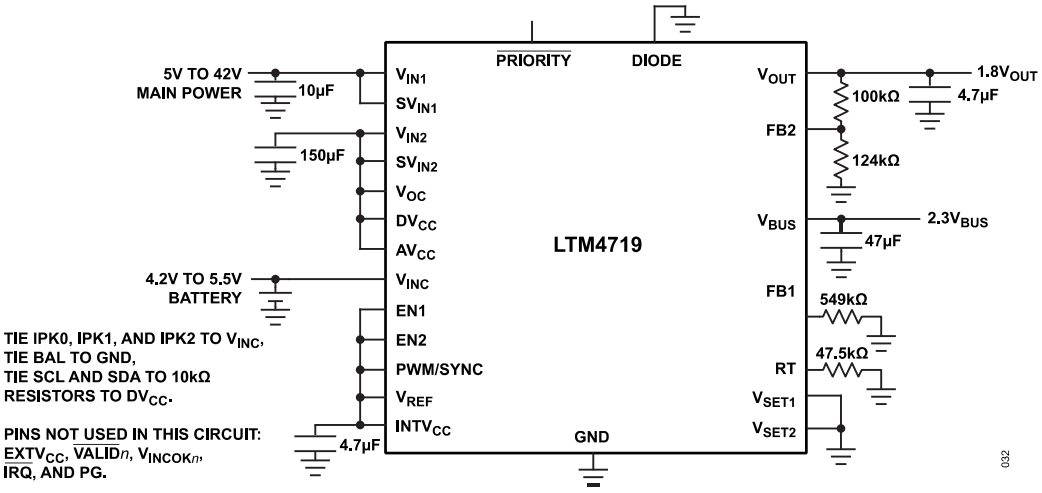


Figure 32. 700kHz, 1.8V, 150mA Supply from Main Power and Backup Battery

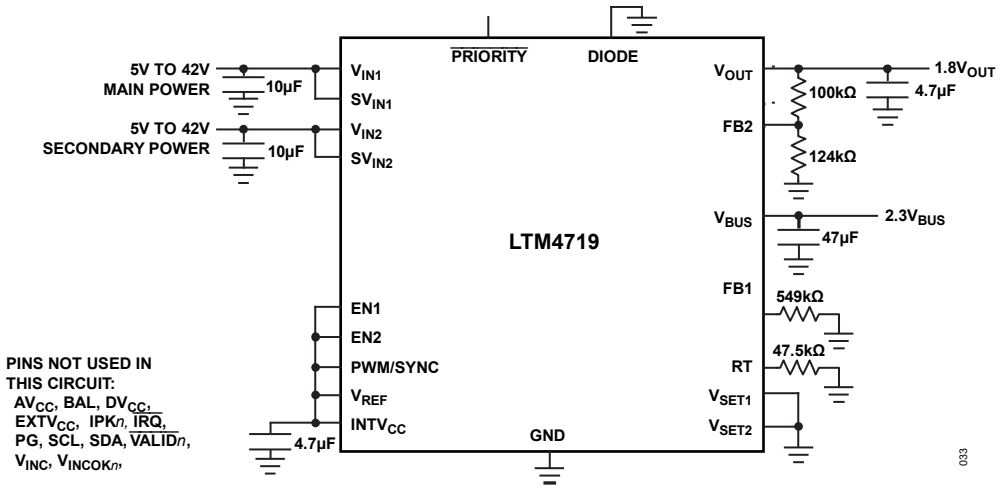


Figure 33. 700kHz, 1.8V, 150mA Supply from Main/Secondary Power, No Battery SoH Monitor

Related Parts

Table 18. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM4693	Ultrathin, low V_{IN}, 2A buck-boost µModule regulator	$2.6V \le V_{IN} \le 5.5V$, $1.8V \le V_{OUT} \le 5.5V$, 3.5mm × 4mm × 1.25mm LGA
LTM8083	$36V_{IN}$, 1.5A buck-boost µModule regulator with programmable current limit	$3V \le V_{IN} \le 36V$, $1V \le V_{OUT} \le 36V$, 6.25mm × 6.25mm × 2.22mm BGA
LTM8074	$40V_{IN}$, 1.2A Silent Switcher µModule regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 12V$, 4mm × 4mm × 1.82mm BGA

OUTLINE DIMENSIONS

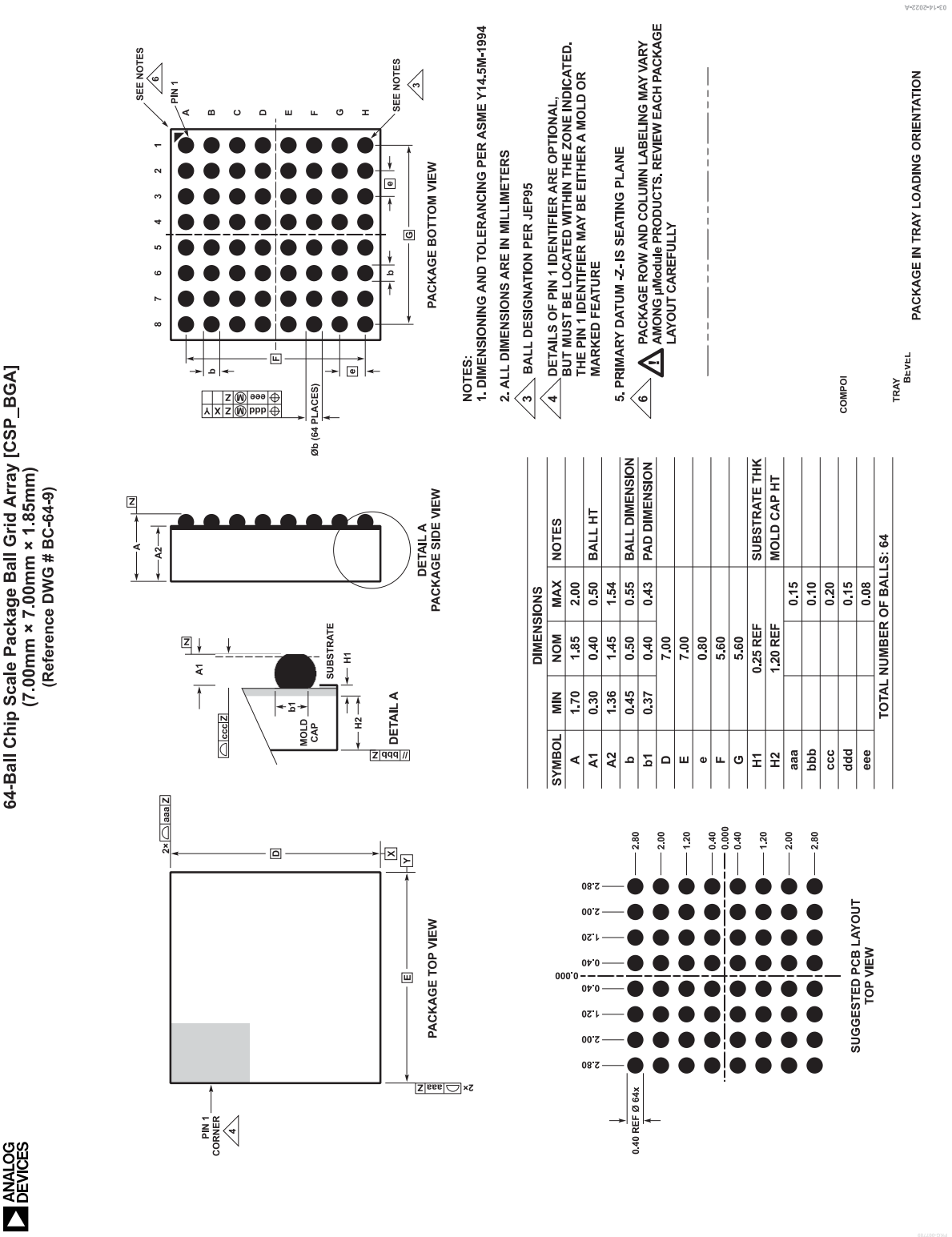


Figure 34.64-Pin BGA, 7mm × 7mm × 1.85mm

ORDERING GUIDE

Table 19.Ordering Guide

MODEL	TEMPERATURE RANGE [1]	PACKAGE DESCRIPTION	PACKAGE OPTION
LTM4719EY#PBF	–40°C to 125°C	Part marking: 4719 SAC305 (RoHS) pad finish* e1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*64-Pin BGA, 7mm × 7mm × 1.85mm*
LTM4719IY#PBF	–40°C to 125°C	Part marking: 4719 SAC305 (RoHS) pad finish* e1 finish code Moisture sensitivity level 4 (MSL 4) rated device	*64-Pin BGA, 7mm × 7mm × 1.85mm*

1 The LTM4719 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4719E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specification over the –40°C to 125 °C operation junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4719I specifications are guaranteed over the –40°C to 125 °C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by the specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *Pad finish code is per IPC/JEDEC J-STD-609. The device temperature grade is indicated by a label on the shipping container.This product is not recommended for second-side reflow. This product is moisture sensitive. For more information, go to ***Recommended LGA and BGA PCB assembly and manufacturing procedures.***

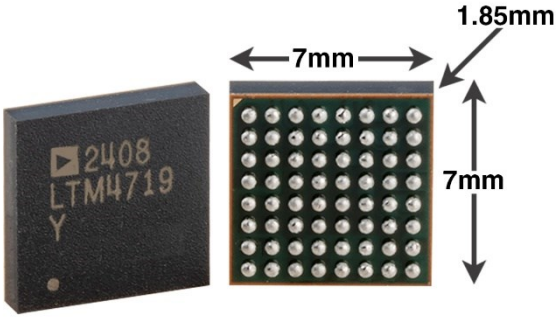
LGA and BGA package and tray drawings.

Table 20.Evaluation Boards

PART NUMBER	DESCRIPTION
EVAL-LTM4719-AZ	The evaluation board features the LTM4719, a 42V dual input, low noise 150mA µModule regulator with I^2C battery health monitor.

SELECTOR GUIDE

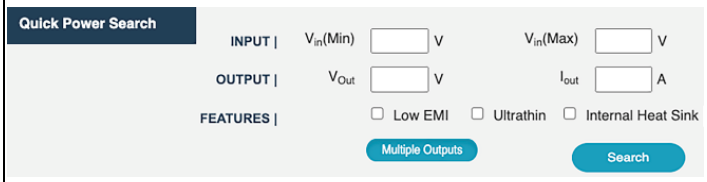
Package Photos



(Part Marking Is Laser Mark)

Design Resources

Table 21.Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	Design: ▶ Selector guides ▶ Evaluation boards and Gerber files ▶ Free simulation tools	Manufacturing: ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining, and sequencing, and feature EEPROM for storing user configurations and fault logging.	