Data Sheet

LTM4640

20V_{IN}, 20A Step-Down DC-to-DC µModule Regulator

FEATURES

- Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)
- Wide Input Voltage Range: 3.1V to 20V
- 0.6V to 3.3V Output Voltage
- Up to 20A DC output current
- ±1.5% Maximum Total DC Output Voltage Error
- Differential Remote Sensing Amplifier
- Fast Transient Response
- External Frequency Synchronization
- Multiphase Parallel Current Sharing with up to 4 × LTM4640s
- Power Good Indicator
- Overvoltage and Overtemperature Protection
- *49-Pin, 6.25mm × 6.25mm × 5.07mm,* BGA package
- Pin compatible with *LTM4626*, *LTM4638*, and *LTM4657*

APPLICATIONS

- Telecom, Datacom, Networking, and Industrial Equipment
- Medical Diagnostic Equipment
- Data Storage Rack Units and Cards
- Test and Debug Systems

GENERAL DESCRIPTION

The ***LTM4640*** is a complete 20A step-down switching mode power µModule® (micromodule) regulator in a tiny 6.25mm × 6.25mm × 5.07mm BGA package. The package includes the switching controller, the power MOSFETs, an inductor, and the supporting components. Operating over an input voltage range of 3.1V to 20V, the LTM4640 supports an output voltage range of 0.6V to 3.3V, set by a single external resistor. Its high-efficiency design delivers up to 20A continuous output current. Only bulk input and output capacitors are needed.

The LTM4640 supports selectable discontinuous-conduction mode (DCM) operation and output voltage tracking for supply rail sequencing. Its high switching frequency and controlled on-time valley current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. Fault protection features include overvoltage and overtemperature protection.

The LTM4640 is available with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

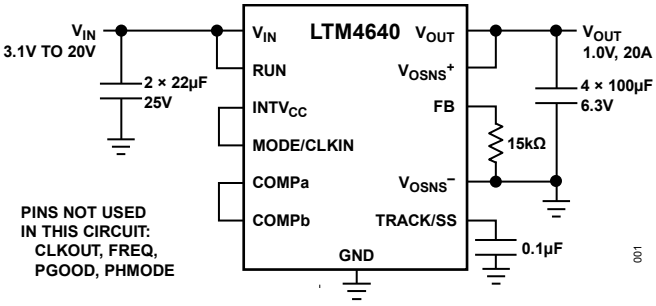

Figure 1. 20A, 1V_{OUT} DC-to-DC Step-Down µModule Regulator

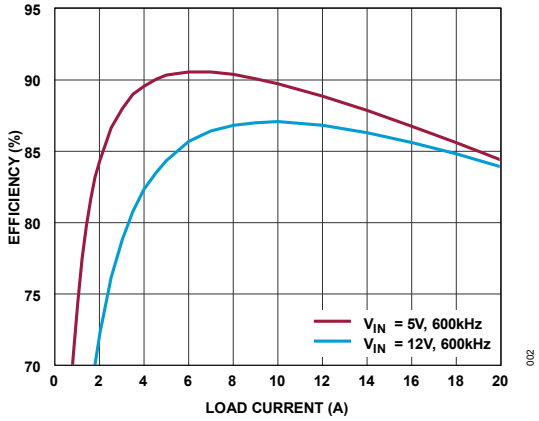

Figure 2. 1V_{OUT} Efficiency vs. Load Current

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REVISION HISTORY

10/2024 - Rev. 0: Initial Release.

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C. V_{IN} = 12V per the typical application shown in *Figure 1*, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Switching Regulator Section (per Channel)							
Input DC voltage	V_{IN}		–40°C ≤ T_J ≤ 125°C	3.1		20	V
Output voltage range	V_{OUT}		–40°C ≤ T_J ≤ 125°C	0.6		3.3	V
Output voltage, total variation with line and load	$V_{OUT(DC)}$	R_{FB} = 6.65kΩ, MODE = $INTV_{CC}$, I_{OUT} = 0A to 15A [2]	–40°C ≤ T_J ≤ 125°C	1.477	1.50	1.523	V
		R_{FB} = 6.65kΩ, MODE = $INTV_{CC}$, I_{OUT} = 0A to 20A		1.477	1.50	1.523	V
RUN pin ON threshold	V_{RUN}	V_{RUN} rising		1.15	1.25	1.35	V
Input supply bias current	$I_{Q(VIN)}$	V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$, I_{OUT} = 0A			100		mA
		V_{IN} = 12V, V_{OUT} = 1.5V, MODE = GND, I_{OUT} = 0.1A			18		mA
		Shutdown, RUN = 0, V_{IN} = 12V			20		µA
Input supply current	$I_{S(VIN)}$	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 20A			3.25		A
Output continuous current range	$I_{OUT(DC)}$	V_{IN} = 12V, V_{OUT} = 1.5V		0		20	A
Line regulation accuracy	ΔV_{OUT} (Line)/V_{OUT}	V_{OUT} = 1.5V, V_{IN} = 3.1V to 20V, I_{OUT} = 0A	–40°C ≤ T_J ≤ 125°C		0.01	0.1	%/V
Load regulation accuracy	ΔV_{OUT} (Load)/V_{OUT}	V_{OUT} = 1.5V, I_{OUT} = 0A to 15A	–40°C ≤ T_J ≤ 125°C		0.1	0.5	%
		V_{OUT} = 1.5V, I_{OUT} = 0A to 20A			0.1	0.5	%
Turn-on overshoot	$\Delta V_{OUT(START)}$	I_{OUT} = 0A, C_{OUT} = 4 × 220µF ceramic, V_{IN} = 12V, V_{OUT} = 1.5V [5]			30		mV
Turn-on time	t_{START}	No load, TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V			1		ms
Peak-to-peak output voltage deviation for dynamic load step	ΔV_{OUTLS}	Load: 0% to 50% to 0% of full load, 10A/µs slew rate, C_{OUT} = 4 × 220µF ceramic, V_{IN} = 12V, V_{OUT} = 1.5V [5]			160		mV
Settling time for dynamic load step	t_{SETTLE}	Load: 0% to 50% to 0% of full load, 10A/µs slew rate, C_{OUT} = 4 × 220µF ceramic, V_{IN} = 12V, V_{OUT} = 1.5V [5]			60		µs

(T_A = 25°C. V_{IN} = 12V per the typical application shown in *Figure 1*, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output current limit	I_{OUTPK}	V_{IN} = 12V, V_{OUT} = 1.5V			26		A
Voltage at FB pin	V_{FB}	I_{OUT} = 0A, V_{OUT} = 1.5V	–40°C ≤ T_J ≤ 125°C	0.594	0.60	0.606	V
Current at FB pin	I_{FB}	[3]				±30	nA
Resistor between V_{OSNS}^+ and FB pins	R_{FBHI}				10		kΩ
Track pin soft start pull-up current	$I_{TRACK/SS}$	TRACK/SS = 0V			6	10	µA
V_{IN} Undervoltage lockout	$V_{IN(UVLO)}$	V_{IN} falling		2.45	2.6	2.75	V
		V_{IN} hysteresis			350		mV
Minimum on-time	$t_{ON(MIN)}$	[3]			25		ns
Minimum off-time	$t_{OFF(MIN)}$	[3]			50		ns
PGOOD trip level	V_{PGOOD}	V_{FB} with respect to set output V_{FB} ramping negative		–12	–8	–5	%
		V_{FB} with respect to set output V_{FB} ramping positive		5	8	12	%
PGOOD leakage	I_{PGOOD}	V_{PGOOD} = $INTV_{CC}$, V_{FB} = 0.6V				2	µA
PGOOD voltage low	V_{PGL}	I_{PGOOD} = 1mA			0.02	0.1	V
Internal V_{CC} voltage	V_{INTVCC}	V_{IN} = 4V to 20V		3.2	3.3	3.4	V
Oscillator frequency	f_{OSC}				600		kHz

The LTM4640, including the E-grade and I-grade parts (see *Table 14*), is tested under pulsed load conditions such as that $T_J \approx T_A$. The LTM4640E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4640I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

[1]

[2] See *Thermal Considerations and Output Current Derating* for different V_{IN}, V_{OUT}, and T_A conditions.

[3] 100% tested at wafer level.

The LTM4640, includes overtemperature protection that is intended to protect the device during momentary overload conditions. The junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair the device's reliability.

[4]

[5] Guaranteed by design. Validated from bench measurements.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}	–0.3V to 22V
V_{OUT}	–0.3V to 3.6V
$INTV_{CC}$	–0.3V to 3.6V
RUN	–0.3V to 20V
PGOOD, FREQ, COMPa, COMPb, PHMODE, CLKOUT, FB	–0.3V to 3.6V
MODE/CLKIN, TRACK/SS	–0.3V to $INTV_{CC}$
V_{OSNS}^+	–0.3V to 3.6V
V_{OSNS}^-	–0.3V to 0.3V
Internal operating temperature range [1, 2]	–40°C to 125°C
Storage temperature range	–55°C to 125°C
Peak solder reflow body temperature	250°C

1 The LTM4640, including the E-grade and I-grade parts (see *Table 14*), is tested under pulsed load conditions such as that $T_J \approx T_A$. The LTM4640E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4640I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

2 The LTM4640, includes overtemperature protection that is intended to protect the device during momentary overload conditions. The junction temperature exceeds 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair the device's reliability.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to Printed Circuit Board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 3. LTM4640 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±2500	3A
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

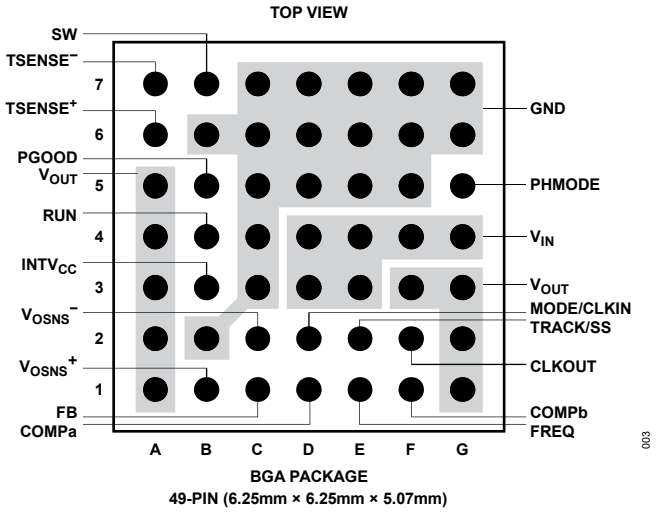


Figure 3. Pinout Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
A1–A5, F3, G1–G3	V_{OUT}	Power Output Pins of the Switching Mode Regulator. Apply output load between these pins and GND. Recommend placing output decoupling capacitance directly between these pins and the GND. See the *Applications Information* section for paralleling outputs.
A6	$TSENSE^+$	Temperature Monitor Pin. An internal diode-connected NPN transistor is placed between $TSENSE^+$ and $TSENSE^-$ pins. See the *Applications Information* section for details.
A7	$TSENSE^-$	Low-Side of the Internal Temperature Monitor.
B1	V_{OSNS}^+	Positive Input to the Differential Remote Sense Amplifier. Internally, this pin is connected to the FB pin with a 10kΩ ±0.5% precision resistor. See the *Applications Information* section for details.
B2, B6, C3–C7, D5–D7, E5–E7, F5–F7, G6–G7	GND	Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect the GND pins together.

PIN CFG 1	NAME	DESCRIPTION
B3	$INTV_{CC}$	Internal 3.3V Regulator Output of the Switching Mode Regulator Channel. The internal power drivers and control circuits are powered by this voltage. The LTM4640 has an internal 2.2µF decoupling capacitor. No external decoupling capacitor is required.
B4	RUN	Run Control Input Pin. Enable regulator operation by connecting the RUN pin above 1.35V. Connecting it below 1.1V shuts down the specific regulator channel.
B5	PGOOD	Output Power Good Pin with Open-Drain Logic. The PGOOD pin is pulled to ground when the voltage on the FB pin is out of ±8% of the internal 0.6V reference.
B7	SW	Switching node of each channel that is used for testing purposes. Also, an R-C snubber network is applied to reduce or eliminate switch node ringing. Otherwise, leave it floating. See the *Applications Information* section for details.
C1	FB	The Negative Input of the Error Amplifier for the Switching Mode Regulator. This pin is internally connected to V_{OSNS}^+ with a 10kΩ precision resistor. The output voltage is programmed with an additional resistor between FB and V_{OSNS}^- pins. In a PolyPhase® operation, connect the FB pins together to allow for a parallel operation. See the *Applications Information* section for details.
C2	V_{OSNS}^-	Negative Input to the Differential Remote Sense Amplifier. Connect an external resistor between FB and V_{OSNS}^- pins to set the output voltage of the specific channel. See the *Applications Information* section for details.
D1	COMPa	Current control threshold and error amplifier compensation point of the switching mode regulator channel. The internal current comparator threshold is linearly proportional to this voltage. Connect the COMPa pins from different channels together for a parallel operation. The device is internally compensated. Connect to the COMPb pin to use the internal compensation. Or connect to a Type-II C-R-C network to use customized compensation.
D2	MODE/CLKIN	Discontinuous Mode Select Pin and External Synchronization Input to Phase Detector. Connect MODE/CLKIN to GND for discontinuous-conduction mode (DCM) operation. Floating MODE/CLKIN or connecting it to a voltage above 1V selects forced continuous mode (FCM). Furthermore, connecting MODE/CLKIN to an external clock synchronizes the system clock to the external clock and puts the part in FCM. See the *Applications Information* section for details.
D3–D4, E3–E4, F4, G4	V_{IN}	Power input pins connect to the drain of the internal top MOSFET, and the signal V_{IN} to the internal 3.3V regulator for the control circuitry for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of the V_{IN} pins and the GND pins.
E1	FREQ	Switching Frequency Program Pin. The frequency is set internally to 600kHz. An external resistor is placed from this pin to GND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the *Applications Information* section for frequency adjustment.
E2	TRACK/SS	Output Tracking and Soft Start Pin of the Switching Mode Regulator. The TRACK/SS pin allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function

PIN CFG 1	NAME	DESCRIPTION
		stops, and the internal reference resumes control of the error amplifier. There's an internal 6µA pull-up current from $INTV_{CC}$ on this pin, putting a capacitor here provides a soft start function. See the *Applications Information* section for details.
F1	COMPb	Internal Loop Compensation Network. Connect to COMPa pin to use the internal compensation in the majority of applications.
F2	CLKOUT	Output Clock Signal for PolyPhase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the respective PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See the *Applications Information* section for details.
G5	PHMODE	Control Input to the Phase Selector of the Switching Mode Regulator. It determines the phase relationship between the internal oscillator and CLKOUT. Connect it to $INTV_{CC}$ for a 2-phase operation, connect it to GND for a 3-phase operation, and connect it to $INTV_{CC}/2$ for a 4-phase operation. See the *Applications Information* section for details.

Table 5. LTM4640 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1–G4							
A1	V_{OUT}	A2	V_{OUT}	A3	V_{OUT}	A4	V_{OUT}
B1	$V_{OSNS}+$	B2	GND	B3	$INTV_{CC}$	B4	RUN
C1	FB	C2	$V_{OSNS}-$	C3	GND	C4	GND
D1	COMPa	D2	MODE/CLKIN	D3	V_{IN}	D4	V_{IN}
E1	FREQ	E2	TRACK/SS	E3	V_{IN}	E4	V_{IN}
F1	COMPb	F2	CLKOUT	F3	V_{OUT}	F4	V_{IN}
G1	V_{OUT}	G2	V_{OUT}	G3	V_{OUT}	G4	V_{IN}
A5–G7							
A5	V_{OUT}	A6	$TSENSE^+$	A7	$TSENSE^-$		
B5	PGOOD	B6	GND	B7	SW		
C5	GND	C6	GND	C7	GND		
D5	GND	D6	GND	D7	GND		
E5	GND	E6	GND	E7	GND		
F5	GND	F6	GND	F7	GND		
G5	PHMODE	G6	GND	G7	GND		

TYPICAL PERFORMANCE CHARACTERISTICS

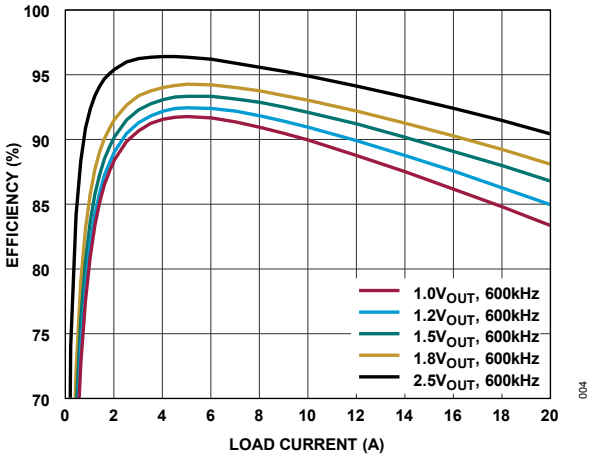


Figure 4. Efficiency vs. Load Current from $3.3V_{IN}$

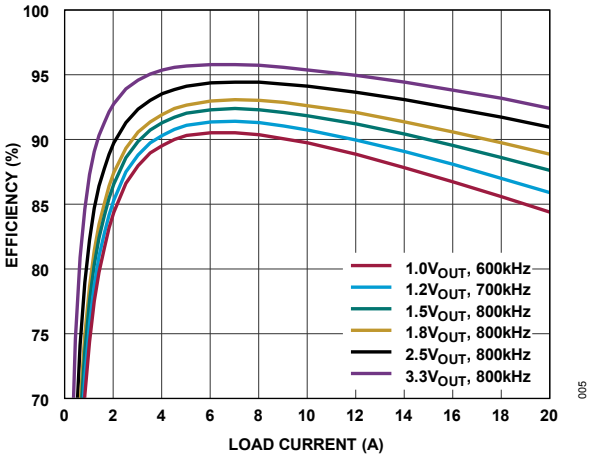


Figure 5. Efficiency vs. Load Current from $5V_{IN}$

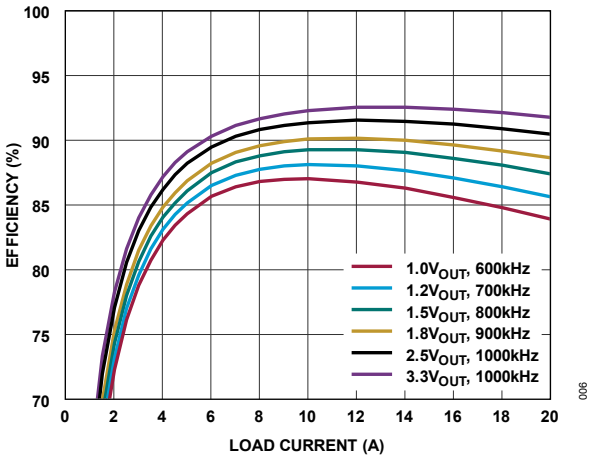
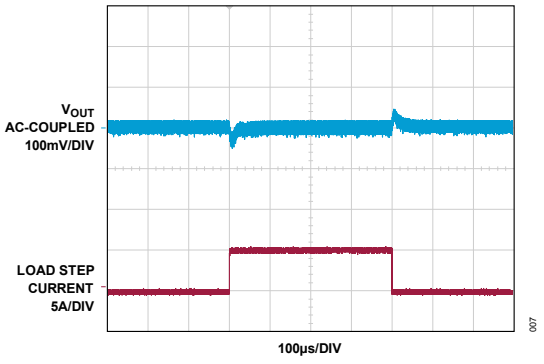
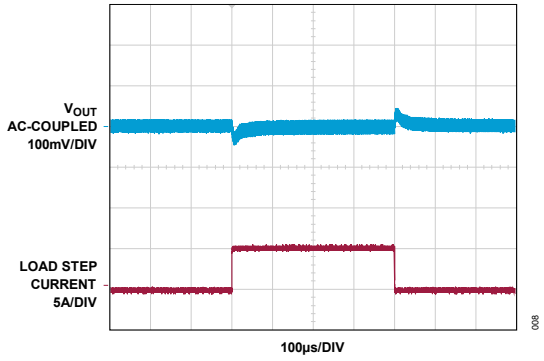


Figure 6. Efficiency vs. Load Current from $12V_{IN}$



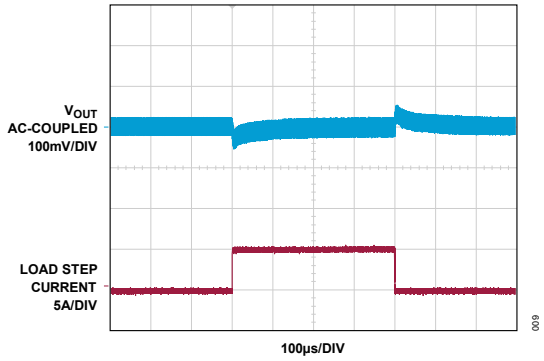
V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 600kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, 10A ~ 15A (25%) LOAD STEP
10A/µs SLEW RATE

Figure 7. $1V_{OUT}$ Transient Response



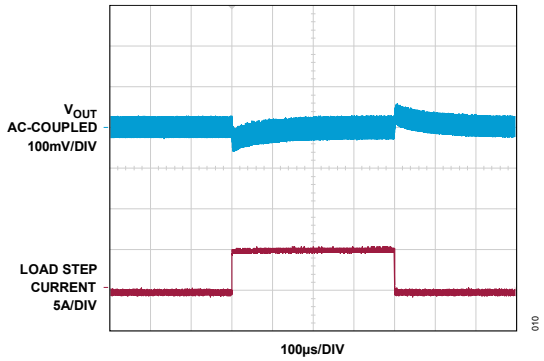
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, 10A ~ 15A (25%) LOAD STEP
10A/µs SLEW RATE

Figure 8. $1.5V_{OUT}$ Transient Response



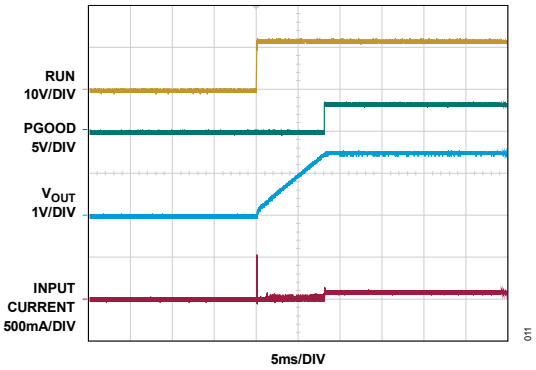
V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1MHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, 10A ~ 15A (25%) LOAD STEP
10A/µs SLEW RATE

Figure 9. $2.5V_{OUT}$ Transient Response



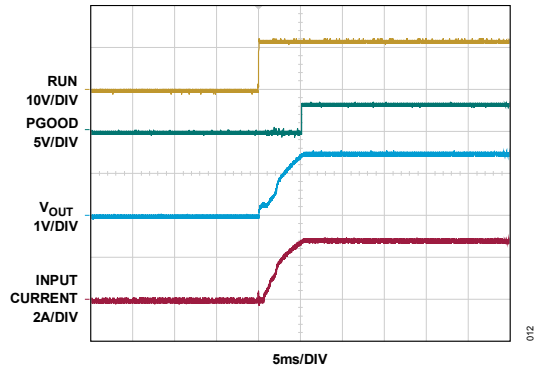
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, 10A ~ 15A (25%) LOAD STEP
10A/µs SLEW RATE

Figure 10. 3.3V_{OUT} Transient Response



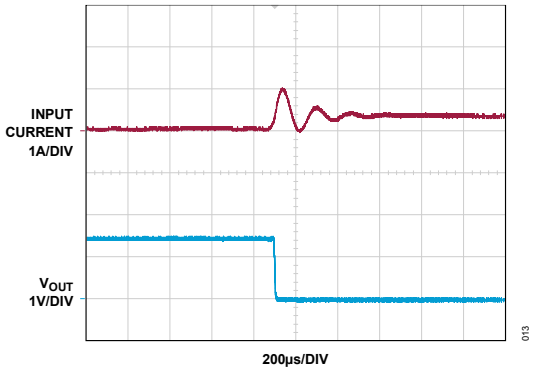
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, C_{SS} = 0.1µF

Figure 11. Startup Waveform without Load Current



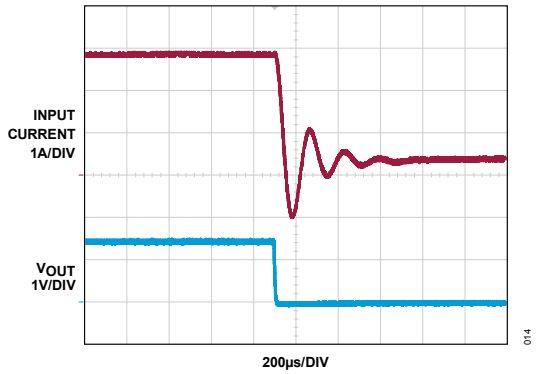
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, C_{SS} = 0.1µF

Figure 12. Startup Waveform with 20A Load Current



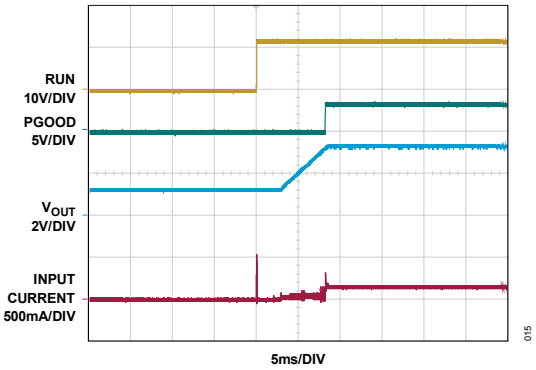
V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF

Figure 13. Output Short-Circuit Waveform without Load Current Applied



V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF

Figure 14. Output Short-Circuit Waveform with 20A Load Current Applied



V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 800kHz
C_{OUT} = 4 × 220µF + 2 × 2.2µF + 1µF CERAMIC CAPACITOR
INTERNAL COMPENSATION, COMPa CONNECT TO
COMPb, C_{FF} = 100pF, C_{SS} = 0.1µF

Figure 15. Startup into Prebiased Output

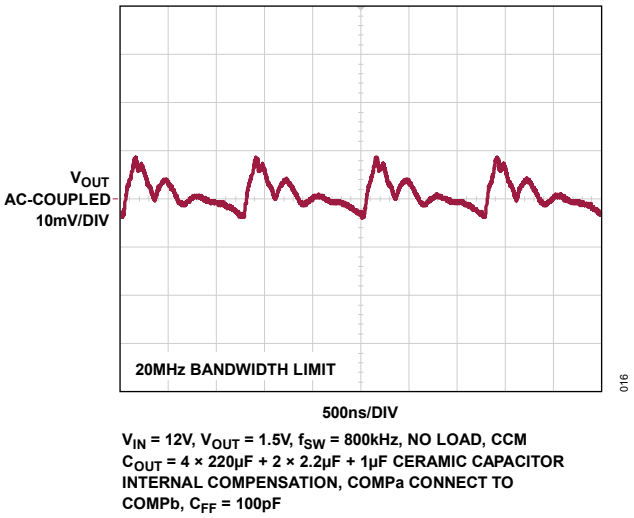


Figure 16. Steady-State Output Voltage Ripple

THEORY OF OPERATION

LTM4640 Overview

The LTM4640 is a standalone non-isolated switch mode DC-to-DC power supply. The LTM4640 can deliver up to 20A DC output current with few external input and output capacitors. This µModule provides precisely regulated output voltage adjustable between 0.6V to 3.3V through one external resistor over an input voltage range of 3.1V to 20V. A typical application schematic is shown in *Figure 37*.

The LTM4640 contains an integrated controlled on-time valley current mode controller, the power MOSFETs, an inductor, and other supporting discrete components. The default switching frequency is 600kHz. For noise-sensitive applications, the switching frequency can be adjusted by external resistors, and the µModule regulator can be externally synchronized to a clock within ±30% of the set frequency. See the *Applications Information* section for details.

With current mode control and internal feedback loop compensation, the LTM4640 has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all the ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. Internal output overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±8% window around the regulation point. Continuous operation is forced during overvoltage and undervoltage conditions, except during startup when the TRACK pin is ramping up to 0.6V.

Furthermore, to protect the internal power MOSFET devices against transient voltage spikes, the LTM4640 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 24.5V, the regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator does not execute its soft start function when exiting an overvoltage condition.

A multiphase operation can easily be employed with the synchronization and phase mode controls. Up to four phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin to

different levels. The LTM4640 has MODE/CLKIN and CLKOUT pins for PolyPhase operation of multiple devices or frequency synchronization.

Pulling the RUN pin to GND forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, discontinuous-conduction mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous-conduction mode (CCM) by pulling the MODE/CLKIN pin to GND. The TRACK/SS pin is used for power supply tracking and soft start programming. See the *Applications Information* section for details.

Simplified Block Diagram

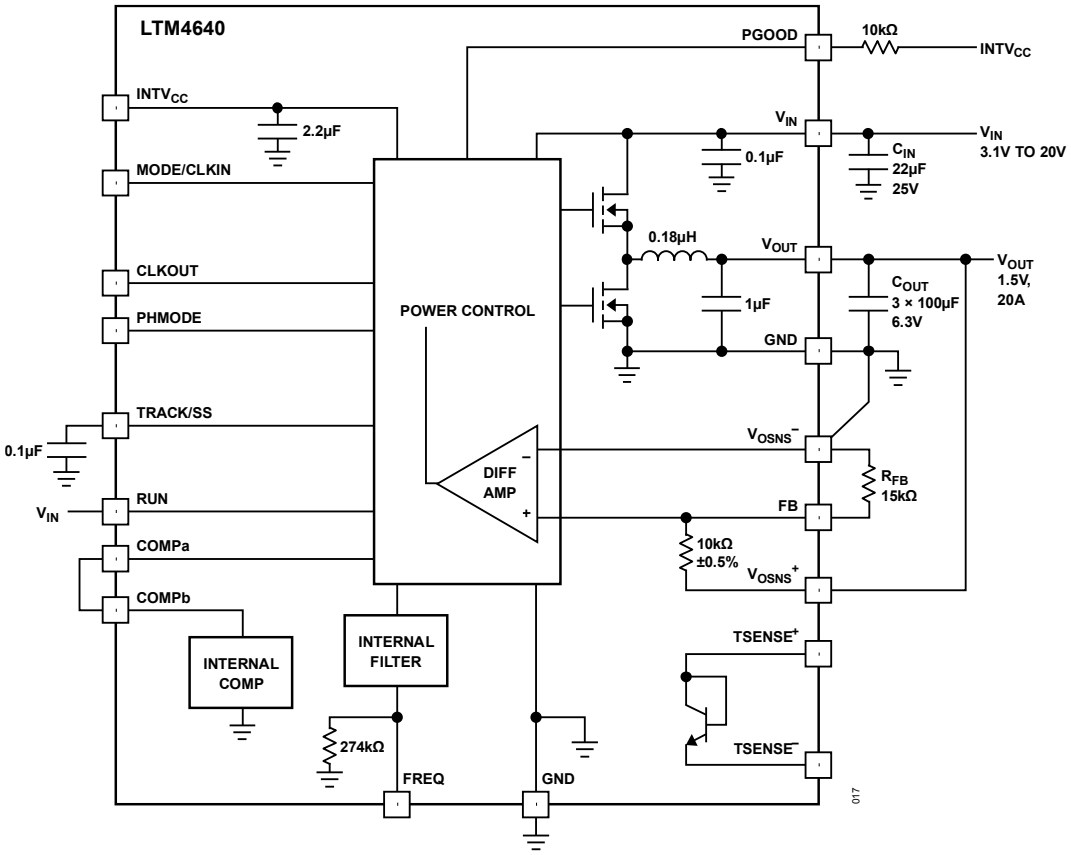


Figure 17. LTM4640 Simplified Block Diagram

Decoupling Requirements

Table 6. Decoupling Requirements

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External input capacitor requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 20A	33	44		µF
C_{OUT}	External output capacitor requirement (V_{IN} = 3.1V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 20A	330 [1]	470 [1]		µF

[1]Additional capacitance may be required under extreme temperature and/or capacitor bias voltage conditions because of the variation of the actual capacitance over bias voltage and temperature.

APPLICATIONS INFORMATION

The typical LTM4640 application circuit is shown in *Figure 37*. The external component selection is primarily determined by the input voltage, output voltage, load transient, and maximum load current. See *Table 12* for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions on the maximum V_{IN} and V_{OUT} step-down ratios that can be achieved for a given input voltage because of the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which is calculated with Equation *1*.

$$D_{MAX} = 1 - (t_{OFF(MIN)} \times f_{SW}) \quad (1)$$

where $t_{OFF(MIN)}$ is the minimum off-time, typically 50ns for LTM4640, and f_{SW} (Hz) is the switching frequency. Conversely, the minimum on-time limit imposes a minimum duty cycle of the converter which is calculated with Equation *2*.

$$D_{MIN} = t_{ON(MIN)} \times f_{SW} \quad (2)$$

where $t_{ON(MIN)}$ is the minimum on-time, typically 25ns for LTM4640. In the rare cases where the minimum duty cycle is surpassed, the output voltage remains in regulation, but the switching frequency decreases from its programmed value. Note that additional thermal derating may be applied. See the *Thermal Considerations and Output Current Derating* section.

Output Voltage Programming

The pulse-width modulation (PWM) controller has an internal 0.6V reference voltage. As shown in *Figure 17* (Simplified Block Diagram), a 10kΩ internal feedback resistor connects the V_{OSNS}^+ and the FB pins. Adding a resistor, R_{FB}, from FB pin to V_{OSNS}^- pin programs the output voltage given by Equation *3*.

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \times 10k\Omega \quad (3)$$

Table 7 summarizes the R_{FB} values required for some of the typical output voltage applications.

Table 7. R_{FB} Resistor Table vs. Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3
R_{FB} (kΩ)	OPEN	15	10	6.65	4.99	3.16	2.21

For parallel operation of multiple channels, the same feedback setting resistor is used for the parallel design. This is done by connecting the V_{OSNS}^+ to the output, as shown in *Figure 18*, thus connecting one of the internal 10kΩ resistors to the output. All the V_{FB} pins connect with one programming resistor, as shown in *Figure 18*. See *Figure 39* for an example of a parallel operation.

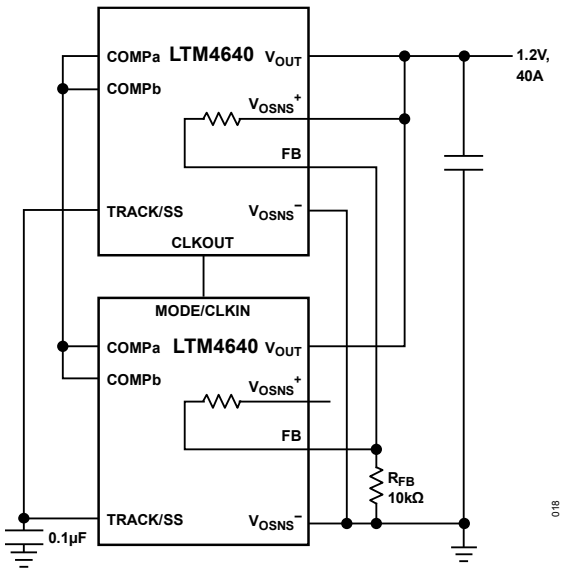


Figure 18. 2-Phase Parallel Configurations

Input Decoupling Capacitors

The LTM4640 should be connected to a low AC impedance DC source. For the regulator, a 22µF input ceramic capacitor is required for root mean square (RMS) ripple current decoupling. Bulk input capacitance is only needed when the input source impedance is compromised by long inductive leads, traces, or not enough source capacitance. The bulk capacitor is an aluminum electrolytic capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor is estimated with Equation 4.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}^2}} \quad (4)$$

where η% is the estimated efficiency of the power µModule regulator.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a single low equivalent series resistance (ESR) output ceramic capacitor is required for the LTM4640 to achieve low output ripple voltage and very good transient response. In extreme cold or hot temperatures, or high output voltage cases, an additional ceramic capacitor or a tantalum-polymer capacitor is required because of the variation of the actual capacitance over bias voltage and temperature. *Table 12* shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A load-step transient. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. The Analog Devices *LTpowerCAD*® design tool is available to download online for output ripple, stability, and transient response analysis for further optimization.

Discontinuous-Conduction Mode

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous-conduction mode (DCM) should be used by connecting the MODE/CLKIN pin to GND. At light loads, the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

Forced Continuous Mode

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, FCM operation should be used. FCM operation can be enabled by connecting the MODE/CLKIN pin to $INTV_{CC}$. In this mode, the inductor current can reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During startup, FCM is disabled, and the inductor current is prevented from reversing until the LTM4640's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4640 is optimized to achieve the compact package size and the minimum output ripple voltage while keeping high efficiency. The default operating frequency is 600kHz. In most applications, no additional frequency adjustment is required.

If an operating frequency other than 600kHz is required by the application, the operating frequency is increased by adding a resistor, RFSET, between the FREQ pin and GND, as shown in *Figure 38*, or is decreased by adding a resistor between the FREQ pin and INTVCC. The RFSET resistance value is calculated with Equation 5.

$$R_{FSET} = \begin{cases} \dfrac{1.67 \times 10^{11}\Omega \times Hz}{f - 600kHz} \ (f > 600kHz) \\ \dfrac{2.72 \times 10^{11}\Omega \times Hz}{600kHz - f} \ (f < 600kHz) \end{cases} \quad (5)$$

The programmable operating frequency range is from 400kHz to 3MHz.

Frequency Synchronization and Clock In

The LTM4640 has a phase-locked loop comprised of an internal voltage-controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The external clock frequency range must be within ±30% around the operating frequency set by the R_{FSET} resistor. A pulse detection circuit detects a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock must be at least 100ns. The clock's high level must be above 1V and the clock's low level below 0.3V. During the startup of the regulator, the phase-locked loop function is disabled.

Multiphase Operation

For output loads that demand more than 20A of current, multiple LTM4640s are paralleled to run out-of-phase to provide more output current without increasing input and output voltage ripples.

The CLKOUT signal is connected to the MODE/CLKIN pin of the following LTM4640 stage to line up both the frequency and the phase of the entire system. Connecting the PHMODE pin to $INTV_{CC}$, GND, or FLOAT generates a phase difference (between CLKIN and CLKOUT) of 180°, 120°, or 90°, respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation. *Figure 39* shows a 2-phase design. For a 3-phase or a 4-phase operation to achieve the best performance, it is recommended to use an external clock integrated circuit (IC) to provide the desired phase difference for each LTM4640. An optional low-pass filter is added to each external clock signal before it is fed to the LTM4640. *Figure 19* shows a 4-phase design in such a way. Interleaving among more than four phases is not recommended.

Table 8. PHMODE Pin Status and Corresponding Phase Relationship (Relative to CLKIN)

PHMODE	$INTV_{CC}$	GND	FLOAT
CLKOUT	180°	120°	90°

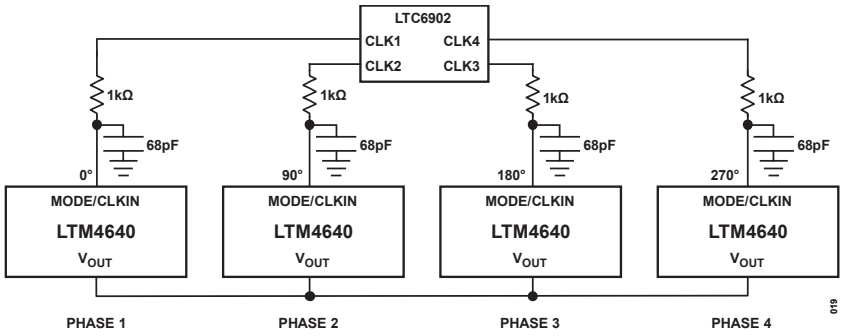


Figure 19. 4-Phase Operation with an External Clock IC and Low-Pass Filters

A multiphase power supply significantly reduces the amount of ripple current in both the input and the output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (if the input voltage exceeds the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all the outputs are connected to achieve a single high output current design.

The LTM4640 is an inherently current mode-controlled device, which ensures good current sharing in parallel operation. This balances the thermals on the design. Connect the RUN, TRACK/SS, FB, and COMPa pins of each paralleling channel together. *Figure 39* shows an example of a parallel operation and the pins connection.

Input RMS Ripple Current Cancellation

Analog Devices *Application Note 77* provides a detailed explanation of a multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. *Figure 20* shows this graph.

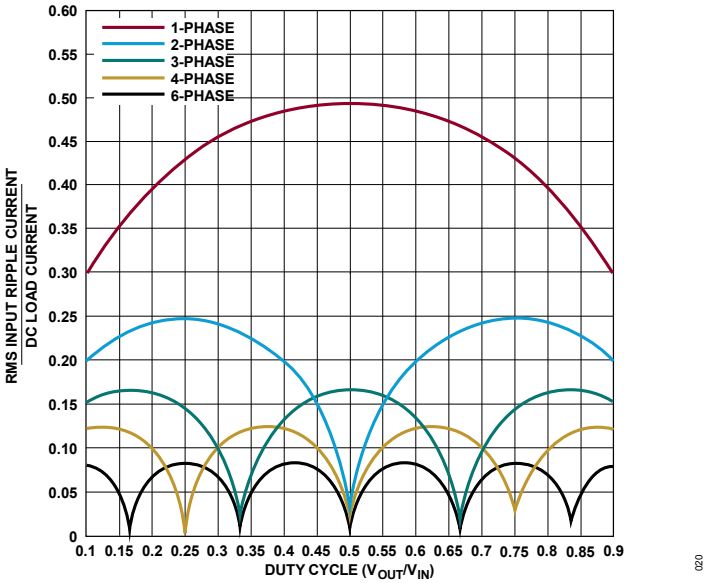


Figure 20. The RMS Input Ripple Current to DC Load Current Ratio as a Function of the Duty Cycle

Soft Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin programs the ramp rate of the output voltage. An internal 6µA current source charges up the external soft start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it takes over the internal 0.6V reference voltage to control the output voltage. The total soft start time is calculated with Equation 6.

$$t_{SS} = 0.6V \times \frac{C_{SS}}{6\mu A} \quad (6)$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and FCM are disabled during the soft start process.

Output voltage tracking can also be externally programmed using the TRACK/SS pin. The output is tracked up and down with another regulator. *Figure 21* and *Figure 22* show examples of a waveform and the schematic of ratio metric tracking where the subordinate regulator's output slew rate is proportional to the main device.

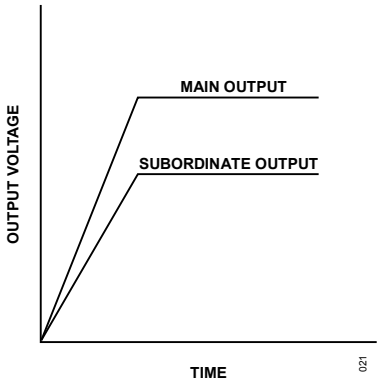


Figure 21. Output Ratio Metric Tracking Waveform

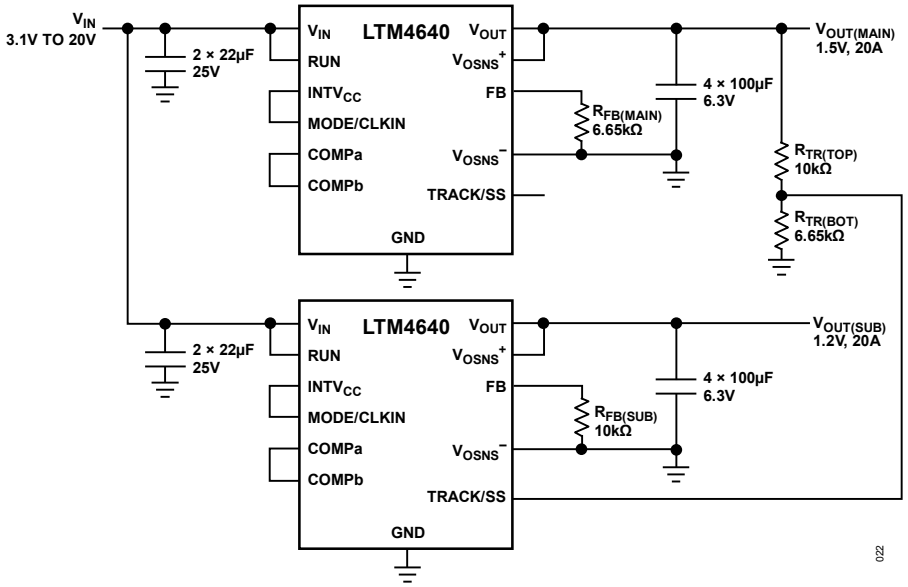


Figure 22. Example Schematic of Ratio Metric Output Voltage Tracking

Since the subordinate regulator's TRACK/SS is connected to the main device output through an $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider, and its voltage is used to regulate the subordinate device output voltage when TRACK/SS voltage is below 0.6V, the subordinate device output voltage and the main device output voltage should satisfy Equation 7 during startup.

$$V_{OUT(SUB)} \times \frac{R_{FB(SUB)}}{R_{FB(SUB)} + 10k\Omega} = V_{OUT(MAIN)} \times \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (7)$$

The $R_{FB(SUB)}$ is the feedback resistor, and the $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the subordinate regulator, as shown in *Figure 22*.

Following Equation 7, the ratio of the main device output slew rate (MR) to the subordinate device output slew rate (SR) is given by Equation 8.

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SUB)}}{R_{FB(SUB)} + 10k\Omega}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}} \quad (8)$$

For example, $V_{OUT(MAIN)}$ = 1.5V, MR = 1.5V/1ms and $V_{OUT(SUB)}$ = 1.2V, SR = 1.2V/1ms. From Equation 8, we could solve that $R_{TR(TOP)}$ = 10kΩ and $R_{TR(BOT)}$ = 6.65kΩ are a good combination for the ratio metric tracking.

The TRACK/SS pin has the 6µA current source on when a resistive divider implements tracking on the subordinate regulator. This imposes an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from Equation 8 are recommended to mitigate such impact. For example, where the 10kΩ is used, then a 5kΩ is used to reduce the TRACK/SS pin offset to a negligible value.

Coincident output tracking is recognized as a special ratio metric output tracking in which the main device output slew rate (MR) is the same as the subordinate device output slew rate (SR), waveform as shown in *Figure 23*.

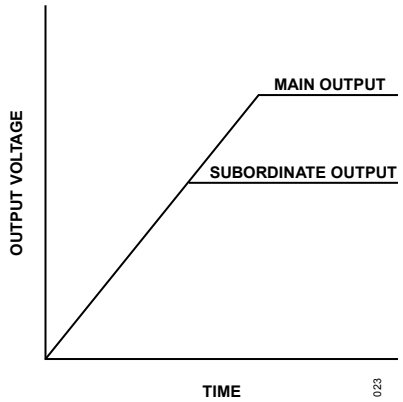


Figure 23. Output Coincident Tracking Waveform

From Equation 8, we could easily find that, in coincident tracking, the subordinate regulator's TRACK/SS pin resistor divider is always the same as its feedback divider (Equation 9).

$$\frac{R_{FB(SUB)}}{R_{FB(SUB)} + 10k\Omega} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \qquad (9)$$

For example, $R_{TR(TOP)}$ = 10kΩ and $R_{TR(BOT)}$) = 10kΩ is a good combination for coincident tracking for a $V_{OUT(MAIN)}$ = 1.5V and $V_{OUT(SUB)}$ = 1.2V application.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin is pulled low when the output voltage exceeds a ±8% window around the regulation point. To prevent unwanted PGOOD glitches during transients or dynamic VOUT changes, the LTM4640's PGOOD falling edge includes a blanking delay of approximately 25 switching cycles.

RUN Enable

Pulling the RUN pin to ground forces the LTM4640 into the shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.6V turns on the internal reference only, while keeping the power MOSFETs off. Increasing the RUN pin voltage above 1.35V turns on the entire device.

Prebiased Output Startup

There may be situations that require the power supply to start up with some charge on the output capacitors. The LTM4640 can safely power up into a prebiased output without discharging it.

The LTM4640 accomplishes this by forcing discontinuous-conduction mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This prevents the bottom FET from turning on during the prebiased output startup, which would discharge the output.

SW Pins and Optional Snubber Circuit

The SW pin is generally for testing purposes. The SW pin can also be used to dampen out switch node ringing caused by the LC parasitic in the switched current path using a series R-C snubber circuit. The resistor dampens the resonance, and the capacitor is chosen to only affect the high-frequency ringing across the resistor. The snubber circuit is optional, as the LTM4640 can operate well with proper PCB layout. If needed, below are suggestions regarding snubber circuit design.

If the stray inductance or capacitance can be measured or approximated, then it is possible to use an analytical technique to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First, the SW pin is monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency is measured for its value. The impedance Z_L is calculated with Equation 10.

$$Z_L = 2\pi \times f \times L \qquad (10)$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z_L, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. This is calculated with Equation 11.

$$Z_C = \frac{1}{2\pi \times f \times C} \quad (11)$$

These values are a good place to start. Modifications to these components should be made to attenuate the ringing with the least amount of power loss.

Stability Compensation

The LTM4640 has already been internally compensated for all output voltages and capacitor combinations, including all ceramic capacitor applications when COMPb is connected to COMPa. Note that a 22pF to 100pF feedforward capacitor (C_{FF}) is required for connecting from V_{OUT} to V_{FB} pins for all ceramic output capacitor applications to achieve high bandwidth control loop compensation with enough phase margin. *Table 12* provides most of the application requirements using optimized internal compensation.

For specific optimized requirements, disconnect COMPb from COMPa and apply a Type II compensation network from COMPa to GND to achieve external compensation. Choose the components of the Type-II network dependent on the desired output response for line and load variations as well as loop stability parameters—phase margin and gain margin of the feedback loop. In general, selecting a low capacitance and a high resistance for the Type-II network at COMPa pin leads to a fast transient response but may adversely affect the loop stability parameters.

The *LTpowerCAD* design tool is available to download online to perform specific control loop optimization and to analyze the control stability and load transient performance.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is built into the LTM4640 to sense output voltages accurately at the remote load points. This is especially true for high current loads. It is important that the V_{OSNS+} and V_{OSNS-} pins are connected properly at the remote output sense point, and that the feedback resistor, R_{FB}, is connected between the V_{FB} and V_{OSNS-} pins (see *Figure 37)*.

In a multiphase single output application, only one set of differential sensing amplifiers and one set of feedback resistors is required, while connecting RUN, TRACK/SS, V_{OUT}, V_{FB}, and COMPa of different channels together. See *Figure 39* for an example of a paralleling application.

Input Overvoltage Protection

To protect the internal power MOSFET devices against transient voltage spikes, the LTM4640 constantly monitors the V_{IN} pin for an overvoltage condition. When the V_{IN} rises above 24.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once V_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator executes its soft start function when exiting an overvoltage condition.

Output Current Limit

Under overload or short-circuit conditions, the output current is no higher than the specified output current limit. The LTM4640 may still be switching, but the output voltage regulation is not guaranteed, which is dependent on the load resistance under such conditions. Continuous operation under such conditions is not recommended, as this may cause the maximum operating junction temperature to be exceeded, which may impair the device's reliability.

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage, and temperature described by the classic diode Equation 12.

$$I_D = I_S \times e^{\frac{V_D}{\eta \times V_T}}$$

or

$$V_D = \eta \times V_T \times ln\frac{I_D}{I_S} \quad (12)$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1), and I_S (saturation current) is a process-dependent parameter. The V_T is broken out with Equation 13.

$$V_T = \frac{K \times T}{q} \quad (13)$$

where T is the diode junction temperature in Kelvin, q is the electron charge, and K is Boltzmann's constant. The V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in Equation 13 is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and must always be less than I_D. Combining all the constants into one term (see Equation 14).

$$K_D = \frac{\eta \times k}{q} \quad (14)$$

where $K_D = 8.62 \times 10{-}5$ V/K, assuming the ideality factor is 1 and knowing ln (I_D/I_S) is always positive because I_D is always greater than I_S, leaves us with the results given in Equation 15.

$$V_D = T_{(KELVIN)} \times K_D \times ln\frac{I_D}{I_S} \quad (15)$$

It should be noted that as the temperature increases, the I_S term increases more quickly, and thus, the ln (I_D/I_S) absolute value reduces faster, yielding a negative coefficient of diode voltage vs. temperature, which is an approximate –2mV/°C temperature relationship as shown in Figure 24.

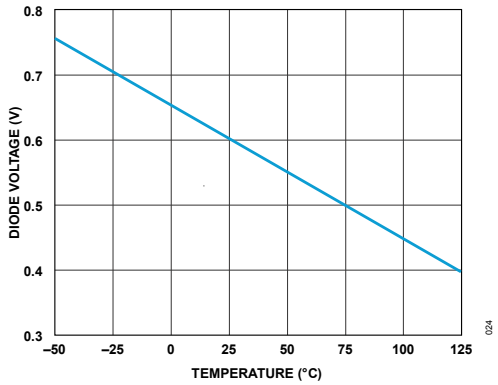


Figure 24. Diode Voltage V_D vs. Temperature T(°C)

To obtain a linear voltage proportional to the temperature, we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from Equation 15. This is accomplished by measuring the diode voltage at two currents: I_1 and I_2, where $I_1 = 10 \times I_2$, and subtracting is given in Equation 16.

$$\Delta V_D = T_{(KELVIN)} \times K_D \times ln\frac{I_1}{I_S} - T_{(KELVIN)} \times K_D \times ln\frac{I_2}{I_S} \quad (16)$$

Combining like terms, and then simplifying the natural log terms yields Equation 17.

$$\Delta V_D = T_{(KELVIN)} \times K_D \times ln(10) \quad (17)$$

and redefining the constant is given in Equation 18.

$$K'_D = K_D \times ln(10) = \frac{198\mu V}{K} \quad (18)$$

yields Equation 19.

$$\Delta V_D = K'_D \times T_{(KELVIN)} \quad (19)$$

Equation 20 solves for temperature.

$$T_{(KELVIN)} = \frac{\Delta V_D}{K'_D}$$
$$T_{(°CELSIUS)} = T_{(KELVIN)} - 273.15 \quad (20)$$

Where 300.15K = 27°C is an example.

If we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The internal diode-connected NPN transistor between TSENSE+ and TSENSE– pins is used to monitor the internal temperature of the LTM4640.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the *Pin Configurations and Function Descriptions* section are consistent with those parameters defined by JESD5112 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD5112 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may use laboratory equipment and a test vehicle, such as an evaluation (demo) board, to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to complement any FEA activities. Without FEA software, the thermal resistances reported in the *Pin Configurations and Function Descriptions* section are, in and of themselves, not relevant to providing guidance on thermal performance; instead, the derating curves provided in *Figure 29* through *Figure 34* can be used in a manner that yields insight and guidance about the user's application and can be adapted to correlate thermal performance to the user's application.

The *Pin Configurations and Function Descriptions* section gives three thermal coefficients explicitly defined in JESD5112; these coefficients are quoted or paraphrased as follows.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as “still air”, although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.

2. $\theta_{JCbottom}$, the thermal resistance from the junction to the bottom of the product case, is determined with all the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.

3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all the component’s power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.

A graphical representation of the thermal resistances is given in *Figure 25*; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

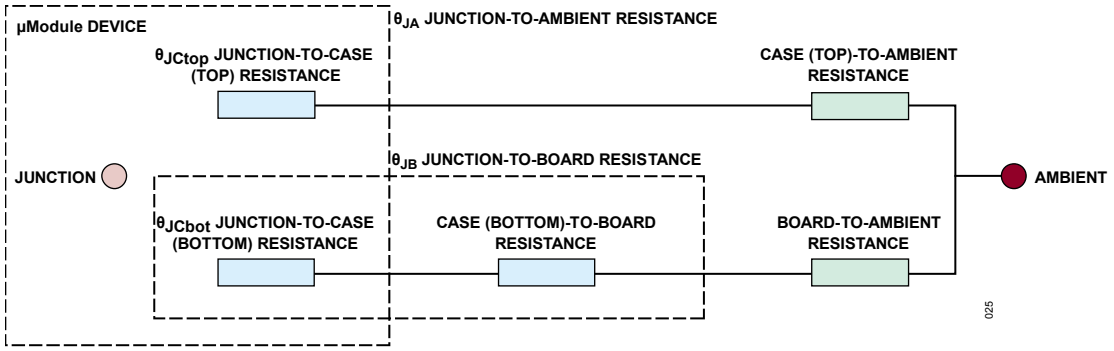


Figure 25. Graphical Representation of JESD51–12 Thermal Coefficients

As a practical matter, it should be clear to the user that no individual or sub-group of the three thermal resistance parameters defined by JESD5112 or provided in the *Pin Configurations and Function Descriptions* section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device’s total power loss (heat) thermally conducts exclusively through the top or exclusively through the bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, most of the heat flow is into the board.

Airflow and Heat Sinking

Within the LTM4640, be aware that there are multiple power devices and components dissipating power with a consequence that the thermal resistances relative to different junctions of components or dies are not exactly linear with respect to the total package power loss. To reconcile this complication without sacrificing modeling

simplicity—but also, not ignoring practical realities—an approach has been taken by using FEA software modeling and laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software accurately builds the mechanical geometry of the LTM4640 and the specified PCB with all of the correct material coefficients and accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED5112 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software evaluates the LTM4640 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as the one which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in *Figure 29* through *Figure 34*. After these laboratory tests have been performed and correlated to the LTM4640, then the θ_{JB} and θ_{BA} are summed together to provide a value that should closely equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1V, 1.5V, and 3.3V power loss curves in *Figure 26* through *Figure 28* can be used in coordination with the load current derating curves in *Figure 29* through *Figure 34* for calculating an approximate θ_{JA} thermal resistance for the LTM4640 with various airflow conditions. The power loss curves are taken at room temperature and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is 1.2 for 120°C, at junction temperature. The maximum load current is achievable while increasing ambient temperature if the junction temperature is less than 120°C, which is a 5°C guard band from a maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C, while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 20A and the ambient temperature at 30°C. The output voltages are 1V, 1.5V, and 3.3V. These are chosen to include the lower and higher output voltage ranges to correlate the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber and thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature.

The decreased output current decreases the internal µModule loss as the ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much µModule temperature rise can be allowed. For example, in *Figure 30*, the load current is derated to ~10A at ~95°C with no airflow or heat sink, and the power loss for the 12V to 1V at 10A output is about 1.8W. The 1.8W loss is calculated with the ~1.5W room temperature loss from the 12V to 1V power loss curve at 10A, and the 1.2 multiplying factor at 120°C junction temperature. If the 95°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25°C divided by 1.8W equals a 13.9°C/W θ_{JA} thermal resistance. *Table 9* specifies a 14°C/W value, which is very close. *Table 10* and *Table 11* provide equivalent thermal resistances for 1.5V and 3.3V outputs with and without airflow and heat sinking. The derived thermal resistances in *Table 9*, *Table 10*, and *Table 11* for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the *Typical Performance Characteristics* section and adjusted with the previous ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 6-layer board with two-ounce copper for all six layers. The PCB dimensions are 90mm × 90mm.

T_A = 25°C, unless otherwise noted.

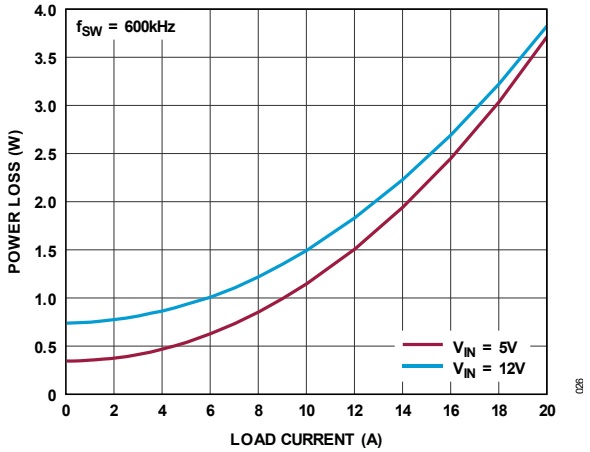


Figure 26. Power Loss at 1V Output

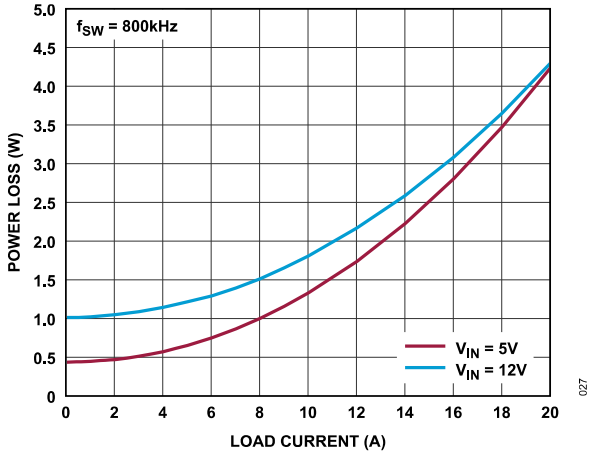


Figure 27. Power Loss at 1.5V Output

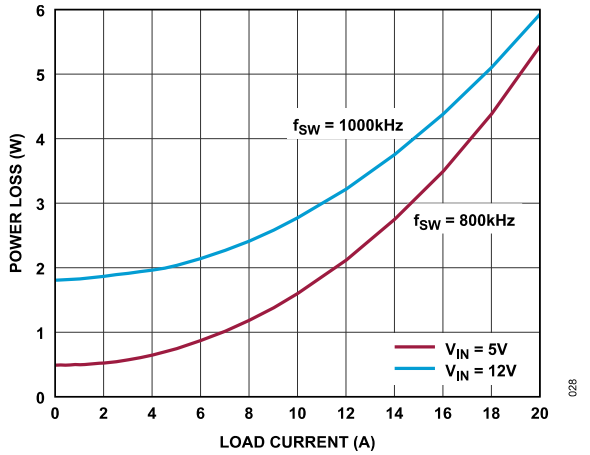


Figure 28. Power Loss at 3.3V Output

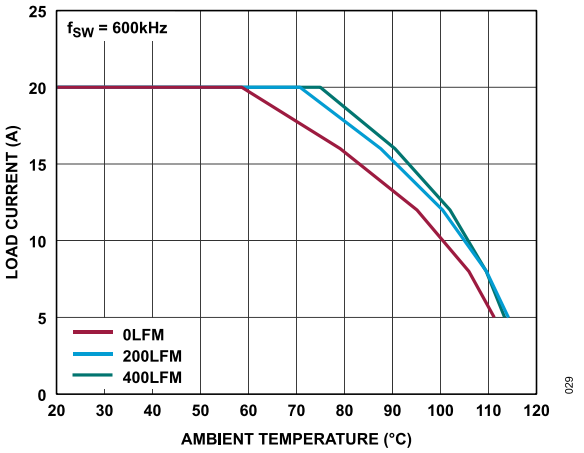


Figure 29. 5V to 1V Derating Curve, No Heat Sink

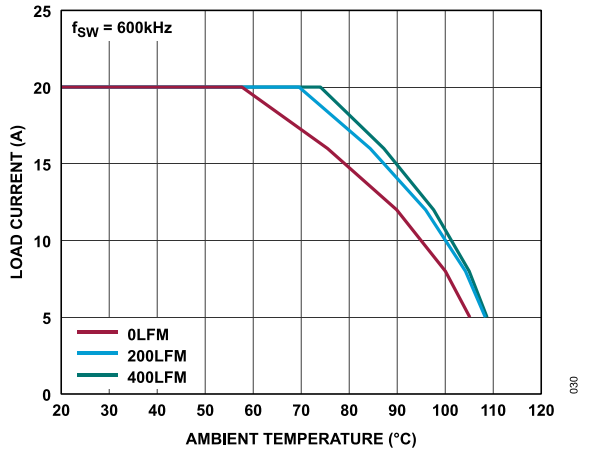


Figure 30. 12V to 1V Derating Curve, No Heat Sink

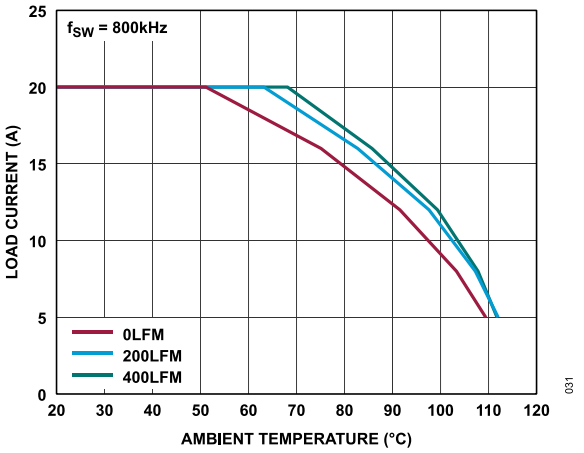


Figure 31. 5V to 1.5V Derating Curve, No Heat Sink

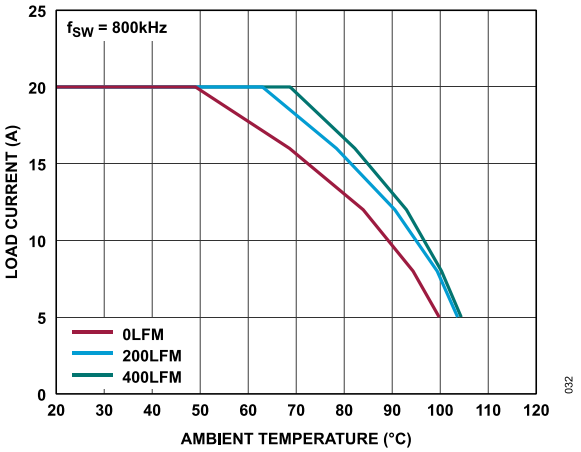


Figure 32. 12V to 1.5V Derating Curve, No Heat Sink

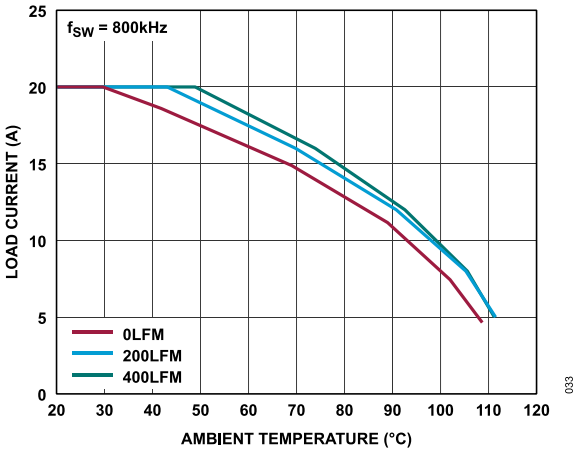


Figure 33. 5V to 3.3V Derating Curve, No Heat Sink

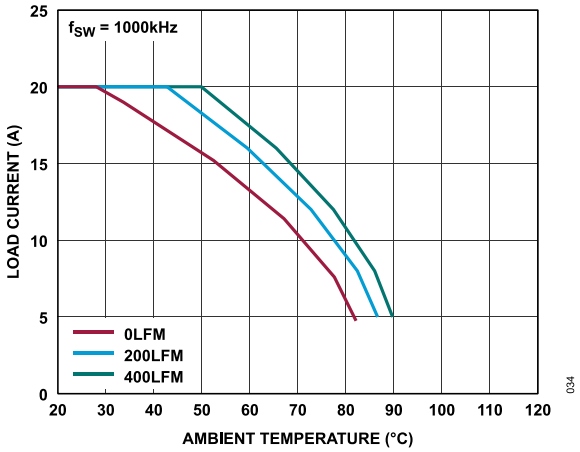


Figure 34. 12V to 3.3V Derating Curve, No Heat Sink

Figure 35 shows a thermal capture of LTM4640 with 12V input, 1V output at 20A, 600kHz, 21°C ambient temperature, without airflow and heat sink conditions.

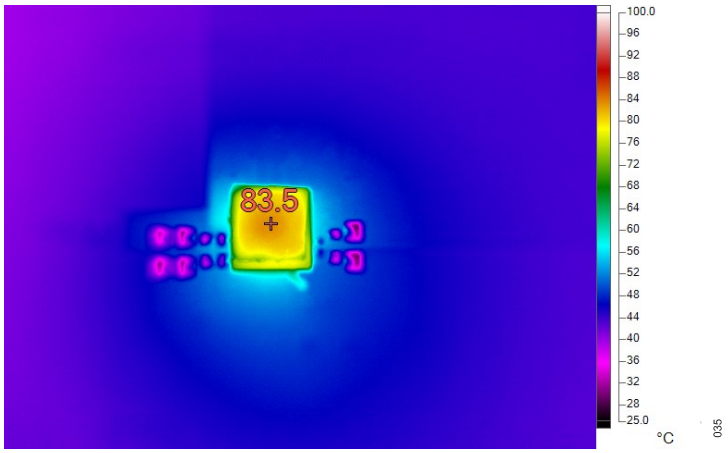


Figure 35. Thermal Image at $12V_{IN}$, $1V_{OUT}$ at 20A, 600kHz, 21°C Ambient Temperature, without Airflow and Heat Sinking

Table 9. 1V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 29, *Figure 30*	5, 12	*Figure 26*	0	None	14
Figure 29, *Figure 30*	5, 12	*Figure 26*	200	None	11
Figure 29, *Figure 30*	5, 12	*Figure 26*	400	None	10

Table 10. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 31, *Figure 32*	5, 12	*Figure 27*	0	None	14
Figure 31, *Figure 32*	5, 12	*Figure 27*	200	None	11
Figure 31, *Figure 32*	5, 12	*Figure 27*	400	None	10

Table 11. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 33, *Figure 34*	5, 12	*Figure 28*	0	None	15
Figure 33, *Figure 34*	5, 12	*Figure 28*	200	None	12
Figure 33, *Figure 34*	5, 12	*Figure 28*	400	None	11

Table 12. Output Voltage Response vs. Component Matrix (See *Figure 37*)

C_{OUT1} VENDORS	PART NUMBER	DESCRIPTION	C_{OUT2} VENDORS	PART NUMBER	DESCRIPTION
Murata	GRM32EC70J107ME15L	100µF, 6.3V, X7S, 1210	Panasonic	EEF-GX0E471L	470µF, 2.5V, 3mΩ
Taiyo Yuden	JMK325AC7107MM	100µF, 6.3V, X7S, 1210			
TDK	C3225X6S0J107M250AC	100µF, 6.3V, X6S, 1210			
Murata	GRM31CR60J227ME11L	220µF, 6.3V, X5R, 1206			

All Ceramic Output Capacitors

V_{OUT} (V)	V_{IN} (V)	R_{FB} (kΩ)	f_{SW} (kHz)	C_{OUT1} (CERAMIC CAP)	C_{OUT2} (BULK CAP)	COMPa (pF)	R_{TH} ON COMPa (kΩ)	C_{TH} ON COMPa (pF)	LOAD STEP (A)	PK-PK DEVIATION (mV)	RECOVERY TIME (µs)
1	5	15	600	4 × 220µF	None	Short to COMPb	None	None	5	90	40
1	12	15	600	4 × 220µF	None	Short to COMPb	None	None	5	100	40
1.5	5	6.65	800	4 × 220µF	None	Short to COMPb	None	None	5	97	60
1.5	12	6.65	800	4 × 220µF	None	Short to COMPb	None	None	5	97	60
2.5	5	3.16	800	4 × 220µF	None	Short to COMPb	None	None	5	110	80
2.5	12	3.16	1000	4 × 220µF	None	Short to COMPb	None	None	5	114	80
3.3	5	2.21	800	4 × 220µF	None	Short to COMPb	None	None	5	121	80
3.3	12	2.21	1000	4 × 220µF	None	Short to COMPb	None	None	5	124	80

Safety Considerations

The LTM4640 does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current must be provided to protect the unit from catastrophic failure. The device does support thermal shutdown.

Layout Checklist/Example

The high integration of LTM4640 makes the printed circuit board (PCB) layout very simple and easy to use. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

1. Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
2. To minimize noise coupling on the output, reduce the copper area border between V_{IN} and V_{OUT}, and separate them with GND copper.
3. Place high-frequency ceramic input and output capacitors next to the V_{IN}, PGND, and V_{OUT} pins to minimize high-frequency noise.
4. Place a dedicated power ground layer underneath the unit.
5. To minimize the via conduction loss and reduce the µModule thermal stress, use multiple vias for interconnection between the top layer and other power layers.
6. Do not put vias directly on the pad unless they are capped or plated over.
7. Bring out test points on the signal pins for monitoring.
8. Keep separation between CLKIN, CLKOUT, and FREQ pin-traces to minimize the possibility of noise due to crosstalk between these signals.

Figure 36 gives a good example of the recommended PCB layout.

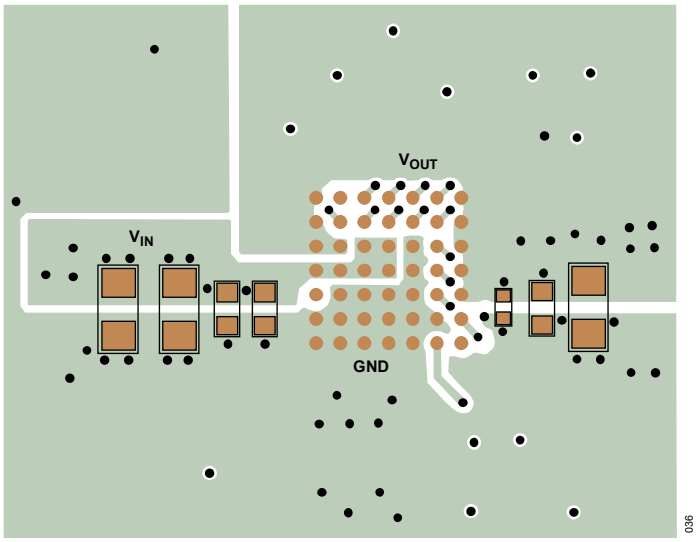


Figure 36. Recommended PCB Layout

Typical Applications

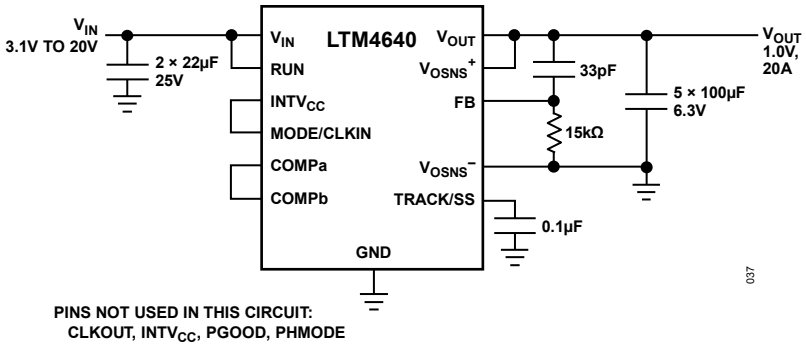


Figure 37. 3.1V_{IN} to 20V_{IN}, 1V Output at 20A Design

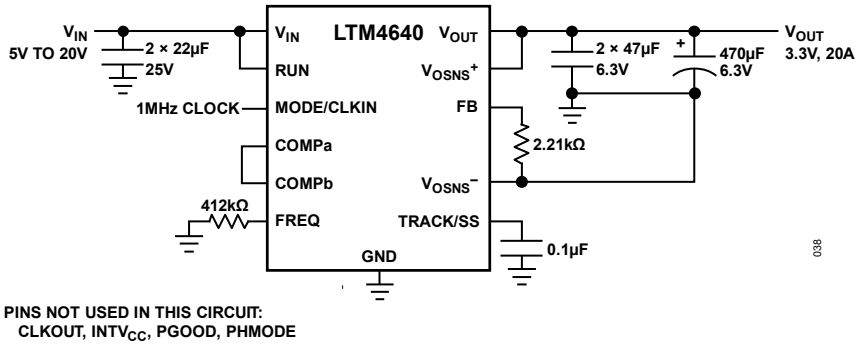


Figure 38. 5V_{IN} to 20V_{IN}, 3.3V Output with 1MHz External Clock

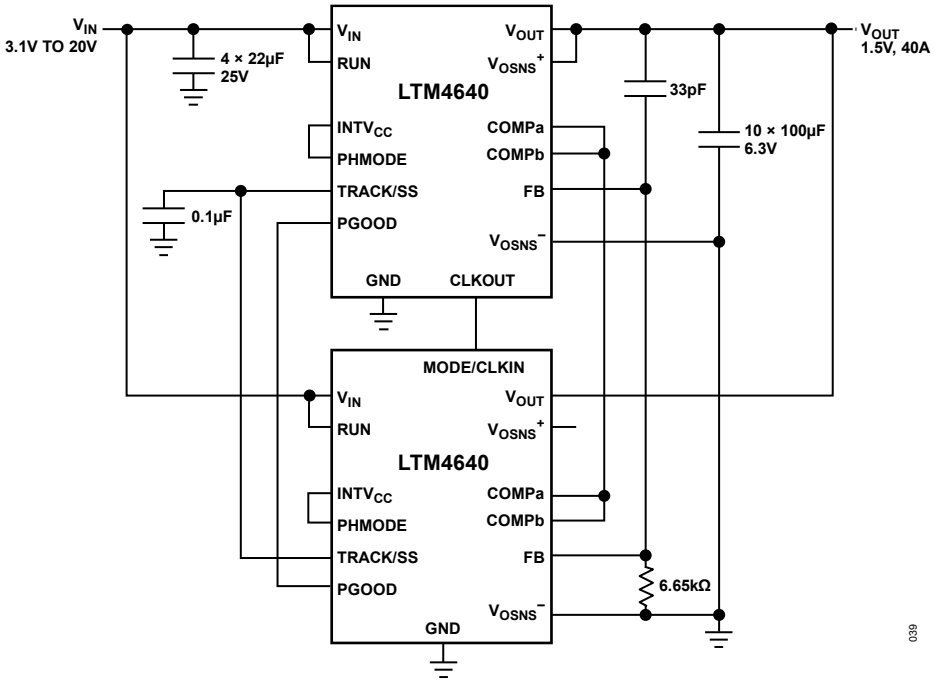


Figure 39. 3.1V_{IN} to 20V_{IN}, Two Phases, 1.5V at 40A Design

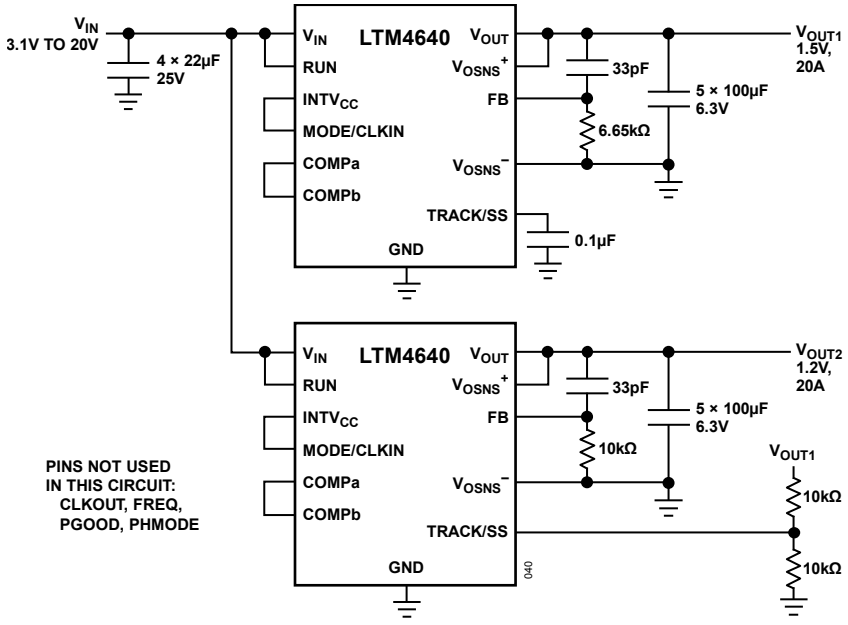


Figure 40. 3.1V_{IN} to 20V_{IN}, 1.2V and 1.5V with Coincident Tracking

Related Parts

Table 13.Related Parts

PART NUMBER	DESCRIPTION	COMMENT
LTM4657	8A µModule regulator, pin compatible with LTM4626, LTM4638 and LTM4640	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule regulator, pin compatible with LTM4657, LTM4638 and LTM4640	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule regulator, pin compatible with LTM4657, LTM4626 and LTM4640	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 5.02mm BGA
LTM4702	10A Silent Switcher 3 µModule regulator, pin compatible with LTM4703 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4703	12A Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4707	15A Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4703	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4622	Dual 2.5A or single 5A µModule regulator	3.6V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 1.82mm (LGA) or 2.42mm (BGA)
LTM4705	Dual 5A or single 10A µModule regulator	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 7.5mm × 3.22mm BGA
LTM4646	Dual 10A or single 20A µModule regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 11.25mm × 15mm × 5.01mm BGA
LTM4630/ LTM4630A	Dual 18A or single 36A µModule regulator, pin compatible with LTM4650	4.5V ≤ V_{IN} ≤ 15V (18V for LTM4630A), 0.6V ≤ V_{OUT} ≤ 1.8V (8V for LTM4630A), 16mm × 16mm × 4.41mm (LGA) or 5.01mm (BGA)
LTM4650/ LTM4650A	Dual 25A or single 50A µModule regulator, pin compatible with LTM4630	4.5V ≤ V_{IN} ≤ 15V (16V for LTM4650A), 0.6V ≤ V_{OUT} ≤ 1.8V (5.5V for LTM4650A), 16mm × 16mm × 4.41mm (LGA) or 5.01mm (BGA)
LTM4668/ LTM4668A	Configurable quad 1.2A µModule regulator	2.7V ≤ V_{IN} ≤ 17V, 0.6V ≤ V_{OUT} ≤ 1.8V (5.5V for LTM4668A), 6.25mm × 6.25mm × 2.1mm BGA
LTM4643	Configurable quad 3A µModule regulator, Pin compatible with LTM4644	4V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 3.3V, 9mm × 15mm × 1.82mm LGA, 2.42mm BGA
LTM4644	Configurable quad 4A µModule regulator, pin compatible with LTM4643	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, 9mm × 15mm × 5.01mm BGA

OUTLINE DIMENSIONS

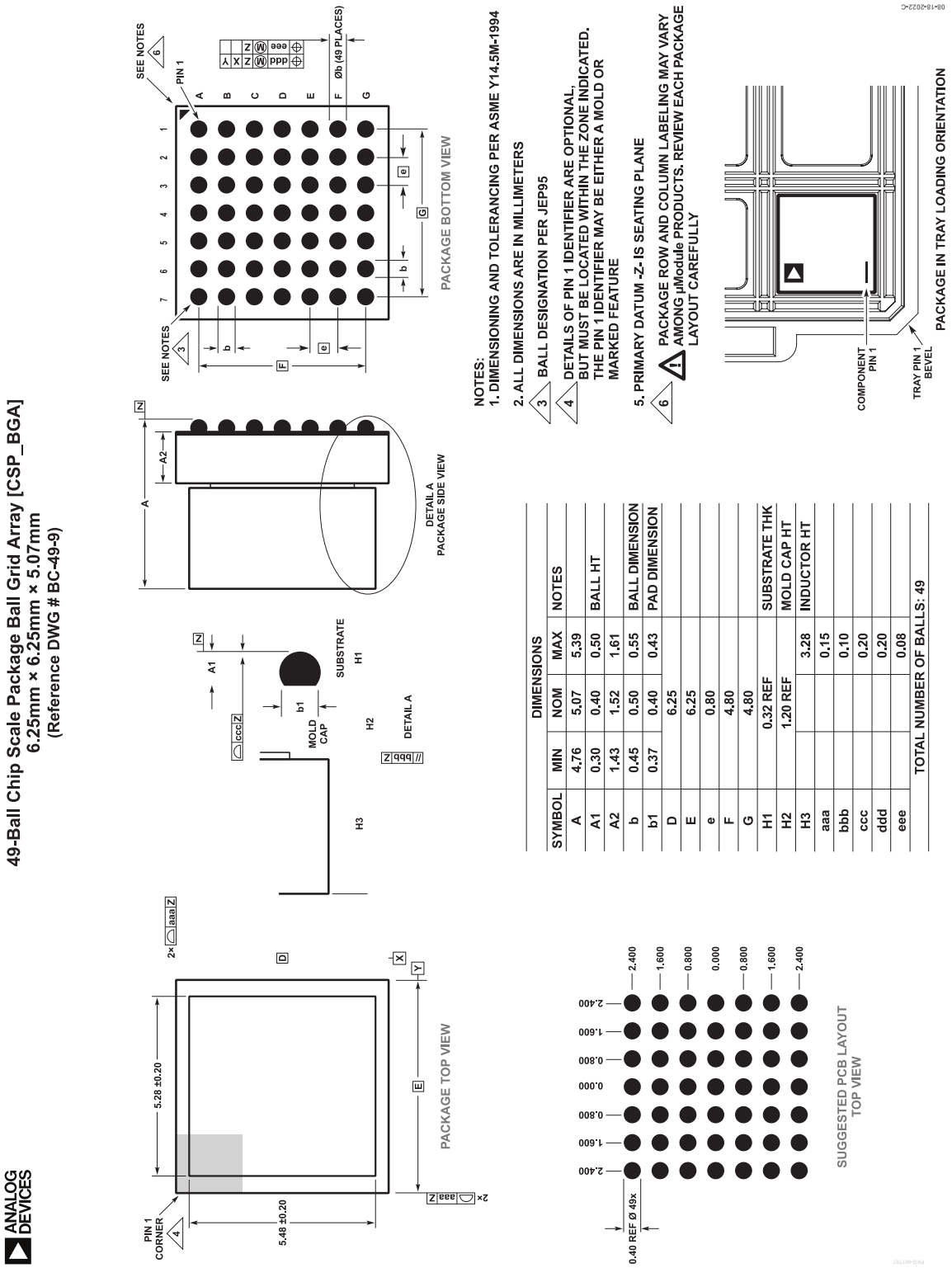


Figure 41. 49-Pin, 6.25mm × 6.25mm × 5.07mm, BGA

ORDERING GUIDE

Table 14.Ordering Guide

MODEL	TEMPERATURE RANGE [1]	PACKAGE DESCRIPTION*	PACKAGE OPTION
LTM4640EY#PBF	–40°C to 125°C	Part marking: 4640, SAC305 (RoHS) ball finish, e1 finish code, moisture sensitivity level (MSL 4) rated device.	*49-Pin, 6.25mm × 6.25mm × 5.07mm, BGA* package.
LTM4640IY#PBF	–40°C to 125°C	Part marking: 4640, SAC305 (RoHS) ball finish, e1 finish code, moisture sensitivity level (MSL 4) rated device.	*49-Pin, 6.25mm × 6.25mm × 5.07mm, BGA* package.

1 The LTM4640, including E-grade and I-grade parts (see *Table 14*), is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4640E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4640I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *Ball finish code is per IPC/JEDEC J-STD-609. The temperature grade is identified by a label on the shipping container.

Recommended LGA and BGA PCB assembly and manufacturing procedures.

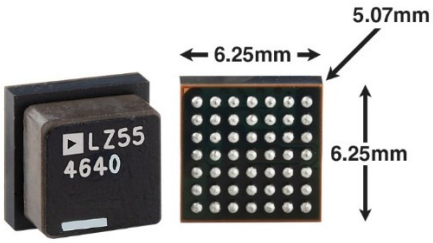
LGA and BGA package and tray drawings.

Table 15. Evaluation Boards

PART NUMBER	DESCRIPTION
DC3107A	20V_{IN}, 20A Step-Down DC-to-DC µModule Regulator evaluation (demo) board.

SELECTOR GUIDE

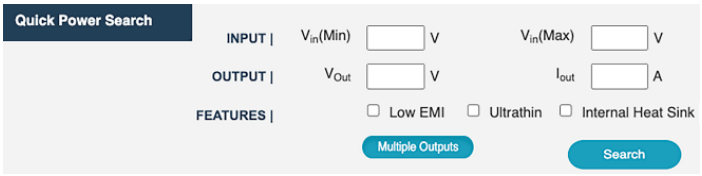
Package Photos



(Part marking is laser mark)

Design Resources

Table 16. Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	Design: ▶ Selector guides ▶ Evaluation (demo) boards and Gerber files ▶ Free simulation tools	Manufacturing: ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	