Data Sheet

LTC9105

IEEE 802.3bt PD with Telemetry and Power Priority

FEATURES

- IEEE 802.3bt Powered Device (PD) Controller
- 400kHz I²C Interface
- Continuous Voltage, Current, and Power Telemetry
- Dedicated 14-Bit Delta-Sigma Current and Voltage ADCs
- Automatic Maintain Power Signature (MPS)
- Supports Up to 90W PDs with Extended Power
- 5-Event Classification Sensing with PSE Allocated Power Readback
- Seamless Switchover between Dual PD or PD/AUX Inputs
- Superior Surge Robustness (100V Absolute Maximum)
- Wide Junction Temperature Range (-40ºC to 125ºC)
- External Hot Swap N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- 50mΩ Current Sense Resistor
- Auxiliary Input Sense with Standby Modes
- 20-Pin 5mm x 5mm QFN Package

APPLICATIONS

- IEEE 802.3bt PDs with Power Telemetry
- Wireless Access Points/Pico Cells
- Internet Protocol (IP) Security Cameras
- Power over Ethernet (PoE) Lighting

DESCRIPTION

The LTC9105 is an IEEE 802.3af/at/bt ("PoE 2") Power over Ethernet (PoE) powered device (PD) controller with input current, voltage, and power telemetry. The LTC9105 includes an I²C interface to read telemetry, power sourcing equipment (PSE) allocated power, and auxiliary input status, and to write power input priority. The LTC9105 also features a configurable downstream power-up disable with under-power indication when the PSE allocated power is less than the PD requested power.

The LTC9105 utilizes an external, low $R_{DS(ON)}$, N-Channel, Hot Swap MOSFET, and a 50mΩ current sense resistor, and supports the LT4321 ideal bridge to extend the end-to-end power delivery efficiency. Also included are a power good output, external signature resistor, resistor programmable classification and pin-configurable PD requested Class. The presence of an auxiliary power supply is sensed at the AUX pin and reported through the I²C interface. Automatic maintain power signature (MPS) circuitry keeps the PD interface powered when downstream current draw falls below an internal MPS threshold.

Two dedicated Delta-Sigma ADCs continuously measure PD controller input voltage and current with a typical conversion time of 100ms and with 14-bit resolution. Simultaneous conversion of current and voltage measurements enables high-accuracy power calculations.

TYPICAL APPLICATION

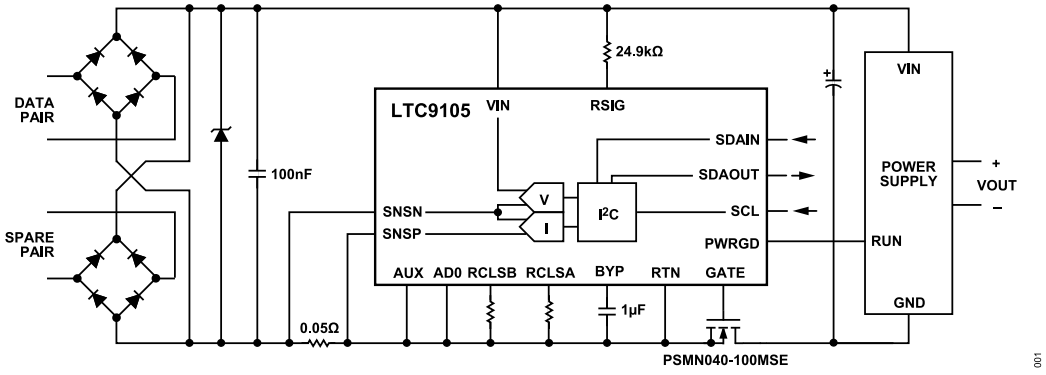

Figure 1. LTC9105 IEEE 802.3bt Powered Device with Telemetry and I²C

19-101904; Rev A; 2/25

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

2/2025—Rev. 0 to Rev. A: Initial public release

Changes to Features Section ... 1
Changes to Applications Section ... 1
Changes to Dual-Input Prioritization Section ... 13

6/2024—Revision 0: Initial release

ABSOLUTE MAXIMUM RATINGS

Table 1. Absolute Maximum Ratings

Parameter	Rating
VIN, RSIG, SDAOUT, SDAIN, SCL, AD0, PWRGD, SDAIN Voltages	−0.3V to 100V
RCLSA, RCLSB Voltages	−0.3V to 2V
RCLSA, RCLSB Current	−50mA
GATE, SNSP Voltages	−0.3V to 80V
AUX, BYP, M1, M0 Voltage	−0.3V to 5.5V
SNSN Voltage	−2V to 0.3V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability. Absolute Maximum Voltages are specified with respect to RTN (pins 7, 19, and exposed pad 21) connected together.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 2. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	Unit
UH-20-1	34	3	°C/W

[1] Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. See the Order Information.

[2] θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

[3] θ_{JC} is the junction-to-case thermal resistance.

ORDER INFORMATION

Table 3.

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC9105ATP+	LTC9105ATP+T	9105	20-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The * denotes the specifications that apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. VIN – RTN = 55V, unless otherwise noted.

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VIN Operating Input Voltage	VIN-RTN	*			60	V
I_{OFFSET}	Input Offset Current	VIN-RTN in range of V_{SIG}	*			10	µA
V_{SIG}	VIN Signature Range	VIN-RTN	*	1.5		10	V
V_{CLASS}	VIN Classification Range	VIN-RTN	*	12.5		21	V
V_{MARK}	VIN Mark Range	VIN-RTN	*	5.6		10	V
	Class/Mark Hysteresis	VIN-RTN			1.2		V
V_{ON}	VIN Gate Turn On	VIN-RTN	*	33		37	V
V_{OFF}	VIN Gate Turn Off	VIN-RTN	*	30			V
	Hot Swap On/Off Hysteresis	VIN-RTN			3.3		V
V_{RESET}	Reset Threshold	VIN-RTN, Preceded by V_{CLASS}	*	2.6		5.6	V
V_{BYP}	Bypass Pin Voltage	VIN > V_{ON}			4.3		V
Supply Current							
	Supply Current	VIN > V_{ON}	*		2.2	3.0	mA
	Supply Current During Classification	VIN = 17.5V, RCLSA and RCLSB open	*	330		600	µA
	Supply Current During Mark Event	VIN = V_{MARK} After 1st Classification Event	*	0.85		1.6	mA
Detection and Classification Signature							
	RSIG Pin Resistance	VIN = V_{SIG}, I_{RSIG}= 1mA	*			270	Ω
	Resistance During Mark Event	$R_{VIN-RTN}$, VIN = V_{MARK} After 1st Classification Event	*		8	12	kΩ
	RCLSA, RCLSB Operating Voltage	−1mA ≥ I_{RCLSA}, I_{RCLSB} ≤ −44mA, VIN = V_{CLASS}	*	0.953	0.983	1.013	V
	Classification Signature Stability Time		*	0.25		2	ms
Gate Driver							
	Active Current Limit During Inrush	SNSP-SNSN, VIN > V_{ON}, t_{ON} < t_{PWRGD}			5		mV
	GATE Pin On Voltage	GATE-RTN, I_{GATE} = 1µA	*	11	12	14	V
	GATE Pin Pull Down Current	VIN < V_{OFF}, GATE-RTN = 1V	*			0.5	mA
Auxiliary Supply Input Sense							
V_{AUX_TH}	Auxiliary Pin Threshold	AUX-RTN, VIN > V_{ON}, `aux_thresh` = 0	*	1.0	1.05	1.1	V
Digital Input/Output							
V_{IH}	Digital Input High Voltage	AD0, M1, M0	*	2.5			V
		SCL, SDAIN	*	2.2			V
V_{IL}	Digital Input Low Voltage	AD0, M1, M0	*			1.9	V
		SCL, SDAIN	*			1.7	V
	SDAOUT Pin Output Low Voltage	I_{SDAOUT} = 3mA	*			0.4	V
		I_{SDAOUT} = 5mA	*			0.7	V
	Internal Pull-Down to RTN	AD0, M1, M0			50		kΩ
	Internal Pull-Up to BYP	SCL, SDAIN			50		kΩ
Power Good							
t_{PWRGD}	PWRGD Delay Timer	From V_{ON} Threshold to PWRGD HI-Z (Note 1)			93.75		ms
I_{PWRGD}	PWRGD Current During t_{PWRGD}	PWRGD = 1V, VIN > V_{ON}, t_{ON} < t_{PWRGD}	*	195	250	305	µA
Maintain Power Signature							
	DC Integration Time				100		ms
	MPS Pulse Time				100		ms
	MPS Backoff time				200		ms
	DC MPS Threshold	SNSP-SNSN (Note 1)	*	900	1000		µV

ELECTRICAL CHARACTERISTICS

Table 4. Electrical Characteristics (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	MPS Pulse Current	I_{VIN}, In Addition To Supply Current	*	20			mA
Voltage Readback (Note 1)							
	Full Scale Range	VIN-RTN			81.55		V
	LSB Weight	VIN-RTN			9.955		mV/LSB
	Conversion Period	VIN > V_{ON}			100		ms
	Full Scale Count				16384		bits
Current Readback (Note 1)							
	Full Scale Range	SNSP-SNSN			101.1		mV
	LSB Weight	SNSP-SNSN			12.34		µV/LSB
	Conversion Period	VIN > V_{ON}			100		ms
	Full Scale Count				16384		bits
Power Readback (Note 1)							
	Full Scale Range	VIN-RTN, SNSP-SNSN = 50mΩ			165.5		W
	LSB Weight	VIN-RTN, SNSP-SNSN = 50mΩ			20.20		mW/LSB
	Conversion Period	VIN > V_{ON}			100		ms
I^2C Timing (Note 1, Figure 22)							
f_{SCLK}	Clock Frequency		*			400	kHz
t_1	Bus Free Time		*	1300			ns
t_2	Start Hold Time		*	600			ns
t_3	SCL Low Time		*	1300			ns
t_4	SCL High Time		*	600			ns
t_5	SDAIN Data Hold Time		*	0			ns
	SDAOUT Data Valid Time	$R_{BYP-SCL}$, $R_{BYP-SDAOUT}$ = 10kΩ, $C_{BYP-SCL}$, $C_{BYP-SDAOUT}$ = 10pF			470		ns
t_6	Data Setup Time		*	100			ns
t_7	Start Setup Time		*	600			ns
t_8	Stop Setup Time		*	600			ns
t_r	SCL, SDAIN Rise Time		*			300	ns
t_f	SCL, SDAIN Fall Time		*			300	ns
	SCL Fall to ACK Low	$R_{BYP-SCL}$, $R_{BYP-SDAOUT}$ = 10kΩ, $C_{BYP-SCL}$, $C_{BYP-SDAOUT}$ = 10pF			470		ns

Note 1: Guaranteed by design, not subject to test.

PIN CONFIGURATION AND FUNCTION

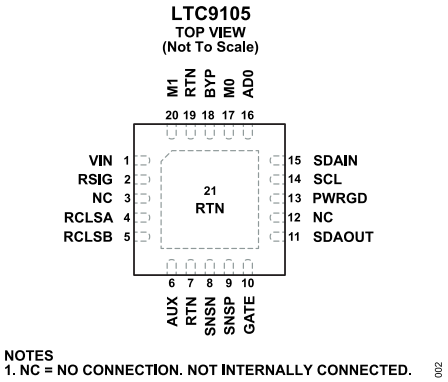


Figure 2. Pin Configuration

Table 5. Pin Function

Pin No.	Mnemonic	Description
1	VIN	PD Interface Supply Voltage. Positive input voltage for IEEE state machine and PD input voltage are referenced to this pin.
2	RSIG	External Signature Resistor Connection. Connect a 24.9kΩ resistor between RSIG and VIN.
4	RCLSA	Class Select Input. Connect a resistor between RCLSA and RTN per Table 6.
5	RCLSB	Class Select Input. Connect a resistor between RCLSB and RTN per Table 6.
6	AUX	Auxiliary Power Supply Input Sensing. This pin senses the presence of another power supply input. The AUX pin status is reflected in the `aux_status` bit. The AUX pin threshold can be configured by the `aux_thresh` bit. See Dual-Input Prioritization for a description of AUX pin behavior with respect to port or auxiliary priority.
8	SNSN	Current Sense Negative Input. System current is monitored using a 50mΩ sense resistor between SNSP and SNSN. See **Sense Resistor** for kelvin sense requirements.
9	SNSP	Current Sense Positive Input. System current is monitored using a 50mΩ sense resistor between SNSP and SNSN. See **Sense Resistor** for kelvin sense requirements.
10	GATE	External Hot Swap MOSFET Gate Control. Connect to gate of the external MOSFET.
11	SDAOUT	Serial Data Output. Open Drain Data Output for the I^2C Serial Interface Bus. The LTC9105 uses two pins to implement the bidirectional SDA function to simplify isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See I2C Interface for more information.
13	PWRGD	Power Good Open Drain Output. During inrush this pin sinks 250µA (typ.) to prevent the power supply from starting up. Current draw begins when VIN-RTN exceeds the V_{ON} threshold and continues for t_{PWRGD} (93.75ms typ.). The PWRGD pin is high impedance before and after inrush.
14	SCL	Serial Clock Input. High impedance clock input for the I^2C serial interface bus. Internally pulled up to BYP through a 50kΩ (typ.) resistor. See I2C Interface for more information.
15	SDAIN	Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC9105 uses two pins to implement the bidirectional SDA function to simplify isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. Internally pulled up to BYP through a 50kΩ (typ.) resistor. See I2C Interface for more information.
16	AD0	I^2C Chip Address Bit 0 Select. Use this pin to change the I^2C chip address. Tie this pin to RTN to set I^2C address bit AD0 to 0. Tie this pin to BYP to set bit AD0 of the I^2C chip address to 1. Internally pulled down to RTN through a 50kΩ (typ.) resistor. See I2C Interface for more information.
17, 20	M[1:0]	PoE Minimum Power Select. Use these pins to set the minimum number of Mark events required to enable the external MOSFET and power up the load. Tie high by connecting to BYP. Tie low by connecting to RTN. Internally pulled down to RTN through a 50kΩ (typ.) resistor.
18	BYP	Internal Power Supply Bypass. Connect a 1µF ceramic capacitor between this pin and RTN.
7, 19, 21 (Exposed Pad)	RTN	PD Interface Return Rail. Pin 21 (Exposed Pad) must be connected to pin 7, pin 19, and PCB heat sink.
3, 12	NC	No Connection. Not internally connected.

TYPICAL PERFORMANCE CHARACTERISTICS

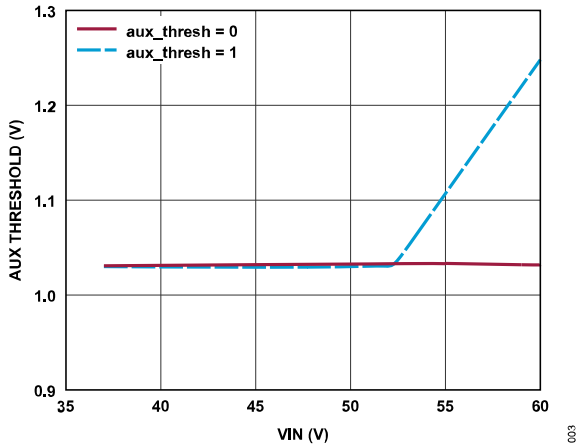


Figure 3. AUX Pin Thresholds

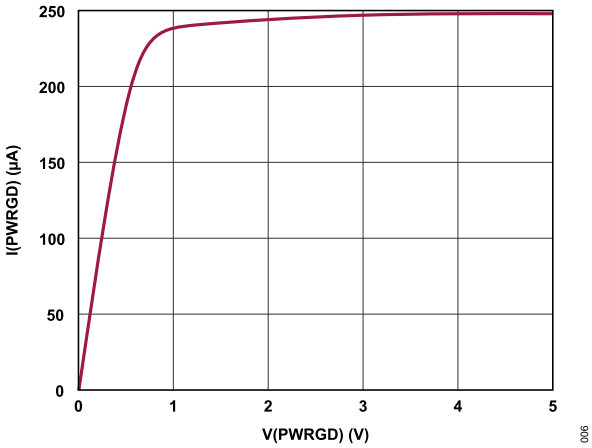


Figure 6. PWRGD Pin Pull-down Current

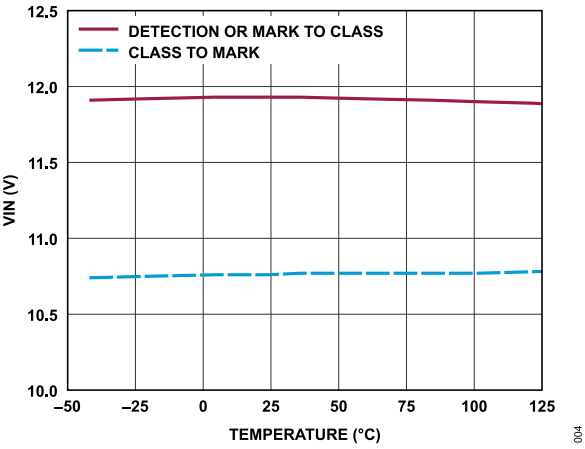


Figure 4. V_{CLASS} and V_{MARK} Thresholds

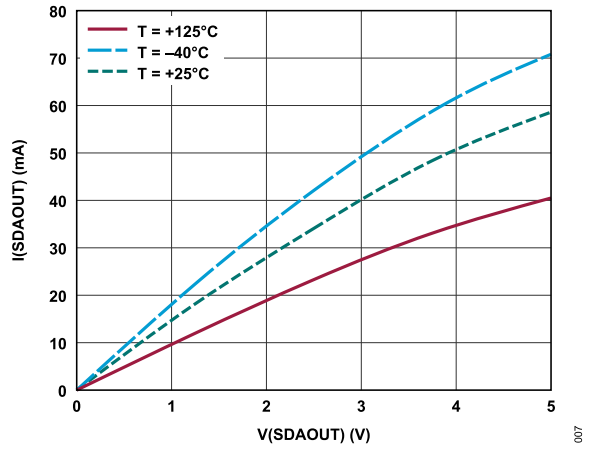


Figure 7. SDAOUT Pin Pull-down Current

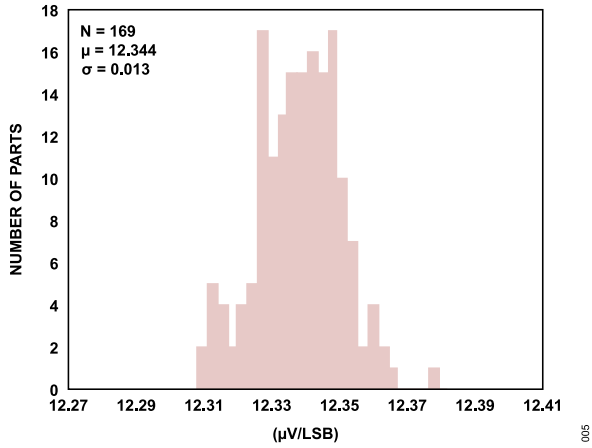


Figure 5. Current Readback LSB Weight

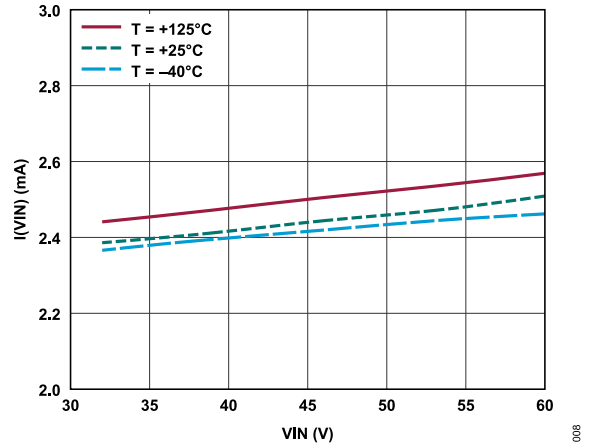


Figure 8. VIN Pin Power On Operating Current

TYPICAL PERFORMANCE CHARACTERISTICS

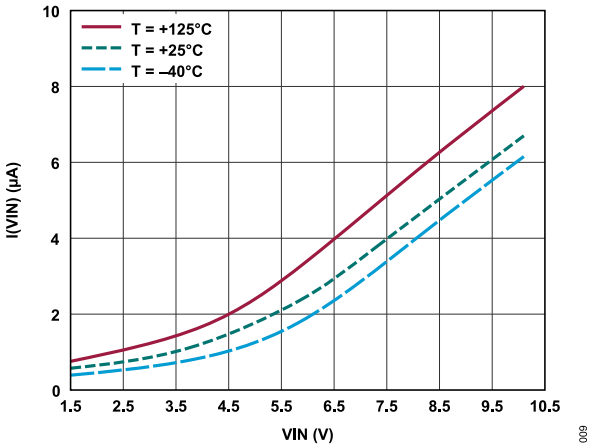


Figure 9. VIN Pin Detection Current

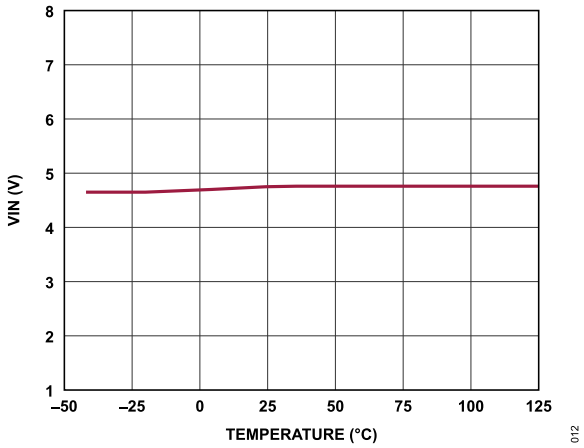


Figure 12. VIN Pin Reset Threshold

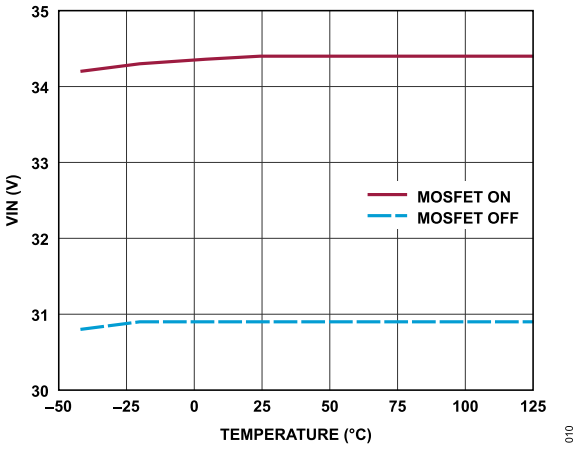


Figure 10. V_{ON} and V_{OFF} Thresholds

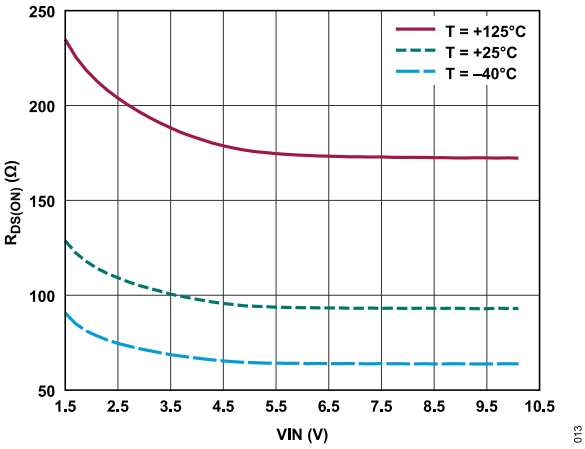


Figure 13. RSIG Pin Pull-down Resistance

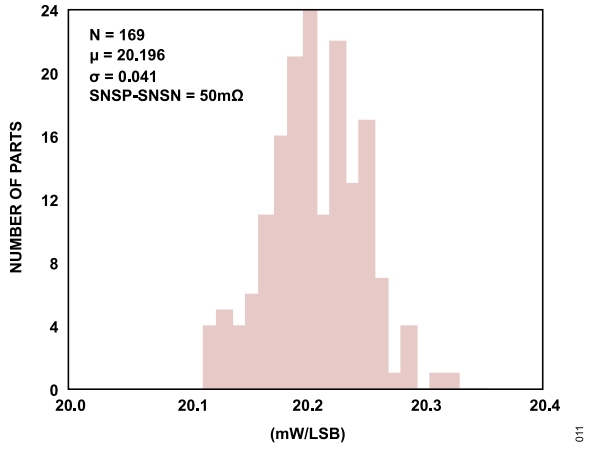


Figure 11. Power Readback LSB Weight

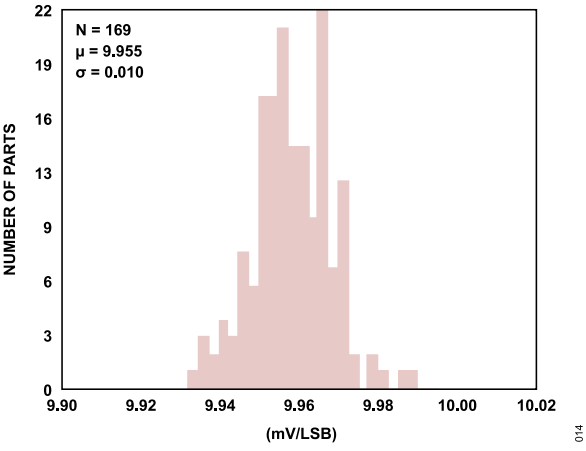


Figure 14. Voltage Readback LSB Weight

THEORY OF OPERATION

OVERVIEW

The LTC9105 is an IEEE 802.3af/at/bt-compliant powered device (PD) interface controller, allowing up to 90W operation while maintaining backwards compatibility with existing power sourcing equipment (PSE). The I^2C interface on the LTC9105 provides a simple and standard interface for the read back of the PD interface controller's input state, including PSE allocated power, auxiliary power supply presence, input voltage, and system current. Further, the LTC9105 can be configured through I^2C. Two LTC9105s, or a single LTC9105 and an optional auxiliary supply, can provide hot backup applications with automatic, seamless fail-over. An LTC9105 can also be configured not to apply power to downstream circuitry when the attached PSE provides insufficient power for the PD application.

The LTC9105 controls a low $R_{DS(ON)}$ N-channel MOSFET to maximize efficiency and delivered power. System current is sensed across a 50mΩ resistor. Analog Devices also provides a complete family of PSE, PD, and ideal bridge solutions. See Related Parts section at the end of this data sheet for more information.

MODES OF OPERATION

Detection Signature

During detection, the PSE looks for a 25kΩ signature resistor, which identifies the device as a PD. The PSE applies two voltages in the range of 2.7V to 10.1V and measures the corresponding currents. Figure 15 shows the detection voltages. The PSE calculates the signature resistance using a ΔV/ΔI measurement technique.

The LTC9105 presents the external signature resistor by connecting the RSIG pin to RTN, allowing the PSE to recognize that the PD is present and requesting power to be applied. A value of 24.9kΩ is recommended for the external signature resistor.

IEEE 802.3bt Single-Signature vs Dual-Signature PDs

IEEE 802.3bt defines two PD topologies: single-signature and dual-signature. The LTC9105 primarily targets single-signature PD topologies, eliminating the need for a second PD controller. All PD descriptions and IEEE 802.3 standard references in this data sheet are limited in scope to single-signature PDs. The LTC9105 may also be deployed in dual-signature PD applications. For more information, contact Analog Devices.

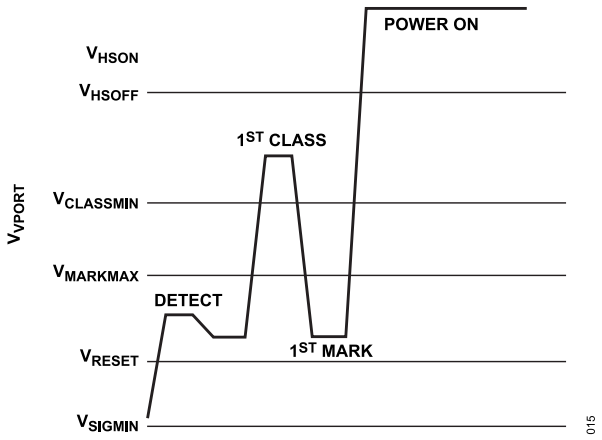


Figure 15. Type 3 or 4 PSE, Detection and 1-Event Class Sequence

IEEE 802.3bt Physical Classification, Mark, and Demotion

IEEE 802.3af/at/bt defines physical layer classification to allow a PD to request a power allocation from the connected PSE and to allow the PSE to inform the PD of the PSE's available power. A PSE, after a successful detection, may apply a classification probe voltage of 14.5V to 20.5V and measure the PD classification signature current. Once the PSE applies a classification probe voltage, the PSE may return the PD voltage to the mark voltage range before applying another classification probe voltage, or powering up the PD. An IEEE 802.3bt PSE may apply as many as five events before powering up the PD.

IEEE 802.3af/at/bt defines nine PD classes and four PD types. The LTC9105 requested class is configured by connecting RCLSA and RCLSB to RTN with 1% resistors, as shown in Table 6.

Table 6. IEEE 802.3bt Single-Signature Classification, Power Levels, and Resistor Selection

PD Requested Class	PD Requested Power (W)	PD Type	Nominal Class Current (mA)	RCLSA (Ω)	RCLSB (Ω)
0	13	Type 1	2.5	487	Open
1	3.84	Type 1 or 3	10.5	97.6	Open
2	6.49	Type 1 or 3	18.5	54.9	Open
3	13	Type 1 or 3	28	35.7	Open
4	25.5	Type 2 or 3	40	24.9	Open
5	40	Type 3	40 / 2.5	487	26.1
6	51	Type 3	40 / 10.5	97.6	33.2
7	62	Type 4	40 / 18.5	54.9	45.3
8	71.3	Type 4	40 / 28	35.7	78.7

A PD is demoted when the requested power level is not available from the PSE. If demoted, the PD must operate in a lower power state. The PSE allocated power is determined by the PD requested Class and the `pse_mark` field, as shown in Table 7.

THEORY OF OPERATION

Table 7. PSE Allocated Power

PD Requested Class	pse_mark	PSE Allocated Power
0	Any	13W
1	Any	3.84W
2	Any	6.49W
3	Any	13W
4	00b	13W
	01b, 10b, 11b	25.5W
5	00b	13W
	01b	25.5W
	10b, 11b	40W
6	00b	13W
	01b	25.5W
	10b, 11b	51W
7	00b	13W
	01b	25.5W
	10b	51W
	11b	62W
8	00b	13W
	01b	25.5W
	10b	51W
	11b	71.3W

Minimum Initial Required Power

IEEE compliance requires PDs to provide an active indication to the user when a PSE allocates insufficient power through a PSE behavior known as demotion. For PD applications that do not support demotion, the LTC9105 can be configured to block the PD application from powering up and to provide an indication.

To determine if the LTC9105 should apply power, the LTC9105 compares the number of mark events provided by the PSE to the M1 and M0 pin settings. Connect pins M1 and M0 to BYP or RTN according to Table 8 to configure the minimum initial required power.

Table 8. Setting Minimum Initial Required Power

Initial Power Requirement	M1 PIN	M0 PIN	pse_mark	MOSFET State
13W or less	RTN	RTN	Any	ON
13W thru 25.5W	RTN	BYP	00b	OFF
			01b, 10b, 11b	ON
25.5W thru 51W	BYP	RTN	00b, 01b	OFF
			10b, 11b	ON
Greater than 51W	BYP	BYP	00b, 01b, 10b	OFF
			11b	ON

When insufficient power is allocated and the AUX pin is low, the PWRGD pin sinks I_{PWRGD}, the Hot Swap MOSFET is turned off, and the LTC9105 draws minimal current (see Automatic Maintain Power Signature) to keep the PoE input powered. The PWRGD pin and MOSFET state can be combined as an indication of insufficient power allocation.

Link Layer Discovery Protocol (LLDP) Power Negotiation

In PoE systems, after initial power-on, power may be renegotiated through LLDP. The LTC9105 does not have access to Ethernet data and does not react automatically to LLDP power negotiation, including PWRGD pin state, MOSFET state, and seamless switchover settings.

For seamless switchover applications, the application processor may need to update the LTC9105's power priority mode when renegotiating power through LLDP. See Dual-Input Prioritization.

Inrush and Power On

Once the PSE detects and classifies the PD, the PSE applies power to the PD depending on the rules described in Dual-Input Prioritization. When the port voltage rises above the V_{ON} threshold, and the LTC9105 determines if the PSE allocated power is equal or higher than the PD requested power, and if an auxiliary power source is not present (through the aux_status bit), the LTC9105 drives the external MOSFET GATE pin so as to allow a 100mA (typ) current to charge the external bulk capacitor. When the bulk capacitor is fully charged and the MOSFET current drops below 100mA, the external MOSFET is fully enhanced. In the event the external MOSFET does not enhance within 93.75ms (typ), inrush times out.

When inrush times out, the MOSFET turns off and the Automatic MPS feature is disabled. The PD remains in this state until the port voltage drops below V_{OFF}. See Automatic Maintain Power Signature for further description of the Automatic MPS feature.

Power Good

The PWRGD pin is used to hold off the downstream circuitry until inrush is complete and the external MOSFET is fully enhanced.

The PWRGD pin first sinks I_{PWRGD} (250uA, typ.) starting when the port voltage rises above V_{ON} and continuing for up to t_{PWRGD} (93.75ms, typ.), then enters a high impedance state to allow an external PWRGD pull-up to assert the power good indication.

AUXILIARY INPUT

The AUX pin is used to detect when an auxiliary power supply is attached. Figure 16 shows an example of an AUX sensing circuit.

When an auxiliary power supply is detected, aux_status is set to 1. The LTC9105 MOSFET state (ON or OFF) is configurable, based on stdby_dis and priority bit settings; see Dual-Input Prioritization for seamless switchover options, example AUX sensing circuit, and register configuration.

THEORY OF OPERATION

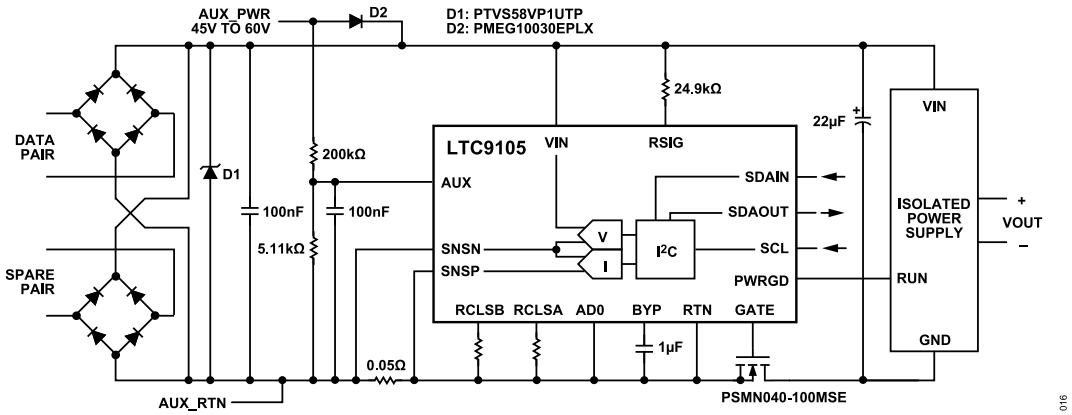


Figure 16. LTC9105 with Auxiliary Power Supply Input

THEORY OF OPERATION

DUAL-INPUT PRIORITIZATION

The LTC9105 supports dual-input power path prioritized solutions. The first input is a primary LTC9105 and the second input may be either an auxiliary supply (see Figure 17) or a secondary LTC9105. The LTC9105 targets seamless switchover topologies, which only draw power from one input at a time, switching over to the secondary input when power is removed from the primary input.

Details on PD/auxiliary seamless switchover are provided in this data sheet. Contact Analog Devices for information and support regarding dual PD seamless switchover, to enable hitless failover between dual-port PoE supplies.

LTC9105 systems enable three power priority modes, as shown in Table 9. An LTC9105 configured in Primary mode provides power to the load. An LTC9105 configured in Hot Secondary mode enables seamless switchover, providing power to the load when power is removed from the first input. An LTC9105 may be ineligible to provide seamless switchover due to insufficient power allocation; in this case, an LTC9105 may be configured in Cold Secondary mode to prevent seamless switchover when power is removed from the first input, forcing a system reboot and power allocation refresh.

If the AUX pin is low (AUX < V_{AUX_TH}) at LTC9105 power on, the LTC9105 sets its `priority` bit and clears its `stdby_dis` bit, entering Primary mode.

If the AUX pin is high (AUX > V_{AUX_TH}) at LTC9105 power on, the LTC9105 automatically clears its `priority` and `stdby_dis` bits, entering Hot Secondary mode.

In Hot Secondary mode, the LTC9105 will automatically transition to Primary mode when AUX pin goes low. This seamless switchover ensures power is maintained at the load.

In Cold Secondary mode, the LTC9105 automatically removes MPS when the AUX pin goes low. This behavior enables a port power cycle through the IEEE DC MPS feature to force a system reboot and power allocation refresh. Cold Secondary mode is used to ensure a higher power primary input does not fail-over to a lower power secondary input. Applications implementing Cold Secondary mode must take care to reduce total current below the minimum IEEE DC MPS threshold (4mA) to meet IEEE requirements for power removal.

Current is limited by the PSE during a seamless switchover event.

The switchover threshold from primary to secondary is set using an external AUX circuit. The switchover threshold should be set just under the $V_{PORT\_PD-2P,MIN}$ threshold for the application's requested PoE Class as specified in IEEE 802.3bt standard. The IEEE standard specifies V_{PORT_PD-2P} at the RJ-45 interface. Remember to consider any extra voltage drops due to diode forward voltage or resistance between the RJ-45 connector and the AUX circuit.

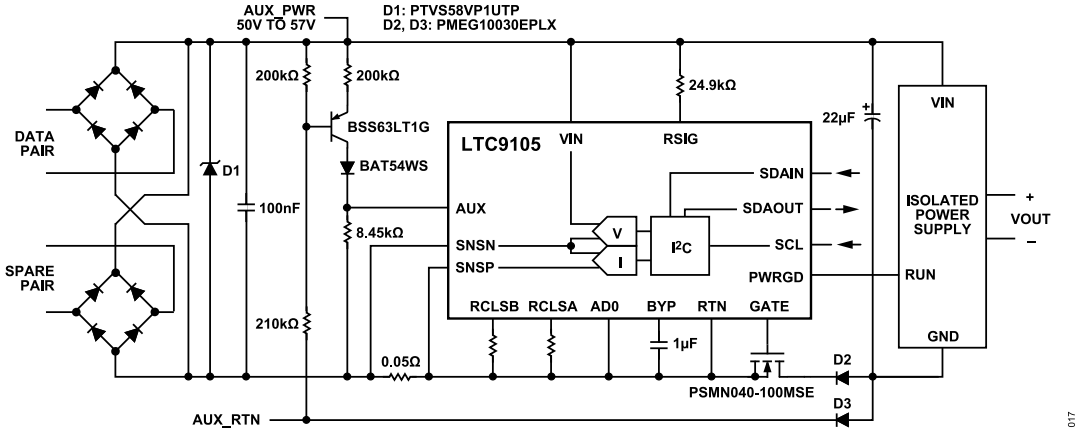


Figure 17. LTC9105 with Dual-Input Auxiliary Circuit

Table 9. Power Priority Modes and Behaviors

Mode	`priority`	`stdby_dis`	MOSFET State	Description
Primary	1	0	ON	MPS current is drawn automatically if load current drops below MPS.
Hot Secondary	0	0	OFF	MPS current is drawn automatically, to keep the PoE input powered. If the primary input drops, as sensed at AUX pin, the secondary input automatically becomes the primary input by enabling the LTC9105's MOSFET and setting the `priority` bit.

THEORY OF OPERATION

Table 9. Power Priority Modes and Behaviors (Continued)

Mode	priority	stdby_dis	MOSFET State	Description
Cold Secondary	0	1	OFF	MPS current is drawn automatically, to keep the PoE input powered. If the primary input drops, as sensed at AUX pin, the MPS current is removed and the LTC9105's MOSFET remains disabled, enabling a port power cycle.

AUTOMATIC MAINTAIN POWER SIGNATURE

A PSE removes power when a connected PD no longer draws a minimum amount of current, known as the maintain power signature (MPS) current. The LTC9105 implements an Automatic MPS feature, which detects when the current falls below the DC MPS threshold (20mA typ., $R_{SNSP-SNSN}$ = 50mΩ) and automatically generates a current pulse to maintain PoE power. This feature is enabled by default at power-up.

Figure 18 shows an example of Automatic MPS timing. The LTC9105's MPS state machine works on a 100ms (typ.) time base. An MPS pulse is issued when the average current over a 100ms (typ.) period drops below the DC MPS threshold. The MPS pulse current has an amplitude greater than 20mA and a duration of 100ms (typ.). No pulses are issued in the following 200ms (typ.). The LTC9105 stops drawing MPS pulse current once the average current is above the DC MPS threshold.

Automatic MPS is disabled in one of two conditions. First is when the inrush timer expires, that is, if power up of the load does not complete within 93.75ms (typ.). And second, when `stdby_dis` is set to 1 and an auxiliary supply is not present (when `aux_status` reports 0; when AUX < V_{AUX_TH}).

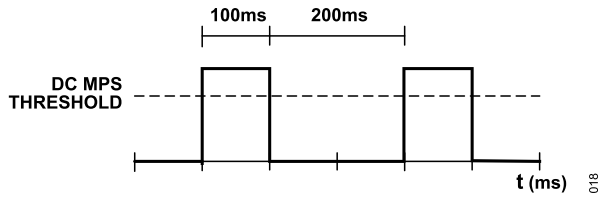


Figure 18. MPS Timing

ANALOG-TO-DIGITAL CONVERTERS (ADC)

The LTC9105 has two first order delta sigma analog-to-digital converters (ADCs) that simultaneously measure application current and supply voltage. The converters operate at an over sample rate (OSR) of 2.5MHz (typ.) and complete a full conversion every 100ms (typ.). First order delta sigma converters provide superior performance for power monitoring applications because the measured signals are averaged with even weight across the conversion period. Delta-sigma converters produce a mean average by integrating the area under the signal curve across the conversion period. Furthermore, simultaneous conversion of voltage and current allows high accuracy power calculations, ensuring the voltage and current factors are sampled during the same period.

Measuring application power at the PD controller input captures the DC/DC conversion losses missed by traditional power monitors after the converter. Analog Devices recommends using the LT4321 ideal diode bridge for minimal bridge voltage drop and increased telemetry accuracy with respect to the RJ45 input (see **PoE Input Bridge** in External Component Selection).

VIN Readback

When configured to report voltage telemetry by clearing the `padc_en` bit, the LTC9105 continuously measures the VIN voltage with a dedicated A/D converter. This measurement is fully synchronized to the current measurement and can continue to monitor until VIN drops below V_{OFF}. This telemetry is updated every 100ms.

When the `padc_data` bit reports '0', the `voltage_power` field contains voltage readings.

Power Readback

When configured to report power telemetry by setting the `padc_en` bit, the LTC9105 continuously measures the PD power by internally multiplying port voltage and current, and reports the power telemetry to the `voltage_power` field. This measurement is fully synchronized to the current and voltage measurements and can continue to monitor until VIN drops below V_{OFF}. This telemetry is updated every 100ms.

When the `padc_data` bit reports '1', the `voltage_power` field contains power readings.

Current Readback

The LTC9105 measures the voltage across the SNSP and SNSN pins through a 50mΩ sense resistor. This measurement is fully synchronized to the power/voltage measurements and can continue to monitor until VIN drops below V_{OFF}. Current telemetry is reported to the `current` field. This telemetry is updated every 100ms.

I²C INTERFACE

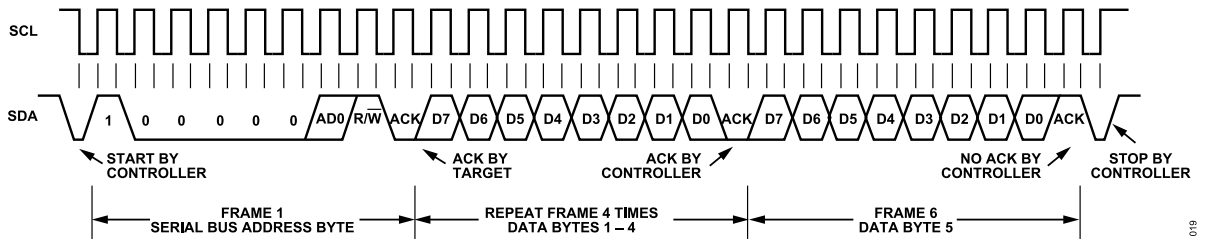


Figure 19. Short Form I²C Multi-Byte Read

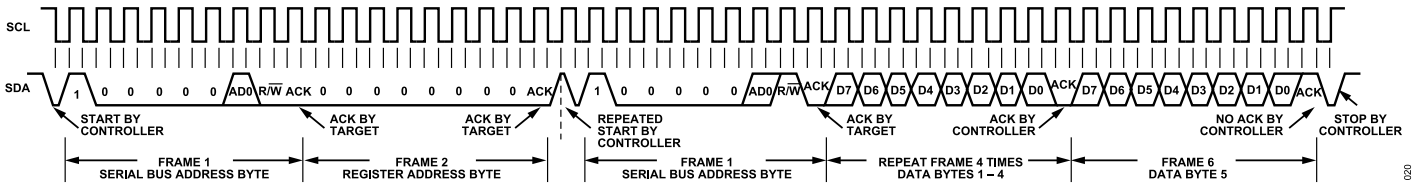


Figure 20. Long Form I²C Multi-Byte Read

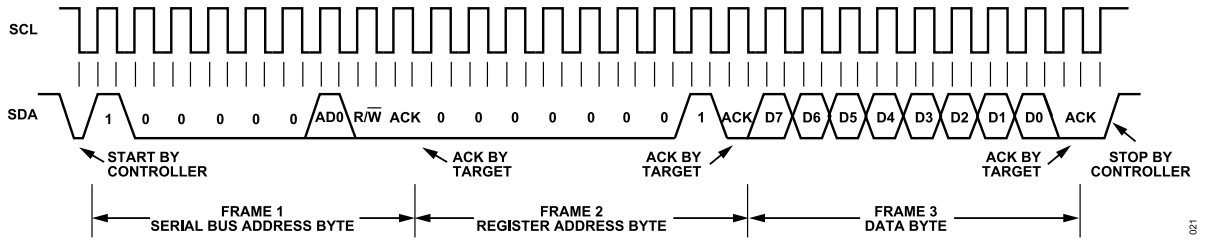


Figure 21. I²C Write

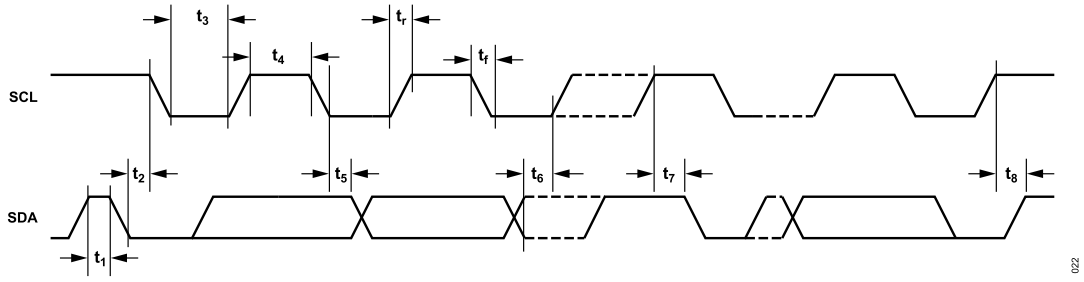


Figure 22. I²C Interface Timing

I²C Interface Overview

The LTC9105 includes an I²C serial interface, enabling the PD's application processor to read parametric telemetry, PSE allocated power, and auxiliary input status; and to write power input priority. See Table 10 for register details and descriptions.

Figure 22 presents the I²C interface timing parameters. These parameters are defined for the LTC9105 in Electrical Characteristics.

I²C Serial Address Byte

The LTC9105 chip address (bits [7:1] of the serial address byte) is settable to 0x40 or 0x41, based on the AD0 pin setting. Tie AD0 to RTN to set the chip address to 0x40, or tie AD0 to BYP to set the chip address to 0x41.

I²C Read

There are two ways to read data from the I²C port on the LTC9105. The LTC9105 responds to either a short form multi-byte read (Figure 19) or a long form multi-byte read (Figure 20). When reading from the LTC9105 with a long form multi-byte read, always read from register address 0x00.

I²C data is gathered from the LTC9105 in a single 5-byte read. Reading multiple bytes in the same transaction ensures that parametric data is from the same ADC conversion. For example, the current LSB and current MSB must be read concurrently to ensure that the upper byte and lower byte values are from the same conversion. Similarly, voltage (or power) and current read back must

I²C INTERFACE

be done concurrently to ensure that data for power (or voltage) calculations are from the same period in time.

I²C Write

The LTC9105 can be configured using an I²C write, as shown in Figure 21. When writing to the LTC9105, always write to register address 0x01, and only write a single byte of data; only the first byte in the register map is writable.

REGISTER MAP

Table 10. I²C Register Map

Byte	BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
1	aux_status	pse_mark[1:0]		aux_thresh	padc_enable	stdby_dis	priority	brownout
2	old_data	ioverflow	current[13:8]					
3	current[7:0]							
4	padc_data	vpoverflow	voltage_power[13:8]					
5	voltage_power[7:0]							

Table 11. I²C Register Details

Byte	Bit	Data	Access	Reset Value	Description
1	7	aux_status	RO	See description	Auxiliary Status. Returns 1 if an auxiliary supply is detected. Returns 0 if an auxiliary supply is absent. See Auxiliary Input and Dual-Input Prioritization. The reset value is determined by the AUX pin state.
1	6:5	pse_mark	RO	See description	PSE Mark Response. Combine this field with PD requested Class to determine PSE allocated power. See Table 7. 0 : 0-1 Mark Events, PSE allocated power is Min(PD Requested Class, 13W) 1 : 2-3 Mark Events, PSE allocated power is 25.5W 2 : 4 Mark Events, PSE allocated power is Min(PD Requested Class, 51W) 3 : 5+ Mark Events, PSE allocated power is Min(PD Requested Class, 71.3W) The reset value is a function of the preceding physical classification result.
1	4	aux_thresh	R/W	0	Auxiliary Threshold Configuration. When set, the LTC9105 AUX pin uses a variable threshold (see Figure 3). When cleared, the LTC9105 AUX pin uses a 1.05V (typ.) threshold.
1	3	padc_enable	R/W	0	Power ADC Enable. When set, the LTC9105 reports input average power in the voltage_power field and the padc_data bit is set. When clear, the LTC9105 reports the input average voltage in the voltage_power field and the padc_data bit is cleared.
1	2	stdby_dis	R/W	0	Standby Disable. Controls MOSFET state and Automatic MPS feature based on AUX pin state and priority setting. See Dual-Input Prioritization.
1	1	priority	R/W	See description	Port Priority. Controls MOSFET state and Automatic MPS feature based on AUX pin state and stdby_dis setting. See Dual-Input Prioritization. The reset value is the inverse of the AUX pin state, and is latched on reset exit.
1	0	brownout	R/W1C	0	Brownout Indication. Indicates that the input voltage has fallen below V_{OFF} threshold, then returned to V_{ON} without crossing the V_{RESET} threshold. Remains set until cleared by user. Clear by writing a 1 to this bit.
2	7	old_data	RO	0	Old Data Indication. This bit is set when an ADC conversion is read over the I²C interface and cleared when a new ADC conversion is available.
2	6	ioverflow	RO	0	Current Overflow Status. If set, the current readback is an overflow (the measurement was outside the full scale range of the ADC). Disregard the value in current[13:0] when ioverflow is set. This field is updated with every ADC conversion.
2	5:0	current[13:8]	RO	0	Current Telemetry MSB. Upper bits of the current telemetry. Combine with current[7:0] for a complete current telemetry reading. This field is updated with every ADC conversion.
3	7:0	current[7:0]	RO	0	Current Telemetry LSB. Lower bits of the current telemetry. Combine with current[13:8] for a complete current telemetry reading. Representing 246.8µA/LSb (14-bit) with an offset of 0x2000. Full scale range ±2.022A. All values are typical and assume $R_{SNSP-SNSN}$ = 50mΩ. This field is updated with every ADC conversion.
4	7	padc_data	RO	0	Power Telemetry Indicator. Returns 1 if voltage_power[13:0] contains power data. Returns 0 if voltage_power[13:0] contains voltage data. This field is updated with every ADC conversion.

REGISTER MAP

Table 11. I²C Register Details (Continued)

Byte	Bit	Data	Access	Reset Value	Description
4	6	vpoverflow	RO	0	Voltage/Power Overflow Status. If set, the voltage or power readback is an overflow (the measurement was outside the full scale range of the ADC). Disregard the value in voltage_power[13:0] when vpoverflow is set. This field is updated with every ADC conversion.
4	5:0	voltage_power[13:8]	RO	0	Voltage/Power Telemetry MSB. Upper bits of the voltage or power telemetry. Combine with voltage_power[7:0] for a complete voltage/power telemetry reading. This field is updated with every ADC conversion.
5	7:0	voltage_power[7:0]	RO	0	Voltage/Power Telemetry LSB. Lower bits of the voltage or power telemetry. Combine with voltage_power[13:8] for a complete voltage or power telemetry reading. When padc_data is cleared, voltage_power contains a voltage reading, representing 9.955mV/LSB (14-bit) with an offset of 0x2000. Full scale range ±81.55V. When padc_data is set, voltage_power contains a power reading, representing 20.20mW/LSB (14-bit) with an offset of 0x2000. Full scale range ±165.5W. All values are typical and assume $R_{SNSP-SNSN}$ = 50mΩ. This field is updated with every ADC conversion.

Access Key:

R/W = Read/Write. Field can be read and written normally.

RO = Read Only. Field can be read normally. Writes to a "Read Only" field are ignored.

R/W1C = Read/Write-1-to-Clear. Field can be read normally. Bits that have '1' written to them are cleared. Bits that have '0' written to them are unchanged.

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

PoE Input Bridge

A PD is required to polarity-correct its input voltage. There are several different options available for bridge rectifiers; silicon diodes, Schottky diodes, and ideal diodes. When silicon or Schottky diode bridges are used, the diode forward voltage drops affect the voltage at the VIN pin. The LTC9105 is designed to tolerate these voltage drops. Note, the parameters shown in Electrical Characteristics are specified at the LTC9105 package pins.

A silicon diode bridge consumes up to 4% of the available power. In addition, silicon diode bridges exhibit poor pairset-to-pairset unbalance performance. Each branch of a silicon diode bridge shares source/return current, and thermal runaway can cause large, non-compliant current unbalances between pairsets.

While using Schottky diodes can help reduce the power loss with a lower forward voltage, the Schottky bridge may not be suitable for high temperature PD applications. Schottky diode bridges exhibit temperature induced leakage currents. The leakage current has a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications.

For high efficiency applications, the LT9105 supports an LT4321-based PoE ideal diode bridge that reduces the forward voltage drop from 0.7V to 20mV per diode while maintaining IEEE 802.3 compliance. The LT4321 simplifies thermal design, eliminates costly heat sinks, and can operate in space-constrained applications. In addition, with the very low voltage drop of the LT4321 ideal diode bridge, the LTC9105's voltage readback is closer to the PD's true input voltage.

Input Capacitor

A 0.1µF capacitor is needed from VIN to SNSN to meet the input impedance requirement in IEEE 802.3 and to properly bypass the LTC9105. When operating with the LT4321, locally bypass each with a 0.047µF capacitor, thus keeping the total port capacitance within specification. Place each capacitor as close as possible to both the LTC9105 and LT4321. See Figure 26.

Transient Voltage Suppressor

The LTC9105 specifies an absolute maximum voltage of 100V and is designed to tolerate brief over voltage events due to Ethernet cable surges. To protect the LTC9105 from an overvoltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ58A or PTVS58VP1UTP between the VIN and SNSN pins. Place the TVS as close as possible to the LTC9105.

Exposed Pad

The LTC9105 package has an exposed pad internally connected to RTN. The exposed pad may only be connected to RTN on the printed circuit board. Ensure the Exposed Pad has access to a printed circuit board plane as a heat sink.

Signature Resistor (RSIG)

A 24.9kΩ, 1% resistor must be connected between VIN and RSIG for IEEE compliant detection. The RSIG pin is low impedance when the input voltage is in the V_{SIG} range, then switches to high impedance as the input voltage crosses into the V_{CLASS} range to save power. The RSIG pin becomes low impedance again when the input voltage falls below V_{RESET}.

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. Choosing a MOSFET requires extensive analysis and testing of the MOSFET SOA curve against the various PD current limit conditions. Analog Devices recommends the PSMN075-100MSE for PDs configured to deliver up to 51W maximum port power (single-signature) or 25.5W maximum pairset power (dual-signature). For PDs configured to power up to 71.3W maximum port power (single-signature) or 35.6W maximum pairset power (dual-signature), Analog Devices recommends the PSMN040-100MSE. These MOSFETs are selected for their proven reliability in PoE applications. Contact Analog Devices before using a MOSFET other than one of these recommended parts.

I^2C Interface Isolation

A high speed isolation interface is recommended for I^2C communications with the LTC9105. Analog Devices recommends the ADuM1252ASA for I^2C isolation.

Figure 23 shows the suggested connection of the I^2C interface when the system processor is powered by an isolated supply.

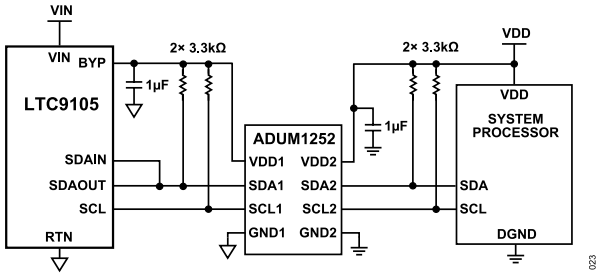


Figure 23. I^2C Interface Isolation

Pull-up resistors connected to the isolator should be adjusted based on the specific isolator and the desired speed of the I^2C interface.

LAYOUT CONSIDERATIONS

Sense Resistor

The LTC9105 is designed for a low 50mΩ current sense resistance. For the LTC9105 ADC to present an accurate current telemetry, the sense resistors should have ±1% tolerance or better and no more than ±200ppm/°C temperature coefficient.

APPLICATIONS INFORMATION

Proper connection of the current Kelvin sense lines (SNSP, SNSN) is important for current measurement accuracy. See Figure 24 for an example layout of these Kelvin sense lines. The LTC9105 SNSP and SNSN pins are Kelvin connected to the sense resistor pad and are not otherwise connected in the power path. Figure 24 shows the two Kelvin traces from the LTC9105 to the sense resistor (RSENSE).

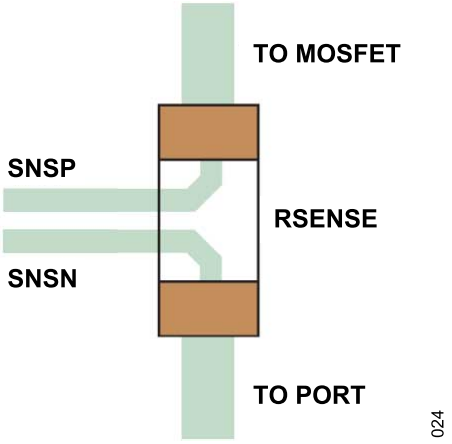


Figure 24. Sense Resistor Kelvin Sense

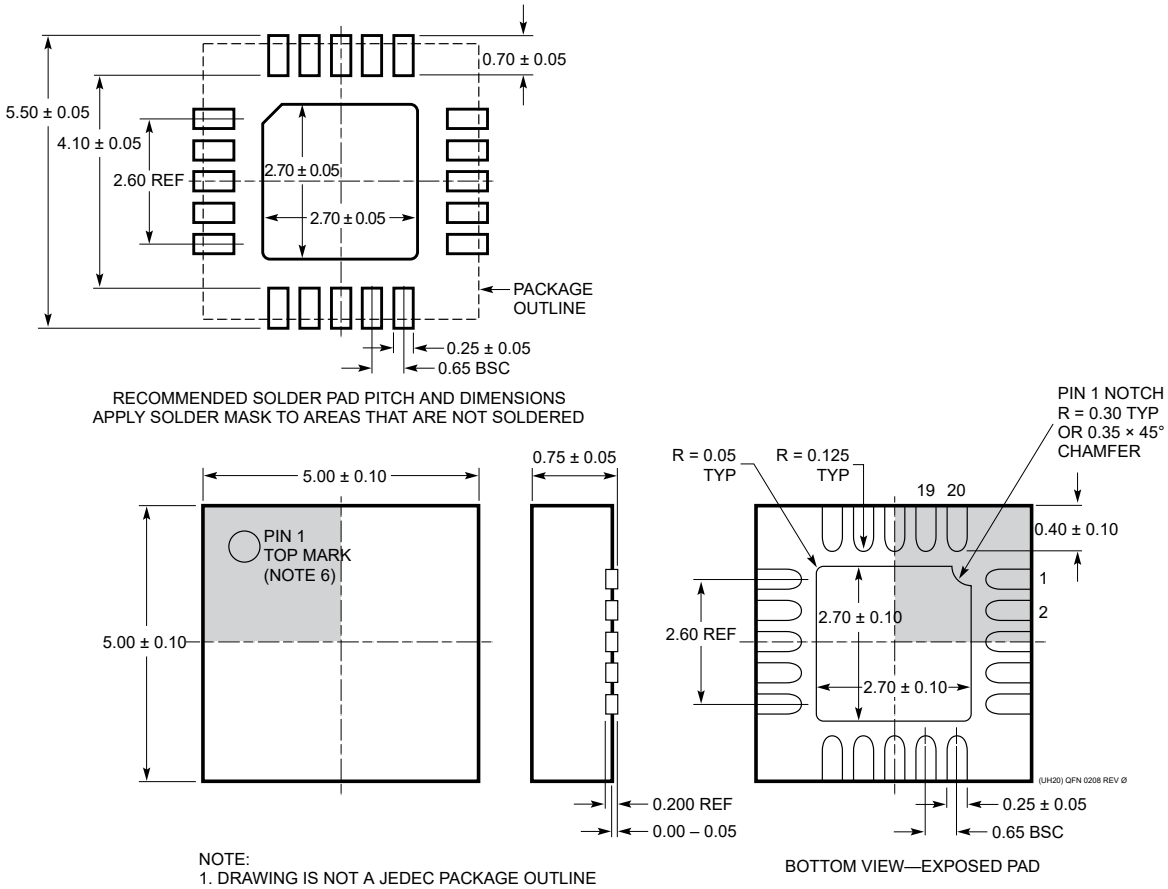
RCLSA and RCLSB

Avoid excessive parasitic capacitance on the RCLSA and RCLSB pins and place resistors RCLSA and RCLSB close to the LTC9105.

BYP Capacitor

Connect a 1µF ceramic capacitor from BYP to RTN as close as possible to the LTC9105 package.

OUTLINE DIMENSIONS



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 25. UH Package (20-Lead Plastic QFN (5mm × 5mm))

TYPICAL APPLICATION

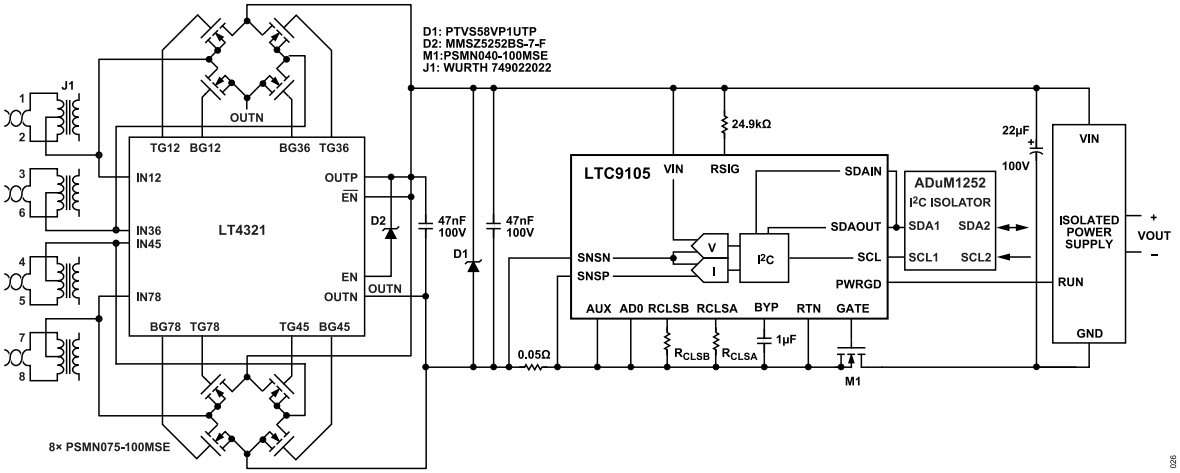


Figure 26. LTC9105 IEEE 802.3bt Powered Device with Telemetry and Isolated I²C

RELATED PARTS

Table 12. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTC9101-1/LTC9102/ LTC9103	48-Port IEEE 802.3bt PoE PSE Controller	Lowest in Industry Power Path Dissipation with 0.1Ω Sense, Transformer Isolated Communications
LTC4292/LTC4291-1	4-Port IEEE 802.3bt PoE PSE Controller	Transformer Isolation, 14-bit Current Monitoring per Port with Programmable Current Limit, Supports Type 1-4 PDs
MAX5996	IEEE 802.3bt-Compliant PD Controller	Power Telemetry and Power/Current Limit. Internal MOSFET.
MAX5995	IEEE 802.3bt-Compliant, PD Controller	Integrated 91W High-Power MOSFET
LT4293	LTPoE++®/IEEE 802.3bt PD Controller	External Switch, LTPoE++ and IEEE 802.3bt Support, Configurable Class and AUX Support
LT4294	IEEE 802.3bt PD Controller	External Switch, IEEE 802.3bt Support, Configurable Class and AUX Support
LT4295	IEEE 802.3bt PD with Forward/Flyback Switching Regulator Controller	External Switch, Configurable Class, Forward or No-Opto Flyback Operation, Frequency, PG/SG Delays, Soft-Start, and Aux Support as Low as 9V. Includes Housekeeping Buck, Slope Compensation
LTC4290/LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs
LTC4263	Single IEEE 802.3af PSE Controller	Internal MOSFET Switch
LTC4265	IEEE 802.3at PD Controller	Internal 100V, 1A Switch, 2-Event Classification Recognition
LTC4266	Quad IEEE 802.3at PoE PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification, and Port Current and Voltage Monitoring
LTC4267	IEEE 802.3af PD Controller with Integrated Switching Regulator	Internal 100V, 400mA Switch, Dual Inrush Current, Programmable Class
LTC4270/LTC4271	12-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports Type 1, Type 2 and LTPoE++ PDs
LTC4278	IEEE 802.3at PD Controller with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4279	Single PoE/PoE+/LTPoE++ PSE Controller	Supports IEEE 802.3af, IEEE 802.3at, LTPoE++ and Proprietary PDs
MAX5974A/B/C/D	Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers	Regulation Without Optocoupler (A/B Variants), Internal 1% Error Amplifier, Programmable PWM Soft-Start
ADP1074	Isolated, Synchronous Forward Controller with Active Clamp and iCoupler®	Up to 5kV Dielectric Isolation, Wide Voltage Supply Range, Programmable Frequency (50kHz to 600kHz)