Data Sheet

LTC7897

140V, Low I_Q, Synchronous Buck Controller with Programmable 5V to 10V Gate Drive

FEATURES

- Wide V_{IN} Range: 4V to 135V (140V ABS MAX)
- Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 135V (140V ABS MAX)
- Adjustable Gate Drive Level: 5V to 10V (OPTI-DRIVE, 15V ABS MAX)
- Adjustable Driver Voltage UVLO
- Adaptive or Resistor Adjustable Dead Times
- Split-Output Gate Drivers for Adjustable Turn-On and Turn-Off Driver Strengths
- 100% Duty Cycle Operation
- Low Operating I_Q: 5µA (48V_{IN} to 3.3V_{OUT})
- Spread Spectrum Frequency Modulation
- Programmable Frequency (100kHz to 2.5MHz)
- Synchronizable Frequency (100kHz to 2.5MHz)
- 28-Pin (4mm x 5mm) QFN Package

APPLICATIONS

- Industrial Power Systems
- Military/Avionics
- Telecommunications Power Systems

GENERAL DESCRIPTION

The *LTC®7897* is a high performance, 100% duty cycle capable, synchronous step-down, DC/DC switching regulator controller that drives all N-channel synchronous silicon metal oxide field effect transistor (MOSFET) power stages. Synchronous rectification increases efficiency, reduces power loss, and simplifies the application design by reducing thermal requirements.

The wide input and output voltage ranges of the LTC7897 enable not only high step-down ratios but also a wide range of positive to negative voltage conversion.

The gate drivers of the LTC7897 provide robustness with a 15V ABS MAX rating and flexibility with adjustable drive levels and dead times to optimize applications. The gate drive voltage of the LTC7897 can optionally be adjusted from 5V to 10V to allow use of logic-level or standard threshold MOSFETs. The dead times of the LTC7897 can be optimized with external resistors for margin or to tailor the application for higher efficiency and allow for high frequency operation.

TYPICAL APPLICATION

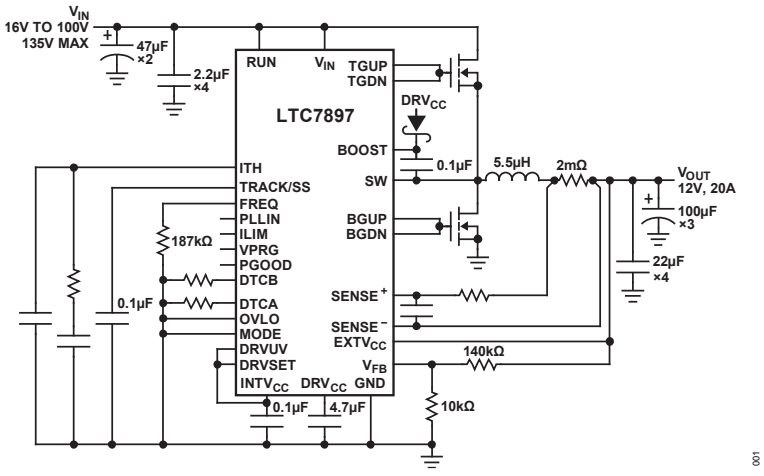

Figure 1. High Efficiency 100V/12V Output Step-Down Converter

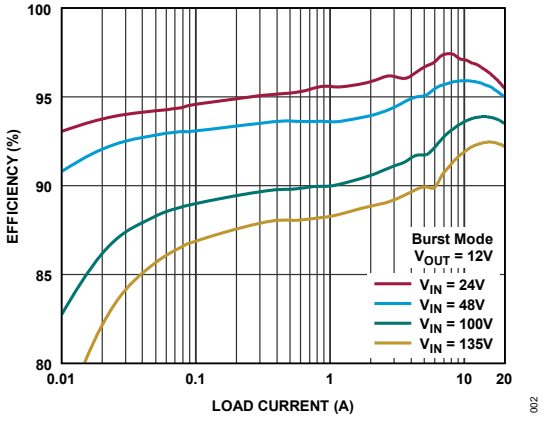

Figure 2. V_{OUT} Efficiency for Figure 1

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	2/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = floating, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Supply (V_{IN})						
Input Supply Operating Range	V_{IN}		4		135	V
Input Supply Current in Regulation	I_{VIN}	48V to 5V, no load[1] 14V to 3.3V, no load[1]		5 9		µA µA
Controller Operation						
Regulated Output Voltage Set Point	V_{OUT}		0.8		135	V
Regulated Feedback Voltage[2]	V_{FB}	V_{IN} = 4V to 135V, ITH Voltage = 0.6V to 1.2V VPRG = floating, T_A = 25°C VPRG = floating VPRG = 0V VPRG = $INTV_{CC}$	 0.792 0.788 4.890 11.73	 0.8 0.8 5.0 12	 0.808 0.812 5.110 12.27	 V V V V
Feedback Current[2]		VPRG = floating, T_A = 25°C VPRG = 0V or $INTV_{CC}$, T_A = 25°C	-50	0 1	+50 2	nA µA
Feedback Overvoltage Threshold		Relative to V_{FB}, T_A = 25°C	7	10	13	%
Transconductance Amplifier g_m[2]	g_m	ITH = 1.2V, Sink and Source = 5µA		1.8		mMho
Maximum Current Sense Threshold	$V_{SENSE(MAX)}$	V_{FB} = 0.7V, $SENSE^-$ = 3.3V ILIM = 0V ILIM = floating ILIM = $INTV_{CC}$	 21 45 67	 25 50 75	 29 55 83	 mV mV mV
$SENSE^+$ Pin Current	I_{SENSE^+}	$SENSE^+$ = 3.3V, T_A = 25°C	-1		+1	µA
$SENSE^-$ Pin Current	I_{SENSE^-}	$SENSE^-$ < 3V 3.2V ≤ $SENSE^-$ < $INTV_{CC}$ – 0.5V $SENSE^-$ > $INTV_{CC}$ + 0.5V		2 30 700		µA µA µA

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = floating, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Soft-Start Charge Current		TRACK/SS = 0V	7	9	11	µA
RUN Pin ON Threshold RUN Pin Hysteresis		RUN Rising	1.15	1.20 120	1.25	V mV
OVLO Pin OFF Threshold OVLO Pin Hysteresis	OVLO	OVLO Rising	1.15	1.20 120	1.25	V mV
DC Supply Current						
V_{IN} Shutdown Current		RUN = 0V		1		µA
V_{IN} Sleep Mode Current		$SENSE^-$ < 3.2V, $EXTV_{CC}$ = 0V		15		µA
Sleep Mode Current[3] V_{IN} Current V_{IN} Current $EXTV_{CC}$ Current $SENSE^-$ Current		 $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ = 0V $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ ≥ 12V $SENSE^-$ ≥ 3.2V, $EXTV_{CC}$ ≥ 12V $SENSE^-$ ≥ 3.2V		 5 1 4 10		 µA µA µA µA
Pulse-Skipping or Forced Continuous Mode (FCM), V_{IN} or $EXTV_{CC}$ Current[3]				2		mA
Gate Drivers						
TGxx or BGxx On-Resistance		DRVSET = $INTV_{CC}$ Pull-up Pull-down		 2.0 1.0		 Ω Ω
TGxx or BGxx Transition Time[4] Rise Time Fall Time		 C_{LOAD} = 3300pF C_{LOAD} = 3300pF		 25 15		 ns ns
TGxx Off to BGxx On Adaptive Delay Time[4]		DTCA = 0V DTCA = $INTV_{CC}$		50 30		ns ns

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = floating, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
BGxx Off to TGxx On Adaptive Delay Time[4]		DTCB = 0V DTCB = $INTV_{CC}$		50 30		ns ns
BGxx Off to TGxx On Smart Delay[5]		DTCA = 10k DTCA = 50k DTCA = 100k		13 50 100		ns ns ns
TGxx Off to BGxx On Smart Delay[5]		DTCB = 10k DTCB = 50k DTCB = 100k		13 50 100		ns ns ns
TG Minimum On-Time[6]	$t_{ON(MIN)}$			60		ns
Maximum Duty Cycle		Output in Dropout, FREQ = 0V	100			%
Charge Pump for BST-SW Supply						
Charge Pump Output Current		V_{BST-SW} = 7V, V_{SW} = 0V V_{SW} = 12V		 −50 −80		 µA µA
Charge Pump Output Voltage	V_{BST-SW}	I_{BST} = −1µA, V_{SW} = 0V and 12V	10	11	12	V
Low Dropout (LDO) Linear Regulators						
DRV_{CC} Voltage for V_{IN} and $EXTV_{CC}$ LDOs		$EXTV_{CC}$ = 0V for V_{IN} LDO, $EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO DRVSET = $INTV_{CC}$ DRVSET = 64.9kΩ DRVSET = 0V	 9.5 5.8 5.8	 9.77 6.5 6.0	 10.0 7.0 6.2	 V V V
DRV_{CC} Load Regulation		DRV_{CC} load current = 0mA to 100mA, T_A = 25°C		1	3	%
Undervoltage Lockout	UVLO	DRV_{CC} Rising DRVUV = $INTV_{CC}$ DRVUV = floating DRVUV = 0V	 7.1 5.2 3.8	 7.4 5.35 3.93	 7.6 5.5 4.0	 V V V
		DRV_{CC} Falling DRVUV = $INTV_{CC}$ DRVUV = floating DRVUV = 0V	 6.4 4.9 3.6	 6.64 5.05 3.71	 6.8 5.2 3.8	 V V V

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
$EXTV_{CC}$ LDO Switchover Voltage $EXTV_{CC}$ Rising		DRVUV = $INTV_{CC}$, T_A = 25°C DRVUV = floating, T_A = 25°C DRVUV = 0V, T_A = 25°C	7.5 5.9 4.6	7.7 6.1 4.8	8.0 6.4 5.0	V V V
$EXTV_{CC}$ Switchover Hysteresis $EXTV_{CC}$ Falling				250		mV
$INTV_{CC}$ Regulation Point				4.5		V
Spread Spectrum Oscillator and Phase-Locked Loop						
Fixed Frequency	f_{OSC}	PLLIN/SPREAD = 0V FREQ = 0V, T_A = 25°C FREQ = $INTV_{CC}$ FREQ = 374kΩ FREQ = 75kΩ, T_A = 25°C FREQ = 14.7kΩ	 320 2.0 450 	 370 2.25 100 500 2.5	 420 2.5 550 	 kHz MHz kHz kHz MHz
Synchronizable Frequency Range	f_{SYNC}	PLLIN/SPREAD = External Clock	0.1		2.5	MHz
PLLIN Input High Level			2.2			V
PLLIN Input Low Level					0.5	V
Spread Spectrum Frequency Range (Relative to f_{OSC})		PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency		 0 20		 % %
PGOOD Output						
PGOOD Voltage Low		I_{PGOOD} = 2mA, T_A = 25°C		0.2	0.4	V
PGOOD Leakage Current		PGOOD = 5V, T_A = 25°C	-1		+1	µA
PGOOD Trip Level V_{FB} with Respect to Set Regulated Voltage		T_A = 25°C V_{FB} Rising Hysteresis V_{FB} Falling Hysteresis	 7 -13 	 10 2.5 -10 2.5	 13 -7 	 % % % %

(Specifications are for T_J = -40°C to +150°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{IN} = 12V, RUN = 12V, VPRG = floating, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$, DRVUV = 0V, TGUP = TGDN = TGxx, BGUP = BGDN = BGxx, and DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PGOOD Delay for Reporting a Fault				25		µs

1 This specification is not tested in production.

2 The LTC7897 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

3 $SENSE^-$ bias current is reflected to the input supply by the formula $I_{VIN} = I_{SENSE-} \times V_{OUT}/(V_{IN} \times \eta)$, where η is the efficiency.

4 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

5 SW falling to BGxx rising and BGxx falling to SW rising delay times are measured at rising/falling thresholds on SW and BGxx of approximately 1.5V. See *Figure 36*.

6 The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current (I_{MAX}) (see the *Minimum On-Time Considerations* section).

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Input Supply (V_{IN})	–0.3V to 140V
RUN	–0.3V to 140V
BOOST	–0.3V to 150V
SW	–5V to 150V
BOOST to SW	–0.3V to 15V
TGUP, TGDN, BGUP, BGDN[1]	Not applicable
$EXTV_{CC}$	–0.3V to 30V
DRV_{CC}	–0.3V to 15V
$INTV_{CC}$	–0.3V to 6V
V_{FB}	–0.3V to 140V
PLLIN/SPREAD, FREQ, OVLO	–0.3V to 6V
TRACK/SS, ITH, ILIM	–0.3V to 6V
DRVSET, DRVUV, VPRG, PGOOD	–0.3V to 6V
DTCA, DTCB	–0.3V to 6V
$SENSE^+$, $SENSE^-$	–0.3V to 140V
$SENSE^+$ to $SENSE^-$ Continuous	–6V to 0.3V
$SENSE^+$ to $SENSE^-$ < 1ms	-100mA to 100mA
Operating Junction Temperature Range[2]	–40°C to 150°C
Storage Temperature Range	–65°C to 150°C

1 Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage can occur.

2 The LTC7897 is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} is the package thermal impedance and equals 43°C/W for the 28-lead (4mm × 5mm), side wettable, quad flat no lead (QFN) package

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

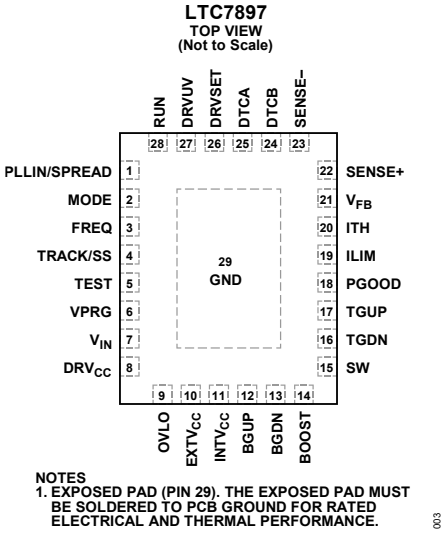


Figure 3. Pin Configuration

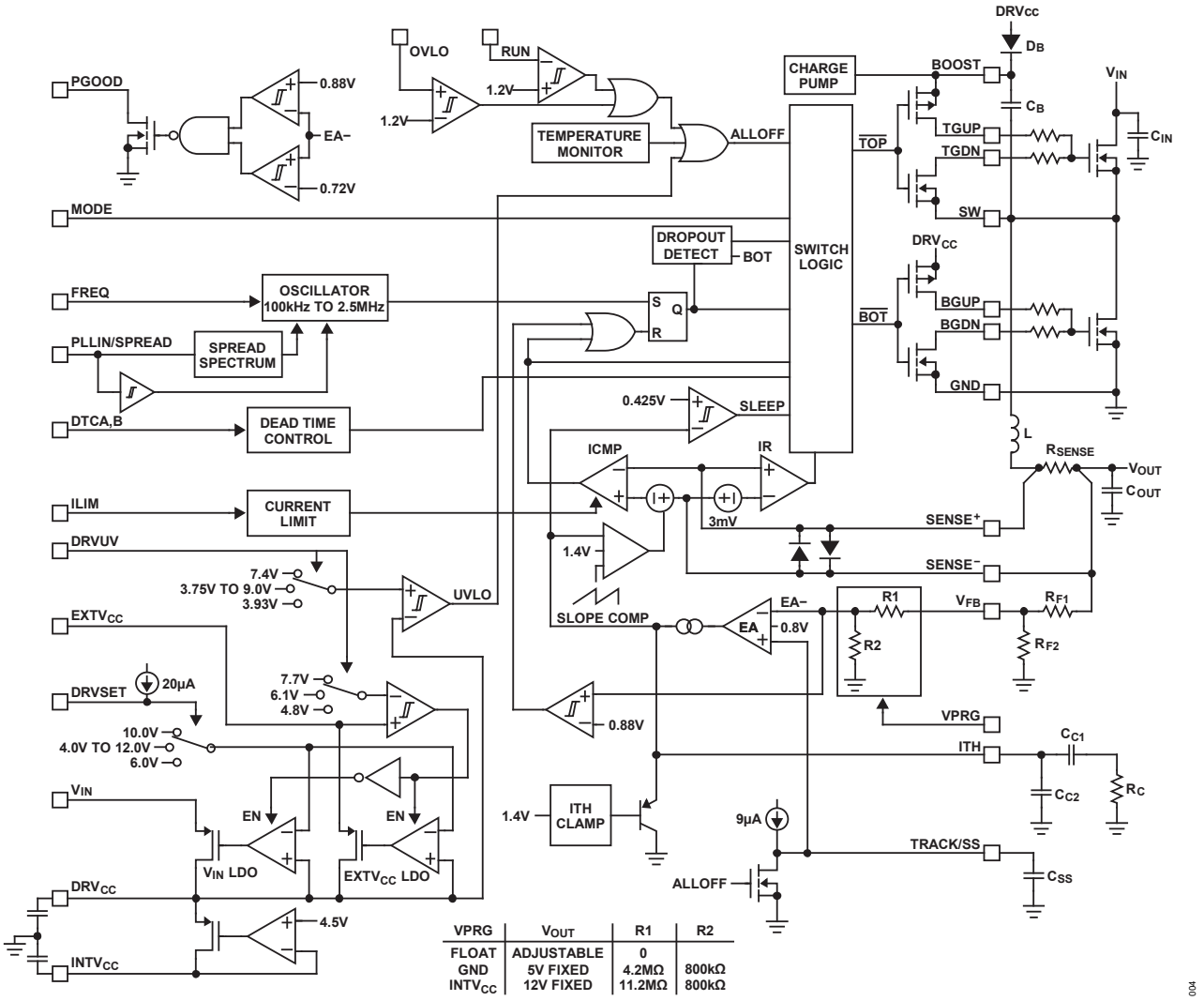
Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	PLLIN/ SPREAD	External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the phase-locked loop forces the rising TGxx signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering.
2	MODE	Mode Select Input. This input determines how the LTC7897 operates at light loads. Connect MODE to GND to select the Burst Mode operation. An internal 100kΩ resistor to GND also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor selects the pulse-skipping operation.
3	FREQ	Frequency Control Pin for the Internal Voltage Controlled Oscillator (VCO). Connect FREQ to GND for a fixed frequency of 370kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25MHz. Program frequencies between 100kHz and 2.5MHz by using a resistor between FREQ and GND. Minimize the capacitance on FREQ.
4	TRACK/SS	External Tracking/Soft-Start Input. TRACK/SS regulates the V_{FB} voltage to the lesser of 0.8V or the voltage on the TRACK/SS pin. An internal 9µA pull-up current source is connected to TRACK/SS. A capacitor to GND at TRACK/SS sets the ramp time to the final regulated output voltage. The ramp time is equal to 1 ms for every 11.25nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to TRACK/SS allows the output to track the other supply during start-up.
5	TEST	Test Pin. This pin must be soldered to PCB GND.
6	VPRG	Output Voltage Control Pin. VPRG sets the adjustable output mode using external feedback resistors or the fixed 12V or 5V output mode. Floating VPRG programs the output from 0.8V to 135V with an external resistor divider, regulating V_{FB} to 0.8V.

		Connect VPRG to $INTV_{CC}$ or GND to program the output to 12V or 5V, respectively, through an internal resistor divider on V_{FB}.
7	V_{IN}	Main Supply Pin. A bypass capacitor must be tied between V_{IN} and GND.
8	DRV_{CC}	Gate Driver Output of the internal LDO regulator from V_{IN} or $EXTV_{CC}$. The gate drivers and the $INTV_{CC}$ internal LDO are powered from DRV_{CC}. A low ESR 4.7µF ceramic bypass capacitor should be connected between DRV_{CC} and GND, as close as possible to the IC.
9	OVLO	Overvoltage Lockout Input. A voltage on this pin above 1.2V disables switching of the controller. The DRV_{CC} and $INTV_{CC}$ supplies maintain regulation during an OVLO event. Exceeding the OVLO threshold also triggers a soft-start reset. If the OVLO function is not used, connect this pin to GND.
10	$EXTV_{CC}$	External Power Input to an Internal LDO Regulator Connected to DRV_{CC}. This LDO regulator supplies $INTV_{CC}$ power, bypassing the internal V_{IN} LDO regulator whenever $EXTV_{CC}$ is higher than the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the *Power and Bias Supplies (VIN, EXTVCC, DRVCC, and INTVCC)* section. Do not exceed 30V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to GND if the $EXTV_{CC}$ LDO regulator is not used.
11	$INTV_{CC}$	Output of the Internal 4.5V Low Dropout Regulator from DRV_{CC}. The internal analog and digital circuits are powered from this pin. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the IC.
12	BGUP	High Current Gate Driver Pull-Up for Bottom MOSFET. BGUP pulls up to DRV_{CC}. Tie BGUP directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP and the bottom MOSFET gate to adjust the gate rising slew rate. BGUP also serves as the Kelvin sense of the bottom MOSFET gate during turn-off.
13	BGDN	High Current Gate Driver Pull-Down for Bottom MOSFET. BGDN pulls down to GND. Tie BGDN directly to the bottom MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN and the bottom MOSFET gate to adjust the gate falling slew rate. BGDN also serves as the Kelvin sense of the bottom MOSFET gate during turn-on.
14	BOOST	Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pins. Also connect a Schottky diode between the BOOST and DRV_{CC} pins. The voltage swing at the BOOST pin is from DRV_{CC} to (V_{IN} + DRV_{CC}).
15	SW	Switch Node Connection to Inductor.
16	TGDN	High Current Gate Driver Pull-Down for Top MOSFET. TGDN pulls down to SW. Tie TGDN directly to the top MOSFET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN and the top MOSFET gate to adjust the gate falling slew rate.
17	TGUP	High Current Gate Driver Pull-Up for Top MOSFET. TGUP pulls up to BOOST. Tie TGUP directly to the top MOSFET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP and the top MOSFET gate to adjust the gate rising slew rate.
18	PGOOD	Power Good Open-Drain Logic Output. PGOOD is pulled to GND when the voltage on V_{FB} is not within ±10% of its set point.

19	ILIM	Current Comparator Sense Voltage Range Input. Tying ILIM to GND or $INTV_{CC}$ or floating ILIM sets the maximum current sense threshold to one three different levels (25mV, 75mV, and 50mV, respectively).
20	ITH	Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.
21	V_{FB}	Error Amplifier Feedback Input. If VPRG is floating, the V_{FB} pin receives the remotely sensed feedback voltage from an external resistive divider across the output. If the VPRG pin is tied to the GND of $INTV_{CC}$, the V_{FB} pin receives the remotely sensed output voltage directly.
22	$SENSE^+$	The Positive Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with the current sense resistor (R_{SENSE}) set the current trip threshold.
23	$SENSE^-$	The Negative Input to the Differential Current Comparator. The $SENSE^-$ pin supplies current to the current comparator when $SENSE^-$ is greater than $INTV_{CC}$. When $SENSE^-$ is 3.2V or greater, the pin supplies the majority of the sleep mode quiescent current instead of V_{IN}, further reducing the input-referred quiescent current.
24	DTCB	Dead Time Control Pin for Top MOSFET Off to Bottom MOSFET On Delay. Connect DTCB to GND to program an adaptive delay of approximately 50ns. Connect DTCB to $INTV_{CC}$ to program an adaptive delay of approximately 30ns. Connect a 10kΩ to 100kΩ resistor between DTCB and GND to add a smart delay (from 13ns to 100ns) between SW falling and BGDN rising.
25	DTCA	Dead Time Control Pin for Bottom MOSFET Off to Top MOSFET On Delay. Connect DTCA to GND to program an adaptive delay of approximately 50ns. Connect DTCA to $INTV_{CC}$ to program an adaptive delay of approximately 30ns. Connect a 10kΩ to 100kΩ resistor between DTCA and GND to add a smart delay (from 13ns to 100ns) between BGUP falling and SW rising.
26	DRVSET	DRV_{CC} Regulation Program pin. This pin sets the regulation point for the DRV_{CC} low dropout (LDO) linear regulator. Connect to GND to set DRV_{CC} to 6.0V. Connect to $INTV_{CC}$ to set DRV_{CC} to 10.0V. Program voltages between 5V and 10V by placing a resistor (50k to 100k) between DRVSET and GND. The resistor and an internal 20µA source current create a voltage used by the DRV_{CC} LDO regulator to set the regulation point.
27	DRVUV	DRV_{CC} UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the DRV_{CC} UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in *Table 1*.
28	RUN	Run Control Input for the Controller. Forcing the RUN pin below 1.1V disables control, while forcing the RUN pin below 0.7V shuts down the entire LTC7897, reducing quiescent current to approximately 1µA. Tie the RUN pin to V_{IN} for always-on operation.
29	GND (EPAD)	Ground (Exposed Pad). The exposed pad must be soldered to PCB GND for rated electrical and thermal performance.

BLOCK DIAGRAM



VPRG	VOUT	R1	R2
FLOAT	ADJUSTABLE	0	
GND	5V FIXED	4.2MΩ	800kΩ
INTVCC	12V FIXED	11.2MΩ	800kΩ

Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

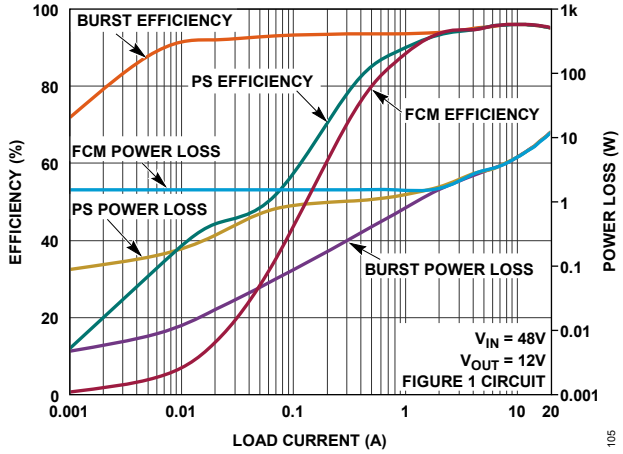


Figure 5. Efficiency and Power Loss vs. Load Current

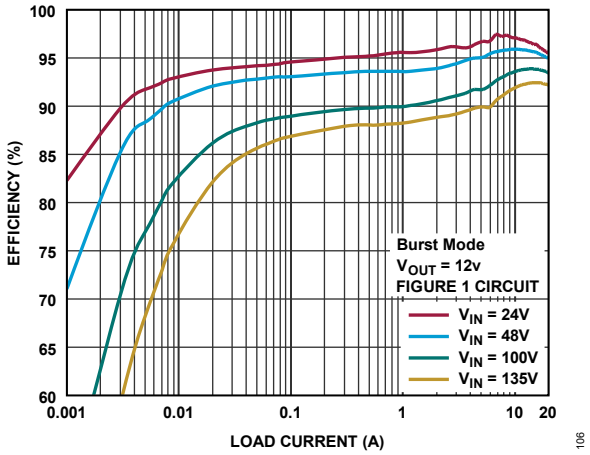


Figure 6. Efficiency vs. Load Current

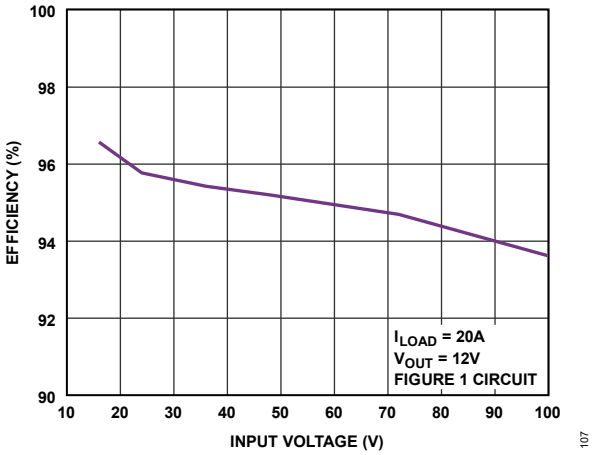


Figure 7. Efficiency vs. Input Voltage

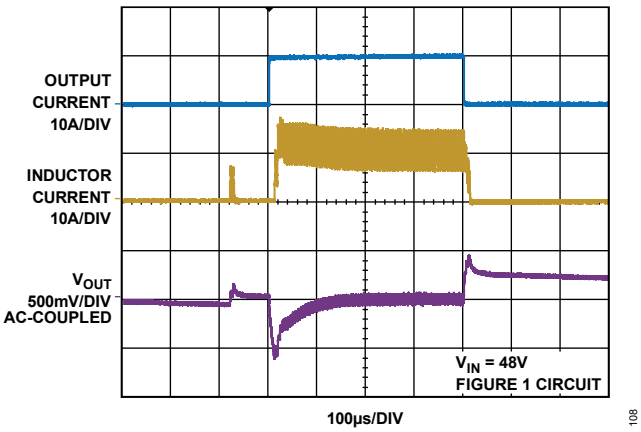


Figure 8. Load Step Burst Mode Operation

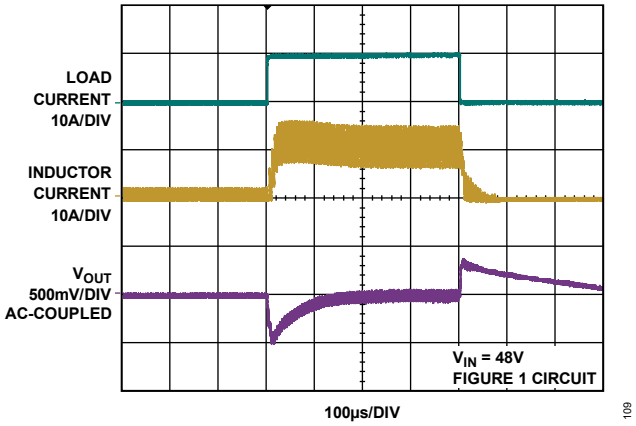


Figure 9. Load Step Pulse-Skipping Mode

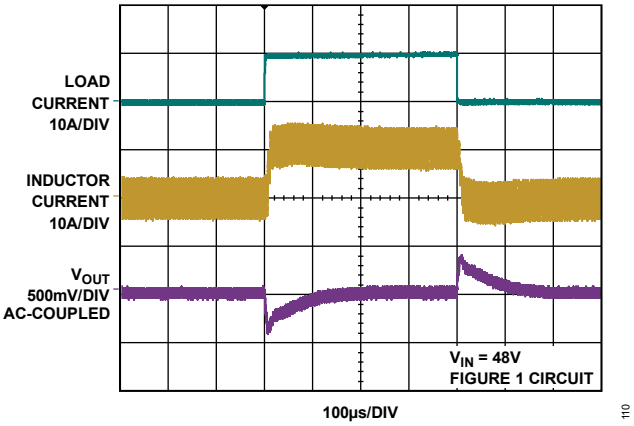


Figure 10. Load Step Forced Continuous Mode

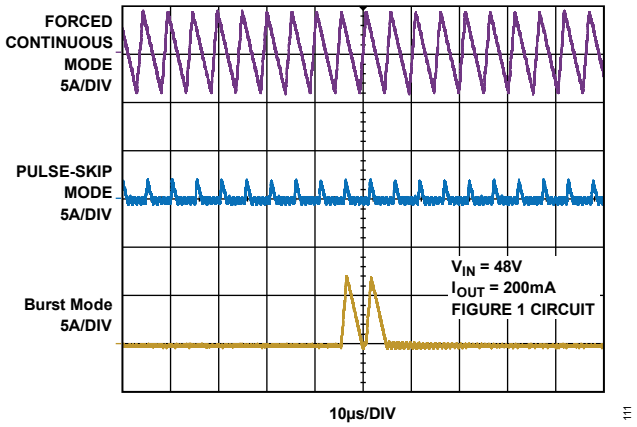


Figure 11. Inductor Current at Light Load

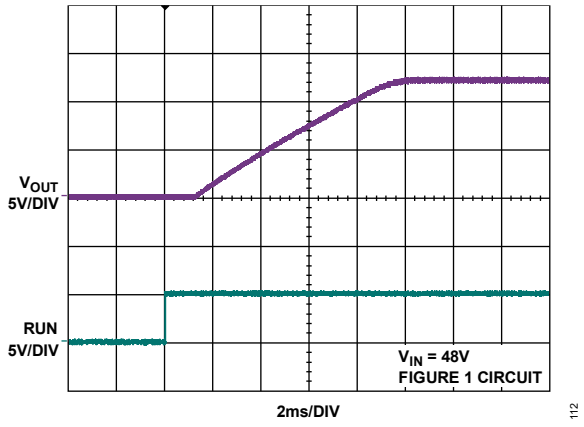


Figure 12. Soft Start-Up

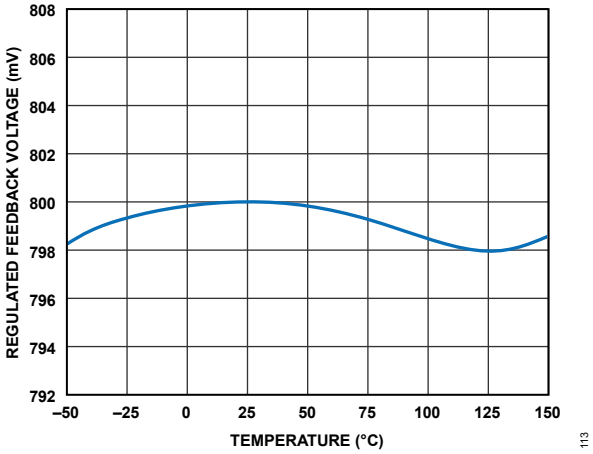


Figure 13. Regulated Feedback Voltage vs. Temperature

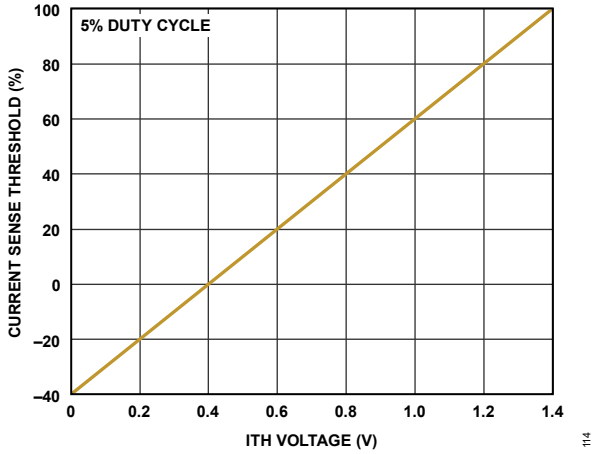


Figure 14. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Forced Continuous Mode

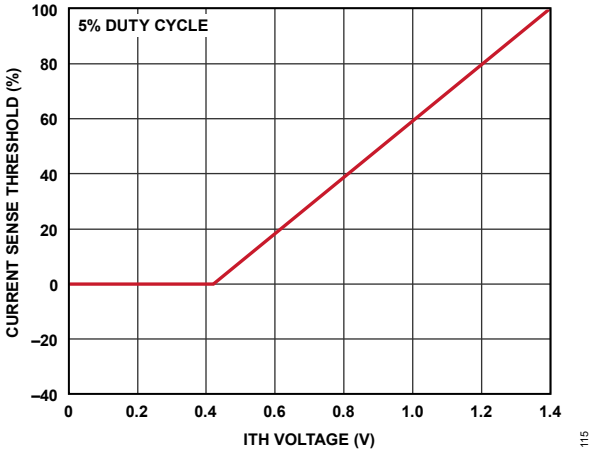


Figure 15. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Pulse-Skipping Mode

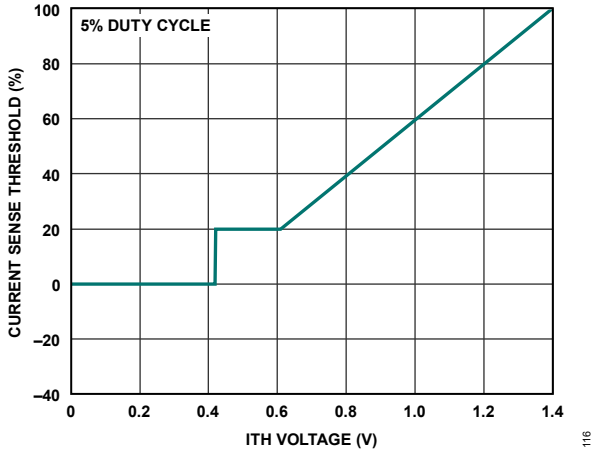


Figure 16. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Burst Mode

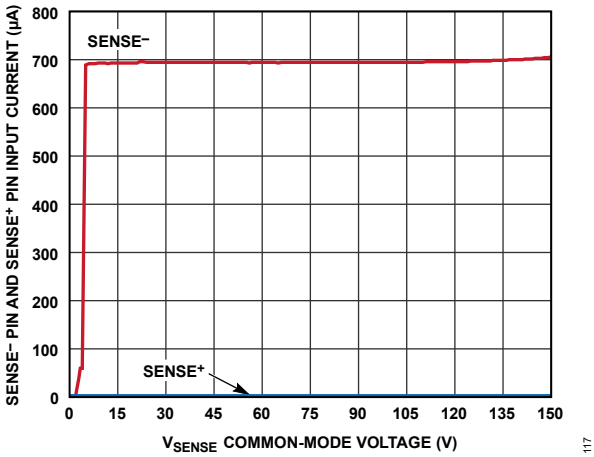


Figure 17. SENSEx Input Current vs. V_{SENSE} Voltage

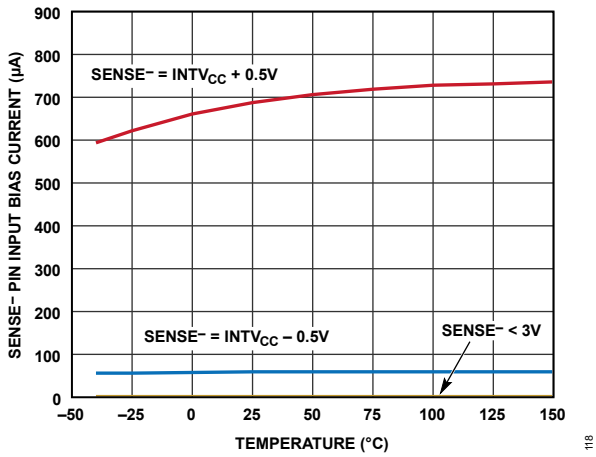


Figure 18. $SENSE^-$ Input Current vs. Temperature

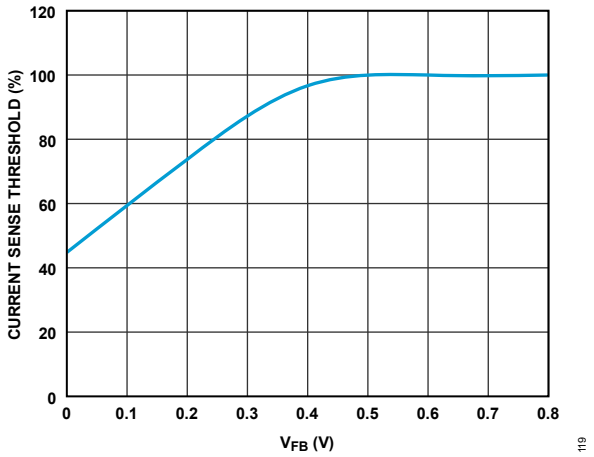


Figure 19. Foldback Current Limit

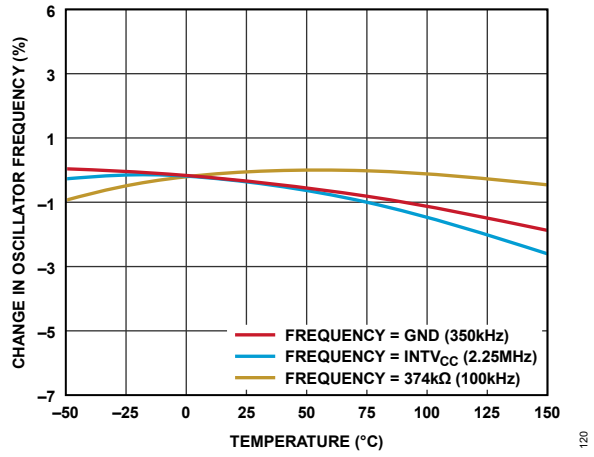


Figure 20. Oscillator Frequency vs. Temperature

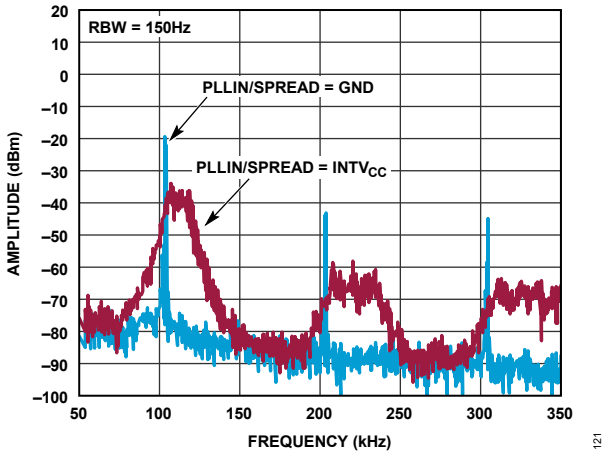


Figure 21. Output Voltage Noise Spectrum

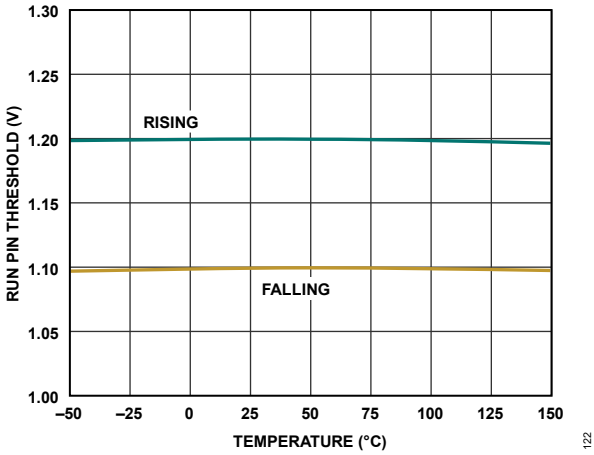


Figure 22. RUN Pin Thresholds vs. Temperature

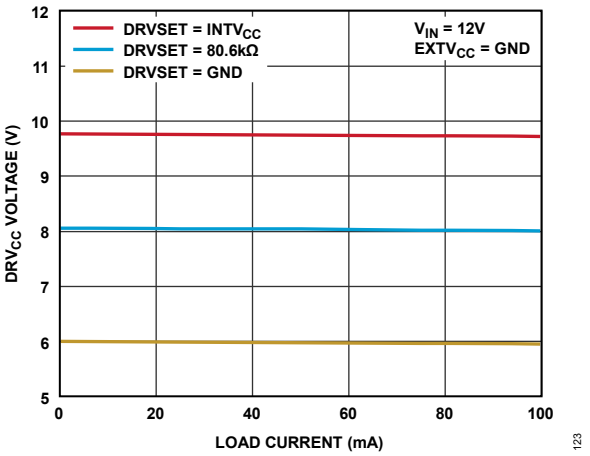


Figure 23. DRV_{CC} Load Regulation

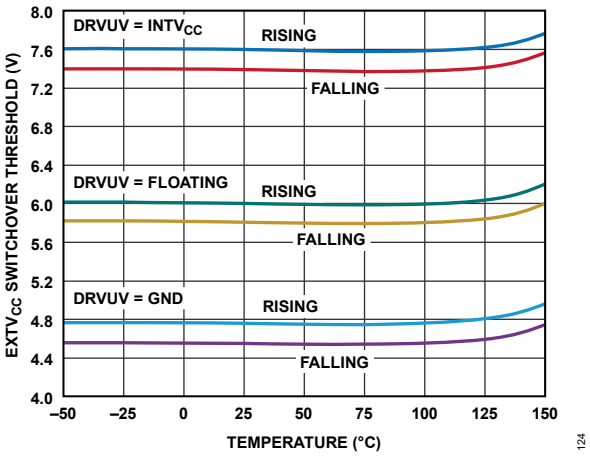


Figure 24. $EXTV_{CC}$ Switchover Voltage vs. Temperature

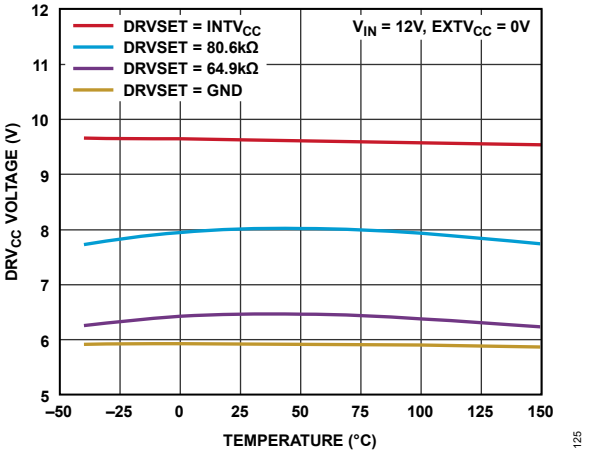


Figure 25. DRV_{CC} Voltage vs. Temperature

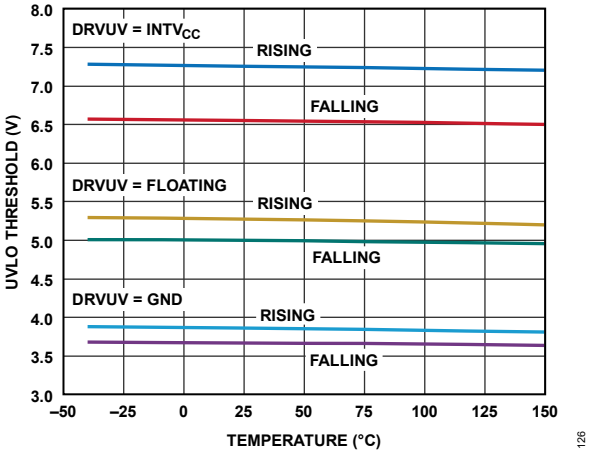


Figure 26. DRV_{CC} Undervoltage Lockout Thresholds vs. Temperature

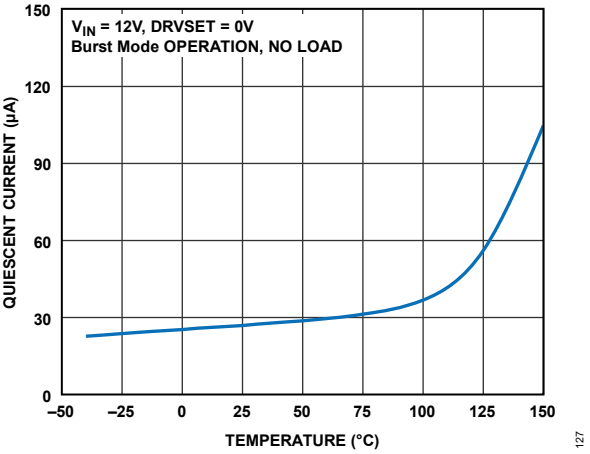


Figure 27. Quiescent Current vs. Temperature

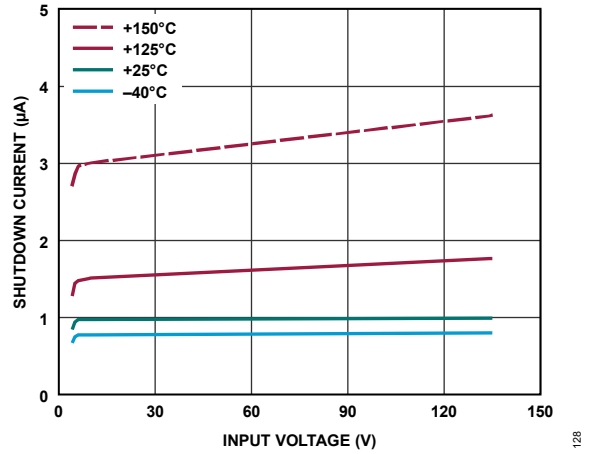


Figure 28. Shutdown Current vs. V_{IN} Voltage

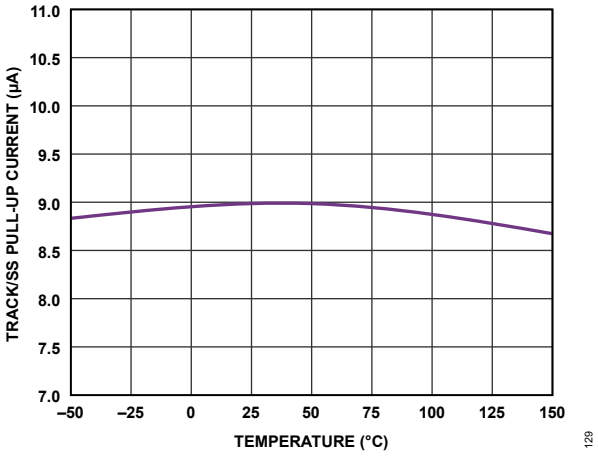


Figure 29. TRACK/SS Pull-Up Current vs. Temperature

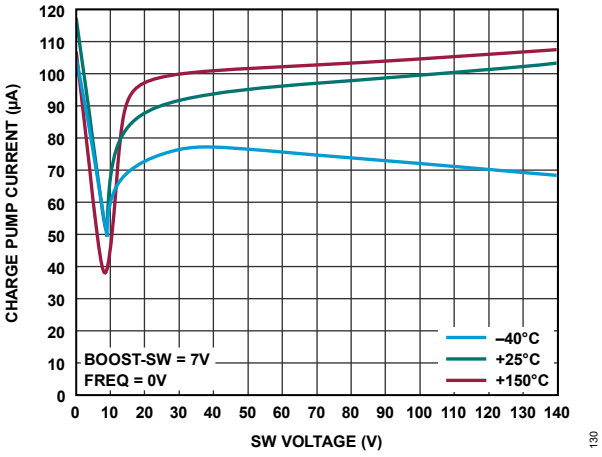


Figure 30. Charge Pump Output Voltage vs. SW Voltage

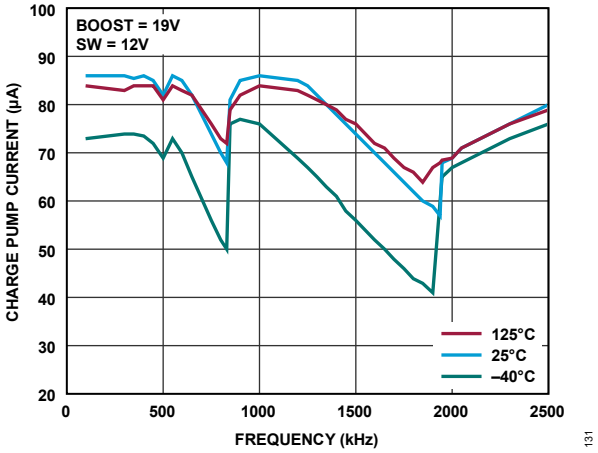


Figure 31. Charge Pump Output Current vs. Frequency

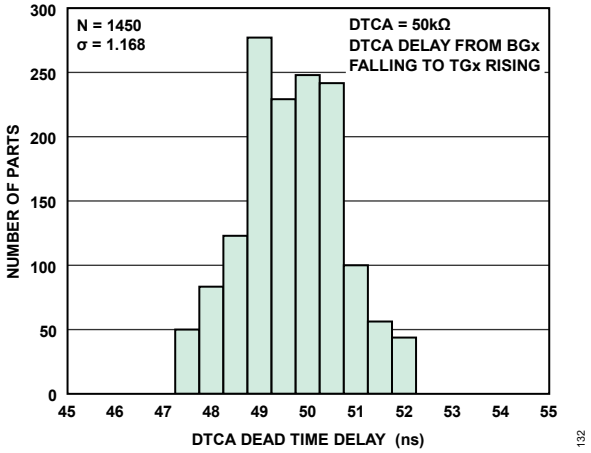


Figure 32. DTCA = 50kΩ Dead Time Delay Histogram

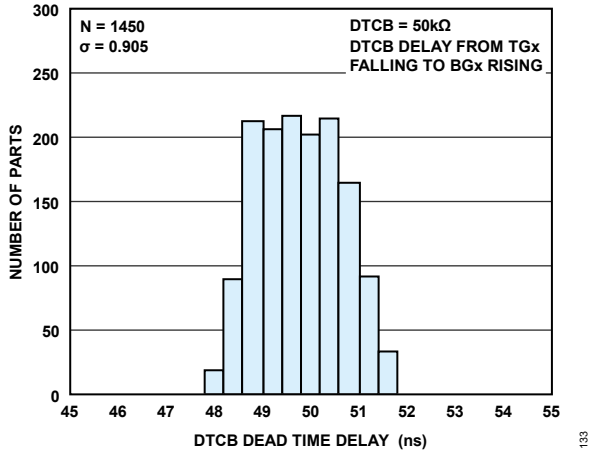


Figure 33. DTCB = 50kΩ Dead Time Delay Histogram

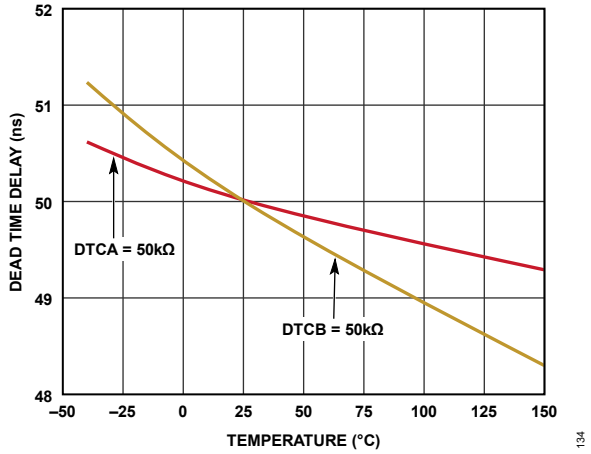


Figure 34. Dead Time Delay vs. Temperature

THEORY OF OPERATION

Main Control Loop

The LTC7897 is a synchronous controller using a constant frequency, peak current mode architecture. During normal operation, the external top MOSFET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the SR latch. After the top MOSFET is turned off each cycle, the bottom MOSFET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier (EA). The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to GND) to the internal 0.8V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

Power and Bias Supplies (V_{IN}, $EXTV_{CC}$, DRV_{CC}, and $INTV_{CC}$)

The DRV_{CC} pin supplies power for the top and bottom MOSFET drivers. LDO linear regulators are available from both the V_{IN} pin and $EXTV_{CC}$ pin to provide power to DRV_{CC}, which can be programmed from 5V to 10V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage, the V_{IN} LDO regulator supplies power to DRV_{CC}. If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator turns on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source, such as the LTC7897 switching regulator output.

The $INTV_{CC}$ pin supplies power for most of the internal circuits in the LTC7897. The $INTV_{CC}$ supply is derived from an LDO linear regulator from DRV_{CC} and is regulated to 4.5V.

High-Side Bootstrap Capacitor

The top MOSFET driver is biased from the floating bootstrap capacitor (C_B), which normally recharges during each cycle through an external diode between BOOST and DRV_{CC} whenever the bottom MOSFET turns on. The LTC7897 also has an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can nominally supply a charging current of 80µA.

If the input voltage (V_{IN}) decreases to a voltage close to its output (V_{OUT}), the loop may enter dropout and attempt to turn on the top MOSFET continuously. In forced continuous mode or pulse-skipping mode, the internal charge pump enables the top MOSFET to be turned on continuously, resulting in a 100% duty cycle.

Dead Time Control (DTCA and DTCB Pins)

The LTC7897 dead time delays can be programmed from 13ns to 100ns by configuring the DTCA and DTCB pins. The DTCA pin programs the dead time associated with the bottom MOSFET turning off and the top MOSFET turning on. The DTCB pin programs the dead time associated with the top MOSFET turning off and the bottom MOSFET turning on. In this section, TG represents the voltage sensed at the top MOSFET gate, and BG represents the voltage sensed at the bottom MOSFET gate.

Tying the DTCA pin to GND or $INTV_{CC}$ programs adaptive dead time control, which means the driver logic waits for the bottom MOSFET to turn off before turning on the top MOSFET. Adaptive dead time control results in dead times between BG falling to TG rising of approximately 50ns with DTCA tied to ground and 30ns with DTCA tied to $INTV_{CC}$.

Tying the DTCB pin to GND or $INTV_{CC}$ programs adaptive dead time control, which means the driver logic waits for the top MOSFET to turn off before turning on the bottom MOSFET. Adaptive dead time control results in dead times between TG falling to BG rising of approximately 50ns with DTCB tied to ground and 30ns with DTCB tied to $INTV_{CC}$.

Placing a resistor between the DTCA pin and GND adds a smart delay between SW rising and BG falling from 13ns to 100ns. See the *Applications Information* section on dead time control for more information.

Placing a resistor between the DTCB pin and GND adds a smart delay between SW falling and BG rising from 13ns to 100ns. See the *Applications Information* section on dead time control for more information.

Start-Up and Shutdown (RUN, OVLO, and TRACK/SS Pins)

The LTC7897 can be shut down using the RUN pin. Pulling the RUN pin below 1.08V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDO regulators. In this shutdown state, the LTC7897 draws only 1µA of quiescent current.

The RUN pin needs to be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 140V (absolute maximum). Therefore, the pin can be tied to V_{IN} in always-on applications where the controller is enabled continuously and never shuts down. Additionally, a resistor divider from V_{IN} to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user-adjustable level.

The OVLO pin inhibits switching when the input voltage rises above a programmable operating range. By using a resistor divider from the input supply to ground, the OVLO pin serves as a precise input supply voltage monitor. Switching is disabled when the OVLO pin rises above 1.2V, which can be configured to limit switching to a specific range of input supply voltage. When switching is disabled, the LTC7897 can safely sustain input voltages up to the absolute maximum rating of 140V. Input supply overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference voltage, the LTC7897 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference voltage. This method allows the TRACK/SS pin to be used as a soft-start, which smoothly ramps the output voltage on start-up, limiting the input supply inrush current. An external capacitor from the TRACK/SS pin to GND is charged by an internal 9µA pull-up current, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), V_{OUT} rises smoothly from zero to its final value.

Alternatively, the TRACK/SS pin can be used to make the start-up of V_{OUT} track that of another supply. Typically, this requires connecting to the TRACK/SS pin through an external resistor divider from the other supply to GND (see the *RUN Pin and Overvoltage/Undervoltage Lockout* section and *Soft-Start and Tracking (TRACK/SS Pin)* section).

Light Load Operation: Burst Mode Operation, Pulse-Skipping Mode, or Forced Continuous Mode (MODE Pin)

The LTC7897 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at light load currents.

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100kΩ resistor to GND invokes Burst Mode operation when the MODE pin is floating and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100kΩ resistor.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITH pin may indicate a lower value. If the average inductor current is higher than the load current, the EA decreases the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode), and both external MOSFETs turn off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current drawn by the LTC7897 to 15µA. When V_{OUT} is 3.2V or higher, the majority of this quiescent current is supplied by the $SENSE^-$ pin, which further reduces the input-referred quiescent current by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the output of the EA rises. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The IR turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7897 operates in pulse-width modulation (PWM) pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At light loads, ICMP can remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference, as compared to Burst Mode operation. Pulse-skipping mode provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7897 switches from Burst Mode operation to forced continuous mode.

Frequency Selection, Spread Spectrum, and PhaseLocked Loop (FREQ and PLLIN/SPREAD Pins)

The free running switching frequency of the LTC7897 controller is selected using the FREQ pin. Tying FREQ to GND selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 2.5MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7897 can operate in spread-spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of the frequency set by the FREQ pin and +20%.

A phase-locked loop (PLL) is available on the LTC7897 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The PLL of the LTC7897 aligns the turn-on of the external top MOSFET to the rising edge of the synchronizing signal.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to synchronize the rising edge of the external clock to the rising edge of TGxx. For more rapid lock in to the external clock, use the FREQ pin to

set the internal oscillator to approximately the frequency of the external clock. The PLL of the LTC7897 is guaranteed to lock to an external clock source whose frequency is between 100kHz and 2.5MHz.

The PLLIN/SPREAD pin is transistor-transistor logic (TTL)-compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

Input Supply Overvoltage Lockout (OVLO Pin)

The OVLO pin provides a protection feature that inhibits switching when the input voltage rises above a programmable level. To accurately sense the input voltage, tie the OVLO pin to a resistor divider between V_{IN} and GND. Switching is disabled when the OVLO pin rises above 1.2V.

The OVLO pin is high impedance and must be pulled down for always-on operation or driven by a resistor divider from V_{IN} to GND. Do not float the OVLO pin.

When the OVLO pin disables switching, the LTC7897 can safely sustain input voltages up the absolute maximum rating of 140V.

Output Overvoltage Protection

In addition to the OVLO pin, which provides a user-adjustable protection against V_{IN} overvoltage, the LTC7897 has an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that can cause output overvoltage. When the V_{FB} pin rises more than 10% above its regulation point of 0.8V, the top MOSFET turns off and the inductor current is not allowed to reverse.

Foldback Current

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the V_{FB} voltage is keeping up with the TRACK/SS voltage).

Power Good

The LTC7897 has a PGOOD pin that is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} voltage is not within ±10% of the 0.8V reference. The PGOOD pin is also pulled low when the RUN pin is low (shutdown) or the OVLO pin voltage is above 1.2V. When the V_{FB} voltage is within the ±10% requirement, the MOSFET turns off, and the pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

Figure 1 is a basic LTC7897 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors and power FETs, can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this trade-off, the effect of the inductor value on the ripple current and low current operation must also be considered. The inductor value has a direct effect on the ripple current.

The maximum average inductor current ($I_{L(MAX)}$) is equal to the maximum output current. The peak current is equal to the average inductor current plus half of the inductor ripple current (ΔI_L), which decreases with higher inductance (L) or higher frequency (f) and increases with higher V_{IN}, as shown in Equation 1, as follows:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \times I_{L(MAX)}$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) cause this transition to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values cause the burst frequency to decrease.

Inductor Core Selection

When the value for L is known, select the type of inductor. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. The actual core loss is independent of the core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Current Sense Selection

The LTC7897 can be configured to use either inductor DC resistance (DCR) sensing or low value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components is driven by the load requirement and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value.

The SENSE+ and SENSE– pins are the inputs to the current comparator. The common mode voltage range on these pins is 0 V to 140V (the absolute maximum), enabling the LTC7897 to regulate output voltages up to a maximum of 135V. The SENSE+ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing. The impedance of the SENSE– pin changes depending on the commonmode voltage. When less than $INTV_{CC}$ – 0.5V, the SENSE– pin is relatively high impedance, drawing ≈1µA. When the SENSE– pin is above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. The SENSE– pin has an additional ≈70µA current when its voltage is above 3.2V to bias internal circuitry from V_{OUT} instead of V_{IN}, which reduces the input referred supply current.

Filter components mutual to the sense lines must be placed close to the LTC7897, and the sense lines must run close together to a Kelvin connection underneath the current sense element (shown in *Figure 35*). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (*Figure 37*), the R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

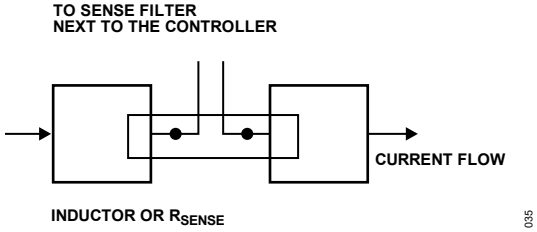


Figure 35. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

Figure 36 shows a typical sensing circuit using a discrete resistor. R_{SENSE} is chosen based on the required output current. The current comparator of the controller has a $V_{SENSE(MAX)}$ of 50mV, 25mV, or 75mV, as determined by the state of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the *Table 1*.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (3µH) or higher current (5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (R_F) into the sense pins, as shown in *Figure 36*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$ (C_F is the filter capacitor). In general, select C_F to be in the range of 1nF to 10nF and calculate the corresponding R_F. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint, and 0.2nH for a resistor with a 1225 footprint.

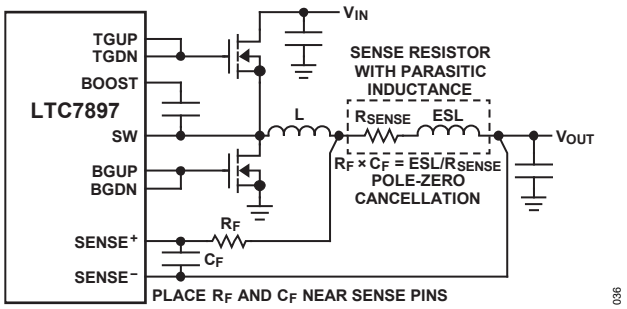


Figure 36. Current Sensing Methods-Using a Resistor to Sense Current

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7897 is capable of sensing the voltage drop across the inductor DCR, as shown in *Figure 37.* The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 +R 2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Consult the data sheet of the manufacturer for detailed information.

Using $I_{L(MAX)}$ and ΔI_L (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1*.

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR (DCR_{MAX}) to the desired sense resistor (R_D) value, use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1µF to 0.47µF. This range forces the equivalent resistance (R1||R2) to around 2kΩ, reducing the error that can result from the ≈1µA current of the SENSE+ pin.

R1||R2 is scaled to the room temperature inductance and the maximum DCR given by Equation 5, as follows:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \cdot C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follows:

$$R1 = \frac{R1||R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \cdot R_D}{1 - R_D} \quad (7)$$

The maximum power loss (P_{LOSS}) in R1 is related to the duty cycle and occurs in continuous mode at the maximum input voltage ($V_{IN(MAX)}$) given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \cdot V_{OUT}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than P_{LOSS} in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

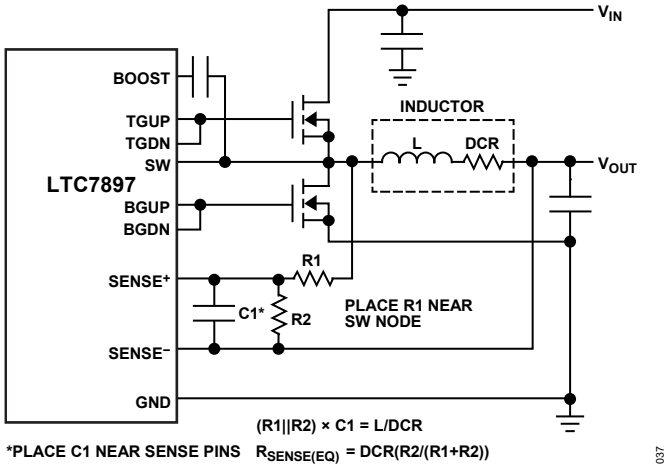


Figure 37. Current Sensing Methods-Using the Inductor DCR to Sense Current

Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses, and can operate at switching frequencies up to 2.5MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in *Table 4*.

Table 4. Setting the Switching Frequency Using FREQ and PLLIN/SPREAD

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	350kHz
$INTV_{CC}$	0V	2.25MHz
Resistor to GND	0V	100kHz to 2.5MHz
Any of the Above	External Clock 100kHz to 2.5MHz	Phase-Locked to External lock
Any of the Above	$INTV_{CC}$	Spread Spectrum f_{OSC} Modulated 0% to +20%

Tying the FREQ pin to GND selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed anywhere between 100kHz and 2.5MHz. Choose a FREQ pin resistor (R_{FREQ}) from *Figure 38* or equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{osc}} \quad (9)$$

To improve EMI performance, spread spectrum mode can be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum mode is enabled, the switching frequency modulates within the frequency selected by the FREQ pin and +20%. Spread spectrum mode can be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping mode, or forced continuous mode).

A PLL is also available on the LTC7897 to synchronize the internal oscillator to an external clock source connected to the PLLIN/ SPREAD pin. After the PLL locks, TGxx is synchronized to the rising edge of the external clock signal. See the *Phase-Locked Loop and Frequency Synchronization* section for details.

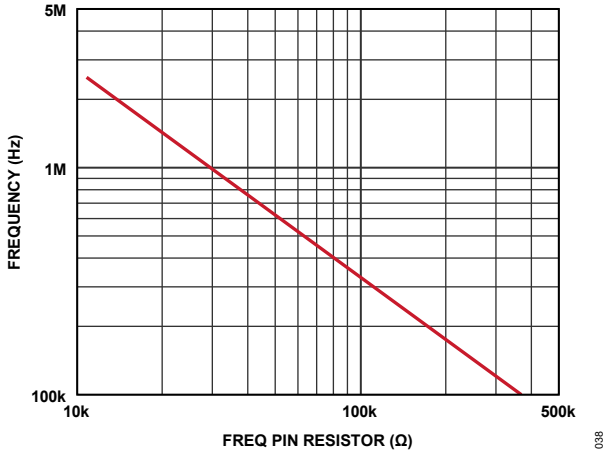


Figure 38. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Selecting the Light-Load Operating Mode

The LTC7897 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100 kΩ resistor. An internal 100kΩ resistor from the MODE pin to GND selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7897 operates in pulse-skipping mode if it is selected. Otherwise, the LTC7897 operates in forced continuous mode. *Table 5* summarizes the use of the MODE pin to select the light load operating mode.

Table 5. Using the MODE Pin to Select Light Load Operating Mode

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V or Floating	Burst Mode	Forced Continuous
100kΩ to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

The requirements of each application dictate the appropriate choice for light load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the

regulator operates in discontinuous operation. In addition, when the load current is light, the inductor current begins bursting at frequencies lower than the switching frequency and enters a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light loads.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of the load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force the top MOSFET to remain off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference compared to Burst Mode operation. Pulse-skipping mode provides higher light load efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple, and EMI.

In some applications, it may be desirable to change the light load operating mode based on the conditions present in the system. For example, if a system is inactive, the user can select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, the user can send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These on-the-fly mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Dead Time Control (DTCA and DTCB Pins)

The dead time delays of the LTC7897 can be adjusted from 13ns to 100ns by configuring the DTCA pin and DTCB pin. See *Figure 39* shows the TG minus SW, BG, and SW waveforms for each DTCx pin setting. In the DTCx Pins tied to GND (Adaptive Dead Time Control), DTCx Pins tied to $INTV_{CC}$, and DTCx Pins connected with a resistor to GND sections, TG represents the voltage sensed at the top MOSFET gate (the threshold for TG falling is sensed at the TGUP pin), and BG represents the voltage sensed at the bottom MOSFET gate (the thresholds for BG rising and falling are sensed at the BGDN and BGUP pins, respectively). The SW waveforms represent operation in continuous conduction mode with positive inductor current. The DTCA pin programs the dead time associated with the bottom MOSFET turning off and the top MOSFET turning on (SW transitioning from low to high). The DTCB pin programs the dead time associated with the top MOSFET turning off and the bottom MOSFET turning on (SW transitioning from high to low).

DTC_X Pins Tied to $INTV_{CC}$ or Ground (Adaptive Dead Time Control)

Tying the DTCA pin and DTCB pin to GND or $INTV_{CC}$ GND programs adaptive dead time control. In adaptive control (see *Figure 39*), the dead time is measured between one MOSFET turning off and the other MOSFET turning on. Tying the DTCA pin to GND fixes the delay between BG going low and TG minus SW going high to approximately 50ns. Tying the DTCA pin to $INTV_{CC}$ fixes the delay between BG going low and TG minus SW going high to approximately 30ns. Tying the DTCB pin to GND fixes the delay between TG minus SW falling and BG rising to approximately 50ns. Tying the DTCB pin to GND fixes the delay between TG minus SW falling and BG rising to approximately 30ns.

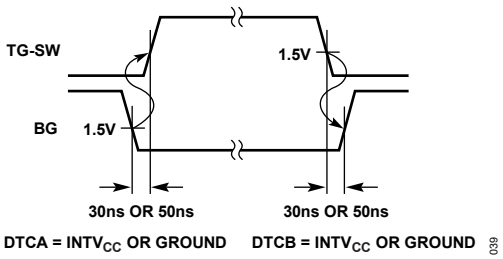


Figure 39. DTCX Pin Tied to INTVCC or GND–Adaptive Dead Time Control

DTCX Pin Connected with a Resistor to GND

Connecting a resistor between the DTCX pins and GND programs an adjustable smart delay from 13ns to 100ns between the SW and BG edges (see *Figure 40*). A resistor tied to the DTCA pin programs a smart delay between BG falling and SW rising.

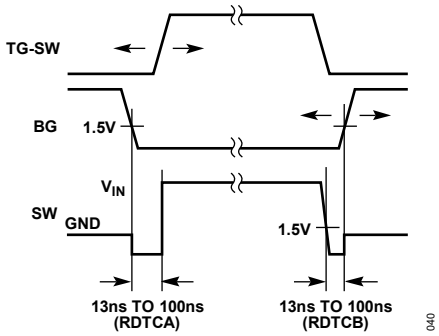


Figure 40. DTCX Pin with Resistor to GND–Adjustable Dead Time Control

A resistor tied to the DTCB pin to GND programs a smart delay between SW falling and BG rising. *Figure 41* shows the relationship between the DTCX pin resistor value and the programmed delay between BG and SW edges. This resistor must not be less than 10kΩ.

With a resistor on the DTCX pins, the maximum delay between one MOSFET turning off and the other MOSFET turning on is set to approximately 60ns beyond the programmed delay time. For the DTCA transition (SW from low to high), this timeout can be reached if the bottom MOSFET turns off with negative inductor current (for example, light load currents in forced continuous mode), such that SW slews high immediately after the bottom MOSFET turns off.

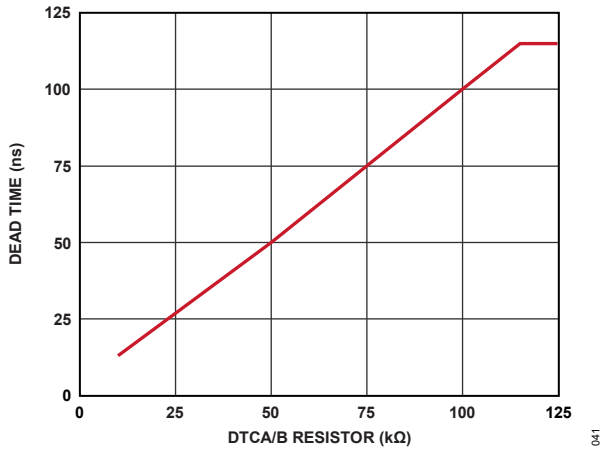


Figure 41. Relationship between Dead Time Delay and Resistor Value at DTC$_X$ Pins

Setting wide dead times can be useful in applications where the MOSFETs are not well defined, and an extra safety margin is required to prevent shoot-through.

Setting aggressive dead times can increase efficiency in applications where the MOSFETs are well defined. The MOSFET data sheet specification for turn-on ($T_{D(ON)}$) and turn-off ($T_{D(OFF)}$) delays can be used as a starting point for setting aggressive dead times. Using *Figure 41* to choose resistor values for the DTC_X pins, an example starting point for aggressive dead times is given by Equation 10 and Equation 11, as follows:

$$R_{DTCA} = (\text{BG MOSFET } T_{D(OFF)} - \text{TG MOSFET } T_{D(ON)}) \quad (10)$$

$$R_{DTCB} = 10k\Omega \quad (11)$$

The resistors on the DTC_X pins can then be easily modified to adjust dead times to maximize efficiency while preventing shoot-through.

Power MOSFET Selection

Two external power FETs must be selected for the LTC7897: one N-channel MOSFET for the top (main) switch and one N-channel MOSFET for the bottom (synchronous) switch. The peak-to-peak drive levels are set by the DRV_{CC} regulation point (5V to 10V). Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the breakdown voltage (BVD_{SS}) specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on resistance ($R_{DS(ON)}$), Miller capacitance (C_{MILLER}), input voltage, and maximum output current. C_{MILLER} can be approximated from the gate charge curve typically provided in the data sheet of the MOSFET manufacturer. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat, divided by the specified change in the voltage difference between the drain and source terminals of the MOSFET (V_{DS}). This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 12 and Equation 13, as follows:

$$\text{MAIN SWITCH DUTY CYCLE} = \frac{V_{OUT}}{V_{IN}} \quad (12)$$

$$\text{SYNCHRONOUS SWITCH DUTY CYCLE} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (13)$$

The MOSFET power dissipations at maximum output current are given by Equation 14 and Equation 15, as follows:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)\,R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\cdot\left[\frac{1}{V_{DRVCC}-V_{THMIN}}+\frac{1}{V_{THMIN}}\right](f) \quad (14)$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} \quad (15)$$

Where:

P_{MAIN} is the power dissipation from the main switch.

V_{DRVCC} is the DRV_{CC} voltage. P_{SYNC} is the power dissipation from the synchronous switch.

δ is the temperature dependency of $R_{DS(ON)}$ (δ ≈ 0.005/°C).

R_{DR} is the effective driver resistance at the Miller threshold voltage of the MOSFET (R_{DR} ≈ 2Ω).

V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses (I^2R is the power loss equation of the MOSFETs), whereas the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20 V, the high current efficiency generally improves with larger FETs. However, for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

C_{IN} and C_{OUT} Selection

The selection of the input capacitance (C_{IN}) is usually based on the worst-case RMS current drawn through the input network (battery, fuse, or capacitor). The highest V_{OUT} × I_{OUT} product needs to be used in Equation 16 to determine the maximum RMS capacitor current requirement.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, use a low effective series resistance (ESR) capacitor sized for the maximum RMS current (I_{RMS}). At I_{MAX}, the maximum RMS capacitor current is given by Equation 16, as follows:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}[(V_{OUT})(V_{IN}-V_{OUT})]^{\frac{1}{2}} \quad (16)$$

Equation 16 has a maximum at V_{IN} = 2V_{OUT}, where I_{RMS} = I_{OUT}/2 (I_{OUT} is the output current). This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings of capacitor manufacturers are often based on only 2000 hours of life. This basis makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors can be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7897, ceramic capacitors can also be used for C_{IN}. Consult the manufacturer if there is any question.

Placing a small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and GND close to the LTC7897 is also suggested. An optional 1Ω to 10Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation from a noisy input supply.

The selection of the output capacitance (C_{OUT}) is driven by the ESR. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated to Equation 17, as follows:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8\cdot f\cdot C_{OUT}}\right) \quad (17)$$

Where:

f is the operating frequency.

ΔI_L is the ripple current in the inductor.

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting the Output Voltage

The LTC7897 output voltages are set by an external feedback resistor divider carefully placed across the output, as shown in *Figure 42* and *Figure 43*. The regulated output voltage is determined by Equation 18, as follows:

$$V_{OUT} = 0.8V\left(1 + \frac{R_B}{R_A}\right) \quad (18)$$

Place the R_A and R_B resistors close to the V_{FB} pin to minimize PCB trace length and noise on the sensitive V_{FB} node. Take care to route the V_{FB} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) can be used.

The LTC7897 can be programmed to a fixed 12V or 5V output through control of the VPRG pin. *Figure 43* shows how the V_{FB} pin is issued to sense the output voltage in fixed output mode. Tying VPRG to $INTV_{CC}$ or GND programs V_{OUT} to 12V or 5V, respectively. Floating VPRG sets V_{OUT} to adjustable output mode using external resistors.

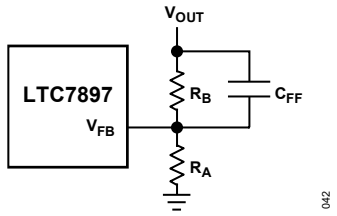


Figure 42. Setting Buck Output Voltage-Setting Adjustable Output Voltage

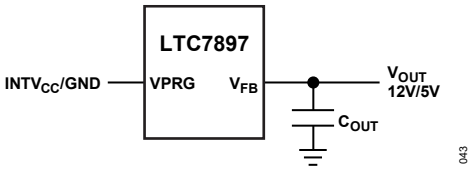


Figure 43. Setting Buck Output Voltage-Setting LTC7897 to Fixed Voltage

RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7897 is enabled using the RUN pin. The RUN pin has a rising threshold of 1.2V with 120mV of hysteresis. Pulling the RUN pin below 1.08V shuts down the main control loop and resets the soft-start. Pulling the RUN pin below 0.7V disables the controller and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDO regulators. In this state, the LTC7897 draws only ≈1µA of quiescent current.

The RUN pin is high impedance, must be externally pulled up or pulled down, and is driven directly by logic. The RUN pin can tolerate up to 140V (the absolute maximum). Therefore, the pin can be conveniently tied to V_{IN} in always on applications where the controller is enabled continuously and never shuts down. Do not float the RUN pin.

The RUN and OVLO pins can alternatively be configured as undervoltage and overvoltage lockouts on the V_{IN} supply with a resistor divider from V_{IN} to GND. A simple resistor divider can be used as shown in *Figure 44* to meet specific V_{IN} voltage requirements.

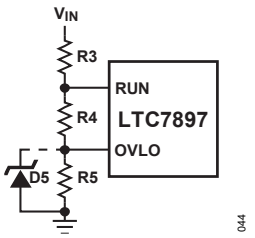


Figure 44. Using the RUN and OVLO Pins as Undervoltage and Overvoltage Lockouts

The current that flows through the R3, R4, and R5 dividers will directly add to the shutdown, sleep, and active current of the LTC7897, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megaohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the total of R3 + R3 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}.

The individual values of R3, R4, and R5 can be calculated from Equation 19, Equation 20, and Equation 21, as follows:

$$R5 = R_{TOTAL} \cdot \frac{1.2V}{\text{RISING } V_{IN} \text{ OVERVOLTAGE THRESHOLD}} \quad (19)$$

$$R4 = R_{TOTAL} \cdot \frac{1.2V}{\text{RISING } V_{IN} \text{ UNDERVOLTAGE THRESHOLD}} - R5 \quad (20)$$

$$R3 = R_{TOTAL} - R5 - R4 \quad (21)$$

For applications that do not require a precise V_{IN} overvoltage lockout, the OVLO pin can be tied directly to GND. The RUN pin in this type of application can be used as an external V_{IN} undervoltage lockout by setting R5 = 0Ω in Equation 19, Equation 20, and Equation 21.

The OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relationship should be satisfied:

$$V_{IN(MAX)} \cdot \left(\frac{R5}{R3+R4+R5}\right) < 6V \quad (22)$$

If the $V_{IN(MAX)}$ relationship for the OVLO pin cannot be satisfied, an external 5V Zener diode should also be placed from OVLO to the ground in addition to any lockout setting resistors.

Similarly, for applications that do not require a precise V_{IN} undervoltage lockout, the RUN pin can be tied to V_{IN}. In this configuration, the undervoltage threshold is limited to the internal DRV_{CC} UVLO thresholds as shown in *Table 1*. The resistor values for the V_{IN} overvoltage lockout can be computed by setting R3 = 0Ω in Equation 19, Equation 20, and Equation 21.

Soft-Start and Tracking (TRACK/SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC7897 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function, or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by connecting a capacitor from the TRACK/SS pin to GND. An internal 9µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC7897 regulates its feedback voltage (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. For a desired soft-start time (t_{SS}), select a soft-start capacitor (C_{SS}) = t_{SS} × 11.25nF/ms.

Alternatively, the TRACK/SS pin can be used to track another supply during start-up, as shown qualitatively in *Figure 45* and *Figure 46*. To track another supply, connect a resistor divider from the leader supply (V_X) to the TRACK/SS pin of the follower supply (V_{OUT}), as shown in *Figure 47*. During start-up, V_{OUT} tracks V_X, according to the ratio set by the resistor divider in Equation 23, as follows:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \cdot \frac{R_{TRACKA}+R_{TRACKB}}{R_A+R_B} \quad (23)$$

Set $R_{TRACKA} = R_A$ and $R_{TRACKB} = R_B$ for coincident tracking ($V_{OUT} = V_X$ during start-up).

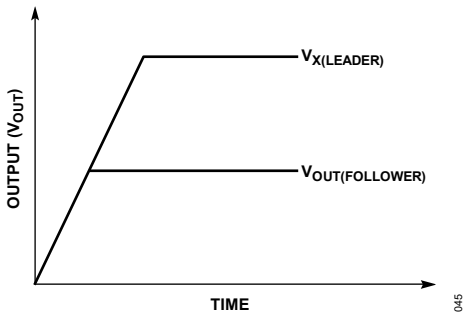


Figure 45. Coincident Tracking

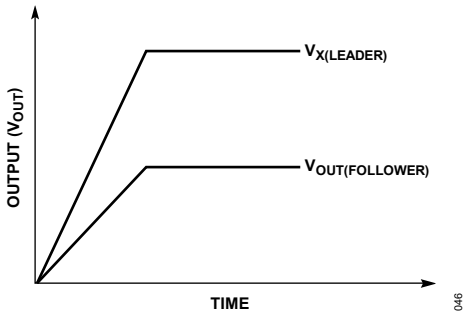


Figure 46. Ratiometric Tracking

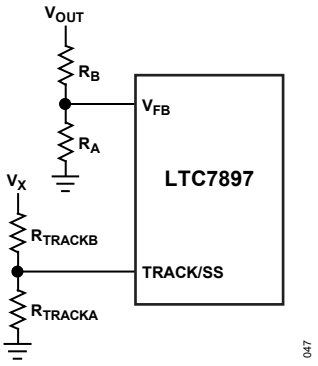


Figure 47. Using the TRACK/SS Pin for Tracking

DRV_{CC} and $INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC7897 features two separate internal LDO linear regulators that supply power at the DRV_{CC} pin from either the V_{IN} pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. Another LDO linear regulator supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. The DRV_{CC} pin is the supply pin for the MOSFET gate drivers and the $INTV_{CC}$ LDO regulator whereas $INTV_{CC}$ pin is the supply pin for much of the LTC7897 internal circuitry. The V_{IN} LDO regulator and the $EXTV_{CC}$ LDO regulator regulate DRV_{CC} between 5V to 10V, depending on how the DRVSET pin is set. Each LDO regulator can supply a peak current of at least 100mA.

Bypass the DRV_{CC} pin to GND with a minimum of 4.7µF ceramic capacitor, and place it as close as possible to the pin. It is recommended to place an additional 1µF ceramic capacitor next to the DRV_{CC} pin and GND pin to supply the high frequency transient currents required by the MOSFET gate drivers. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor.

The DRVSET pin programs the DRV_{CC} supply voltage, and the DRVUV pin selects the different DRV_{CC} UVLO and $EXTV_{CC}$ switchover threshold voltages. *Table 6* summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. *Table 7* summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs DRV_{CC} to 10V. Tying the DRVSET pin to GND programs DRV_{CC} to 6V. Place a 50k to 100k resistor between DRVSET and GND to program the DRV_{CC} voltage between 5V to 10V, as shown in *Figure 48*.

Table 6. DRVSET Pin Configurations and Voltage Settings

DRVSET PIN	DRV_{CC} VOLTAGE (V)
GND	6
$INTV_{CC}$	9.7
Resistor to GND 50kΩ to 100kΩ	5 to 10

Table 7. DRVUV Pin Configurations and Voltage Settings

DRVUV PIN	DRV_{CC} UVLO RISING AND FALLING THRESHOLDS (V)	$EXTV_{CC}$ SWITCHOVER RISING AND FALLING THRESHOLDS (V)
GND	3.93 and 3.71	4.8 and 4.55
FLOAT	5.35 and 5.05	6.1 and 5.85
$INTV_{CC}$	7.4 and 6.64	7.7 and 7.45

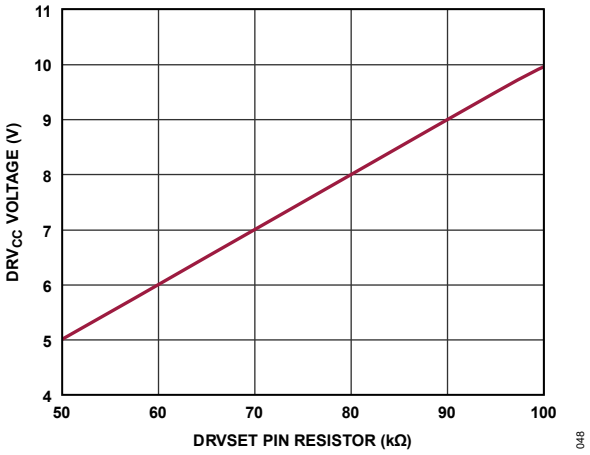


Figure 48. Relationship between DRV_{CC} Voltage and Resistor Value at DRVSET Pin

High input voltage applications in which large MOSFETs are driven at high frequencies can exceed the maximum junction temperature rating for the LTC7897. The DRV_{CC} current, which is dominated by the gate charge current, can be supplied by either the V_{IN} LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.8V, 6.1V or 7.7V, as determined by the DRVUV pin), the V_{IN} LDO regulator is enabled. In this case, power dissipation for the IC is equal to V_{IN} × $INTV_{CC}$ current (I_{INTVCC}). The gate charge current is dependent on the operating frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in Note 2. For example, the LTC7897 DRV_{CC} current is limited to less than 39mA from a 48V supply when not using the $EXTV_{CC}$ supply at an ambient temperature of 70°C, as shown in Equation 24:

$$T_J = 70°C + (39mA)(48V)(43°C/W) = 150°C \quad (24)$$

To prevent the junction temperature from exceeding the maximum rated as shown in *Table 2*, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the V_{IN} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than this voltage, the LDO regulator is in dropout, and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage (up to an absolute maximum of 30V), DRV_{CC} is regulated to the programmed voltage. Using the $EXTV_{CC}$ LDO regulator allows the MOSFET driver and control power to be derived from one of the switching regulator outputs of the LTC7897 (4.7V ≤ V_{OUT} ≤ 30V) during normal operation, and from the V_{IN} LDO when the output is out of regulation (e.g., start up or short circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, add an external Schottky diode between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 15V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from an outpu because the V_{IN} current resulting from the driver and control currents is scaled by a factor of $V_{OUT}/(V_{IN}$ • Efficiency). For 5V to 30V regulator outputs, connect the $EXTV_{CC}$ pin to V_{OUT}. Tying the $EXTV_{CC}$ pin to a 12V supply reduces the junction temperature in Equation 22 from 150°C to the results given by Equation 25, as follows:

$$T_J = 70°C + (39mA)(12V)(43°C/W) = 90°C \quad (25)$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive DRV_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection causes the V_{IN} LDO regulator to power DRV_{CC}, resulting in an efficiency penalty of up to 10% or more at high input voltages.
2. $EXTV_{CC}$ connected directly to the regulator output. This connection is the normal connection for an application with an output range of 5V to 30V and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it can be used to power $EXTV_{CC}$, provided that it is compatible with the MOSFET gate drive requirements. This supply can be higher or lower than V_{IN}. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.
4. $EXTV_{CC}$ connected to an output derived boost or charge pump. For regulators where outputs are below 5V, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output derived voltage that is boosted to greater than the $EXTV_{CC}$ switchover threshold.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the top MOSFET. Capacitor C_B in *Figure 4* is charged through an external diode D_B from DRV_{CC} when the bottom MOSFET is on, and SW is low.

When the top MOSFET turns on, the driver places the C_B voltage across the gate source of the top MOSFET, which enhances the top MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN}, and the BOOST pin follows. With the top MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + VDRV_{CC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the top MOSFET. For a typical application, a value of C_B = 0.1µF is sufficient. The reverse breakdown of the external diode D_B must be greater than $V_{IN(MAX)}$.

Minimum On-Time Considerations

The minimum on-time ($t_{ON(MIN)}$) is the smallest time duration that the LTC7897 is capable of turning on the top MOSFET. $t_{ON(MIN)}$ is determined by internal timing delays and the gate charge required to turn on the MOSFET. Low duty cycle applications can approach this minimum on-time limit. Take care to ensure the results in Equation 26, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \cdot f} \quad (26)$$

If the duty cycle falls below what can be accommodated by the minimum on time, the controller begins to skip cycles. The output voltage continues to be regulated, but the ripple voltage and current increase. The minimum on time for the LTC7897 is approximately 60ns. However, as the peak sense voltage decreases, the minimum on time gradually increases up to about 80ns. This change is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Fault Conditions: Current Limit and Foldback

The LTC7897 includes current foldback to reduce the load current when the output is shorted to GND. If the output voltage falls below 70% of its regulation point, the maximum sense voltage is progressively lowered from 100% to 40% of its maximum value. Under short-circuit conditions with low duty cycles, the LTC7897 begins cycle skipping to limit the short-circuit current. In this situation, the bottom MOSFET dissipates most of the power, but less than in normal operation. The short-circuit ripple current ($\Delta I_{L(SC)}$) is determined by $t_{ON(MIN)} \approx 60ns$, the input voltage, and the inductor value given by Equation 27, as follows:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \cdot V_{IN}/L \quad (27)$$

The resulting average short-circuit current (I_{SC}) is given by Equation 28, as follows:

$$I_{SC} = 40\% \cdot I_{LIM(MAX)} - \frac{\Delta I_{L(SC)}}{2} \quad (28)$$

where $I_{LIM(MAX)}$ is the maximum peak inductor current.

Fault Conditions: Overvoltage Protection

If the output voltage rises 10% above the set regulation point, the top MOSFET turns off, and the inductor current is not allowed to reverse until the overvoltage condition clears.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from DRV_{CC} to GND), internal overtemperature shutdown circuitry shuts down the LTC7897. When the internal die temperature exceeds 180°C, the DRV_{CC} LDO regulator and gate drivers are disabled. When the die cools to 160°C, the LTC7897 enables the DRV_{CC} LDO regulator and resumes operation, beginning with a soft-start start-up. Avoid long-term overstress (T_J > 150°C) because it can degrade the performance or shorten the life of the device.

Phase-Locked Loop and Frequency Synchronization

The LTC7897 has an internal PLL that allows the turn on of the top MOSFET to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase lock and synchronization. Although it is not required, placing the free-running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7897 operates in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7897 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7897 can only be synchronized to an external clock frequency within the range of 100kHz to 2.5MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 29, as follows:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...) \quad (29)$$

where L1, L2, L3, and so on are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7897 circuits: IC V_{IN} current, DRV_{CC} regulator current, I^2R losses, and top MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in *Table 1* , which excludes MOSFET driver and control currents. Other than at light loads in Burst Mode operation, V_{IN} current typically results in a small (<0.1%) loss.
2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power FETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge (dQ) moves from DRV_{CC} to GND. The resulting dQ/time duration (dt) is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = SW frequency (f_{SW})(Q_T + Q_B), where Q_T and Q_B are the gate charges of the top and bottom MOSFETs.

   Supplying DRV_{CC} from an output derived source through $EXTV_{CC}$ scales the V_{IN} current required for the driver and control circuits by a factor of $V_{OUT}/(V_{IN} \times \text{efficiency})$. For example, in a 20V to 5V application, 10mA of DRV_{CC} current results in approximately 2.5mA of V_{IN} current. This result reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.
3. I^2R losses are predicted from the DC resistances of the input fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, the resistance of one MOSFET can be summed with the resistances of L, R_{SENSE}, and ESR to obtain the I^2R losses.

   For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ and ESR = 40mΩ (the sum of both input and output capacitance losses), the total resistance is 130mΩ. The resulting losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems are not doubling, but quadrupling the importance of loss terms in the switching regulator system.
4. Transition losses apply only to the top MOSFETs and become significant only when operating at higher input voltages (typically 15V or greater). Transition losses can be estimated using Equation 30, as follows:

$$\text{Transition Loss} = 1.7(V_{IN})^2 \cdot I_{L(MAX)} \cdot C_{RSS} \cdot f_{SW} \quad (30)$$

   Where C_{RSS} is the reverse transfer capacitance.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance with a maximum of 20mΩ to 50mΩ of ESR. Other losses, including inductor core losses, generally account for less than 2% of the total additional loss. Other losses, including inductor core losses, generally account for less than 2% of the total additional loss.

Checking Transient Response

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} × ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling at this test point reflect the closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in *Figure 52*, *Figure 54*, *Figure 56*, and *Figure 58* provide an adequate starting point for most applications.

The ITH series compensation resistor (R_C) to compensation capacitor (C_C) filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 times to 2 times their initial values) to optimize transient response when the final PCB layout is done and the particular output capacitor type and value are determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of the full load current, with a rise time of 1µs to 10µs, produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across from the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITH pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing R_C, and the bandwidth of the loop increases by decreasing C_C. If R_C increases by the same factor that C_C decreases, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately C_{LOAD} × 25µs/µF. Therefore, a 10µF capacitor requires a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume the nominal input voltage $V_{IN(NOMINAL)}$ = 48V, $V_{IN(MAX)}$ = 100V, V_{OUT} = 12V, I_{OUT} = 4A, and f_{SW} = 1MHz.

Take the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to GND is required, with a value given by Equation 31, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega \quad (31)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. The inductor value can then be calculated using Equation 32, as follows:

$$L = \frac{V_{OUT}}{f_{SW}(\Delta I_L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right) = 7.5\mu\text{H} \quad (32)$$

   The highest value of ripple current occurs at the maximum input voltage. In this case the ripple at V_{IN} = 100V is 35%.

3. Verify the minimum on-time of 50ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 33, as follows:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f_{SW})} = 120\text{ns} \quad (33)$$

4. This time is sufficient to satisfy the minimum on-time requirement. If the minimum on time is violated, the LTC7897 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.
5. Select the R_{SENSE} resistor value. The peak inductor current is the maximum DC output current plus half of the inductor ripple current, or 4A • (1 + 0.30/2) = 4.6A in this case. The R_{SENSE} resistor value can then be calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = FLOAT), given by Equation 34, as follows:

$$R_{SENSE} \leq \frac{45\text{mV}}{4.6\text{A}} \cong 10\text{m}\Omega \quad (34)$$

6. To allow for additional margin, a lower value R_{SENSE} can be used (for example, 8mΩ); however, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.
7. Select the feedback resistors. If light load efficiency is required, high value feedback resistors can be used to minimize the current due to the feedback divider. However, in most applications, a feedback divider current in the range of 10µA to 100µA or more is acceptable. For a 50µA feedback divider current, R_A = 0.8V/50µA = 16kΩ. R_B can then be calculated as $R_B = R_A(12V/0.8V - 1)$ = 226kΩ.
8. Select the MOSFETs. The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7897 evaluation board. However, an educated guess about the application is helpful to initially select MOSFETs. Because this is a high current, low voltage application, I^2R losses likely dominate over transition losses for the top MOSFET. Therefore, choose a MOSFET with lower $R_{DS(ON)}$ as opposed to a lower gate charge to minimize the combined loss terms. The bottom MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and higher gate charge than the top MOSFET.

9. Select the input and output capacitors. C_{IN} is chosen for an RMS current rating of at least 2A ($I_{OUT}/2$, with margin) at temperature. C_{OUT} is chosen with an ESR of 10mΩ for low output ripple. Multiple capacitors connected in parallel may be required to reduce the ESR to this level. The output ripple in continuous mode is highest at the maximum input voltage. The output voltage ripple due to ESR is approximately given by Equation 35, as follows:

$$V_{ORIPPLE} = ESR \bullet \Delta I_L = 10m\Omega^{*}1.4A = 14mV_{P-P} \quad (35)$$

   On the 12V output, $14mV_{P-P}$ is equal to 0.12% of peak-to-peak voltage ripple.

10. Determine the bias supply components. Because the regulated output is greater than the $EXTV_{CC}$ switchover threshold, it can be used to bias $EXTV_{CC}$. For an 8ms soft-start, select a 0.1µF capacitor for the TRACK/SS pin. As a first pass estimate for the bias components, select the DRV_{CC} capacitance C_{DRVCC} = 4.7µF, C_{INTVCC} = 0.1µF and C_B = 0.1µF.
11. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can be used to control the minimum input voltage for regulator operation, or it can be tied to V_{IN} for always-on operation. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PC Board Layout Checklist

Figure 49 shows the current waveforms present in the various branches of the synchronous regulators operating in the continuous mode.

When laying out the PCB, use the following checklist to ensure proper operation of the IC.

1. Route the BGUP and BGDN traces together and connect them as close as possible to the bottom MOSFET gate. If using gate resistors, connect the resistor connections to the MOSFET gate as close as possible to the MOSFET. Connecting BGUP and BGDN further away from the bottom MOSFET gate can cause inaccuracies in the dead time control circuit of the LTC7897. Route the TGUP and TGDN traces together and connect them as close as possible to the top MOSFET gate.
2. The combined IC GND pin and the GND return of C_{DRVCC} must return to the combined C_{OUT} negative terminals. The path formed by the top N-channel MOSFET and the C_{IN} capacitor must have short leads and PCB trace lengths. Connect the output capacitor's negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
3. Connect the LTC7897 V_{FB} pin resistive dividers to the positive terminals of C_{OUT} and the signal GND. Place the divider close to the V_{FB} pin to minimize noise coupling into the sensitive V_{FB} node. The feedback resistor connections must not be along the high current input feeds from the input capacitors.
4. Route the $SENSE^-$ and $SENSE^+$ leads together with minimum PCB trace spacing. Route these traces away from the high frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Connect the DRV_{CC} decoupling capacitor close to the IC, between the DRV_{CC} and the power GND pin. This capacitor carries the current peaks of the MOSFET drivers. Place an additional 1µF ceramic capacitor next to the DRV_{CC} and GND pins to help improve noise performance.
6. Keep the switching node (SW), top gate nodes (TGUP and TGDN), and boost node (BOOST) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins. All of these

nodes have large and fast-moving signals. Therefore, keep the nodes on the output side of the LTC7897 and ensure they occupy the minimum PCB trace area.

7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.

PC Board Layout Debugging

Use a DC to 50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold, typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage is maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame an improper PCB layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation. Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TGxx, and possibly BGxx connections and the sensitive voltage and current pins. Place the capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate the common GND path voltage pickup between these components and the GND pin of the IC.

A problem that can be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage.

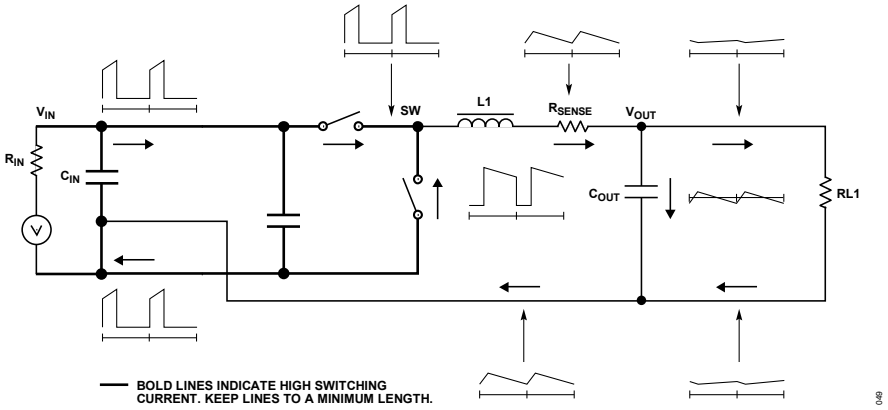


Figure 49. Branch Current Waveforms

TYPICAL APPLICATION

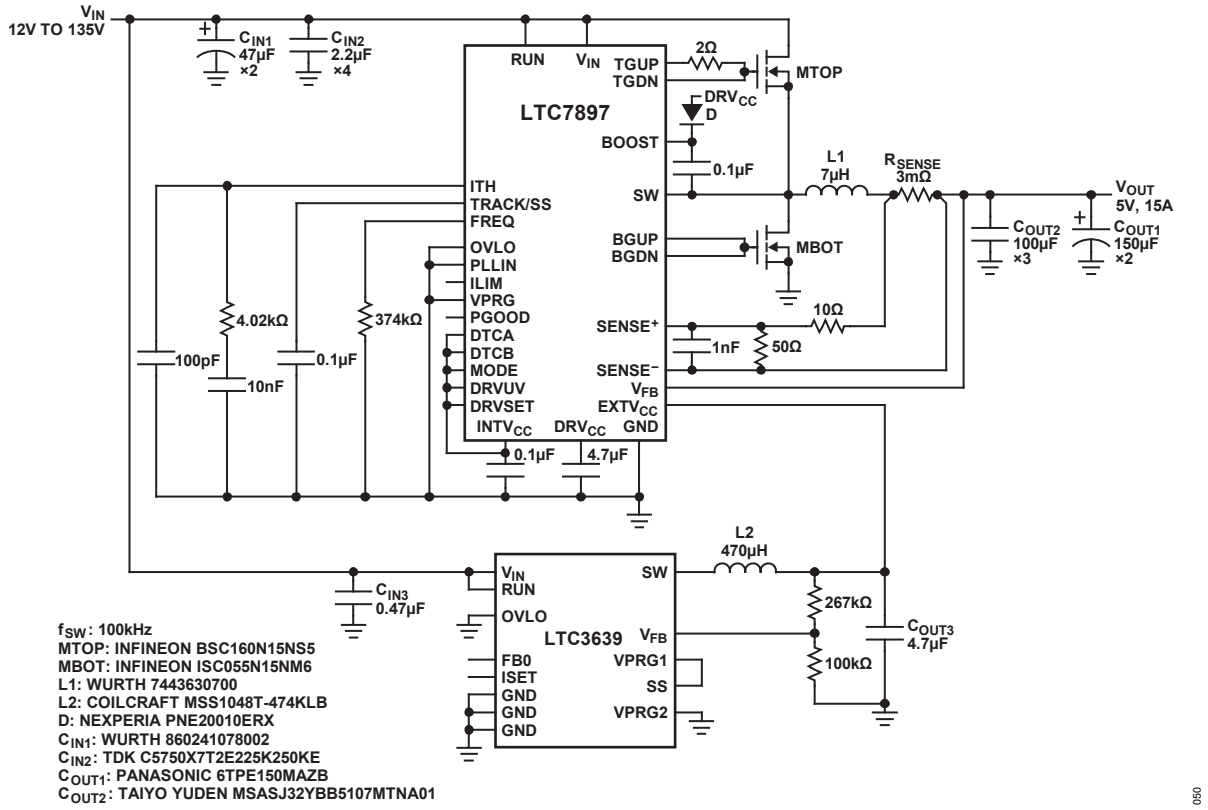


Figure 50. High Efficiency, High Voltage, $5V_{OUT}$, Step-Down Regulator

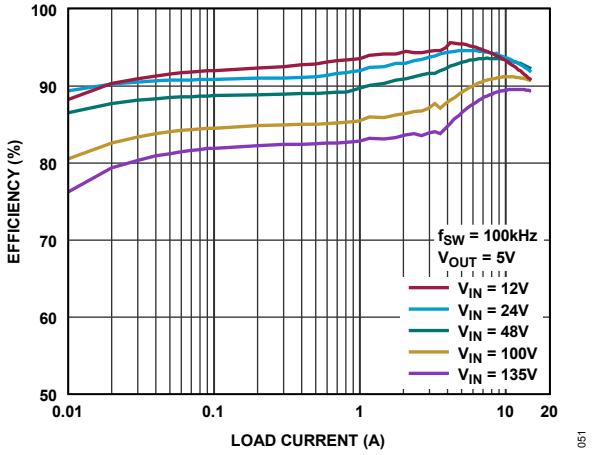


Figure 51. V_{OUT} Efficiency vs. Load Current for Figure 50

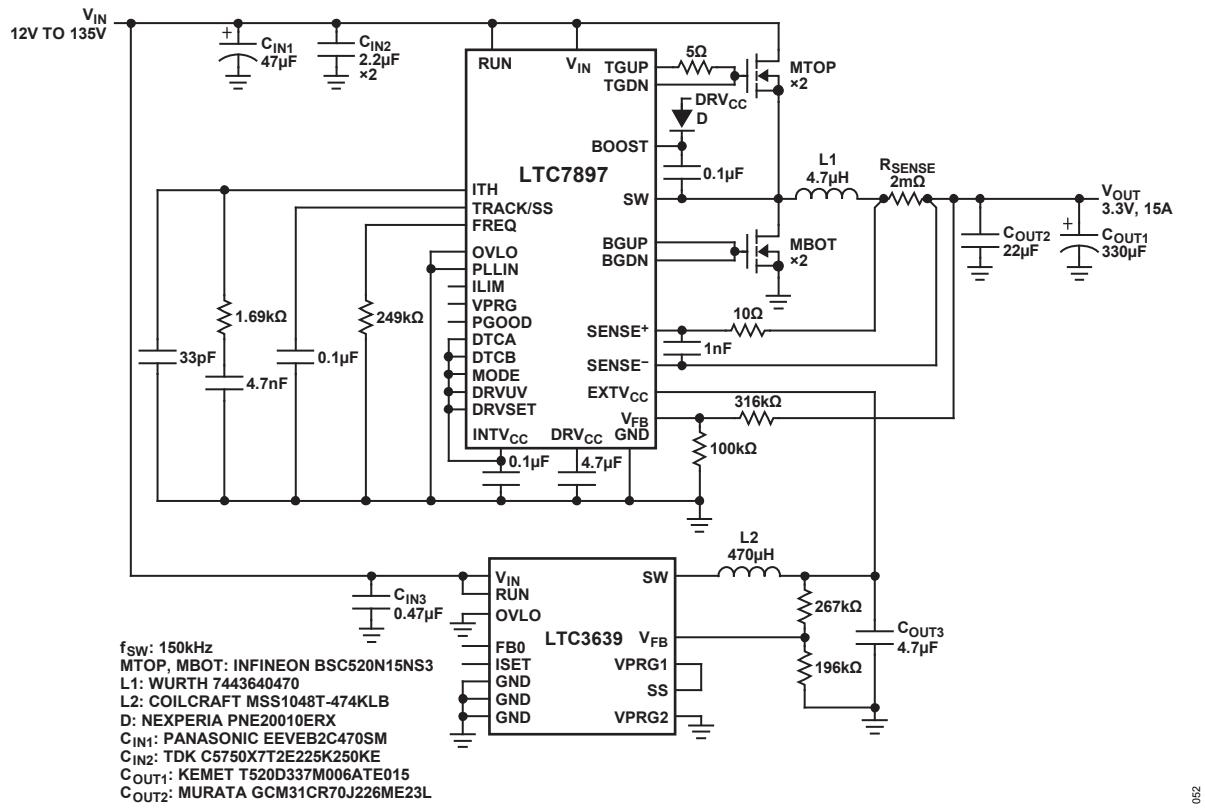


Figure 52. High Efficiency, 3.3V_{OUT}, Step-Down Regulator

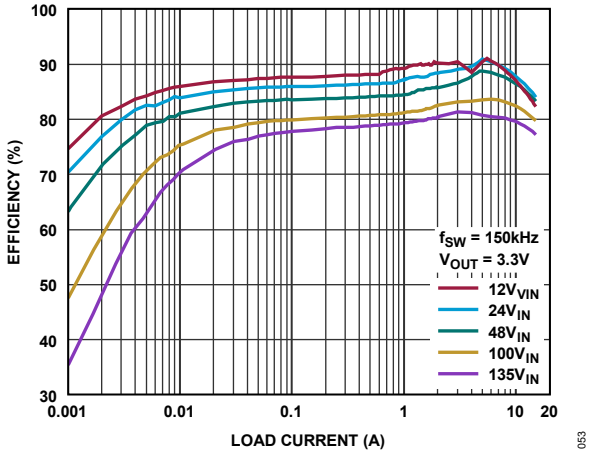


Figure 53. V_{OUT} Efficiency vs. Load Current for Figure 52

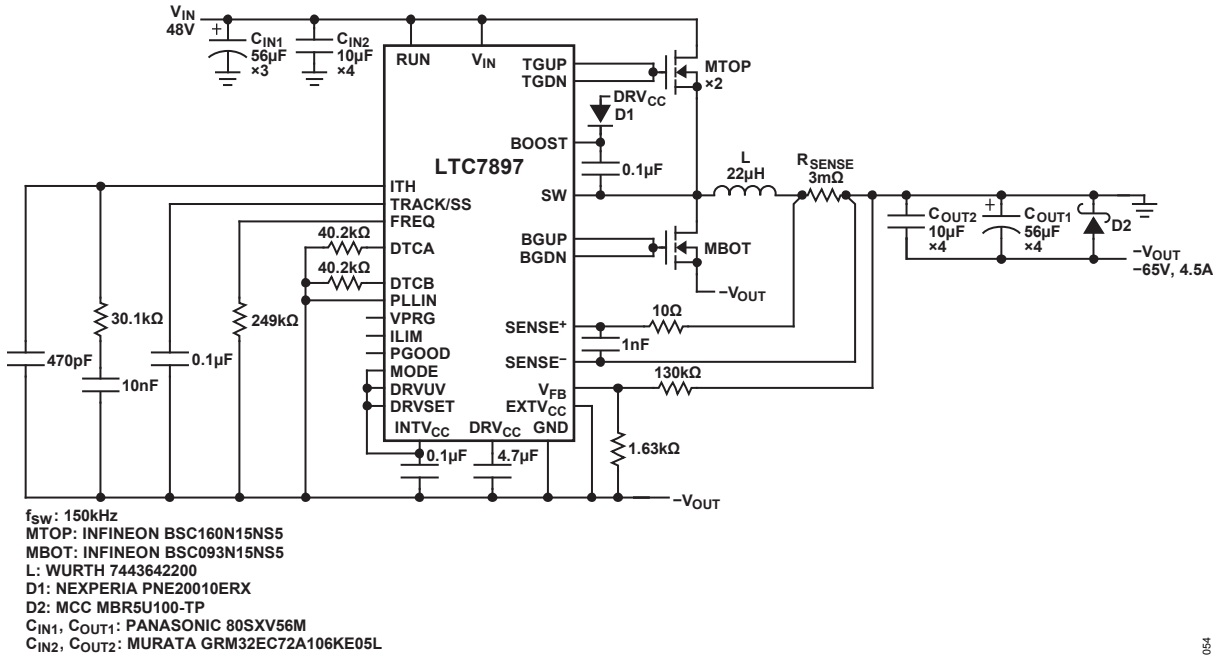


Figure 54. High Efficiency, 48V_{IN} to -65V_{OUT} Regulator

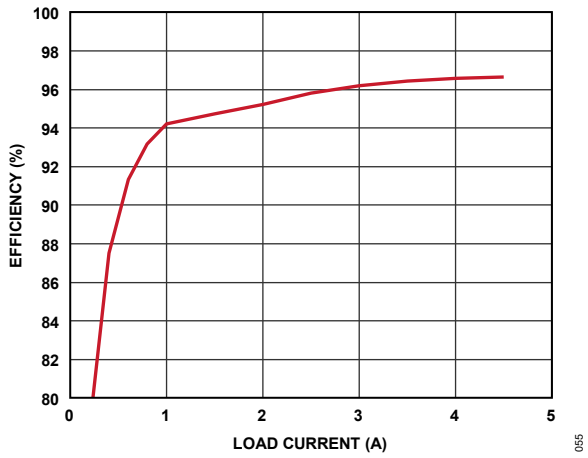


Figure 55. V_{OUT} Efficiency vs. Load Current for Figure 54

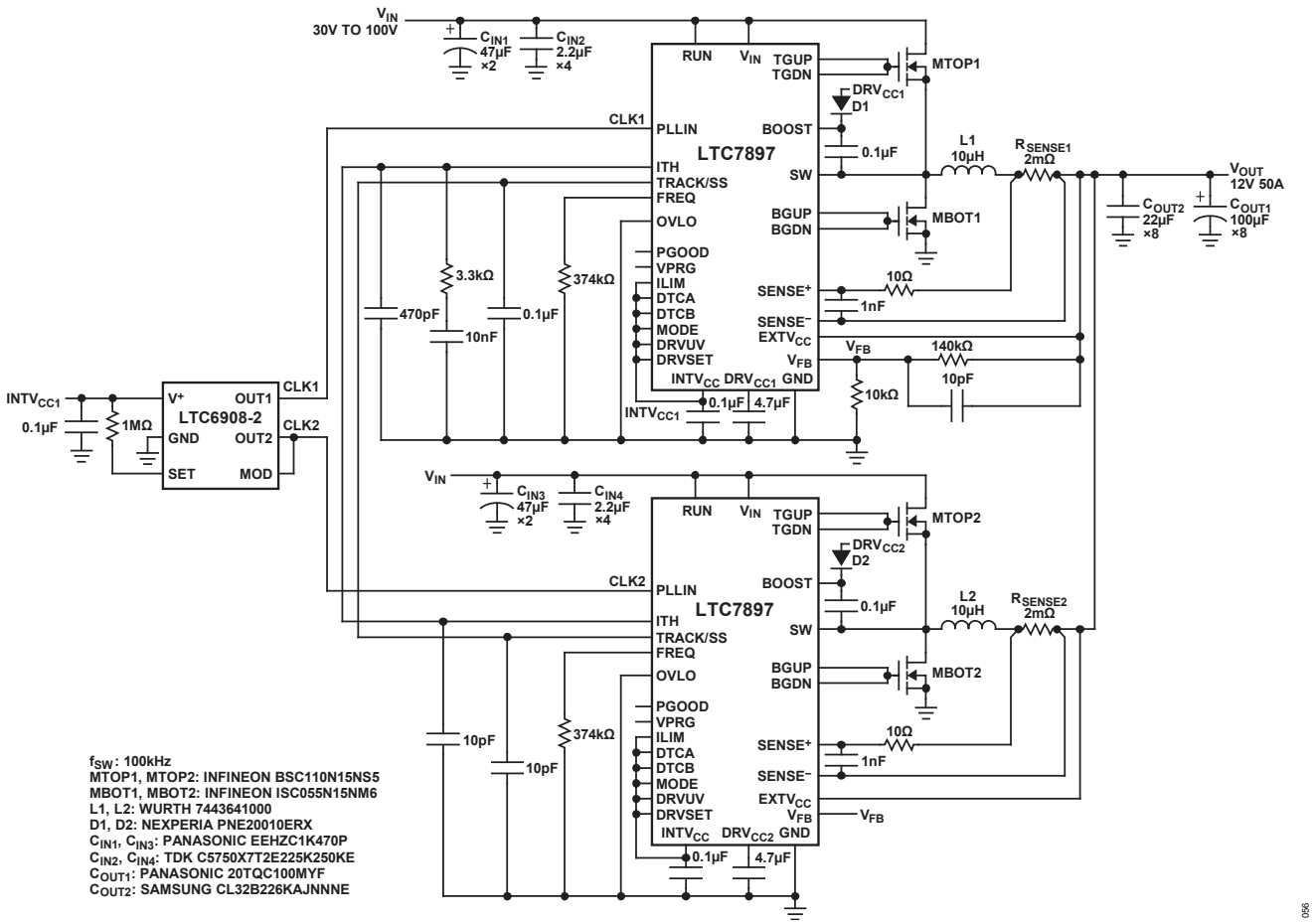


Figure 56. Two-phase, High Efficiency, 12V_{OUT}, Step-Down Regulator

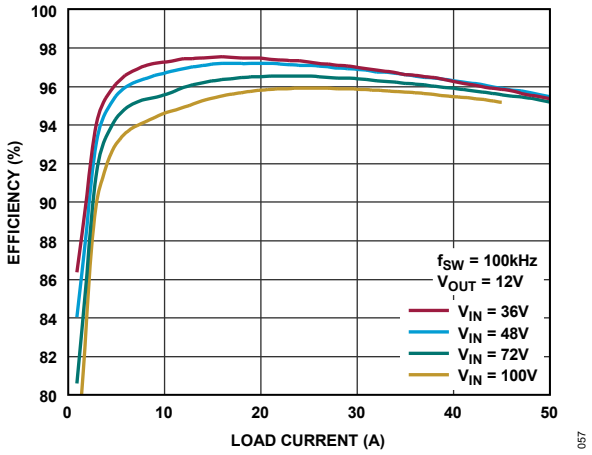


Figure 57. V_{OUT} Efficiency vs. Load Current for Figure 56

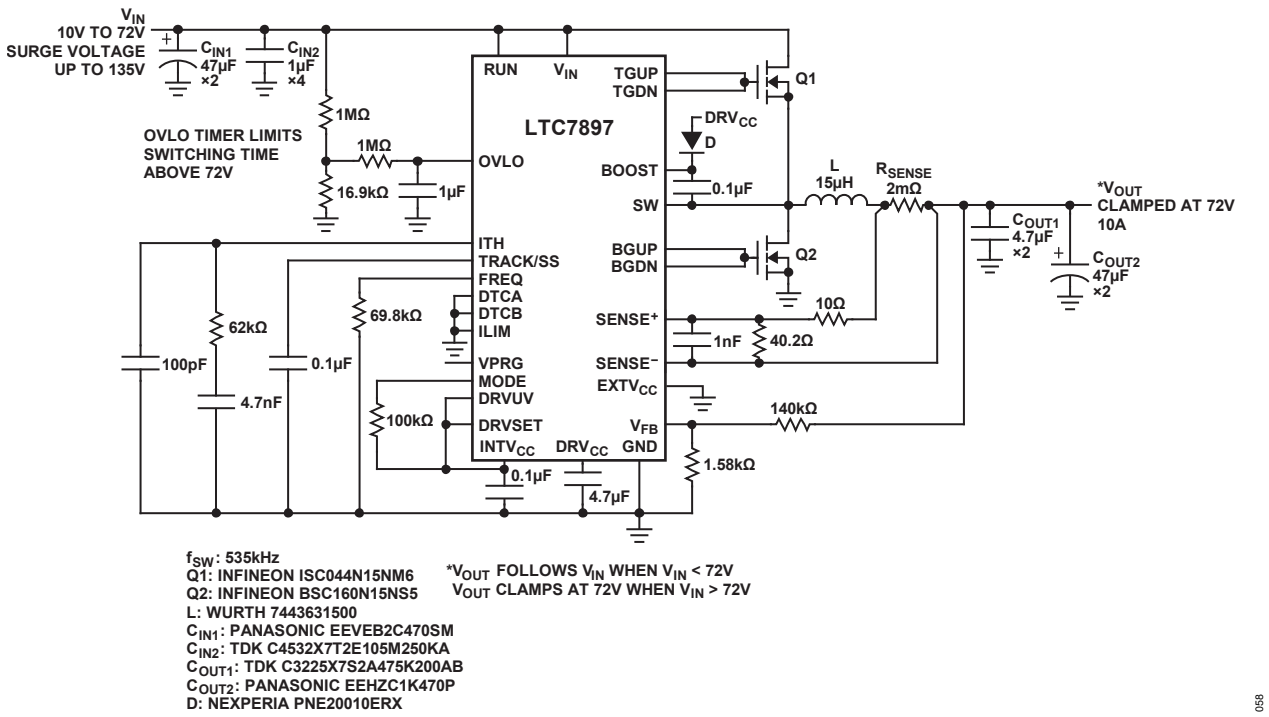


Figure 58. High Efficiency, 72V$_{OUT}$, Surge-Stopper

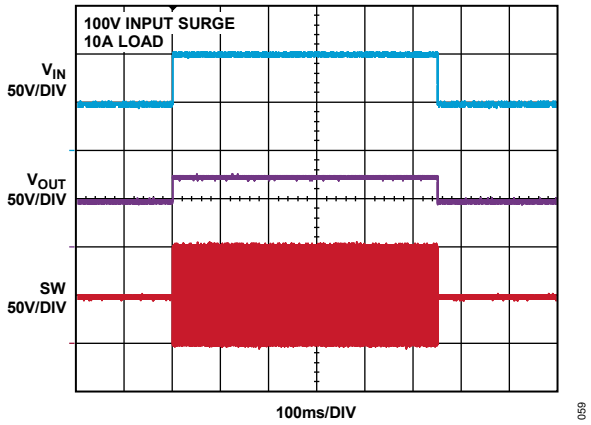


Figure 59. Overvoltage Protector Regulates Output at 72V During V$_{IN}$ Transient for Figure 58

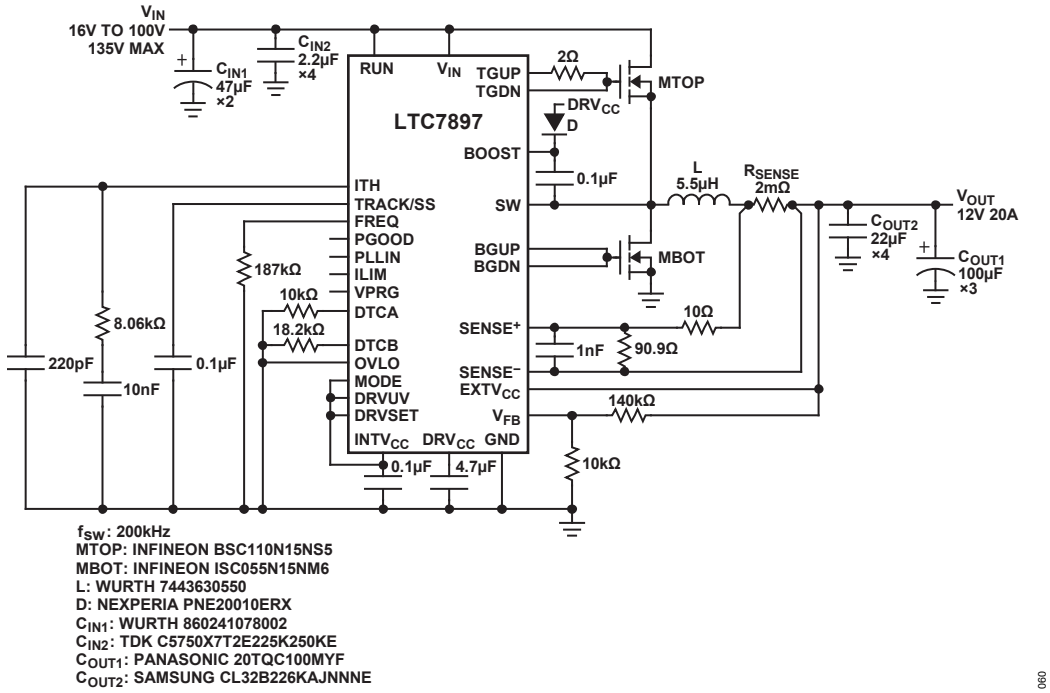


Figure 60. High Efficiency, 12V_{OUT}, Step-Down Regulator

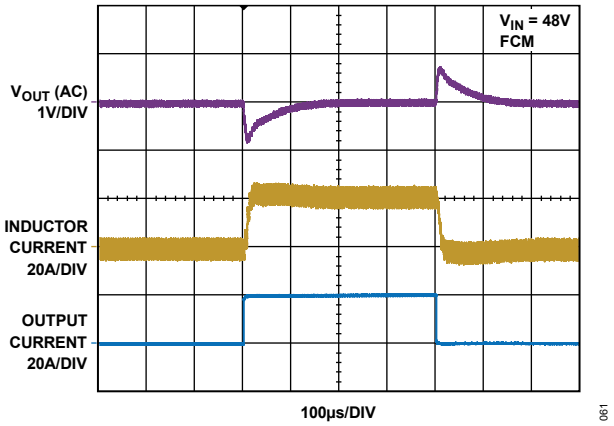


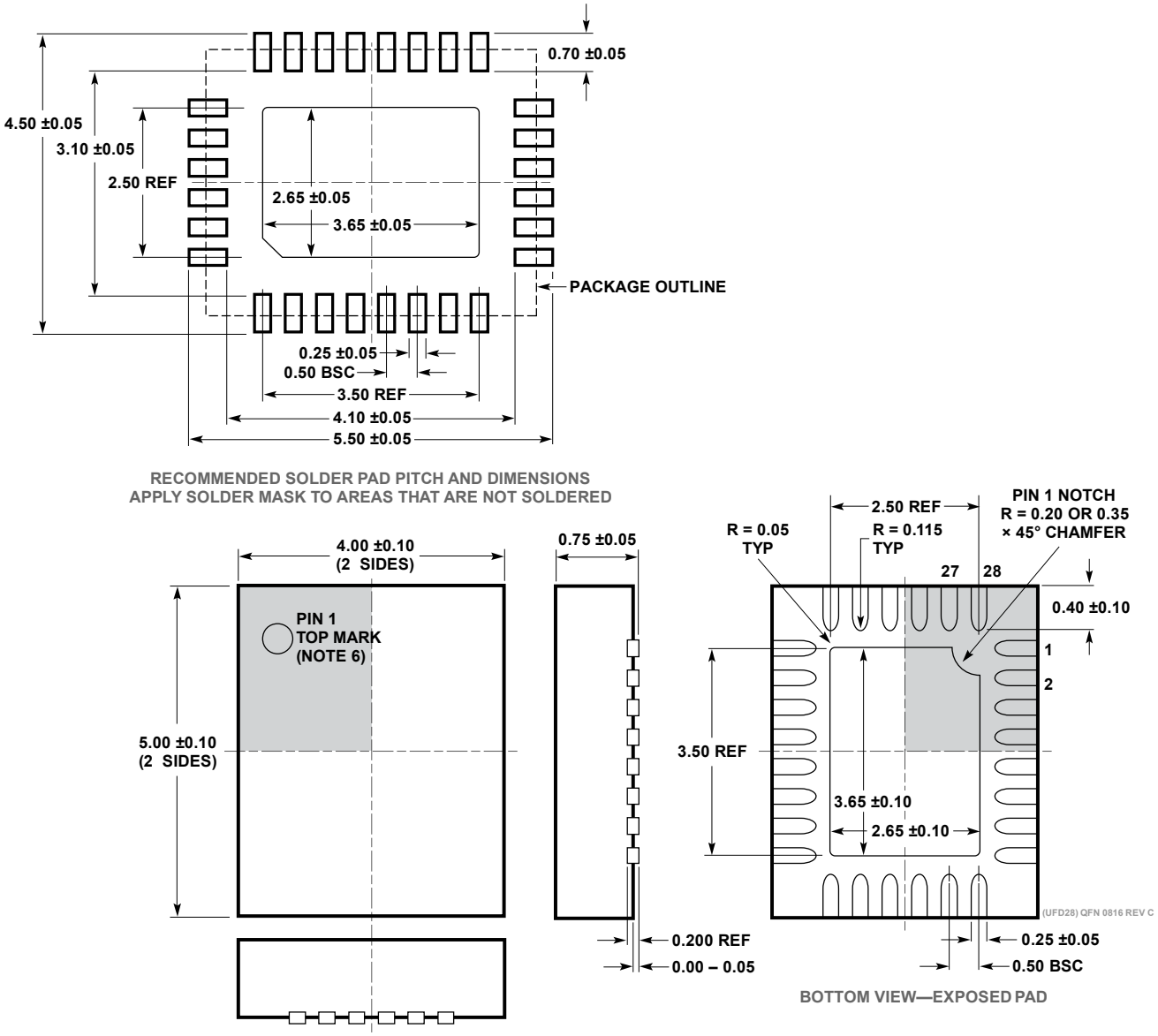
Figure 61. 0A to 20A Load Step Forced Continuous mode for Figure 60

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3895	150V, Low I_Q, Synchronous Step-Down DC/DC Controller, 100% Duty Cycle Capability, Adjustable 5V to 10V Gate Drive	$4V \le V_{IN} \le 140V$, $0.8V \le V_{OUT} \le 60V$, $I_Q = 40\mu A$, PLL Fixed Frequency 50kHz to 900kHz, 38-Lead, TSSOP, High Voltage Package
LTC7810	150V, Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 100% Duty Cycle, 10V Gate Drive	$4.5V \le V_{IN} \le 140V$, $1V \le V_{OUT} \le 60V$, $I_Q = 110\mu A$, PLL Fixed Frequency 50kHz to 750kHz, 48-Lead, 7mm × 7mm, eLQFP Package
LTC7801	150V, Low I_Q, Synchronous Step-Down DC/DC Controller 100% Duty Cycle Capability, Adjustable 5V to 10V Gate Drive	$4V \le V_{IN} \le 140V$, $0.8V \le V_{OUT} \le 60V$, $I_Q = 40\mu A$, PLL Fixed Frequency 50kHz to 900kHz, 24-Pin, 4mm × 5mm, QFN or TSSOP Packages
LTC3896	150V, Low I_Q, Synchronous Inverting DC/DC Controller with Ground-Referenced Control/Interface Pins	$4V \le V_{IN} \le 140V$, 150V Absolute Maximum, PLL Fixed Frequency 50kHz to 900kHz, $-0.8V \le V_{OUT} \le -60V$, Adjustable 5V to 10V Gate Drive, $I_Q = 40\mu A$
LTC7800	60V, Low I_Q, High Frequency, Synchronous Step-Down DC/DC Controller	$4V \le V_{IN} \le 60V$, $0.8V \le V_{OUT} \le 24V$, $I_Q = 50\ \mu A$, PLL fixed frequency of 320kHz to 2.25MHz, 3mm × 4mm, 20-Pin QFN Package
LTC7805	40V, Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with Spread Specturn, 100% Duty Cycle Capable	$4.5V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 40v$, $I_Q = 18\mu A$, 100% Duty Cycle Capable, PLL Fixed Frequency 100kHz to 3MHz, 28-Pin 4mm × 5mm QFN Side-Wettable Package

OUTLINE DIMENSIONS

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 62. Package Description

ORDERING GUIDE

Table 8. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7897RUFD#PBF	LTC7897RUFD#TRPBF	LTC7897	28-Lead (4mm x 5mm) Plastic QFN	−40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.