100V Half-Bridge Driver with Adaptive Shoot-Through Protection

FEATURES

- **100V Maximum Input Voltage Independent of IC Supply Voltage V_{CC}**
- **6V to 14V V_{CC} and Bottom Gate Driver Voltage**
- **4V to 14V Top Gate Driver Voltage**
- **1.3Ω Pull-Down, 1.6Ω Pull-Up**
- **Adaptive Shoot-Through Protection**
- **Three-State PWM Input with Enable Pin**
- **V_{CC} UVLO and Floating Supply UVLO**
- Drives Dual N-Channel MOSFETs
- Available in Thermally Enhanced 10-LEAD MSOP Package

APPLICATIONS

- Industrial Power Systems
- Half-Bridge DC/DC Converters
- Telecommunication Power Systems

GENERAL DESCRIPTION

The LTC7065 is a half-bridge dual N-Channel MOSFET gate driver that operates at up to 100V input voltage and features a supply independent three-state PWM input logic.

The strong 1.3Ω pull-down and 1.6Ω pull-up drive capability can drive large gate capacitances of high-voltage MOSFETs with short transition times in high switching frequency applications. The adaptive shoot-through protection is designed for optimized efficiency and MOSFET cross-conduction protection.

The LTC7065 contains undervoltage lockout circuits on both the V_{CC} supply and floating driver supply that turn off the external MOSFETs when activated. See below for a comparison of the parts in this family.

PARAMETER	LTC7060	LTC7063	LTC7065
Absolute Max Voltage	115V	155V	115V
Floating Bottom Gate Driver	Yes	Yes	No
V_{CC} OVLO	Yes	Yes	No
Package	MS12E	MS12E	MS10E

TYPICAL APPLICATION

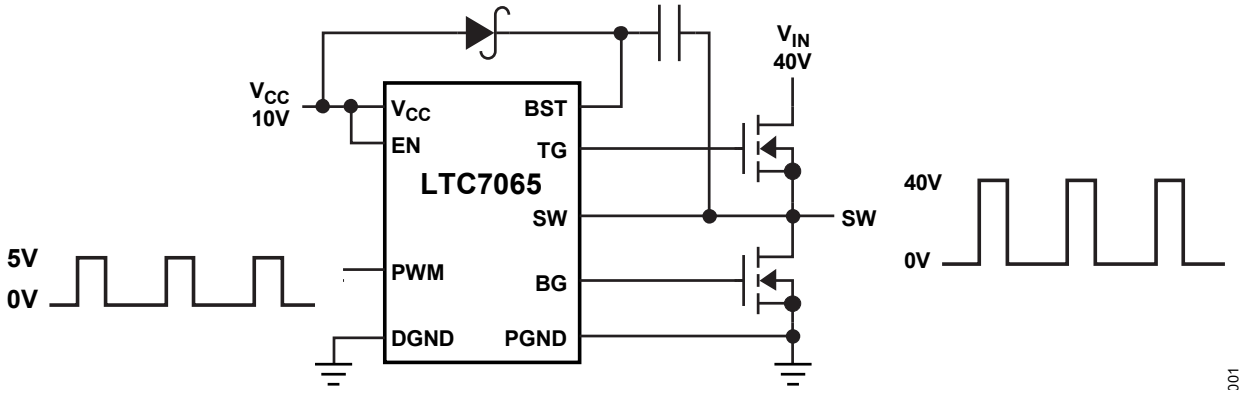

Figure 1. 40V Half-Bridge Driver

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REVISION HISTORY

12/2023 - Rev. 0: Initial Release for Product Intro

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C ([1]), V_{CC} = V_{BST} = 10V, V_{SW} = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Supply and V_{cc} Supply						
Input Voltage	V_{IN}				100	V
IC and BG Driver Supply Voltage Range	V_{CC}		6		14	V
V_{CC} Supply Current ([3])	I_{VCC}	No Switching, BG = Low		150		µA
V_{CC} Supply Current ([3])	I_{VCC}	No Switching, BG = High		300		µA
V_{CC} Undervoltage Lockout Threshold	V_{UVLO_VCC}	V_{CC} Falling		5.4		V
UVLO Hysteresis	V_{UVLO_VCC}			0.3		V
TG Gate Driver Supply (BST)						
TG Driver Supply Voltage Range	V_{BST-SW}	(With Respect to SW)	4		14	V

(T_A = 25°C ([1]), V_{CC} = V_{BST} = 10V, V_{SW} = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Total BST Current ([3])	I_{BST}	No Switching, TG = Low			9		µA
		No Switching, TG = High			105		
Undervoltage Lockout Threshold	V_{UVLO_BST}	BST Falling, With Respect to SW			3.4		V
UVLO Hysteresis	V_{UVLO_BST}				0.3		V
Input Signal (PWM, EN)							
TG Turn-On Input Threshold	$V_{IH(TG)}$	PWM Rising	-40°C ≤ T_J ≤ 150°C	2.7	3.2	3.7	V
TG Turn-Off Input Threshold	$V_{IL(TG)}$	PWM Falling	-40°C ≤ T_J ≤ 150°C	2.45	2.95	3.45	V
BG Turn-On Input Threshold	$V_{IH(BG)}$	PWM Falling	-40°C ≤ T_J ≤ 150°C	0.6	1	1.4	V
BG Turn-Off Input Threshold	$V_{IL(BG)}$	PWM Rising	-40°C ≤ T_J ≤ 150°C	0.85	1.25	1.65	V
PWM Input Three-State Float Voltage	V_{PWM_TRI}			1.9	2.1	2.3	V
PWM Internal Pull-Up Resistor	R_{UP_PWM}	To Internal 4.5V Supply			48		kΩ
PWM Internal Pull-Down Resistor	R_{DOWN_PWM}				42		kΩ
EN Pin Threshold	V_{ENR}	EN Rising	-40°C ≤ T_J ≤ 150°C	1.15	1.25	1.35	V
EN Pin Threshold Hysteresis	V_{ENH}				165		mV
EN Internal Pull-Down Resistor	R_{DOWN_EN}				2		MΩ
Dead-Time							
BG Low to TG High Propagation Delay	$t_{PLH(TG)}$				37		nsec
TG Low to BG High Propagation Delay	$t_{PLH(BG)}$				41		nsec
Low-Side Gate Driver Output (BG)							
BG Pull-Up Resistance	R_{BG_UP}	V_{CC} = 10V, Source 100mA			1.6		Ω

(T_A = 25°C ([1]), V_{CC} = V_{BST} = 10V, V_{SW} = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
BG Pull-Down Resistance	R_{BG_DOWN}	V_{CC} = 10V, Sink 100mA		1.3		Ω
High-Side Gate Driver Output (TG)						
TG Pull-Up Resistance	R_{TG_UP}	BST = 10V, SW = 0V, Source 100mA		1.6		Ω
TG Pull-Down Resistance	R_{TG_DOWN}	BST = 10V, SW = 0V, Sink 100mA		1.3		Ω
Switching Time						
PWM High to BG Low Propagation Delay	$t_{PHL(BG)}$			17		ns
PWM Low to TG Low Propagation Delay	$t_{PHL(TG)}$			24		ns
BG Output Rising Time	$t_{r(BG)}$	10% - 90%, C_{LOAD} = 3nF		23		ns
BG Output Falling Time	$t_{f(BG)}$	10% - 90%, C_{LOAD} = 3nF		20		ns
TG Output Rising Time	$t_{r(TG)}$	10% - 90%, C_{LOAD} = 3nF		29		ns
TG Output Falling Time	$t_{f(TG)}$	10% - 90%, C_{LOAD} = 3nF		28		ns
EN High to TG/BG High Propagation Delay	$t_{PH(EN)}$			35		ns
EN Low to TG/BG Low Propagation Delay	$t_{PL(EN)}$			43		ns

Timing Diagram

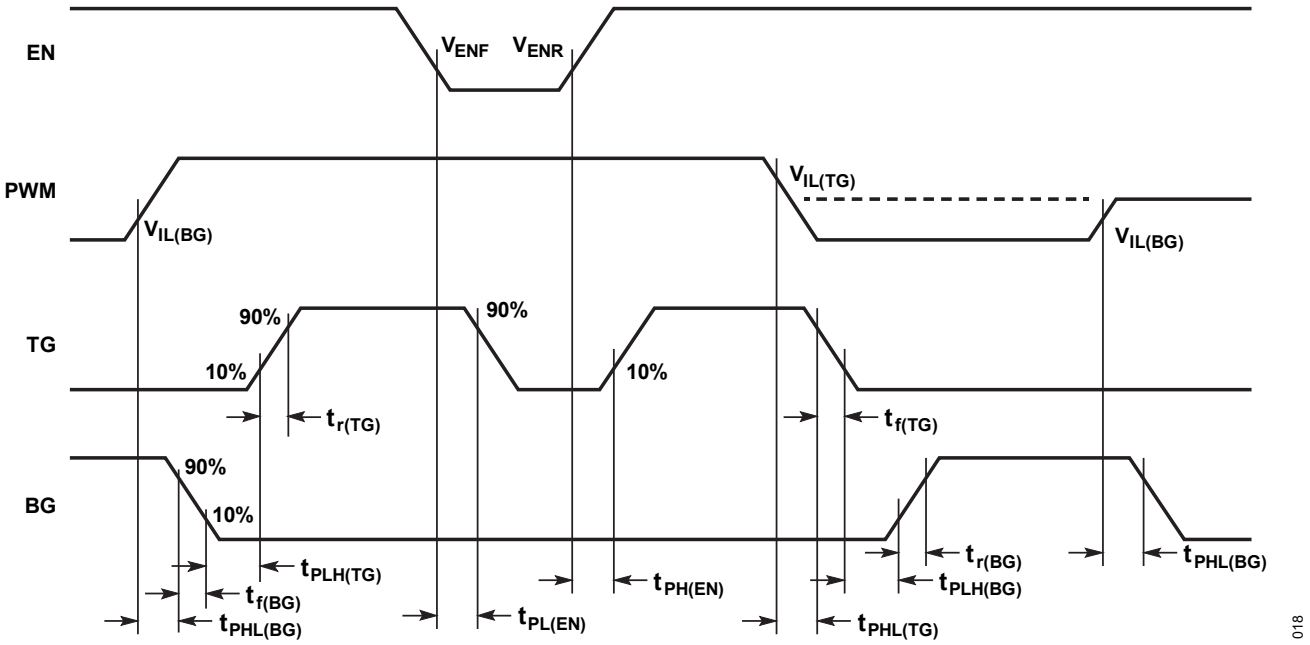


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified. All voltages are referenced to DGND unless otherwise noted.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC} Supply Voltage	-0.3V to 15V
Top Side Driver Voltage (BST)	-0.3V to 115V
SW	-10V to 100V
(BST-SW)	-0.3V to 15V
TG Voltage (Respect to SW)	-0.3V to 15V
BG Voltage (Respect to PGND)	-0.3V to 15V
EN	-0.3V to 15V
PWM	-0.3V to 6V
Operating Junction Temperature Range ([1], [2])	-40°C to 150°C
Storage Temperature Range	-65°C to 150°C

[1] The LTC7065 is guaranteed to meet performance specifications over the full -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating life-times. Operating lifetime is derated at junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

[2] T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula: $T_J = T_A + (P_D \bullet 40°C/W)$ for MSOP package.

[3] The total current includes both the current from V_{CC}/BST to PGND/SW and the current to DGND. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

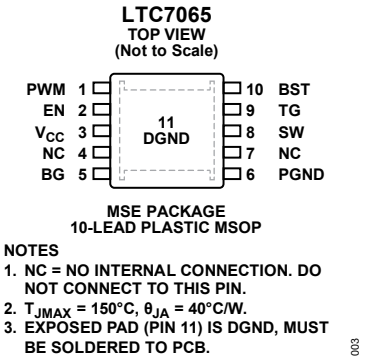


Figure 3. Pin Configurations and Function Descriptions

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
Pin 1	PWM	Three-State Gate Driver Input Signal Referenced to the DGND Pin. The TG/BG state is determined by the voltage at this pin. If this pin is floating, an internal resistor divider triggers the High-Z mode, in which both BG and TG are turned off. The trace capacitance on this pin should be minimized.
Pin 2	EN	Enable Control Input Pin. This pin is referred to the DGND. A voltage on this pin above 1.25V enables the gate drivers. The TG and BG pins are both in the low state if this pin is logic low.
Pin 3	V_{CC}	V_{CC} Supply. The bottom gate driver is powered from the V_{CC} supply. An internal 4.5V supply is generated from the V_{CC} supply to power most of the internal circuitry. A bypass capacitor with a minimum value of 4.7µF low ESR tantalum or ceramic capacitor should be tied between this pin and PGND.
Pin 4 and 7	NC	No Internal Connection. Always keep this pin floating. It is intentionally skipped to isolate adjacent high voltage pins.
Pin 5	BG	Bottom MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between V_{CC} and PGND pins.
Pin 6	PGND	Power Ground Pin. Connect this pin closely to the source of the bottom N-channel MOSFETs.
Pin 8	SW	Top MOSFET Driver Return. The top gate driver is biased between BST and the SW pin. Kelvin connect the SW pin to the top MOSFET source pin for high noise immunity.
Pin 9	TG	Top MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between the BST and SW pins.
Pin 10	BST	Top MOSFET Driver Supply. The top MOSFET gate driver is biased between this pin and the SW pin. An external capacitor should be tied between this pin and the SW pin and placed close to the IC.
Pin 11	DGND	Signal Ground Pin. Connect this pin closely to the negative terminals of Vcc bypassing capacitors. All small-signal components should also connect to this ground. This exposed pad is also connected to PGND and must be soldered to the PCB ground for electrical contact and for rated thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

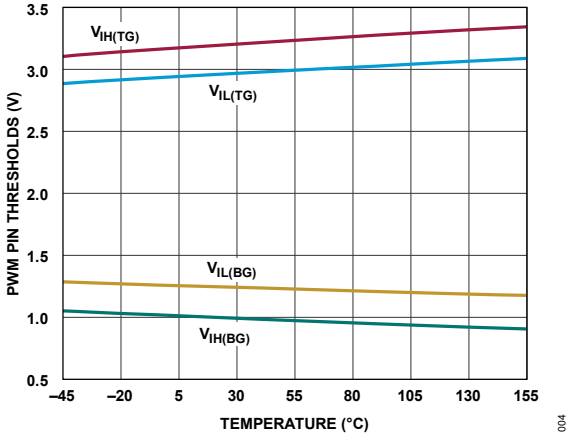


Figure 4. PWM Pin Thresholds vs. Temperature

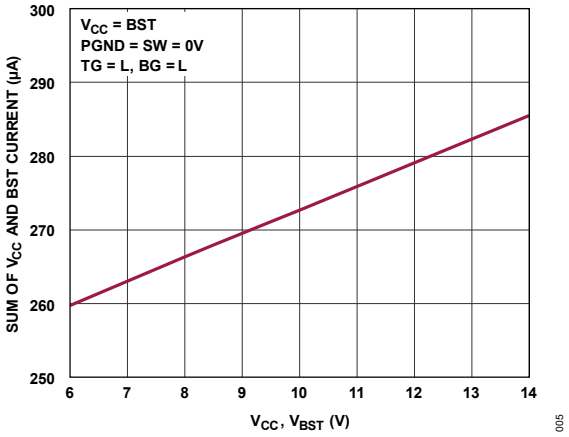


Figure 5. Total Supply Current vs. Supply Voltage

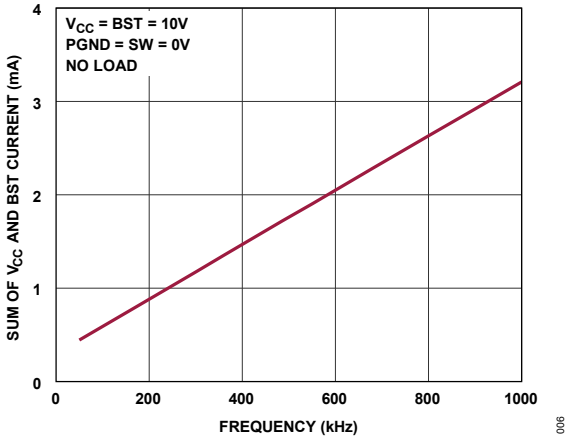


Figure 6. Total Supply Current vs. Input Frequency

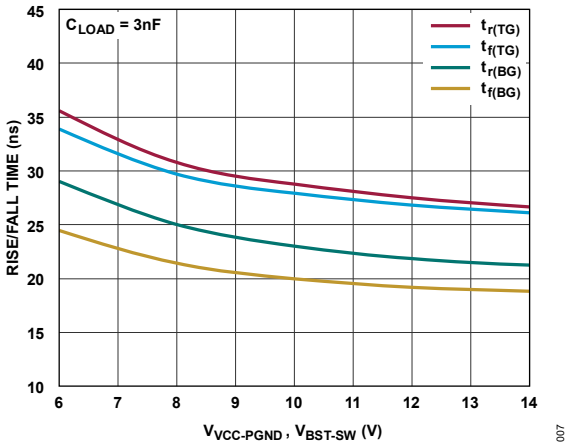


Figure 7. Rise and Fall Time vs. Driver Supply Voltage

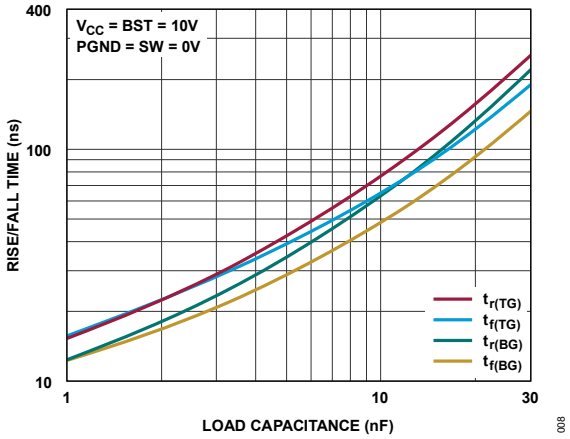


Figure 8. Rise and Fall Time vs. Load Capcitance

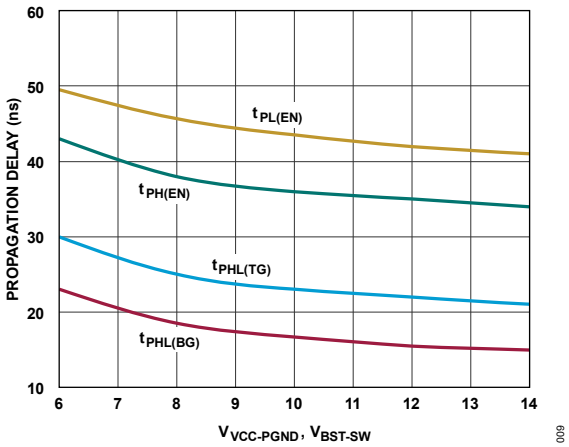


Figure 9. Propagation Delay vs. Driver Supply Voltage

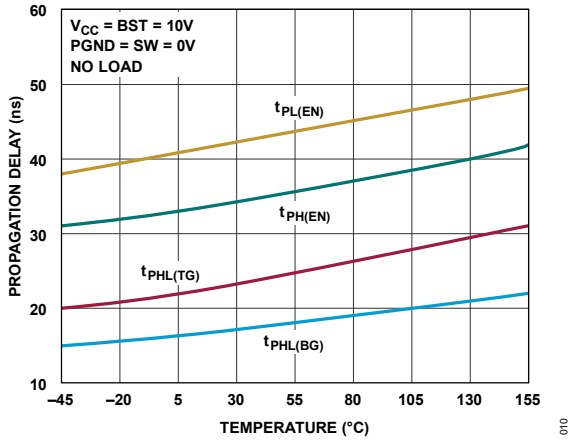


Figure 10. Propagation Delay vs. Temperature

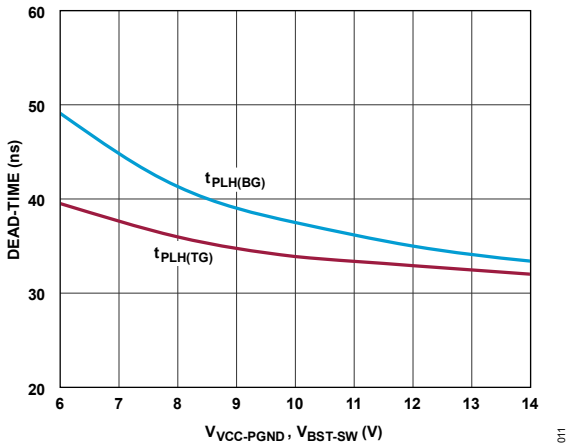


Figure 11. Dead-Time vs. Driver Supply

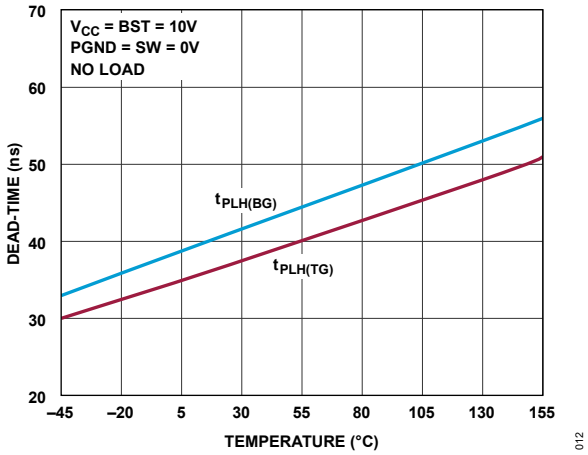


Figure 12. Dead-Time vs. Temperature

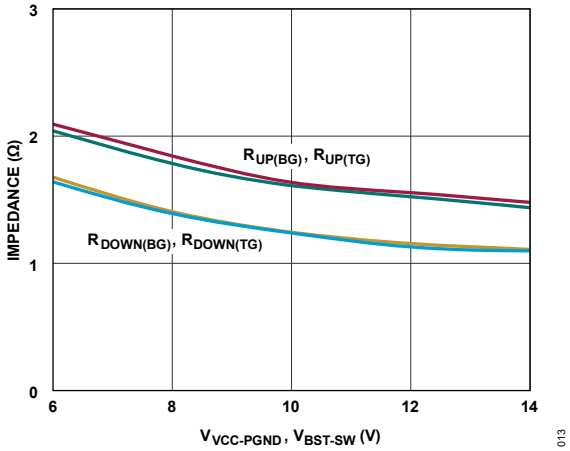


Figure 13. TG/BG Pull-Up and Pull-Down Resistance vs. Driver Supply Voltage

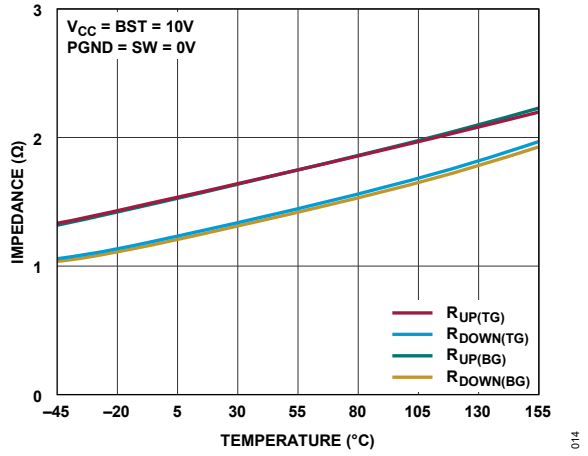


Figure 14.TG/BG Pull-Up and Pull-Down Resistance vs. Temperature

BLOCK DIAGRAM

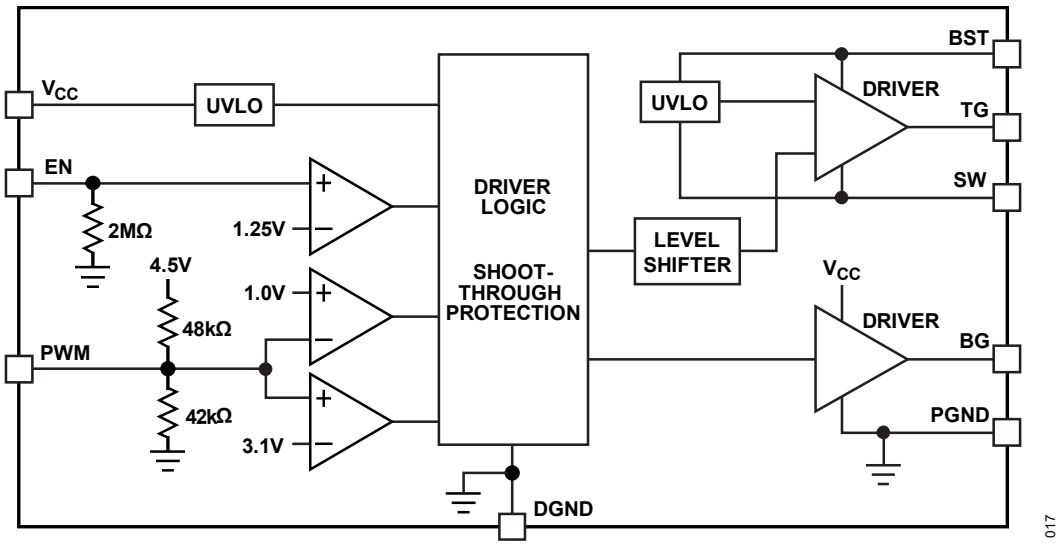


Figure 15. Block Diagram

THEORY OF OPERATION

Overview

The LTC7065 receives a ground-referenced, low voltage digital PWM signal to drive two N-channel power MOSFETs in a half-bridge configuration. The gate of the low-side MOSFET is driven high or low, swinging between V_{CC} and PGND, depending on the state of the PWM pin. Similarly, the gate of the high-side MOSFET is driven complementary to the low side MOSFET, swinging between BST and SW.

V_{cc} Supply

V_{CC} is the power supply for LTC7065. The bottom gate driver is powered from the V_{CC} supply. An internal 4.5V supply is generated from the V_{CC} supply to power the internal circuits referred to DGND. V_{CC} is independent of V_{IN}.

Input Stage (PWM, EN)

The LTC7065 employs a three-state PWM input with fixed transition thresholds. The relationship between the transition thresholds and the three input states of the LTC7065 is illustrated in *Figure 16*. When the voltage on PWM is greater than the threshold $V_{IH(TG)}$, TG is pulled up to BST, turning the high-side MOSFET on. This MOSFET will stay on until PWM falls below $V_{IL(TG)}$. Similarly, when PWM is less than $V_{IH(BG)}$, BG is pulled up to V_{CC}, turning the low-side MOSFET on. BG will stay until PWM increases above the threshold $V_{IL(BG)}$.

The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to the noise during switch transitions. However, care should be taken to keep noise from coupling into the PWM pin, particularly in high frequency, high voltage applications.

The thresholds are positioned to allow for a region in which both BG and TG are low. An internal resistor divider sets the PWM pin voltage into this region if the signal driving the PWM pin goes into a high impedance state.

The EN pin can also be used to keep both BG and TG low if the high impedance state is not available from the PWM driving signal. Driving the EN pin low keeps both TG and BG off. Driving the EN pin high enables TG and BG switching based on the PWM input. There is an internal 2MΩ pull-down resistor from the EN pin to DGND, keeping the EN default state low if its input is not driven.

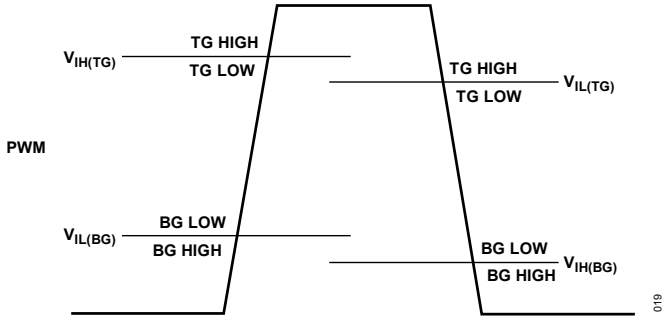


Figure 16. Three-State PWM Operation

Output Stage

A simplified version of the LTC7065's output stage is shown in *Figure 17*. The pull-up device is a PMOS with a typical 1.6Ω $R_{DS(ON)}$, and the pull-down device is a NMOS with a typical 1.3Ω $R_{DS(ON)}$. The bottom driver supply voltage ranges from 6V to 14V. The wide top driver supply voltage ranges from 4V to 14V. The wide driver supply voltage enables the driving of different power MOSFETs, such as logic level or high threshold MOSFETs. However, the LTC7065 is optimized for higher threshold MOSFETs (e.g., BST - SW = 10V and V_{CC} - PGND = 10V). The driver output pull-up and pull-down resistance may increase with a lower driver supply voltage.

Since the power MOSFETs generally account for the majority of the power loss in a converter, it is important to turn them on and off quickly, thereby minimizing the transition time and power loss. The LTC7065's typical 1.6Ω pull-up resistance and 1.3Ω pull-down resistance are equivalent to 2.6A peak pull-up current and 3.6A peak pull-down current at a 10V driver supply. At this supply voltage, both BG and TG can produce a rapid turn-on transition for the MOSFETs with the capability of driving a 3nF load with a 23ns rise time for BG and a 29ns rise time for TG.

Furthermore, a strong pull-down on the driver outputs prevents cross-conduction current. For example, in the half-bridge configuration shown in *Figure 17*, when BG turns the low-side power MOSFET off and TG turns the high-side power MOSFET on, the voltage on the SW pin could rise to V_{IN} very rapidly. This high frequency positive voltage transient will couple through the C_{GD} capacitance of the low-side power MOSFET to the BG pin. If the BG pin is not held down sufficiently, the voltage on the BG pin will rise above the threshold voltage of the low-side power MOSFET, momentarily turning it back on. As a result, both the high-side and low-side MOSFETs will be conducting, which will cause significant cross-conduction current to flow through the MOSFETs from V_{IN} to ground, thereby incurring substantial power loss and potentially damaging the MOSFETs. For this reason, short PCB traces for the BG and TG pins, which minimize parasitic inductances, are recommended.

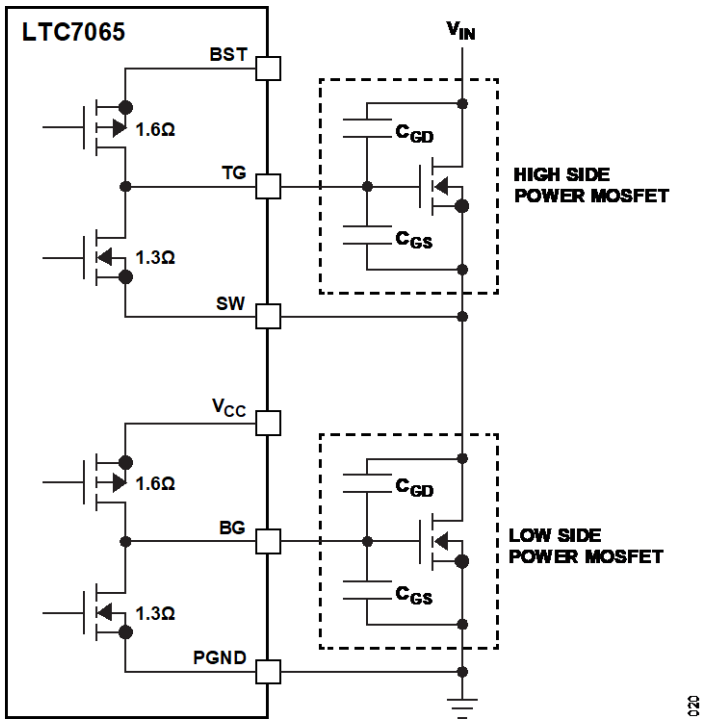


Figure 17. Simplified Output Stage in Half-Bridge Configuration

Protection Circuitry

When using the LTC7065, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section.

The LTC7065 contains an undervoltage lockout detector that monitors the V_{CC} supply. When V_{CC} falls below 5.4V, the output pins BG and TG are pulled to PGND and SW, respectively. This turns off both the external MOSFETs. When V_{CC} reaches an adequate supply voltage, normal operation will resume.

Additional undervoltage lockout circuitry is included in the top gate driver supply. The TG will be pulled down to SW when the floating voltage from BST to SW is less than 3.4V. Both V_{CC} and BST-SW undervoltage lockout circuits have hysteresis.

The normal operation and undervoltage logic are shown in *Table 4*.

Table 4. Normal Operation and Undervoltage Logic

PWM	EN	V_{CC} UVLO	(BST-SW) UVLO	TG	BG
X	L	X	X	L	L
X	X	Y	X	L	L
L	H	N	X	L	H
H	H	N	N	H	L
H	H	N	Y	L	L
HIGH-Z	X	X	X	L	L

Note: X means Don't Care, H means High, L means Low, Y means Yes, and N means No.

Adaptive Shoot-Through Protection

Internal adaptive shoot-through protection circuitry monitors the voltage on the external MOSFETs to ensure that they do not conduct simultaneously. The LTC7065 does not allow the bottom MOSFET gate (BG) to turn on until the gate-source voltage on the top MOSFET (TG-SW) is sufficiently low, and vice versa. This feature improves efficiency and reliability by eliminating the potential large shoot-through current through the MOSFETs during switching transitions.

APPLICATIONS INFORMATION

Bootstrapped Supply (BST-SW)

The BST-SW supply of the LTC7065 is a bootstrapped supply. An external boost capacitor, C_B, connected between BST and SW, supplies the high-side MOSFET gate driver voltage. When the external high-side MOSFET is turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns it on.

The charge to turn on the external MOSFET is referred to gate charge, Q_G, and is typically specified in the external MOSFET data sheet. The boost capacitor, C_B, needs to have at least 10 times the gate charge to turn on the external high-side MOSFET fully. Gate charge can range from 5nC to hundreds of nC and is influenced by the gate drive level and type of external MOSFET used. For most applications, a capacitor value of 0.1µF for the C_B will be sufficient. However, if multiple MOSFETs are paralleled and driven by the LTC7065, the C_B needs to be increased correspondingly, and the following relationship for the C_B should be maintained:

$$C_B > \frac{10 \bullet \text{External MOSFET } Q_G}{1V} \quad (1)$$

An external supply, typically V_{CC} connected through a Schottky diode, is required to keep the C_B charged. The LTC7065 does not charge the C_B and always discharges the C_B. When the TG is high, the total current from BST to SW is typically 105µA; when the TG is low, the total current from BST is typically 9µA.

Power Dissipation

To ensure proper operation and long-term reliability, the LTC7065 must not operate beyond its maximum temperature rating. The package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA}) \quad (2)$$

where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching, and capacitive load power losses.

$P_D = P_{DC} + P_{AC} + P_{QG}$

where:

P_{DC} = quiescent power loss

P_{AC} = internal switching loss at input frequency f_{IN}

P_{QG} = loss due to turning on and off external

MOSEFT with gate charge Q_G at frequency f_{IN}

The LTC7065 consumes very little quiescent current. The DC power loss at V_{CC} = 10V is only (10V)(0.15mA) = 1.5mW.

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load is shown in the Typical Performance Characteristics plot of Total Supply Current vs. Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on BG and TG at switching frequency f_{IN}, the load losses would be.

$$P_{CLOAD} = (C_{LOAD})(f_{IN})[(V_{BST-SW})^2 + (V_{VCC-PGND})^2] \quad (3)$$

In a typical synchronous buck configuration, the V_{CC} is connected to the power for the bottom MOSFET driver. V_{BST-SW} is equal to $V_{CC} - V_D$, where V_D is the forward voltage drop of the external Schottky diode between V_{CC} and BST. If this drop is small relative V_{CC}, the load losses can be approximated as follows:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2 \quad (4)$$

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G. The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs. V_{GS} curves. For identical MOSFETs on BG and TG:

$$P_{QG} \approx 2(Q_G)(f_{IN})(V_{CC}) \quad (5)$$

Bypassing and Grounding

The LTC7065 requires proper bypassing on the V_{CC} and V_{BST-SW} supplies due to their high-speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimal performance for the LTC7065:

- Mount the bypass capacitors as close as possible between the V_{CC} and PGND pins and the BST and SW pins. The leads should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground place to reduce any ground drop and stray capacitance. Remember that the LTC7065 switches have greater than 3A peak currents, and any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Kelvin connect the TG pin to the top MOSFET gate and the SW pin to the top MOSFET source. Kelvin connect the BG pin to the bottom MOSFET gate and the PGND to the bottom MOSFET source. Keep the copper trace between the driver output pin and the load short and wide.

- Be sure to solder the Exposed Pad on the back side of the LTC7065 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than specified for the packages.

TYPICAL APPLICATION

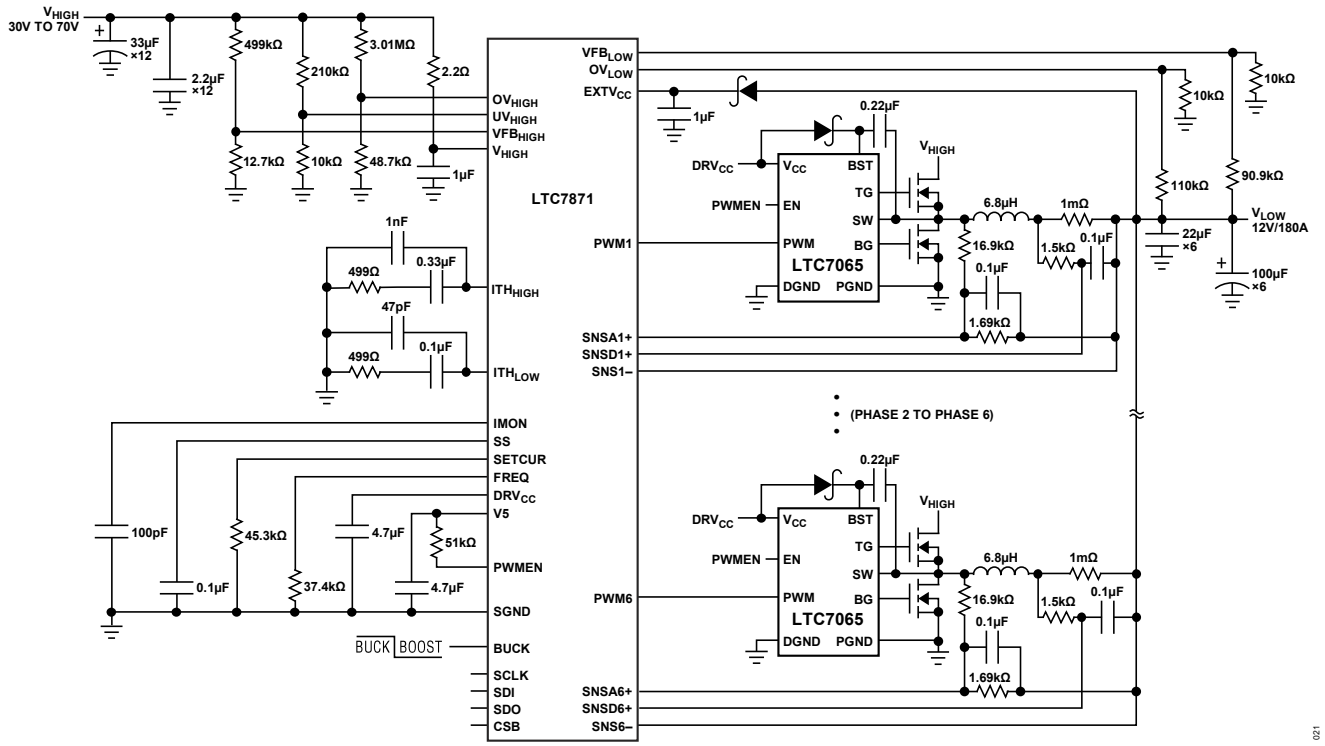


Figure 18. 6-Phase 12V/180A Converter with the LTC7065 and MOSFETs Using LTC7871

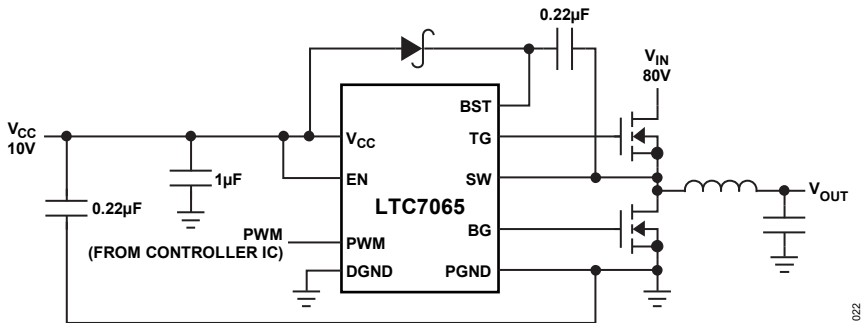


Figure 19. High Input Voltage Buck Converter

ORDERING GUIDE

Table 5. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7065RMSE#PBF	LTC7065RMSE#TRPBF	LTHRG	10-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

The LTC7065 is guaranteed to meet performance specifications over the full -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating life-times. Operating lifetime is derated at junction temperatures greater than 125°C.

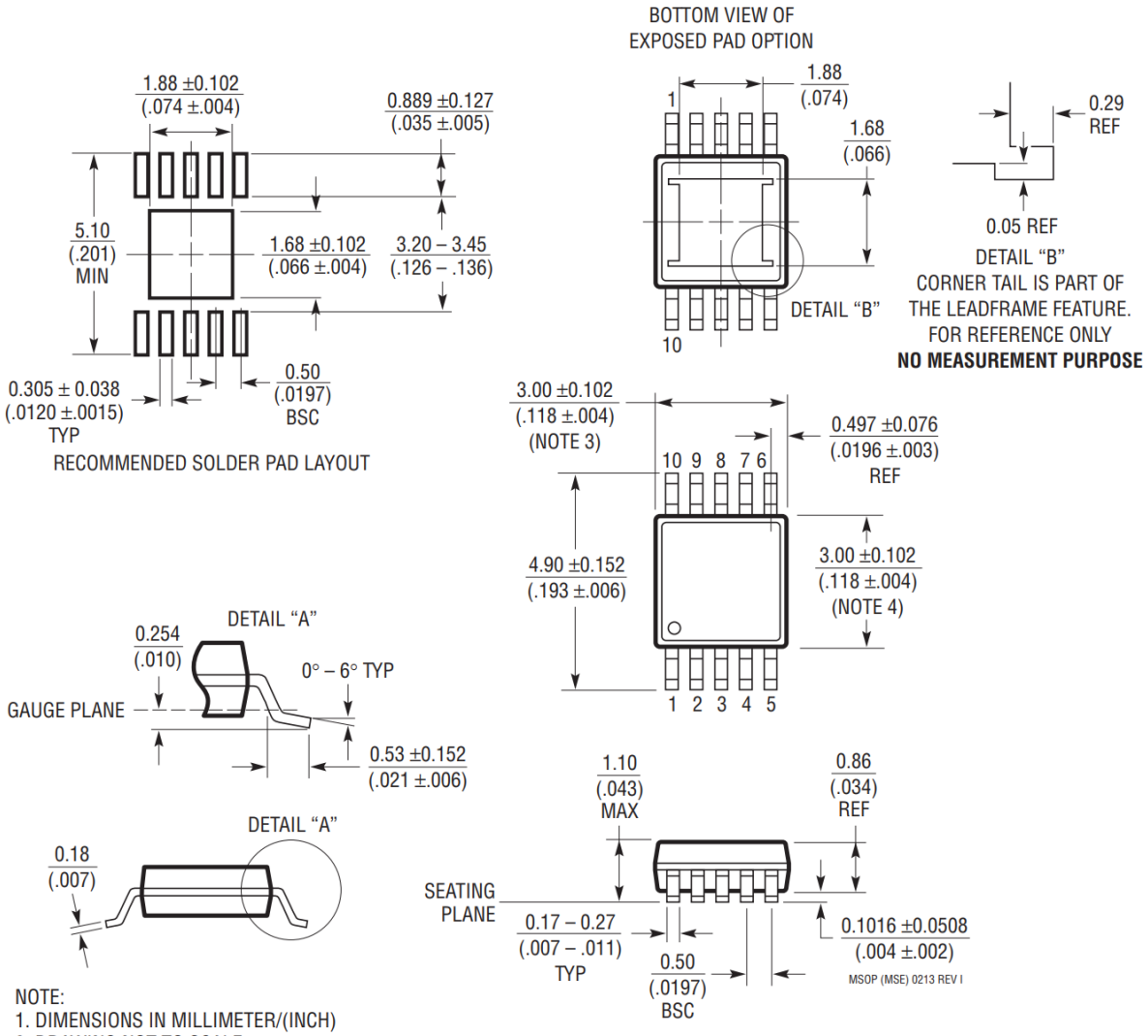
Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7060	100V Half-Bridge MOSFET Driver with Floating Grounds and Programmable Dead-Time and shoot-through protection	Up to 100V Supply Voltage, $6V \le V_{CC} \le 14V$, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Three-State PWM Input with Enable Pin, Thermally Enhanced MSOP-12
LTC7061	100V Half-Bridge MOSFET Driver with Floating Grounds and Programmable Dead-Time and shoot-through protection	Up to 100V Supply Voltage, $6V \le V_{CC} \le 14V$, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Dual PWM Inputs, Thermally Enhanced MSOP-12
LTC7062	100V Dual High-Side MOSFET Gate Driver with Floating Ground Capability	Up to 100V Supply Voltage, Shoot-Through Protection is Disabled which allows Both MOSFETs to Turn-on at the same time
LTC7063	150V Half-Bridge Driver with Floating Grounds and Adjustable Dead-Time	Up to 150V Supply Voltage, $6V \le V_{CC} \le 14V$, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Three-State PWM Input with Enable Pin, Thermally Enhanced MSOP-12
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, $4V \le V_{CC} \le 6.5V$, 3.2A Peak Pull-Up/4.5A Peak Pull-Down
LTC4442/LTC4442-1	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, $6V \le V_{CC} \le 9.5V$, 2.4A Peak Pull-Up/5A Peak Pull-Down
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V Supply Voltage, $7.2V \le V_{CC} \le 13.5V$, 2.5A Peak Pull-Up/3A Peak Pull-Down

OUTLINE DIMENSIONS

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.