Flip-Chip, Silicon Digital Step Attenuator, 1 GHz to 72 GHz

FEATURES

- Usable frequency range: 1 GHz to 72 GHz
- Attenuation range: 4 dB steps to 12 dB
- Bidirectional operation
- Low insertion loss
  - 0.9 dB up to 18 GHz
  - 1.3 dB up to 40 GHz
  - 2.1 dB up to 67 GHz
  - 3.0 dB up to 72 GHz
- Typical step error
  - ±0.50 dB up to 50 GHz
  - ±0.75 dB up to 72 GHz
- High input linearity
  - P0.1dB: >24 dBm typical
  - IP3: >45 dBm typical
- High RF input power handling
  - Through path: 24 dBm
  - Hot switching: TBD dBm
- No low frequency spurious signals
- Parallel mode control, CMOS and LVTTL compatible
- RF switching speed (50% V_{CTRL} to 10/90% of RF output): 10 ns
- 14-ball, 1.940 mm × 1.160 mm, bumped bare die sales

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

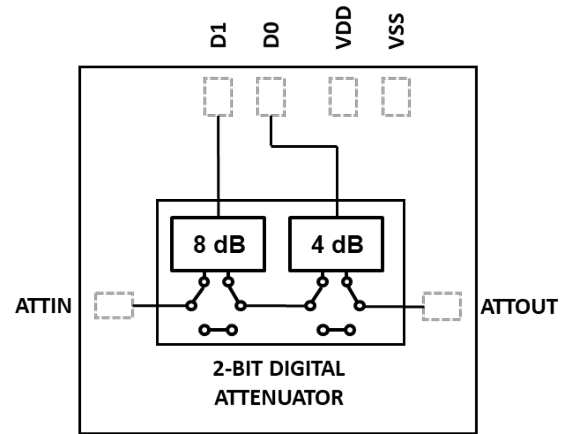

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5476 is a silicon, 2-bit digital attenuator with 12 dB attenuation control range in 4 dB steps.

The ADRF5476 is specified from 1 GHz to 72 GHz with less than 3.0 dB of insertion loss and with ±0.75 dB step error at 72 GHz. The device can operate bidirectionally, the ATTIN and ATTOUT ports of the ADRF5476 have an RF power handling capability of 24 dBm average and 24 dBm peak for all states.

The ADRF5476 draws a low current of 120 μA on the positive supply of +3.3 V and 520 μA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5476 RF ports are designed to match a characteristic impedance of 50 Ω.

The ADRF5476 is a 14-ball, 1.940 mm × 1.160 mm, bumped bare die sales and can operate between −40°C to +105°C.

Rev. PrF

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, D0 = 0 V or 3.3 V, D1 = 0 V or 3.3 V, T_A = 25°C, and it is a 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.1		72	GHz
INSERTION LOSS	10 MHz to 18 GHz		0.9		dB
	18 GHz to 40 GHz		1.3		dB
	40 GHz to 55 GHz		1.6		dB
	55 GHz to 67 GHz		2.1		dB
	67 GHz to 72 GHz		3.0		dB
RETURN LOSS	ATTIN and ATTOUT, all attenuation states				
	10 MHz to 18 GHz		17		dB
	18 GHz to 40 GHz		16		dB
	40 GHz to 55 GHz		16		dB
	55 GHz to 67 GHz		15		dB
	67 GHz to 72 GHz		15		dB
ATTENUATION					
Range	Between minimum and maximum attenuation states		12		dB
Step Size	Between any successive attenuation states		4		dB
Accuracy	Referenced to insertion loss				
	10 MHz to 18 GHz		±(0.3 + 3% of state)		dB
	18 GHz to 40 GHz		±(0.5 + 5% of state)		dB
	40 GHz to 55 GHz		±(0.5 + 5% of state)		dB
	55 GHz to 67 GHz		±(0.5 + 5% of state)		dB
	67 GHz to 72 GHz		±(0.5 + 5% of state)		dB
Step Error	Between any successive state				
	10 MHz to 18 GHz		±0.20		dB
	18 GHz to 40 GHz		±0.40		dB
	40 GHz to 55 GHz		±0.50		dB
	55 GHz to 67 GHz		±0.50		dB
	67 GHz to 72 GHz		±0.75		dB
RELATIVE PHASE	Referenced to insertion loss				
	10 MHz to 18 GHz		14		Degrees
	18 GHz to 40 GHz		34		Degrees
	40 GHz to 55 GHz		48		Degrees
	55 GHz to 67 GHz		56		Degrees
	67 GHz to 72 GHz		57		Degrees
SWITCHING CHARACTERISTICS	All attenuation states at input power = 10 dBm				
Rise and Fall Time (t_{RISE} and t_{FALL})	10% to 90% of RF output		5		ns
On and Off Time (t_{ON} and t_{OFF})	50% triggered control to 90% of RF output		10		ns
RF Amplitude Settling Time					
0.1 dB	50% triggered control to 0.1 dB of final RF output		55		ns
0.05 dB	50% triggered control to 0.05 dB of final RF output		70		ns
RF Phase Settling Time	f = 40 GHz				
5°	50% triggered control to 5° of final RF output		34		ns
1°	50% triggered control to 1° of final RF output		40		ns
INPUT LINEARITY[1]	1 GHz to 72 GHz				
0.1 dB Power Compression (P0.1dB)			>24		dBm

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
1 dB Power Compression (P1dB)			>24		dBm
Third-Order Intercept (IP3)	Two-tone input power = 10 dBm per tone, Δf = 1 MHz, all attenuation states		>45		dBm
DIGITAL CONTROL INPUTS	D1 and D0				
Voltage					
Low (V_{INL})		0		0.8	V
High (V_{INH})		1.2		3.3	V
Current					
Low (I_{INL})			−10		μA
High (I_{INH})			<1		μA
SUPPLY CURRENT					
Positive Supply Current (I_{DD})	VDD pin				
Bias Low	D1 and D0 = 0 V		124		μA
Bias High	D1 and D0 = 3.3 V		104		μA
Negative Supply Current (I_{SS})	VSS pin		−528		μA
RECOMMENDED OPERATING CONDITIONS					
Supply Voltage					
VDD		3.15		3.45	V
VSS		−3.45		−3.15	V
Digital Control Voltage		0		VDD	V
RF Power[2]	f = 3 GHz to 72 GHz, T_{CASE} = 85°C,[3] all attenuation states				
Input at ATTIN and ATTOUT	Steady state, average			24	dBm
	Steady state, peak			24	dBm
	Hot switching, average			24	dBm
	Hot switching, peak			24	dBm
T_{CASE}		−40		+105	°C

[1] Input linearity performance degrades over frequency

[2] For power derating over frequency, see Figure 2. Power derating is applicable for all ATTIN and ATTOUT power specifications.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input Voltage	−0.3 V to VDD + 0.3 V
RF Power[1] (f = 3 GHz to 72 GHz, T_{CASE} = 85°C[2])	
Input at ATTIN & ATTOUT	
Steady State, Average	27 dBm
Steady State, Peak	27 dBm
Hot Switching, Average	27 dBm
Hot Switching, Peak	27 dBm
RF Power Under Unbiased Condition (VDD and VSS = 0 V)	
Input at ATTIN and ATTOUT	TBD
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C
Continuous Power Dissipation (P_{DISS})	TBD W

[1] For power derating vs. frequency, see Figure 2.

[2] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CD-14-1	400	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

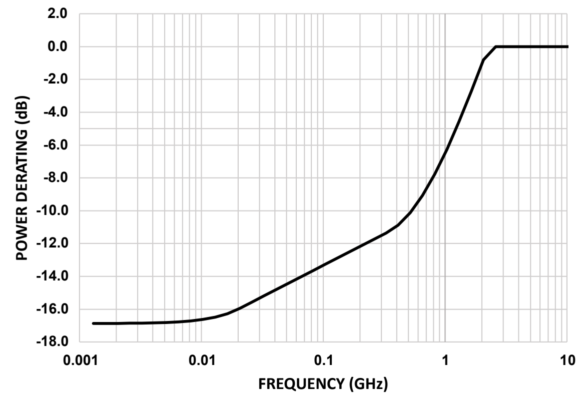

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ESDA/JEDEC JS-002.

ESD Ratings for ADRF5476

Table 4. ADRF5476, 14-Ball Bumped Bare Die Sales

ESD Model	Withstand Threshold (V)
HBM	
ATTIN and ATTOUT Pins	TBD
Supply and Control Pins	TBD
FICDM	TBD

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

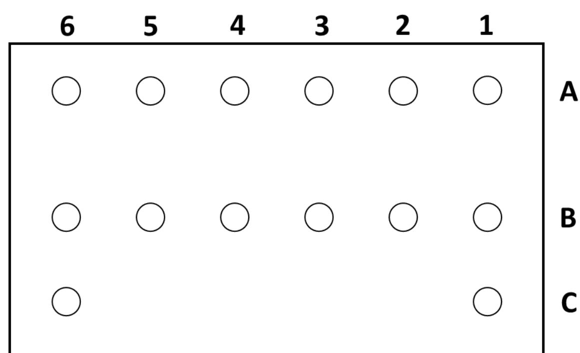

Figure 3. Pin Configuration (Bottom View—Bump Side Up)

Table 5. Pin Function Descriptions

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
A1	GND	−0.750	+0.400	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
A2	D1	−0.450	+0.400	Parallel Control Input for 8 dB Attenuator. The D1 pin is internally pulled up with 330 kΩ. See Figure 5 for the interface schematic.
A3	D0	−0.150	+0.400	Parallel Control Input for 4 dB Attenuator. This D0 pin is internally pulled up with 330 kΩ. See Figure 5 for the interface schematic.
A4	VDD	+0.150	+0.400	Positive Supply Voltage. See Figure 6 for the interface schematic.
A5	VSS	+0.450	+0.400	Negative Supply Voltage. See Figure 7 for the interface schematic.
A6	GND	+0.750	+0.400	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B1	GND	−0.750	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B2	GND	−0.450	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B3	GND	−0.150	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B4	GND	+0.150	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B5	GND	+0.450	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B6	GND	+0.750	−0.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C1	ATTIN	−0.750	−0.350	Attenuator Input. The ATTIN pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.
C6	ATTOUT	+0.750	−0.350	Attenuator Output. The ATTOUT pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 4 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

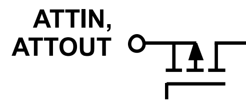

Figure 4. ATTIN, ATTOUT Interface Schematic

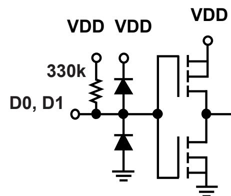

Figure 5. D0, D1 Interface Schematic

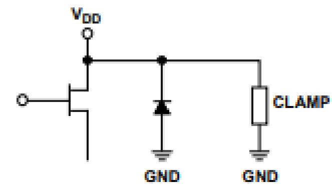

Figure 6. VDD Pin Interface Schematic

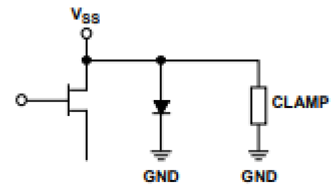

Figure 7. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = −3.3 V, D0 = 0 V or 3.3 V, D1 = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

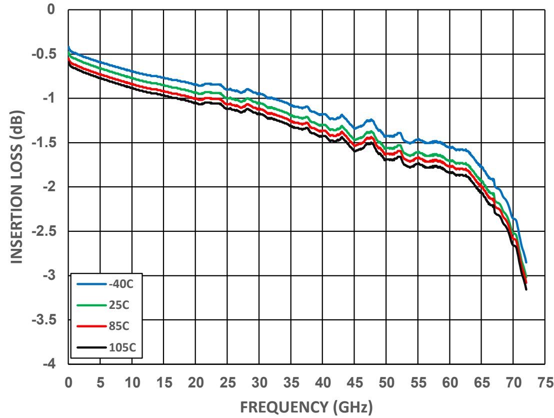

Figure 8. Insertion Loss vs. Frequency

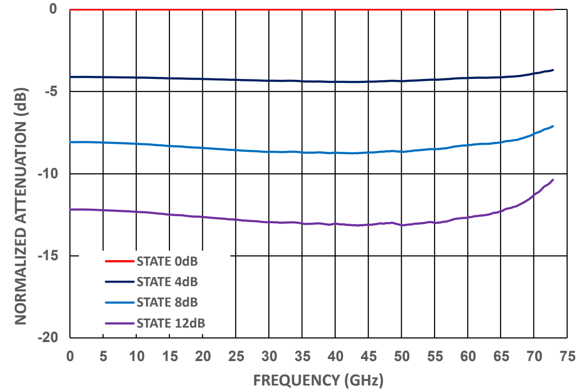

Figure 11. Normalized Attenuation vs. Frequency for All States

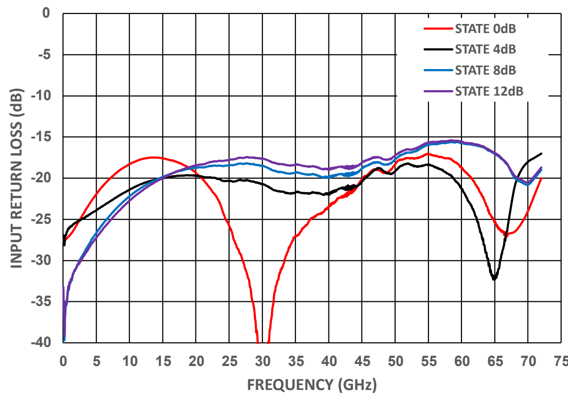

Figure 9. Input Return Loss vs. Frequency for All States

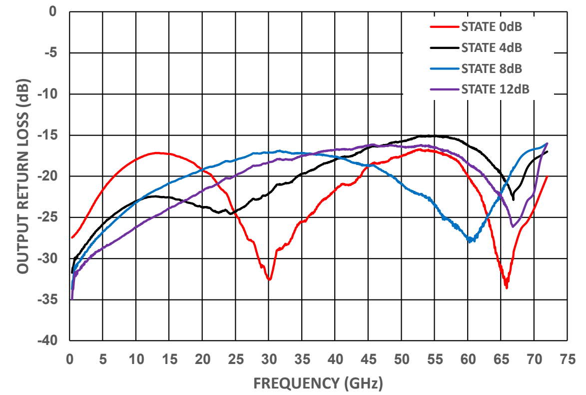

Figure 12. Output Return Loss vs. Frequency for All States

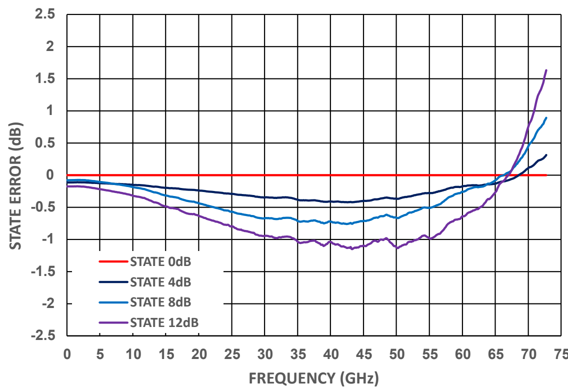

Figure 10. State Error vs. Frequency for All States

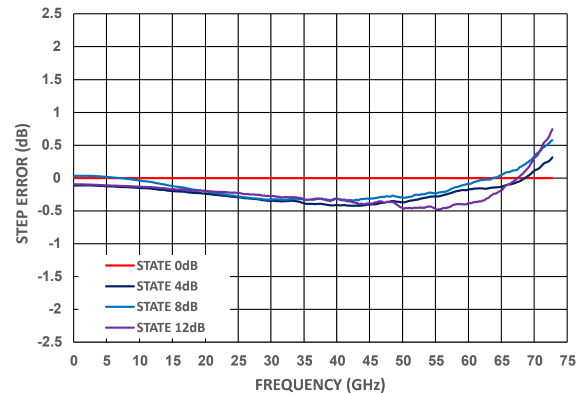

Figure 13. Step Error vs. Frequency for All States

TYPICAL PERFORMANCE CHARACTERISTICS

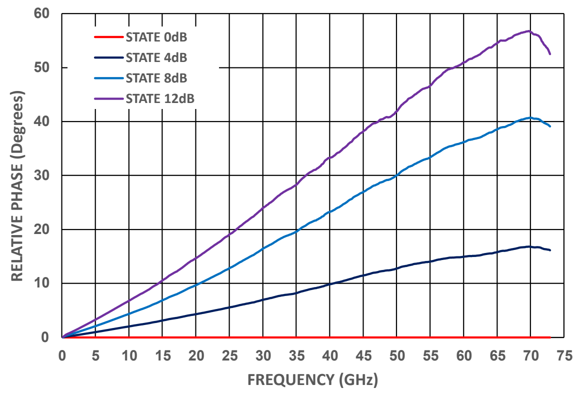

Figure 14. Relative Phase vs. Frequency for All States

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, D0 = 0 V or 3.3 V, D1 = 0 V or 3.3 V, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

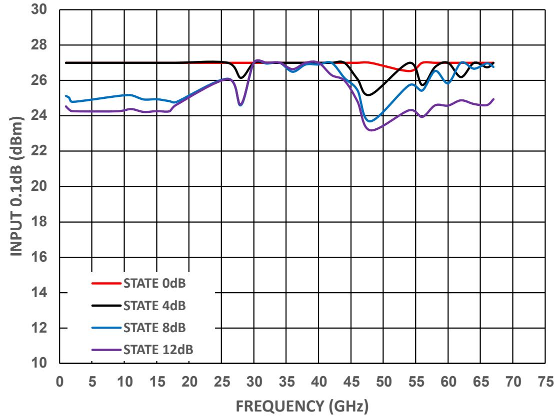

Figure 15. Input P0.1dB vs. Frequency

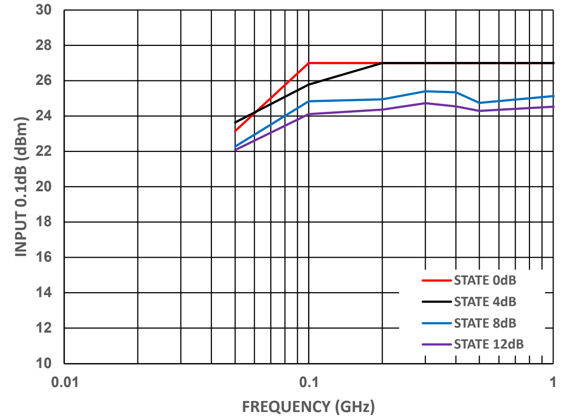

Figure 17. Input P0.1dB vs. Frequency (Low Frequency Detail)

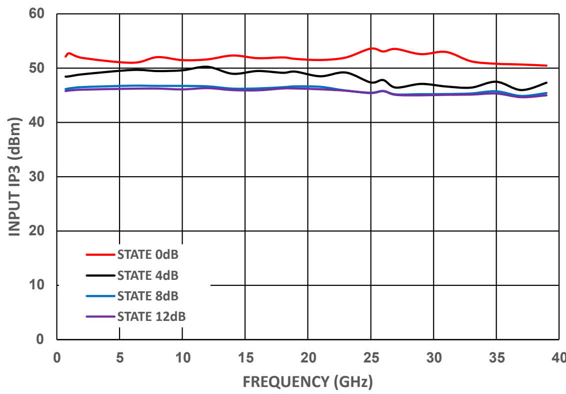

Figure 16. Input IP3 vs. Frequency

Figure 18. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5476 incorporates a 2-bit fixed attenuator array that offers an attenuation range of 12 dB in 4 dB steps. An integrated driver provides parallel mode control of the attenuator array.

The ADRF5476 has two digital control inputs, D0 and D1, to select the desired attenuation state in parallel mode. Internally, there are two 4 dB stages, and these can be controlled by the D0 and D1 pins.

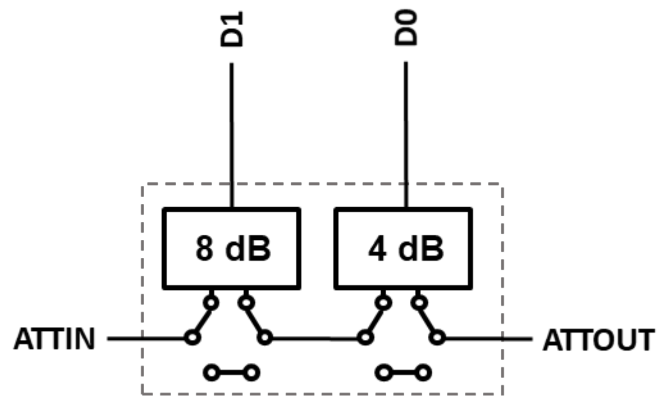

Figure 19. Simplified Circuit Diagram

POWER SUPPLY

The ADRF5476 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Power up the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply may inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin.
4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are DC-coupled to 0 V. DC blocking is not required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5476 supports bidirectional operation. The power handling of the ATTIN and ATTOUT ports are the same. Refer to the RF input power specifications in Table 1.

Table 6. Recommended Truth Table

Digital Control Input		
D1	D0	Attenuation State (dB)
Low	Low	0 (reference)
Low	High	4
High	Low	8
High	High	12

APPLICATIONS INFORMATION

The ADRF5476 has two power supply pins (VDD and VSS) and two control pins (D1 and D2). Figure 20 shows the external components and connections for the supply pin. The VDD, VSS, D1, and D2 pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to the Pin Configuration and Function Descriptions section for further details.

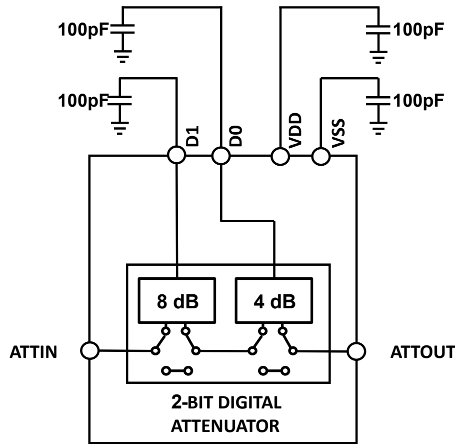

Figure 20. Recommended Schematic

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 21 shows the referenced CPWG RF trace design for an RF substrate with 6 mil thick Megtron6 2×1080 R-5775G dielectric material. The RF trace with a 300 µm width and a 300 µm clearance is recommended for a 42 µm finished copper thickness.

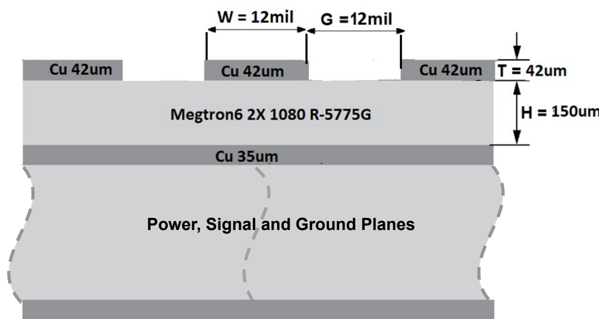

Figure 21. Probe Matrix Board Stackup

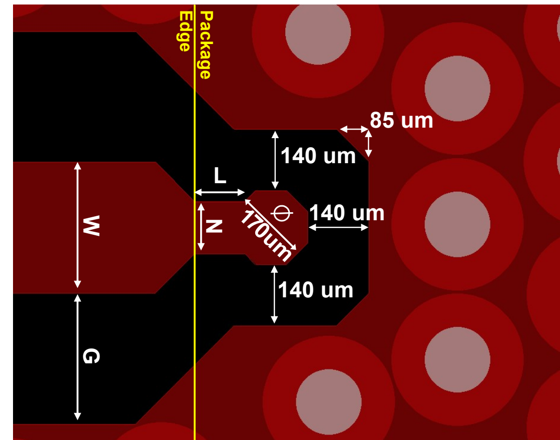

Figure 22. Recommended RF Pin Transition

Figure 22 shows the recommended layout from the RFx pins of the ADRF5476 to the 50 Ω CPWG on the referenced stackup. Signal pads have a 170 µm diameter for ease of assembly. The RF trace from the PCB pad is extended with a thinner neck for broadband tuning and tapered to RF trace with a 45° angle. The RFx pin transition of the ADRF5476 is optimized for different stackups in Table 7 for broadband performance. For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

Table 7. Recommended RFx Pin Transitions for Different Stackups

RF Stackup Height and Dielectric		RF Trace Dimensions		ADRF5476 Mnemonic	Transition Dimensions	
H (µm)	Er	W (µm)	G (µm)		N (µm)	L (µm)
85	3.02	180	250	All	120	250
100	3.34	200	225	All	120	200
115	3.40	225	250	All	120	170
125	3.00	250	225	All	170	170
150[1].	3.40	300	300	All	170	170
175	3.16	360	245	All	170	170
190	3.00	425	225	All	170	170
200	3.55	425	275	All	170	170

[1] Design reference and generic footprint

APPLICATIONS INFORMATION

DIE ASSEMBLY

The ADRF5476 complies with standard RoHS reflow assembly process and its temperature profiles. The device can be assembled with other surface-mounted technology (SMT) components in the same reflow cycle. However, the PCB must be designed according to the pick and place process.

The top copper layer of the PCB is designed for optimum RF performance where the solder mask and paste mask layers are designed for optimum assembly yield. The ground pads are drawn as solder mask defined. The signal pads are drawn as pad defined. The same solder mask and paste mask design can be used for both pads.

The ADRF5476 can also be assembled without applying a solder paste on the PCB. If no solder paste is applied, the ADRF5476 must be dipped into flux prior to placement on the PCB.

Reflow Assembly with Solder Paste

Solder mask openings of 175 µm in a square shape is recommended for signal and RF pads and 150 µm in a square shape is recommended for GND pads. Solder mask thickness must not exceed 50 µm. Paste mask is drawn circular with a 150 µm diameter. Using a stencil with 2 mil thickness and no aperture reduction yields the optimum paste mask print. In this assembly, the device does not need any flux dipping during the pick and place process.

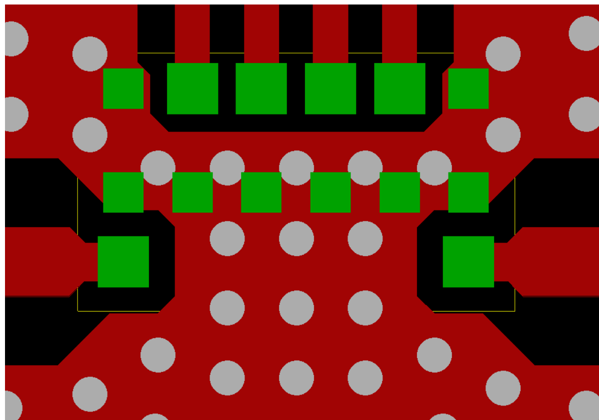

Figure 23. Recommended Footprint for Solder Paste

Reflow Assembly with Flux Dipping

Solder mask openings that are circular and 130 µm in diameter are recommended. Solder mask thickness must not exceed 50 µm. Solder paste is not applied. The ADRF5476 is dipped into flux prior to placement on the board.

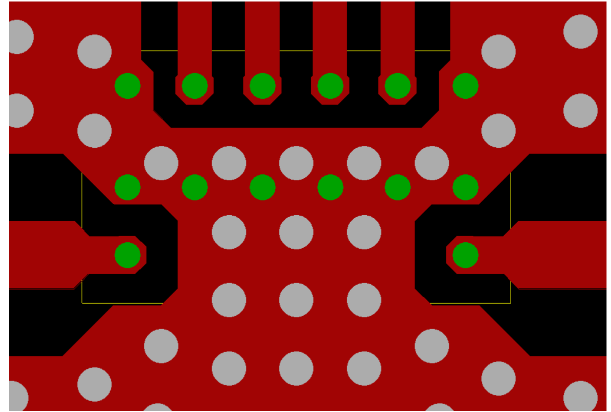

Figure 24. Recommended Footprint for Flux Dip Assembly

OUTLINE DIMENSIONS

Figure 25. 14-Ball Bumped Bare Die Sales [BUMPED_CHIP] (CD-14-1) Dimensions shown in millimeters

ANALOG DEVICES

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