Preliminary Data Sheet

ADRF5440

Flip Chip, Silicon SP4T Switch, 1 GHz to 81 GHz

FEATURES

- Usable frequency range: 1 GHz to 81 GHz
- Low insertion loss
  - 1.9 dB typical to 40 GHz
  - 3.0 dB typical to 67 GHz
  - 4.0 dB typical to 81 GHz
- High Isolation
  - 39 dB typical up to 40 GHz
  - 30 dB typical up to 67 GHz
  - 20 dB typical up to 81 GHz
- High input linearity
  - P0.1dB: 25 dBm typical
  - IP3: 47 dBm typical
- High RF input power handling
  - Through path: 24 dBm
  - Hot switching: 24 dBm
- No low frequency spurs
- CMOS/LVTTL compatible
- Fast RF switching time: 25 ns
- RF settling time (50% V_{CTRL} to 0.1 dB of final RF output): 35 ns
- Single-supply operation capability (VDD = 3.3 V , VSS = 0 V)
- 56-ball, 2.390 mm × 2.540 mm, bumped, bare die sales

APPLICATIONS

- Industrial scanners
- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

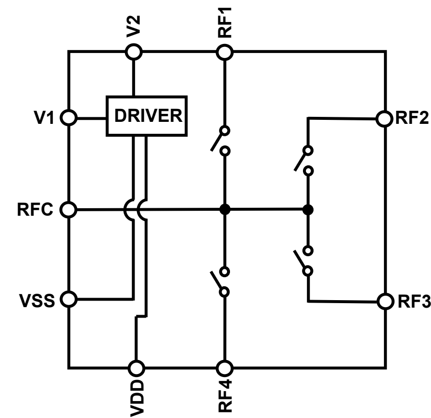

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5440 is a reflective, SP4T switch manufactured in the silicon process. This switch operates from 1 GHz to 81 GHz with better than 4.0 dB of insertion loss and 20 dB of isolation. The ADRF5440 has an RF input power handling capability of 24 dBm for the through path and 24 dBm for hot switching.

The ADRF5440 draws a low current of 145 μA on the positive supply of +3.3 V and 510 μA on negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5440 can also operate with a single positive supply voltage (VDD) applied while the negative supply voltage (VSS) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See Table 2 for more details.

The ADRF5440 RF ports are designed to match a characteristic impedance of 50 Ω. The ADRF5440 is 56-ball, 2.390 mm x 2.540 mm, bumped bare die sales and can operate between −40°C to +105°C.

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = −3.3 V, V1 = V2 = 0 V or VDD, and case temperature (T_{CASE}) = 25°C for 50 Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		81	GHz
INSERTION LOSS						
Between RFC and RFx (On)						
		100 MHz to 18 GHz		1.4		dB
		18 GHz to 40 GHz		1.9		dB
		40 GHz to 55 GHz		2.4		dB
		55 GHz to 67 GHz		3.0		dB
		67 GHz to 81 GHz		4.0		dB
RETURN LOSS						
RFC and RFx (On)						
		100 MHz to 18 GHz		17		dB
		18 GHz to 40 GHz		13		dB
		40 GHz to 55 GHz		13		dB
		55 GHz to 67 GHz		15		dB
		67 GHz to 81 GHz		12		dB
ISOLATION						
Between RFC and RFx (Off)		100 MHz to 18 GHz		45		dB
		18 GHz to 40 GHz		39		dB
		40 GHz to 55 GHz		35		dB
		55 GHz to 67 GHz		30		dB
		67 GHz to 81 GHz		20		dB
Between RFx and RFx		100 MHz to 18 GHz		43		dB
		18 GHz to 40 GHz		38		dB
		40 GHz to 55 GHz		35		dB
		55 GHz to 67 GHz		30		dB
		67 GHz to 81 GHz		15		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		5		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		25		ns
RF Settling Time						
0.1 dB		50% V_{CTRL} to 0.1 dB of final RF output		35		ns
INPUT LINEARITY[1]		1 GHz to 67 GHz				
0.1 dB Power Compression	P0.1dB			25		dBm
Third-Order Intercept	IP3	Two tone input power = 14 dBm each tone, Δf = 1 MHz		47		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			145		μA
Negative Supply Current	I_{SS}			510		μA
DIGITAL CONTROL INPUTS		V1, V2 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		μA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2]	P_{IN}	f = 3 GHz to 70 GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through connected RF1 and RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			24	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 21 to Figure 24.

[2] For power derating over frequency, see Figure 2 and Figure 3.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

VDD = 3.3 V, VSS = 0 V, V1 = 0V or VDD, V2 = 0 V or VDD, T_{CASE} = 25°C for 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		81	GHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		20		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		58		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF output		62		ns
INPUT LINEARITY		f = 1 GHz to 81 GHz				
0.1 dB Power Compression	P0.1dB			13		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, Δf = 1 MHz		41		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1]	P_{IN}	f = 3 GHz to 70 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RFx			13	dBm
Hot Switching		RF signal is applied to the RFC while switching between RFx			13	dBm

[1] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 1 dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.3 V
Digital Control Input Voltage[1]	
Voltage	−0.3 V to VDD + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[2] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 3 GHz to 70 GHz T_{CASE} = 85°C[3])	
Through Path	25 dBm
Hot Switching	25 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 3 GHz to 70 GHz, T_{CASE} = 85°C[3])	
Through Path	14 dBm
Hot Switching (RFC)	14 dBm
RF Input Power , Unbiased (V_{DD}, V_{SS} = 0 V)	14 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for dual supply and 1 dB for single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CD-56-1, Through Path	360	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

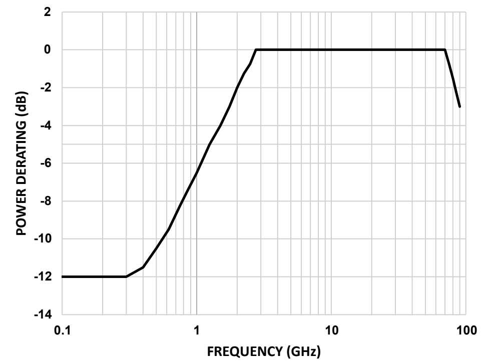


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

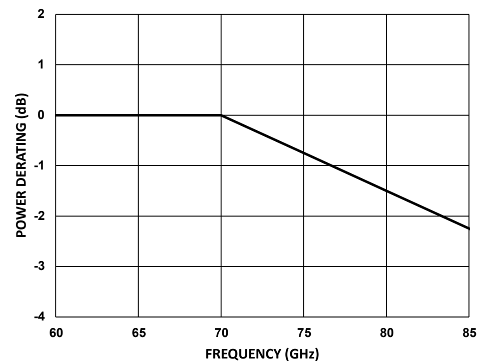


Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

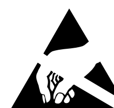
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5440

Table 5. ADRF5440, 56-Ball Bumped Flip Chip Die

ESD Model	Withstand Threshold (V)
HBM	±500 for RF Pins
	±2000 for Supply and Digital Control Pins

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

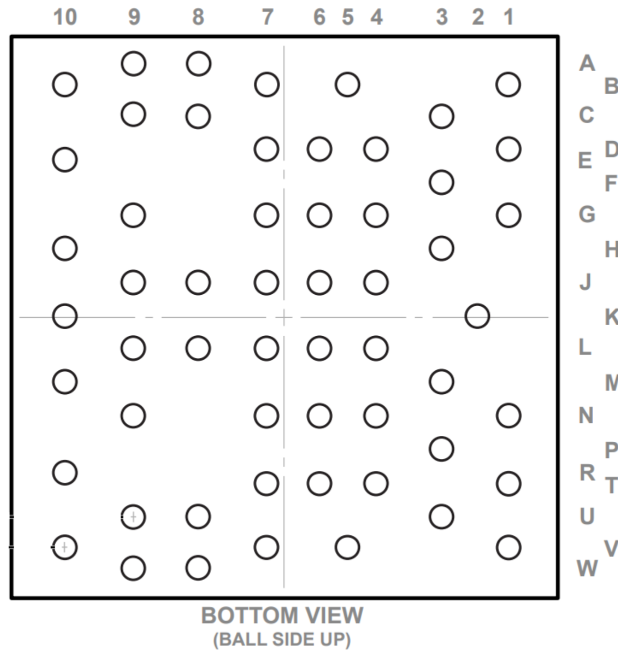


Figure 4. Pin Configuration (Bottom View—Ball Side Up)

Table 6. Pin Function Descriptions

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
A8	GND	+0.400	+1.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
A9	GND	+0.700	+1.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B1	V2	−1.0	+1.050	Control Input Voltage. See Figure 6 for the interface schematic.
B5	RF1	−0.275	+1.050	RF Port 1. The RF1 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
B7	GND	+0.100	+1.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
B10	GND	+1.000	+1.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C3	GND	−0.700	+0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C8	GND	+0.400	+0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
C9	GND	+0.700	+0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
D1	V1	−1.0	+0.750	Control Input Voltage. See Figure 6 for the interface schematic.
D4	GND	−0.400	+0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
D6	GND	−0.150	+0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
D7	GND	+0.100	+0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
E10	RF2	+1.000	+0.700	RF Port 2. The RF2 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
F3	GND	−0.700	+0.600	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G1	GND	−1.0	+0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G4	GND	−0.400	+0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G6	GND	−0.150	+0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G7	GND	+0.100	+0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
G9	GND	+0.700	+0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
H3	GND	−0.700	+0.300	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
H10	GND	+1.000	+0.300	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J4	GND	−0.400	+0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
J6	GND	−0.150	+0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J7	GND	+0.100	+0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J8	GND	+0.400	+0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
J9	GND	+0.700	+0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
K2	RFC	−0.850	+0.000	RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic.
K10	GND	+1.000	+0.000	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L4	GND	−0.400	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L6	GND	−0.150	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L7	GND	+0.100	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L8	GND	+0.400	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
L9	GND	+0.700	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
M3	GND	−0.700	−0.300	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
M10	GND	+1.000	−0.300	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N1	GND	−1.0	−0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N4	GND	−0.400	−0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N6	GND	−0.150	−0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N7	GND	+0.100	−0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
N9	GND	+0.700	−0.450	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
P3	GND	−0.700	−0.600	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
R10	RF3	+1.000	−0.700	RF Port 3. The RF3 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
T1	VSS	−1.0	−0.750	Negative Supply Voltage. See Figure 8 for the interface schematic.
T4	GND	−0.400	−0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
T6	GND	−0.150	−0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
T7	GND	+0.100	−0.750	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
U3	GND	−0.700	−0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
U8	GND	+0.400	−0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
U9	GND	+0.700	−0.900	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
V1	VDD	−1.0	−1.050	Positive Supply Voltage. See Figure 7 for the interface schematic.
V5	RF4	−0.275	−1.050	RF Port 4. The RF4 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
V7	GND	+0.100	−0.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
V10	GND	+1.000	−1.050	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
W8	GND	+0.400	−1.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.
W9	GND	+0.700	−1.150	Ground. The GND pin must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

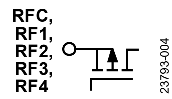


Figure 5. RFx Interface Schematic

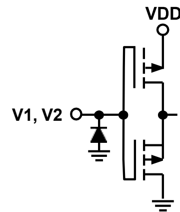


Figure 6. V1, V2 Interface Schematic

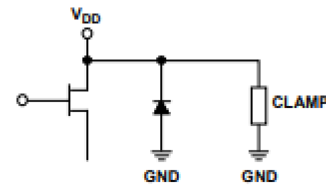


Figure 7. VDD Pin Interface Schematic

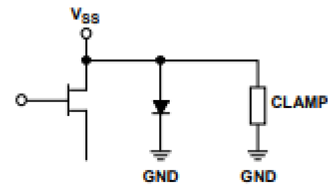


Figure 8. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 3.3 V, VSS = −3.3 V, V1 = V2 = 0 V or VDD, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. Insertion loss, return loss, and isolation are measured on the probe matrix board using ground-signal-ground (GSG) probes close to the RFx pins.

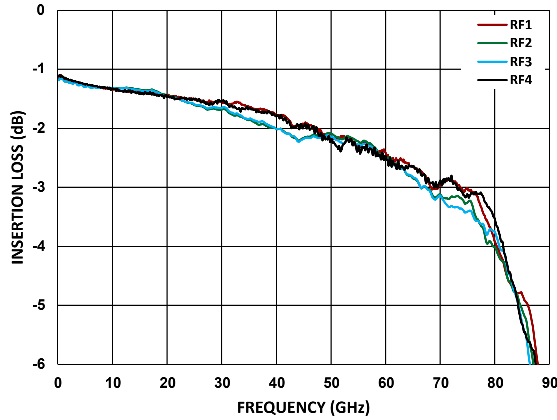


Figure 9. Insertion Loss for RFC to RFx On vs. Frequency

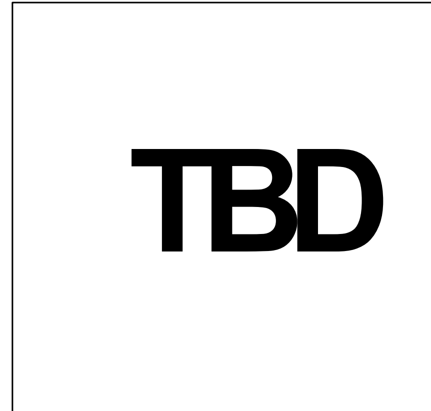


Figure 12. Insertion Loss for RFC to RF1 On vs. Frequency over Various Temperature

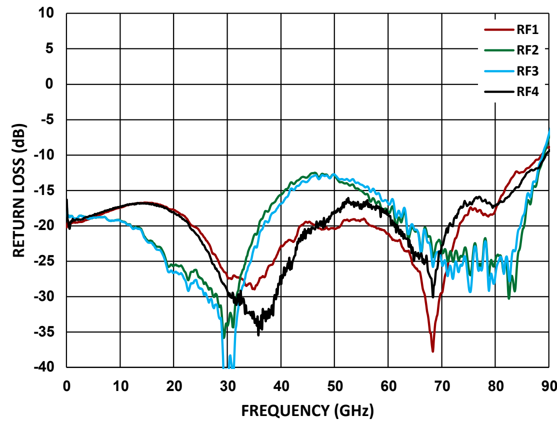


Figure 10. Return Loss for RFC when RFx Selected vs. Frequency

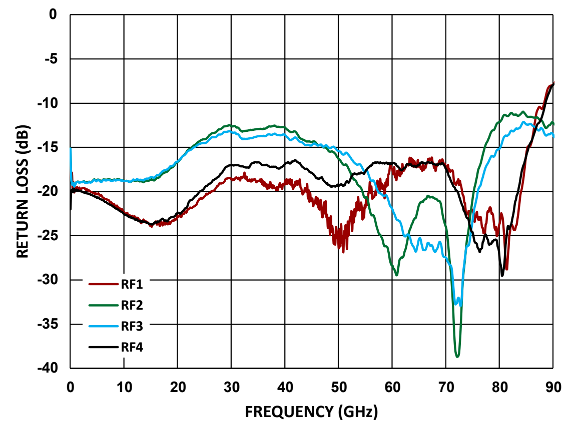


Figure 13. Return Loss for RFx Selected vs. Frequency

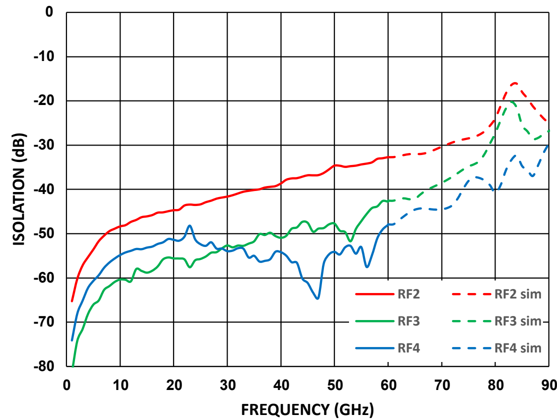


Figure 11. Isolation for RFC to RFx Off vs. Frequency, RFC to RF1 Path On

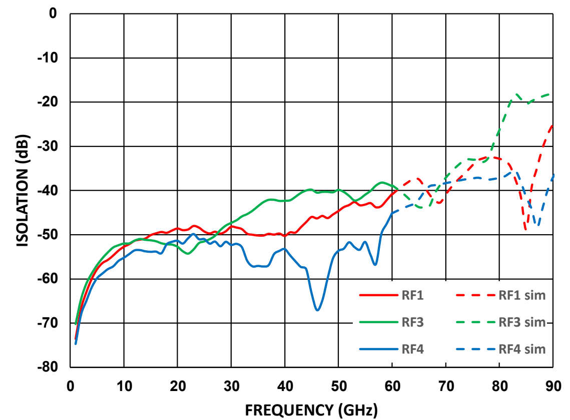


Figure 14. Isolation for RFC to RFx Off vs. Frequency, RFC to RF2 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

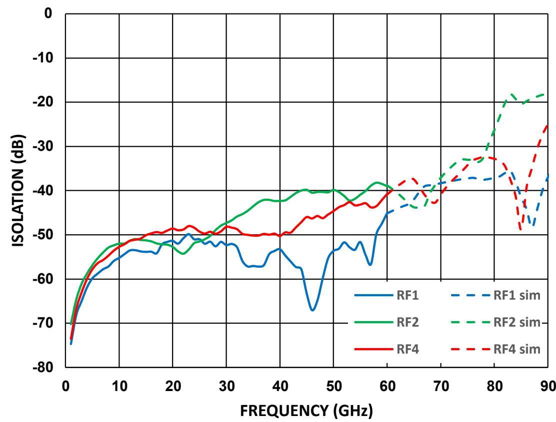


Figure 15. Isolation for RFC to RFx Off vs. Frequency, RFC to RF3 Path On

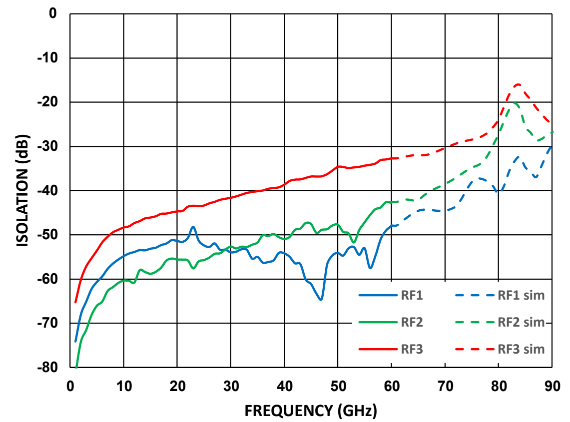


Figure 18. Isolation for RFC to RFx Off vs. Frequency, RFC to RF4 Path On

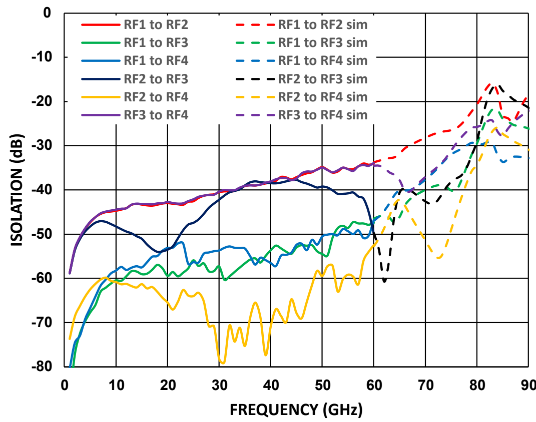


Figure 16. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path On

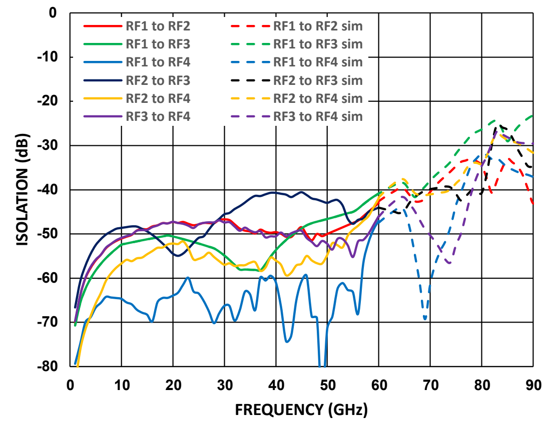


Figure 19. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path On

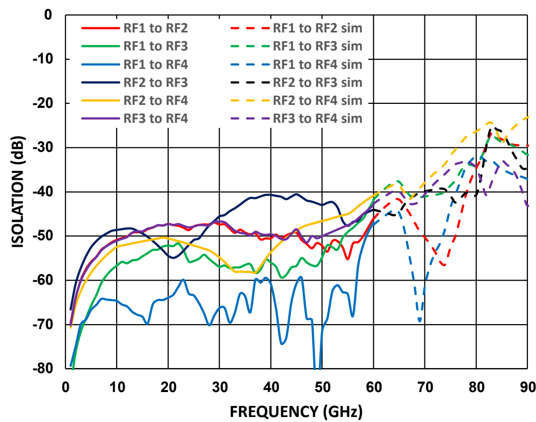


Figure 17. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path On

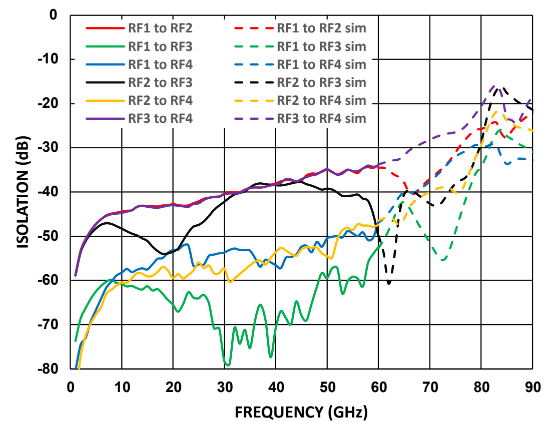


Figure 20. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 3.3 V, VSS = −3.3 V, V1 = V2 = 0 V or VDD, and T_{CASE} = 25°C for a 50 Ω system, unless otherwise noted. All of the large signal performance parameters were measured on the evaluation board.

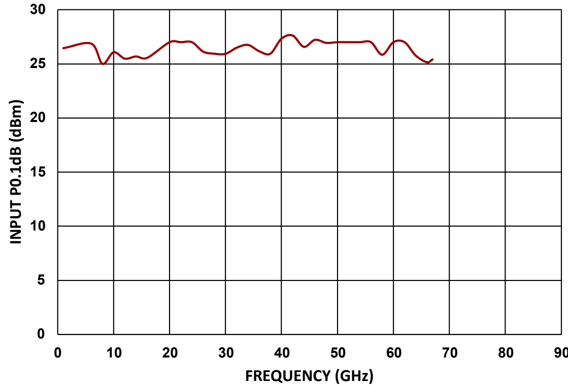


Figure 21. Input P0.1dB vs. Frequency

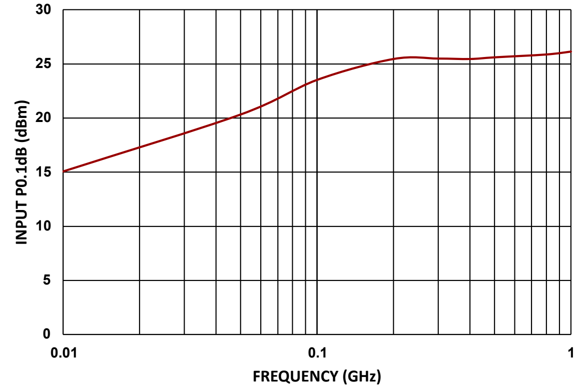


Figure 23. Input P1dB vs. Frequency (Low Frequency Detail)

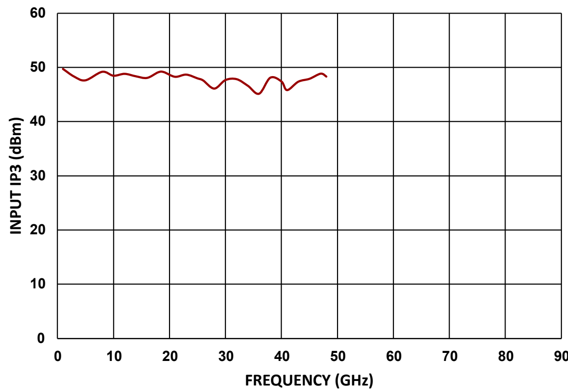


Figure 22. Input IP3 vs. Frequency

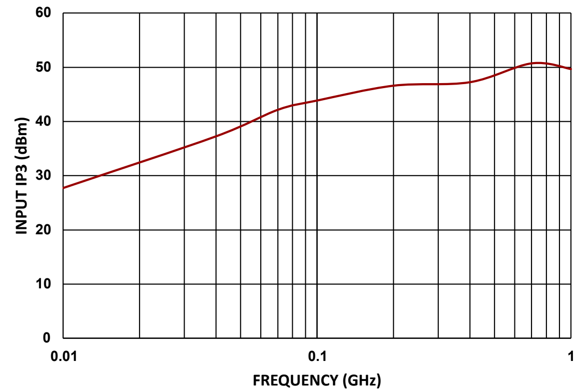


Figure 24. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5440 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. This driver features two digital control input pins, V1 and V2. The logic level applied to the control pins determine which RF port is in the insertion loss state and in the isolation state (see Table 7).

RF INPUT AND OUTPUT

RF ports (RFC, RF1 to RF4) are DC coupled to 0 V and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω.

The ADRF5440 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports. The unselected RF ports of the ADRF5440 is reflective.

The power handling of the ADRF5440 derates with frequency less than 3 GHz and more than 70 GHz. See Figure 2 and Figure 3 for the derating of the RF power towards lower and higher frequencies.

POWER SUPPLY

The ADRF5440 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 7. Control Voltage Truth Table

Digital Control Inputs		RFx Paths			
V1	V2	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

The ADRF5440 has two power supply pins (VDD and VSS) and two control pins (V1 and V2). Figure 25 shows the external components and connections for the supply pin. The VDD, VSS, V1, and V2 pins are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to the Pin Configuration and Function Descriptions section for further details.

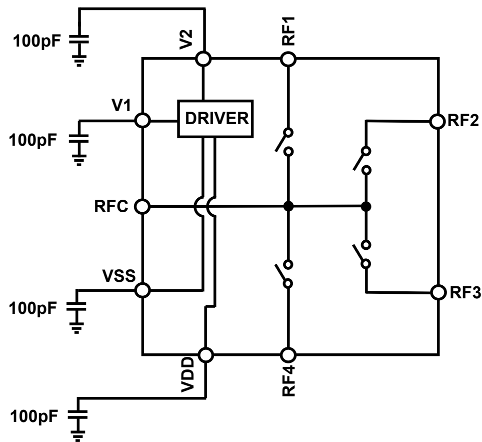


Figure 25. Recommended Schematic

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with 50 Ω characteristic impedance on the PCB. Figure 26 shows the referenced CPWG RF trace design for an RF substrate with 6 mil thick Megtron6 2×1080 R-5775G dielectric material. The RF trace with a 300 µm width and a 300 µm clearance is recommended for a 42 µm finished copper thickness.

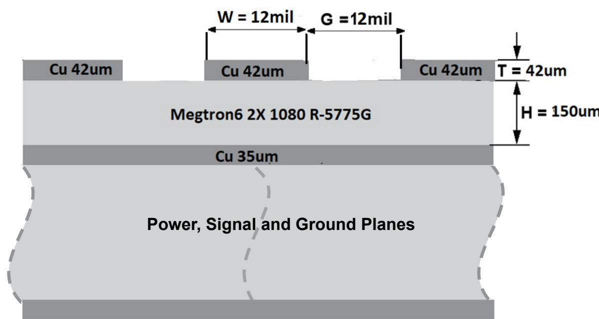


Figure 26. Probe Matrix Board Stackup

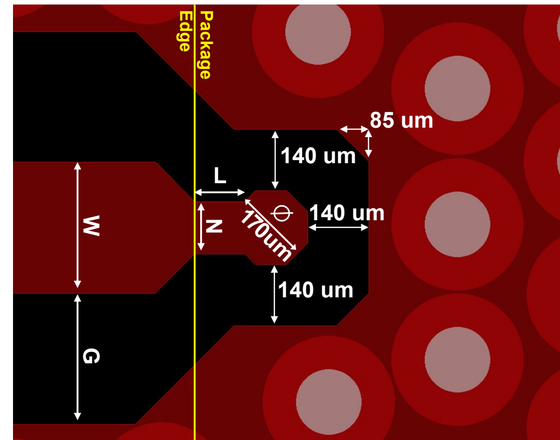


Figure 27. Recommended RFx Pin Transition

Figure 27 shows the recommended layout from the device RFx pins to the 50 Ω CPWG on the referenced stackup. Signal pads have a 170 µm diameter for ease of assembly. The RF trace from the PCB pad is extended with a thinner neck for broadband tuning and tapered to an RF trace with a 45° angle. The RFx pin transition for of ADRF5440 is optimized for the different stackups in Table 4 for broadband performance. For alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

Table 8. Recommended RFx Pin Transitions for Different Stackups

RF Stackup Height and Dielectric		RF Trace Dimensions		ADRF5440	Transition Dimensions	
H (µm)	Er	W (µm)	G (um)	Mnemonic	N (µm)	L (µm)
85	3.02	180	250	RFC,RF1,RF4	120	90
				RF2, RF3	120	190
100	3.34	200	225	RFC,RF1,RF4	120	90
				RF2, RF3	120	140
115	3.40	225	250	RFC,RF1,RF4	120	90
				RF2, RF3	120	140
125	3.00	250	225	All	120	90
150[1].	3.40	300	300	All	120	90
175	3.16	360	245	All	170	90
190	3.00	425	225	All	170	90
200	3.55	425	275	All	170	90

[1] Design reference and generic footprint

APPLICATIONS INFORMATION

DIE ASSEMBLY

The ADRF5440 complies with standard RoHS reflow assembly process and its temperature profiles. The device can be assembled with other surface-mounted technology (SMT) components in the same reflow cycle. However, the PCB must be designed according to the pick and place process.

The top copper layer of the PCB is designed for optimum RF performance where the solder mask and paste mask layers are designed for optimum assembly yield. The ground pads are drawn as the solder mask is defined. The signal pads are drawn pad defined. The same solder mask and paste mask design can be used for both pads.

The ADRF5440 can also be assembled without applying a solder paste on the PCB. If no solder paste is applied, the ADRF5440 must be dipped into flux prior to placement on the PCB.

Reflow Assembly with Solder Paste

Solder mask openings of 175 µm in square shape is recommended for signal and RF pads and 150 µm in square shape is recommended for GND pads. Solder mask thickness must not exceed 50 µm. Paste mask is drawn circular with a 150 µm diameter. Using a stencil with 2 mil thickness and no aperture reduction yields the optimum paste mask print. In this assembly, the device does not need any flux dipping during the pick and place process.

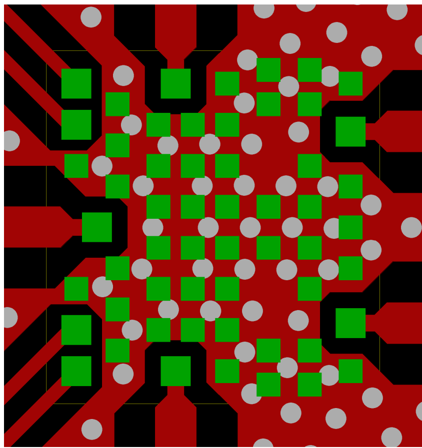


Figure 28. Recommended Footprint for Solder Paste

Reflow Assembly with Flux Dipping

Solder mask openings that are circular and 130 µm in diameter are recommended. Solder mask thickness must not exceed 50 µm. Solder paste is not applied. The device is dipped into flux prior to placement on the board.

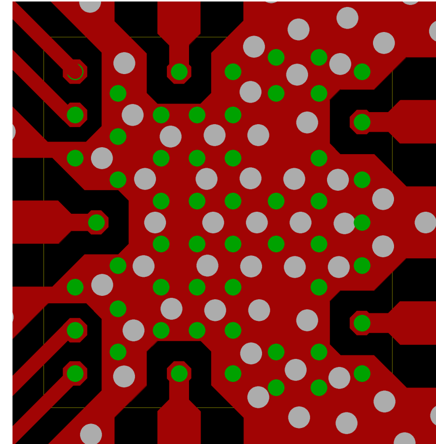


Figure 29. Recommended Footprint for Flux Dip Assembly

OUTLINE DIMENSIONS

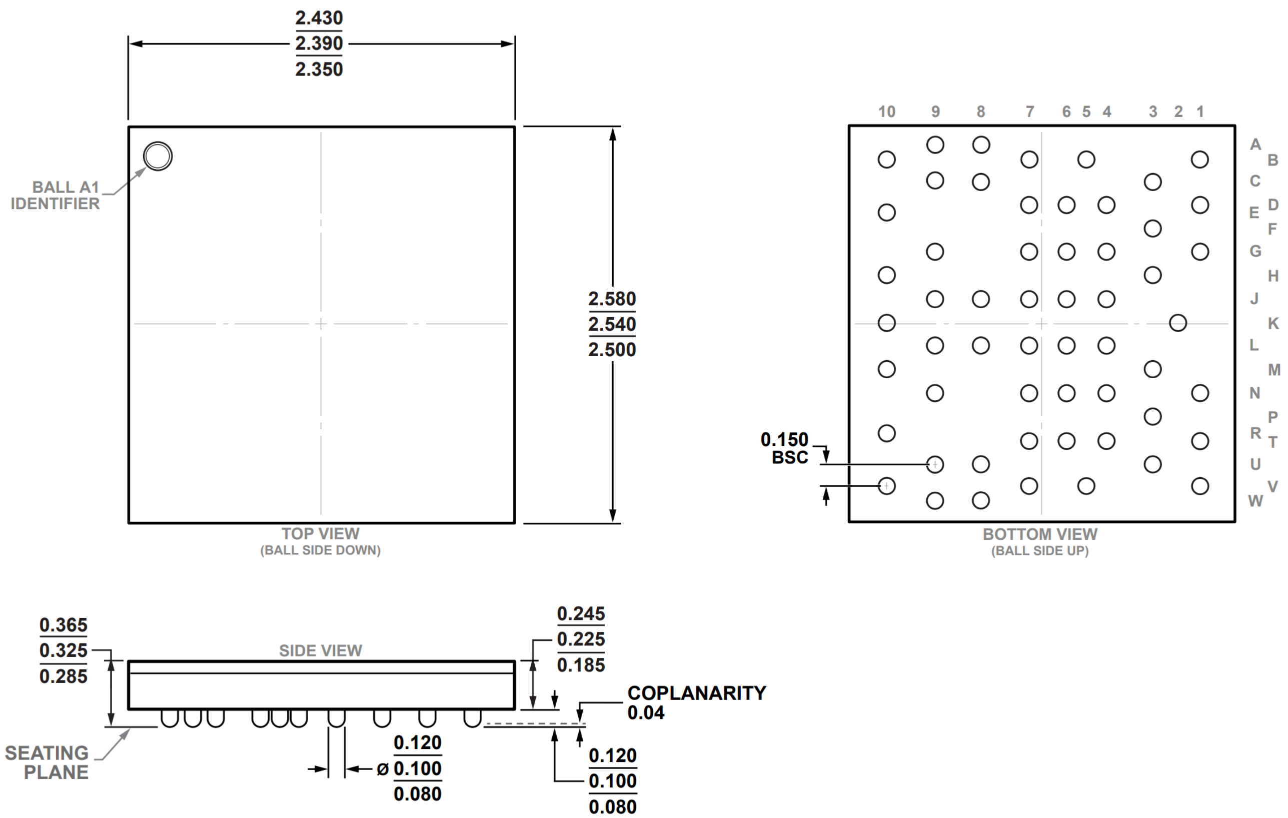


Figure 30. 56-Ball Bumped Bare Die Sales [BUMPED_CHIP]
(CD-56-1)
Dimensions shown in millimeters

ANALOG DEVICES

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