High Isolation, Silicon SPDT, Nonreflective Switch, 0.1GHz to 13GHz

FEATURES

- Frequency range: 100MHz to 13GHz
- Nonreflective, 50Ω design
- Low insertion loss
  - 1.0dB to 7GHz typical
  - 1.3dB to 13GHz typical
- High isolation
  - 49dB to 7GHz typical
  - 41dB to 13GHz typical
- High power handling (average)
  - 35dBm through path
  - 27dBm terminated path
  - 33dBm hot switching (RFC)
- High input linearity
  - P0.1dB: 36dBm typical
  - IP3: 60dBm typical
- Fast RF settling time 0.1dB: 220ns
- Single positive supply: 3.3V to 5V
- All off state control
- CMOS-/LVTTL-compatible
- 12-lead, 2mm × 2mm, LFCSP_RT

APPLICATIONS

- Cellular infrastructure
- Wireless infrastructure
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

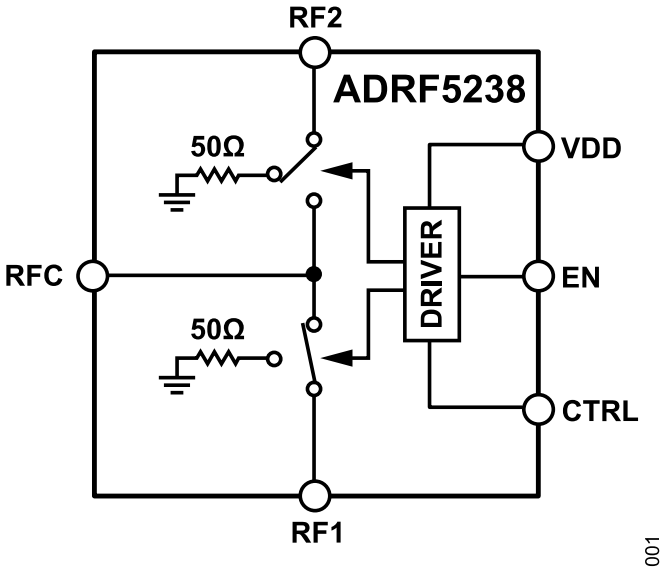

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5238 is a high isolation, nonreflective, 0.1GHz to 13GHz, silicon, SPDT switch in the silicon process.

The ADRF5238 operates from 0.1GHz to 13GHz with an insertion loss lower than 1.3dB and an isolation higher than 41dB at 13GHz. The ADRF5238 has a nonreflective design and the RF ports are internally terminated to 50Ω. The device has input power handling capability of 35dBm for through path, 27dBm for terminated path and 33dBm hot switching at the RFC pin.

The ADRF5238 requires a single-supply voltage (V_{DD}) of 3.3V to 5V. The ADRF5238 employs 1.8V complementary metal-oxide semiconductor (CMOS)-compatible and 3.3V low-voltage transistor logic (LVTTL)-compatible controls. The ADRF5238 has an enable control to put both RF channels in an isolation state.

The ADRF5238 comes in a 12-lead, 2mm × 2mm, LFCSP_RT and can operate from −40°C to +105°C.

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REVISION HISTORY

12/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5V, control voltage (V_{CTRL}) and enable voltage (V_{EN}) = 0V or 3.3V, and T_{CASE} = 25°C, with a 50Ω system, unless otherwise noted. RFx refers to RF1 to RF2.

Table 1. Electrical Characteristics for V_{DD} = 5V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		13	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1GHz to 2GHz		0.7		dB
		2GHz to 7GHz		1.0		dB
		7GHz to 13GHz		1.3		dB
RETURN LOSS						
RFC (On State)		0.1GHz to 13GHz		>20		dB
RFx (On State)		0.1GHz to 7GHz		>20		dB
		7GHz to 13GHz		18		dB
RFx (Terminated State)		0.4GHz to 7GHz		>20		dB
		7GHz to 13GHz		11		dB
ISOLATION						
Between RFC and RFx		0.1GHz to 2GHz		60		dB
		2GHz to 7GHz		49		dB
		7GHz to 13GHz		41		dB
Between RFx and RFx		0.1GHz to 2GHz		59		dB
		2GHz to 7GHz		47		dB
		7GHz to 13GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		25		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		120		ns
RF Settling Time, 0.1dB	$t_{SETTLING}$	50% V_{CTRL} to 0.1dB of final RF_{OUT}		220		ns
INPUT LINEARITY[1]		0.4GHz to 10GHz				
0.1 dB Power Compression	P0.1dB	V_{DD} = 5V		36		dBm
Third-Order Intercept	IP3	Two- tone input power = 14dBm each tone, Δf = 1MHz		60		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 5V		400		µA
DIGITAL CONTROL INPUTS		EN and CTRL pins				
Voltage		V_{DD} = 5V				
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.07		3.3	V
Current						
Low	I_{INL}	V_{EN} and V_{CTRL} = 0V, V_{DD} = 5V		<1		µA
High	I_{INH}	V_{CTRL} = 3.3V, V_{DD} = 5V		<1		µA
		V_{EN} = 3.3V, V_{DD} = 5V		10		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		4.75	5	5.25	V
RF Input Power [2]	P_{IN}	f = 100MHz to 10GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through the connected RF throw port (selected RFx)				
Average					35	dBm
Peak[4]					35	dBm
Terminated Path		RF signal is applied to the unselected RFx port				
Average					27	dBm
Peak					29.5	dBm

SPECIFICATIONS

Table 1. Electrical Characteristics for V_{DD} = 5V (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports				
Average					33	dBm
Peak					33	dBm
Hot Switching (RFx)		RF signal is applied to RFx port while switching				
Average					27	dBm
Peak					29.5	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 13 to Figure 16.

[2] For power derating over frequency, see the Power Derating Curves section.

[3] For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

[4] Peak: (≤100 ns pulse duration, 5% duty cycle).

V_{DD} = 3.3V, V_{CTRL} and V_{EN} = 0V or 3.3V, and T_{CASE} = 25°C, with a 50Ω system, unless otherwise noted. RFx refers to RF1 to RF2.

Table 2. Electrical Characteristics for V_{DD} = 3.3V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		13	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1GHz to 2GHz		0.8		dB
		2GHz to 7GHz		1		dB
		7GHz to 13GHz		1.4		dB
RETURN LOSS						
RFC (On State)		0.1GHz to 13GHz		>20		dB
RFx (On State)		0.1GHz to 7GHz		>20		dB
		7GHz to 13GHz		18		dB
RFx (Terminated State)		0.4GHz to 7GHz		>20		dB
		7GHz to 13GHz		11		dB
ISOLATION						
Between RFC and RFx (Off)		0.1GHz to 2GHz		60		dB
		2GHz to 7GHz		49		dB
		7GHz to 13GHz		41		dB
Between RFx and RFx		0.1GHz to 2GHz		59		dB
		2GHz to 7GHz		47		dB
		7GHz to 13GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		150		ns
RF Settling Time	$t_{SETTLING}$	50% V_{CTRL} to 0.1 dB of final RF_{OUT}		250		ns
INPUT LINEARITY[1]		400MHz to 10GHz				
0.1 dB Power Compression	P0.1dB	V_{DD} = 3.3V		33		dBm
Third-Order Intercept	IP3	Two-tone input power = 14dBm each tone, Δf = 1MHz		59		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 3.3V		200		µA
DIGITAL CONTROL INPUTS		EN and CTRL pins				
Voltage		V_{DD} = 3.3V				
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.07		3.3	V

SPECIFICATIONS

Table 2. Electrical Characteristics for V_{DD} = 3.3V (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Current						
Low	I_{INL}	V_{EN} and V_{CTRL} = 0V, V_{DD} = 3.3V		<1		µA
High	I_{INH}	V_{CTRL} = 3.3V, V_{DD} = 3.3V		<1		µA
		V_{EN} = 3.3V, V_{DD} = 3.3V		<7		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		3.15	3.3	3.45	V
RF Input Power [2]	P_{IN}	f = 100MHz to 10GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)				
Average					33	dBm
Peak[4]					33	dBm
Terminated Path		RF signal is applied to the unselected RFx port				
Average					26	dBm
Peak					28.5	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports				
Average					31	dBm
Peak					31	dBm
Hot Switching (RFx)		RF signal is applied to RFx port while switching				
Average					26	dBm
Peak					28.5	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 13 to Figure 16.

[2] For power derating over frequency, see the Power Derating Curves section.

[3] For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

[4] Peak: (≤100 ns pulse duration, 5% duty cycle).

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	−0.3V to +5.8V
Digital Control Inputs[1]	
Voltage	−0.5V to 3.6V
Current	3mA
RF Input Power (V_{DD} = 5V)[2, 3]	
Through Path	
Average	36dBm
Peak[4]	36dBm
Terminated Path	
Average	28dBm
Peak	30dBm
Hot Switching (RFC)	
Average	34dBm
Peak	34dBm
Hot Switching (RFx)	
Average	28dBm
Peak	30dBm
RF Input Power (V_{DD} = 3.3V)	
Through Path	
Average	34dBm
Peak	34dBm
Terminated Path	
Average	27dBm
Peak	29dBm
Hot Switching (RFC)	
Average	32dBm
Peak	32dBm
Hot Switching (RFx)	
Average	27dBm
Peak	29dBm
RF Power Under Unbiased Condition (V_{DD} = 0V)	18dBm
Temperature	
Junction (T_j)	135°C
Storage	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

4 Peak: (≤100 ns pulse duration, 5% duty cycle).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance (see Table 4).

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CR-12-1		
Through Path	57	°C/W
Terminated Path	100	°C/W

POWER DERATING CURVES

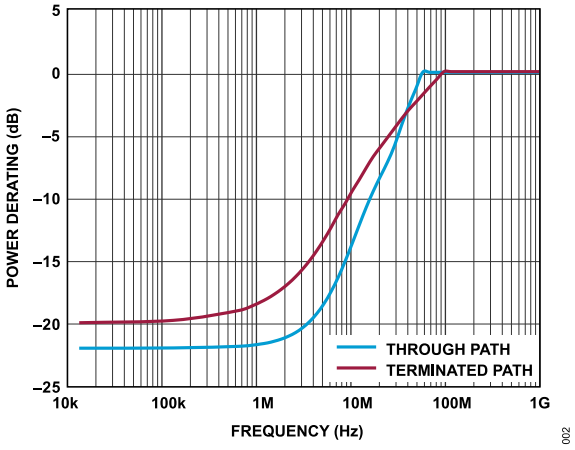

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5238

Table 5. ADRF5238, 12-Lead LFCSP_RT

ESD Model	Withstand Threshold (V)	Class
HBM	±2000 for All Pins	2
CDM	±500 for All Pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

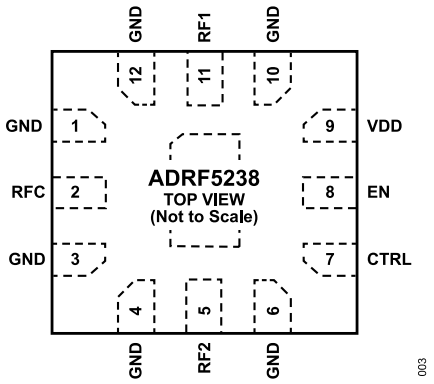

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 10, 12	GND	Grounds. The package bottom has an exposed metal pad that must connect to the PCB RF ground.
2	RFC	RF Common Port. The RFC pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
5	RF2	RF Throw Port 2. The RF2 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
7	CTRL	Control Input Pin. See Figure 6 for the CTRL interface schematic.
8	EN	Enable Input Pin. See Figure 7 for the EN interface schematic.
9	VDD	Supply Voltage Pin. See Figure 8 for the interface schematic.
11	RF1	RF Throw Port 1. The RF1 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. Exposed pad must be connected to RF and DC ground.

INTERFACE SCHEMATICS

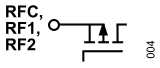

Figure 5. RFC, RF1, and RF2 Interface Schematic

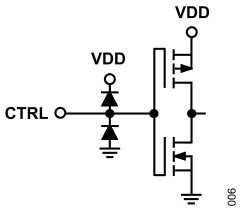

Figure 6. CTRL Interface Schematic

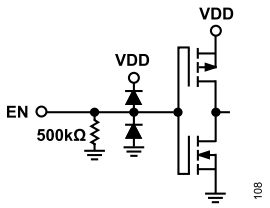

Figure 7. EN Interface Schematic

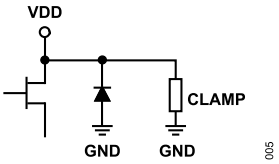

Figure 8. VDD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

V_{DD} = 3.3V or 5V, V_{CTRL} and V_{EN} = 0V or 3.3V, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted.

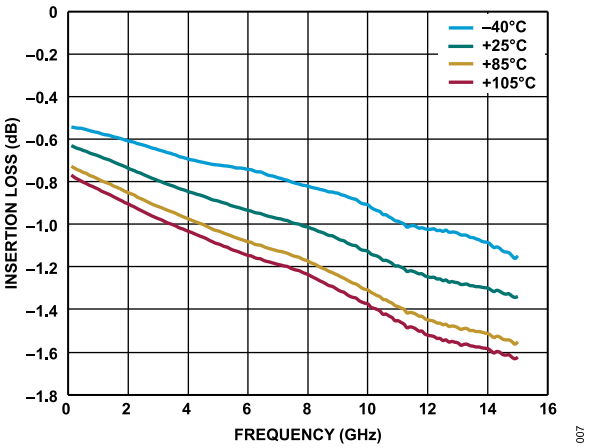

Figure 9. Insertion Loss vs. Frequency over Temperatures, V_{DD}= 5V)

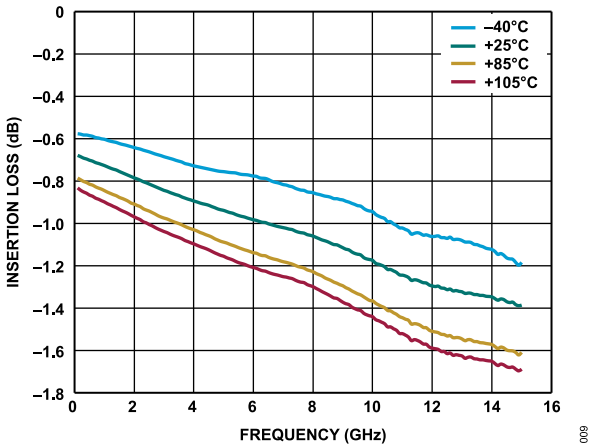

Figure 11. Insertion Loss vs. Frequency over Temperatures (V_{DD}= 3.3V)

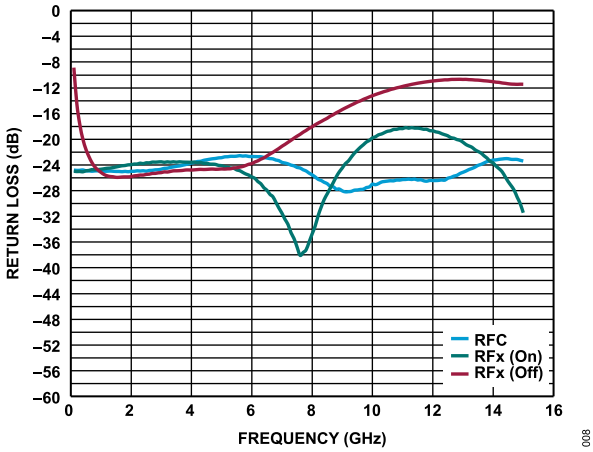

Figure 10. Return Loss vs. Frequency (V_{DD}= 3.3V to 5V)

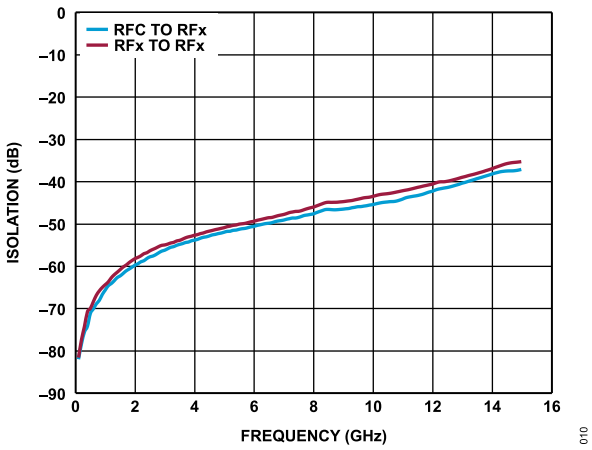

Figure 12. Isolation vs. Frequency (V_{DD}= 3.3V to 5V)

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3V or 5V, V_{CTRL} and V_{EN} = 0V or 3.3V, T_{CASE} = 25°C, with a 50Ω system, unless otherwise noted.

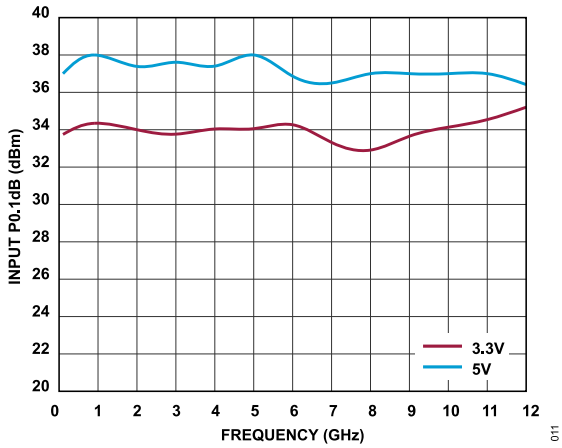

Figure 13. Input P0.1dB vs. Frequency

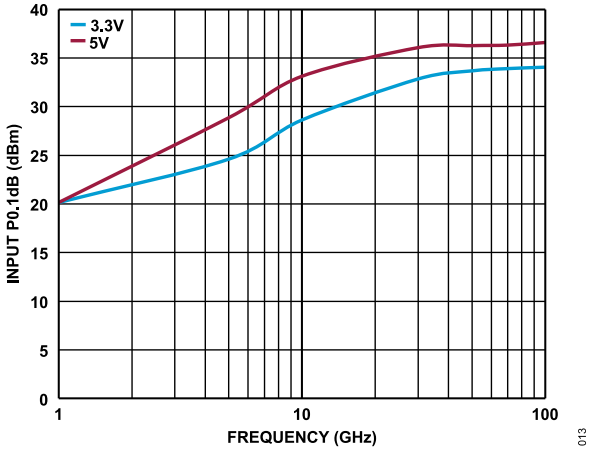

Figure 15. Input P0.1dB vs. Frequency (Low Frequency Detail)

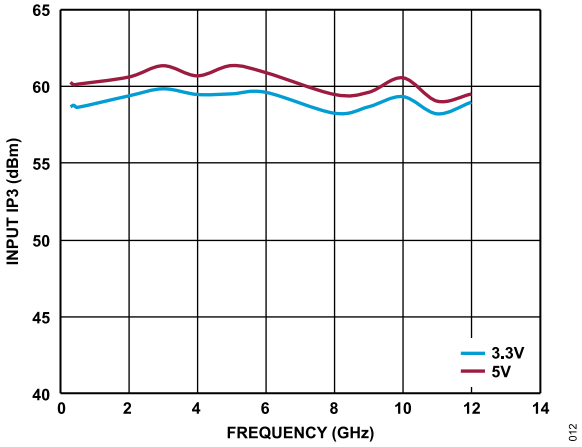

Figure 14. Input IP3 vs. Frequency

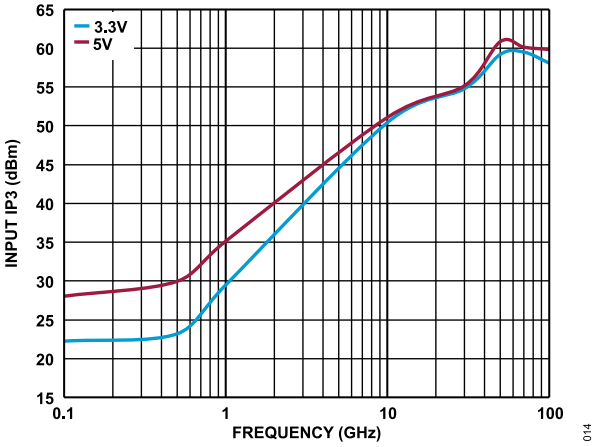

Figure 16. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5238 integrates a driver to perform logic functions internally and to provide the advantage of a simplified CMOS-/LVTTL-compatible control interface. There are two digital control input pins (EN and CTRL) that determine which RF port is in the insertion loss state and in the isolation state. See Table 7 for the control voltage truth table.

When the EN pin is logic high, all RF paths are in isolation state regardless of the logic state of the CTRL pin. The RFx ports are terminated to internal 50Ω resistors, and RFC becomes reflective.

RF INPUT AND OUTPUT

The RF pins (RFC, RF1, and RF2) are DC-coupled, and DC blocking capacitors are required on the RF lines. The RF ports are internally matched to 50Ω. Therefore, external matching networks are not required.

When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF port is in an insertion loss state and which RF port is in an isolation state. The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50Ω resistor.

When the EN pin is logic high, the switch is in an all off state regardless of the logic state of the CTRL pin. Both the RF1 to RFC path and the RF2 to RFC path are in an isolation state. The RF1 and RF2 ports are terminated to internal 50Ω resistors, and the RFC port becomes reflective open.

The ADRF5238 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

POWER SUPPLY

The ADRF5238 requires a positive supply on the VDD pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The power-up sequence is as follows:

1. Connect GND.
2. Power up VDD.
3. Apply the digital control inputs. The relative order of the logic control inputs is not important. Powering the digital control inputs before VDD can inadvertently forward bias and damage ESD protection structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the digital control pins. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 7. Control Voltage Truth Table

CTRL State	EN State	RFC to RF1	RFC to RF2
Low	Low	Off	On
High	Low	On	Off
Low	High	Off	Off
High	High	Off	Off

APPLICATIONS INFORMATION

The ADRF5238 has one power supply pin (VDD) and two digital control pins (CTRL and EN). Figure 17 shows the external components and connections for the supply pin. The VDD pin is decoupled with a 100pF multilayer ceramic capacitor. The ADRF5238 pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins (RFC, RF1, and RF2). Wideband capable DC blocking capacitors are recommended for best performance.

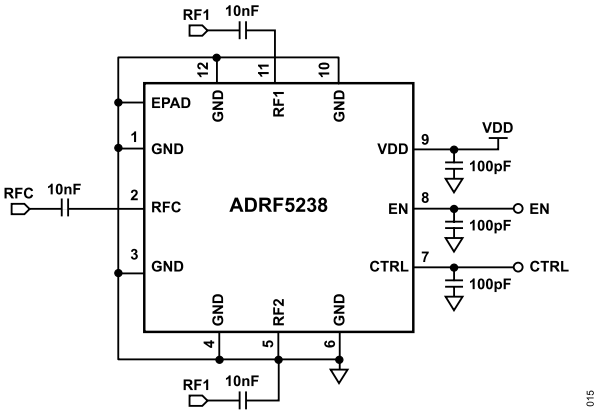

Figure 17. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG RF trace design for an RF substrate with 10mil thick Rogers RO4350B dielectric material. The RF trace with an 18mil width and 13mil clearance is recommended for 2.8mil finished copper thickness.

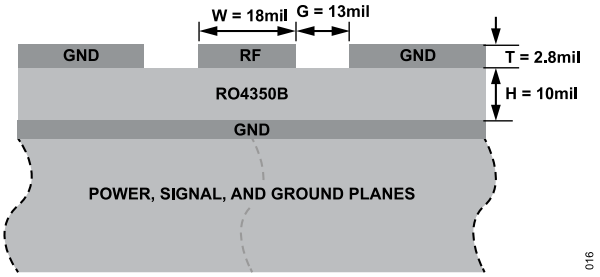

Figure 18. ADRF5238-EVALZ Stack-Up

Figure 19 shows the routing of the RF traces, supply, and control signals from the ADRF5238. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the ADRF5238 is the bottom side.

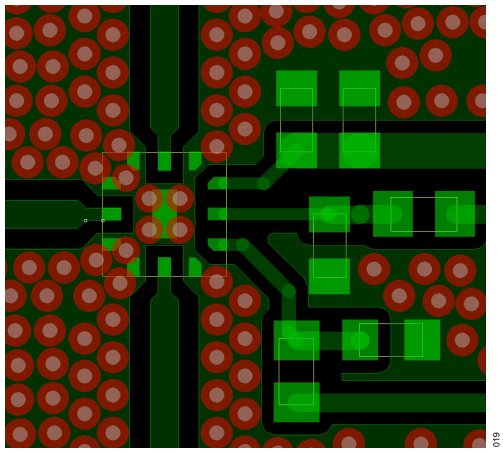

Figure 19. PCB Routings

Figure 20 shows the recommended layout from the RF pins (RFC, RF1, and RF2) of the ADRF5238 to the 50Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn soldermask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width for a 10mil and tapered to the RF trace. The paste mask is designed to match the pads of the ADRF5238 without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

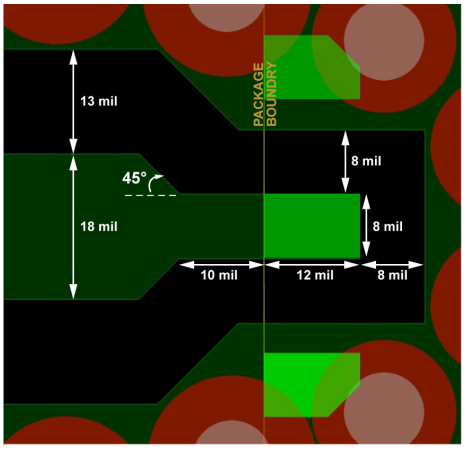

Figure 20. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Center for further recommendations.

OUTLINE DIMENSIONS

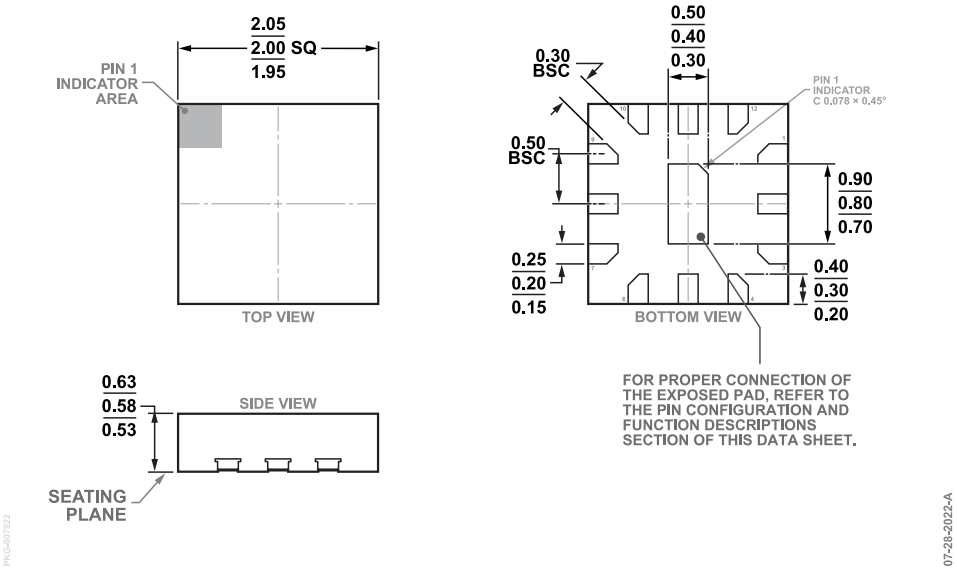

Figure 21. 12-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]
2mm × 2mm and 0.58mm Package Height
(CR-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Quantity	Package Option
ADRF5238BCRZN	−40°C to +105°C	12-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Cut-Tape, <1500	CR-12-1
ADRF5238BCRZN-R7	−40°C to +105°C	12-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Reel, 1500	CR-12-1
ADRF5238BCRZN-RL	−40°C to +105°C	12-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Reel, 5000	CR-12-1

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Table 8. Evaluation Boards

Model[1]	Description
ADRF5238-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.