DC to 12 GHz, Differential, Nonreflective, Silicon SPDT Switch

FEATURES

- Frequency range: DC to 12 GHz
- DC voltage range: ±8 V
- On resistance (R_{ON}): <2.5 Ω
- Fully differential 100 Ω design
- Low insertion loss
  - <0.8 dB at 8 GHz
  - <1 dB at 12 GHz
- High isolation
  - >45 dB at 8 GHz
  - >38 dB at 12 GHz
- High input linearity
  - P0.1dB: 31 dBm typical
  - P1dB: 32 dBm typical
  - IP3: 55 dBm typical
- High power handling
  - 31 dBm through path
  - 24 dBm terminated path
- RF switching time: 1.5 µs
- All off state control
- Termination control
  - 100 Ω differential or high-Z (reflective)
- 22 terminal, 3 mm × 3 mm, RoHS-compliant, land grid array (LGA) package

APPLICATIONS

- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

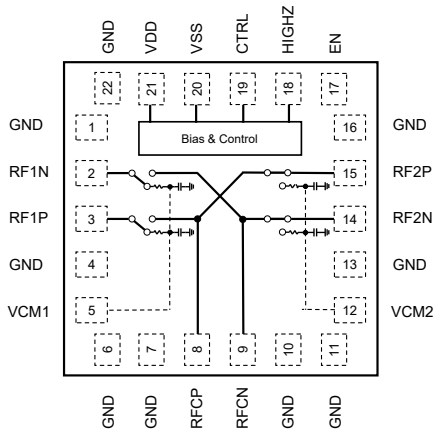

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5203 is a silicon, differential, single-pole double-throw (SPDT) switch. The ADRF5203 operates from DC to 12 GHz with an insertion loss of better than 1 dB and an isolation higher than 38 dB. The device has a DC voltage input range of ±8 V and RF input power handling of differential 31 dBm for through paths and 24 dBm for terminated paths.

The ADRF5203 operates with dual-supply voltages of ±12 V. The ADRF5203 employs complementary metal-oxide semiconductor (CMOS)- and low voltage transistor logic (LVTTL)-compatible controls. The ADRF5203 has an enable control to feature all off state function. The High-Z control selects the termination on the unselected RF channel.

The ADRF5203 comes in a 22-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

TABLE OF CONTENTS

SPECIFICATIONS

VDD = 12 V, VSS = −12 V, CTRL, EN, and HIGHZ = 0 V or 3.3 V, and T_{CASE} = 25°C, with a 100 Ω differential, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0		12	GHz
INSERTION LOSS						
Between RFCx and RFxx (On)		DC to 6 GHz		0.6		dB
		6 GHz to 10 GHz		0.9		dB
		10 GHz to 12 GHz		1.0		dB
RETURN LOSS						
RFCx (On)		DC to 8 GHz		18		dB
		8 GHz to 12 GHz		15		dB
RFxx (On)		DC to 8 GHz		18		dB
		8 GHz to 12 GHz		15		dB
RFxx (Off−Terminated)		DC to 8 GHz		14		dB
		8 GHz to 12 GHz		13		dB
ISOLATION						
Between RFCx and RFxx (Terminated)		DC to 6 GHz		50		dB
		6 GHz to 10 GHz		44		dB
		10 GHz to 12 GHz		36		dB
Between RFCx and RFxx (HIGHZ)		DC to 6 GHz		48		dB
		6 GHz to 10 GHz		38		dB
		10 GHz to 12 GHz		34		dB
Between RFxx and RFxx (Terminated)		DC to 6 GHz		−48		dB
		6 GHz to 10 GHz		−42		dB
		10 GHz to 12 GHz		−35		dB
Between RFxx and RFxx (HIGHZ)		DC to 6 GHz		−52		dB
		6 GHz to 10 GHz		−42		dB
		10 GHz to 12 GHz		−32		dB
DC CHARACTERISTICS		Single ended				
RFCx to RFxx On Resistance	R_{ON}			2.5		Ω
RFCx to RFxx Off Resistance	R_{OFF}			1.2		MΩ
RFCx to GND	R_{CG}			>100		MΩ
	R_{XG}			>100		MΩ
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		275		ns
On Time	t_{ON}	50% CTRL voltage (V_{CTRL}) to 90% of RF output		1.5		µs
Off Time	t_{OFF}	50% V_{CTRL} to 10% of RF output		1		µs
0.1 dB Settling Time	$t_{SETTLING}$	50% V_{CTL} to 0.1 dB of final RF output		2.5		µs
INPUT LINEARITY [1]						
Input Compression						
0.1 dB	P0.1dB	100 MHz to 10 GHz		31		dBm
		10 GHz to 12 GHz		30		dBm
1 dB	P1dB	100 MHz to 10 GHz		32		dBm
		10 GHz to 12 GHz		31		dBm
Third-Order Intercept	IP3	100 MHz to 10 GHz, two-tone Input power = 20 dBm each tone, Δf = 1 MHz		55		dBm
		10 GHz to 12 GHz , two-tone input power = 20 dBm each tone, Δf = 1 MHz		TBD		dBm
Total Harmonic Distortion	THD	DC to 100 MHz, V_{CM}= 0 V		TBD		%

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF IMBALANCE		RFxP and RFxN				
Amplitude		6 GHz		−0.2		dB
		10 GHz		−0.3		dB
		12 GHz		−0.4		dB
Phase		6 GHz		−6		Degrees
		10 GHz		−6		Degrees
		12 GHz		−4		Degrees
Common Mode to Differential Mode Conversion Ratio		Common mode input to differential mode output, f = 10 GHz		−20		dB
Differential Mode to Common Mode Conversion Ratio		Differential mode input to common mode output, f = 10 GHz		−20		dB
POWER SUPPLY REJECTION	PSR	100 Ω differential		TBD		dB
GROUP DELAY	t_{GD}	100 Ω differential, f = 10 GHz		40		ps
SUPPLY CURRENTS						
Positive	I_{DD}			19		mA
Negative	I_{SS}			18		mA
DIGITAL CONTROL INPUTS		CTRL, EN, and HIGHZ pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITIONS		f = 100 MHz to 10 GHz, T_{CASE} = 85°C, −8 V < V_{CM} < +8 V				
Supply Voltage						
Positive	V_{DD}		11.4		12.6	V
Negative	V_{SS}		−12.6		−11.4	V
DC Input						
Voltage Range	V_{DC}		−8		+8	V
Current Range	I_{DC}		−160		+160	mA
Common-Mode Voltage Range	V_{CM}		−8		+8	V
RF Input Power [2, 3]	P_{IN}	f = 100 MHz to 12 GHz, T_{CASE} = 85°C, −8 V < V_{CM} < +8 V				
Through Path						
Average				31		dBm
Peak				31		dBm
Terminated Path						
Average				24		dBm
Peak				31		dBm
Hot Switching						
Average				24		dBm
Peak				TBD		dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For high frequency power derating over frequency, see Figure 2.

[2] For low frequency operation and V_{CM} dependent power derating, see Figure 3.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3V to +13.2 V
Negative	−13.2 V to +0.3 V
Digital Control Inputs [1]	
Voltage	−0.3 V to +3.6 V
Current	3 mA
RF Input Power [2] (VDD = 12 V, VSS = −12 V, f = 100 MHz to 10 GHz, T_{CASE} = 85°C[3])	
Through Path	TBD dBm
Terminated Path	TBD dBm
Hot Switching (RFC)	TBD dBm
RF Input Power, Unbiased (VDD, VSS = 0 V)	TBD dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-22-5		
Through Path	TBD	°C/W
Terminated Path	TBD	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

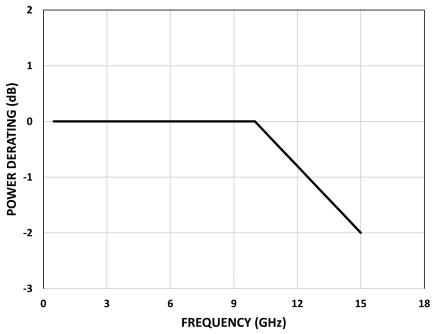

Figure 2. Power Derating vs. Frequency, T_{CASE} = 85°C

Figure 3. V_{CM} Dependent Low Frequency Power Derating vs. Frequency, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5203

Table 4. ADRF5203, 22-Terminal LGA

ESD Model	Withstand Threshold (V)
HBM	±TBD for RFxx Pins
	±TBD for Supply and Digital Control Pins
CDM	±TBD for All Pins

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

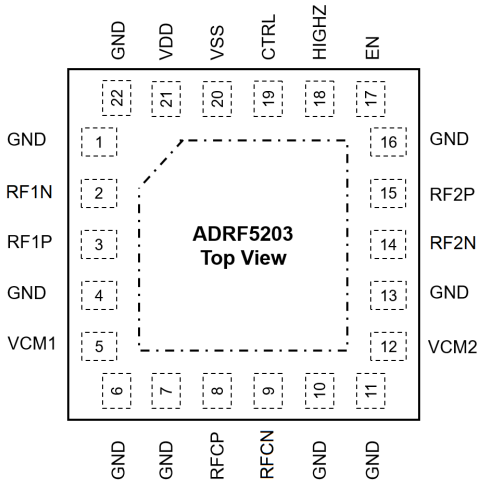

Figure 4. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 7, 10, 11, 13, 16, 22	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
2, 3, 8, 9, 14, 15	RF1N, RF1P, RFCP, RFCN, RF2N, RF2P	Negative and Positive RF Pins. The RFxN and RFxP pins are DC-coupled and AC matched to differential 100 Ω.
5, 12	VCM1, VCM2	Low Frequency and DC Termination Pins. See Figure 9 for the interface schematic
17	EN	Enable Input. See Table 6 for the truth table and Figure 7 for the interface schematic.
18	HIGHZ	The HIGH-Z pin sets the termination type of the unselected channel. See Table 6 for the truth table and Figure 7 for the interface schematic.
19	CTRL	Digital Input to Control the RF Path State. See Table 6 for the truth table and Figure 7 for the interface schematic.
20	VSS	Negative Supply Voltage. See Figure 8 for the interface schematic .
21	VDD	Positive Supply Voltage. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

INTERFACE SCHEMATICS

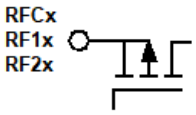

Figure 5. RFCx , RF1x and RF2x Interface Schematic

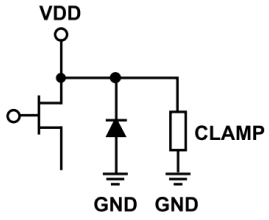

Figure 6. VDD Interface Schematic

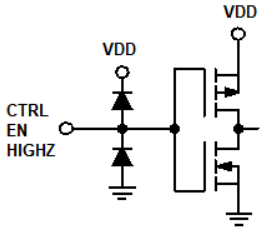

Figure 7. VCTL, EN, and HIGHZ Interface Schematic

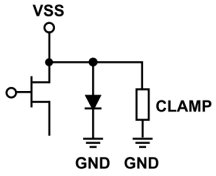

Figure 8. VSS Interface Schematic

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

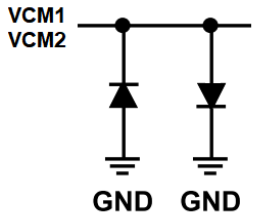

Figure 9. VCM1, VCM2 Interface schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 12 V, VSS = −12 V, CTRL, EN, and HIGHZ = 0 V or 3.3 V, and T_{CASE} = 25°C, with a 100 Ω differential, unless otherwise noted.

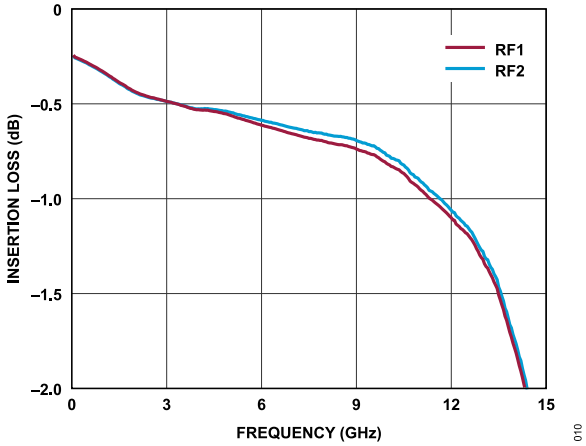

Figure 10. Insertion Loss vs. Frequency

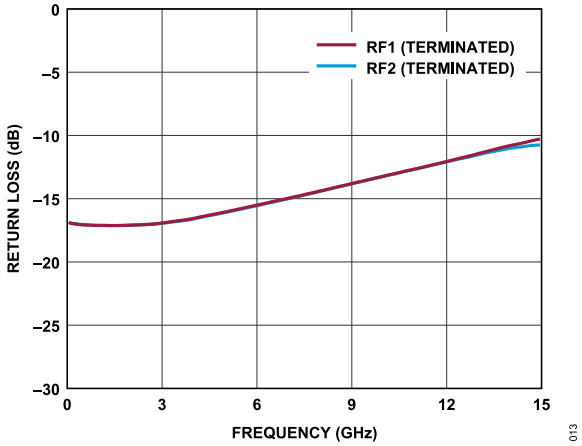

Figure 13. Return Loss vs. Frequency (Off Channel, Terminated)

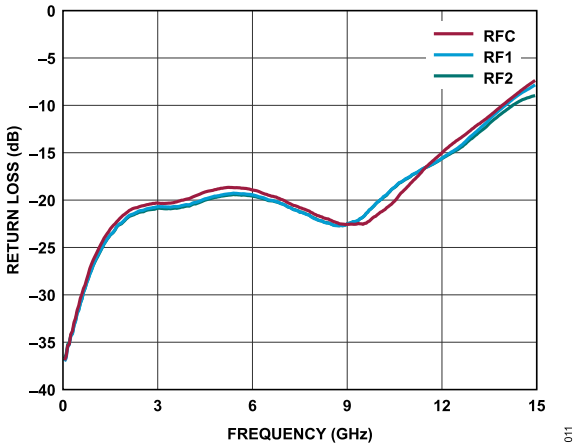

Figure 11. Return Loss (On Channel) vs. Frequency

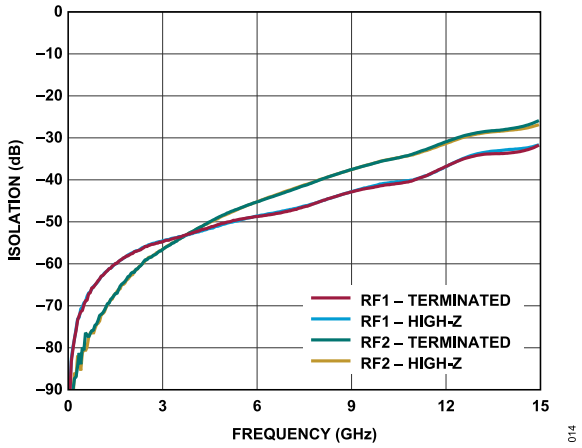

Figure 14. Isolation vs. Frequency (RFCx − RFxx)

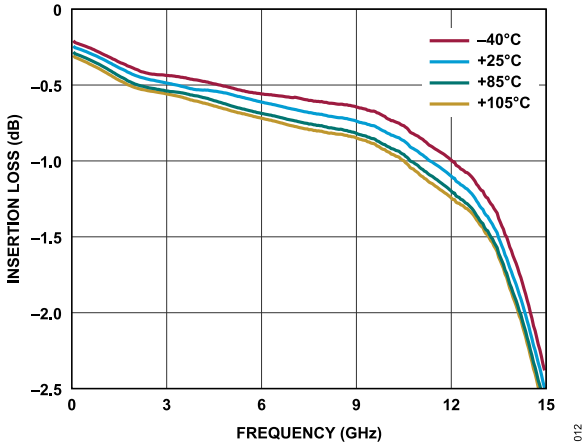

Figure 12. Insertion Loss vs. Frequency over Temperature

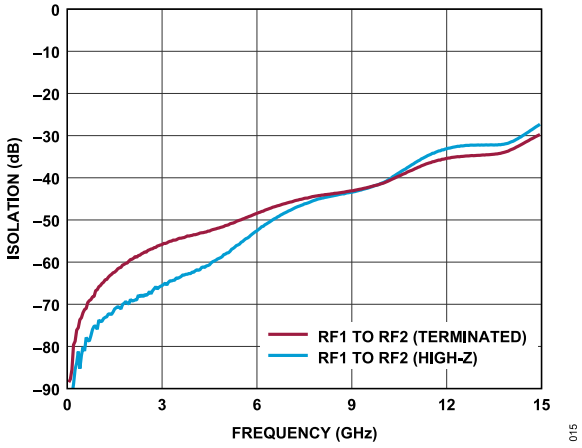

Figure 15. Isolation vs. Frequency (RFxx to RFxx)

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 12 V, VSS = −12 V, CTRL, EN, and HIGHZ = 0 V or 3.3 V, and T_{CASE} = 25°C, with a 100 Ω differential, unless otherwise noted.

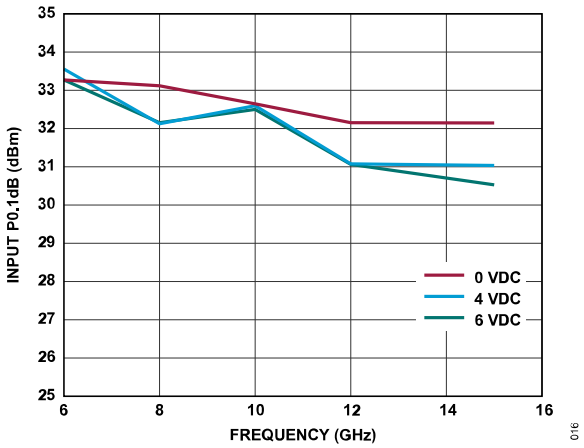

Figure 16. Input P0.1dB vs. Frequency over DC Offset

Figure 18. Input IP3 vs. Frequency

Figure 17. Input P0.1 dB over DC Offset (Low Frequency Detail)

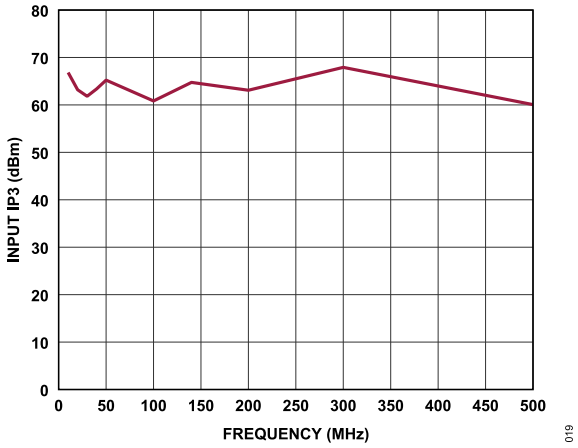

Figure 19. Input IP3 vs. Frequency (Low Frequency Detail)

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE IMBALANCE, PHASE IMBALANCE, GROUP DELAY, AND EYE DIAGRAM

VDD = 12 V, VSS = −12 V, CTRL, EN, and HIGHZ = 0 V or 3.3 V, and T_{CASE} = 25°C, with a 100 Ω differential, unless otherwise noted.

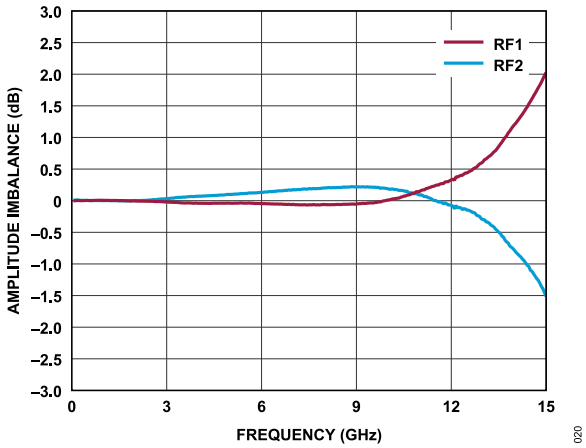

Figure 20. Amplitude Imbalance vs. Frequency

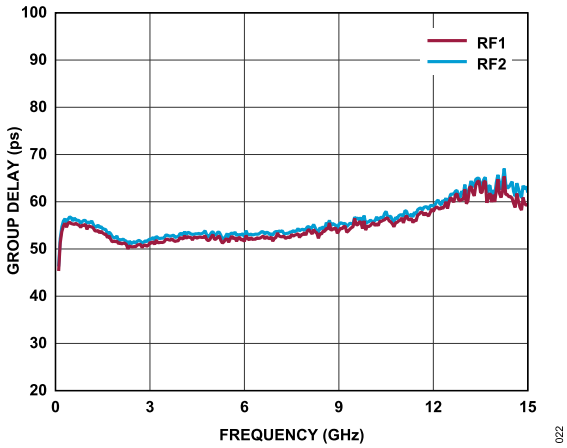

Figure 22. Group Delay vs. Frequency

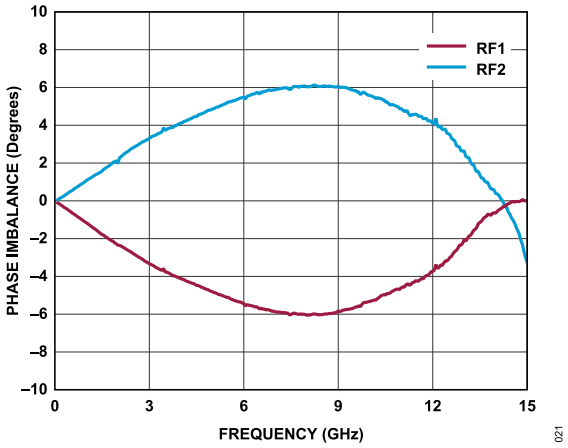

Figure 21. Phase Imbalance vs. Frequency

Figure 23. Eye Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

MODE CONVERSION, TOTAL HARMONIC DISTORTION, AND POWER SUPPLY REJECTION

VDD = 12 V, VSS = −12 V, CTRL, EN, and HIGHZ= 0 V or 3.3 V, and T_{CASE} = 25°C, with a 100 Ω differential, unless otherwise noted.

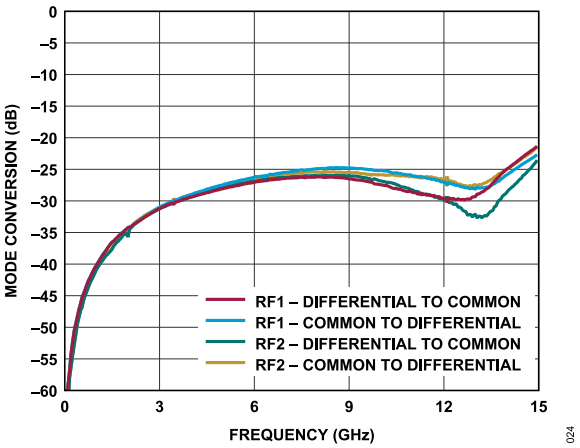

Figure 24. Mode Conversion vs. Frequency

Figure 26. Power Supply Rejection vs. Frequency

Figure 25. Total Harmonic Distortion vs. Frequency

THEORY OF OPERATION

The ADRF5203 can interface CMOS-/LVTTL-compatible control interfaces directly. The CTRL pin determines which RF port is in the insertion loss state and in the isolation state. The EN pin puts the ADRF5203 in the all off state, meaning that both the RFCx and RF1x and the RFCx and RF2x paths are in the isolation state. The HIGHZ pin allows users to choose the termination type of the unselected RF channel that can configure the unselected port to be nonreflective or reflective during the off state. See Table 6 for the control voltage truth table.

DIFFERENTIAL RF INPUTS AND OUTPUTS

The ADRF5203 is a fully differential 100 Ω design. All RF inputs and outputs are differential pairs with the polarity denoted by the N and P suffix on the pin names. When the device is enabled, the RFCN and RFCP pins are connected to the RFxN and RFxP pins of the selected port, respectively. Even if the device is fully differential internally, the device RFxx pins are designed to interface 50 Ω single-ended RF traces on the circuit board.

COMMON-MODE VOLTAGE

The RF ports are dc-coupled and can support a DC voltage range of ± 8V. Figure 27 shows the DC equivalent circuit for selected and unselected channels.

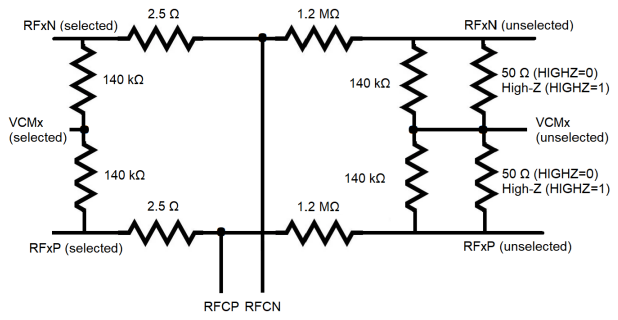

Figure 27. DC Equivalent Circuit

The VCM1 and VCM2 pins can be used to set or to monitor the DC common-mode voltage on RF port. These pins can be left floating or can be decoupled to ensure a low impedance common-mode AC ground for the unselected channel.

When the input signal is driven DC-coupled from the RFC port or the RF port, the selected output port follows the input signal. There is no need to bias the VCMx pin, and the common-mode voltage is set by the input signal.

When the input is driven AC-coupled, the common-mode voltage on the selected channel can be set at the VCMx pin on the RF port.

POWER HANDLING

The RF power handling of the ADRF5203 derates over frequency and is dependent to the DC voltage below 100 MHz. See Figure 3 for power derating of the RF power towards lower frequencies at different DC input voltages. For the low frequency operation, the device ensures constant R_{ON} on the selected channel for the best THD performance.

For the frequencies above 100 MHz, both maximum DC voltage and maximum RF power can be applied at the same time. The device is designed to handle the full RF power independent of the DC input voltage above 100 MHz. See Figure 2 for power derating above 10 GHz.

The ADRF5203 is designed as bidirectional with equal power handling capabilities on RFC and RF ports. Either port can be used as an input or as output.

POWER SUPPLY

The ADRF5203 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.

The ideal power-down sequence is the reverse order of the previous list.

Table 6. Control Voltages Truth Table

Digital Control Inputs			RF Paths	
EN	**HIGHZ**	**CTRL**	**RFCx to RF1x**	**RFCx to RF2x**
Low	Low	Low	Insertion loss	Isolation (terminated)
Low	Low	High	Isolation (terminated)	Insertion loss
Low	High	Low	Insertion loss	Isolation (reflective)

THEORY OF OPERATION

Table 6. Control Voltages Truth Table (Continued)

Digital Control Inputs			RF Paths	
EN	**HIGHZ**	**CTRL**	**RFCx to RF1x**	**RFCx to RF2x**
Low	High	High	Isolation (reflective)	Insertion loss
High	Low	Not applicable	Isolation (terminated)	Isolation (terminated)
High	High	Not applicable	Isolation (reflective)	Isolation (reflective)

APPLICATION INFORMATION

Figure 28 shows the external components and connections for the ADRF5203. The VDD and VSS pins are decoupled with a 100 pF and 0.01 µF multilayer ceramic capacitors. The device pinout allows the placement of the decoupling capacitors close to the device. The VCMx pins can be decoupled to ground or biased with voltage depending on the use case.

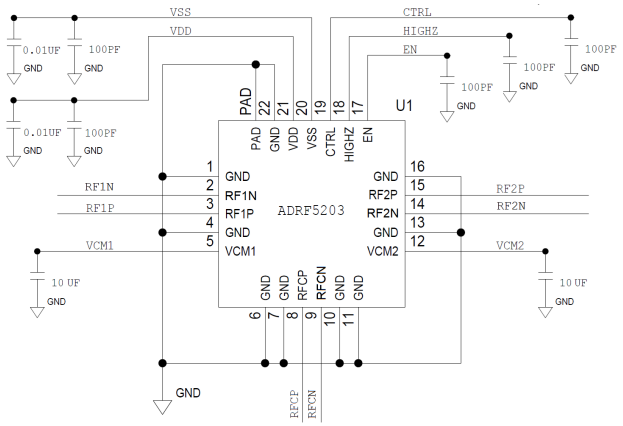

Figure 28. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The ADRF5203 is designed to mate with 50 Ω characteristic impedance on each RFxx pin. The RF ports are matched to differential 100 Ω internally.

Figure 29 shows the reference coplanar waveguide (CPWG) RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. The RF trace with a 14 mil width and a 7 mil clearance is recommended for 2.2 mil finished copper thickness.

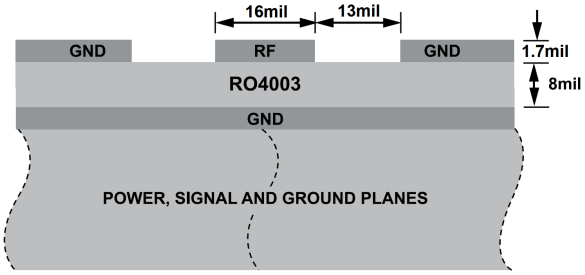

Figure 29. Recommended Stackup

Figure 30 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

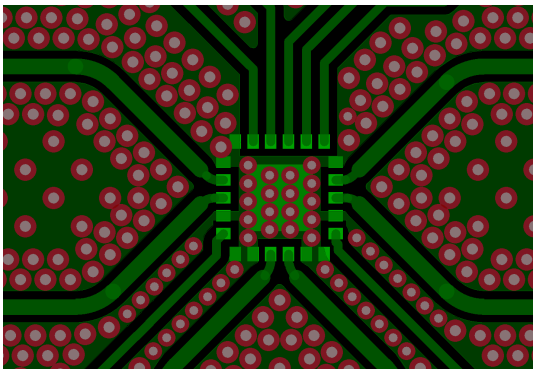

Figure 30. PCB Layout

Figure 31 shows the recommended layout from the device RFxx pins to the 50 Ω CPWG on the referenced stackup. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width until the package edge and tapered to the RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

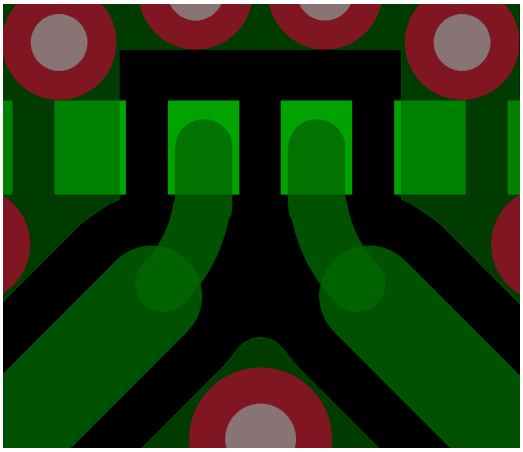

Figure 31. Recommended RFxx Pin Transition

For alternate PCB stackups with different dielectric thickness and RF trace design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

OUTLINE DIMENSIONS

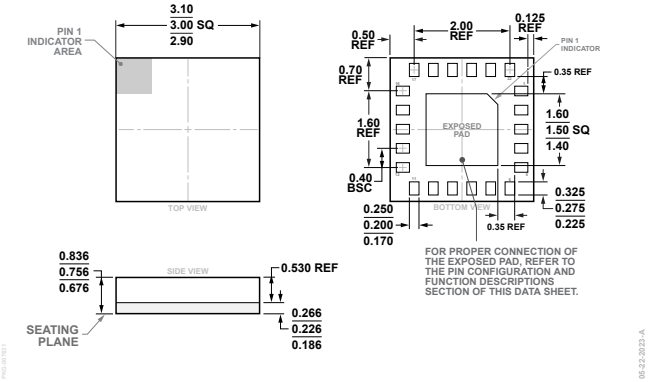

Figure 32. 22-Terminal Land Grid Array [LGA]
(CC-22-5)
Dimensions shown in millimeters