

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance nonreflective 100 MHz to 44 GHz, single pull double throw (SPDT) switch microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/21601</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADRF5026	Nonreflective 100 MHz to 44 GHz, SPDT switch

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	See figure 1	Land grid array (LGA)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Positive supply voltage range (VDD)	-0.3 V to +3.6 V
Negative supply voltage range (VSS)	-3.6 V to +0.3 V
Digital control inputs:	
Voltage	-0.3 V to VDD + 0.3 V
Current	3 mA
RF input power <u>2/</u> (100 MHz to 40 GHz at TCASE = 85°C <u>3/</u>)	
Insertion loss path	26 dBm
Isolation path	25 dBm
Hot switching	25 dBm
Junction temperature range (TJ)	135°C
Storage temperature range (TSTG)	-65°C to +150°C
Reflow temperature	+260°C
Thermal resistance, junction to case (θJC):	
Through path	423°C/W
Terminated path	241°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HDM) :	
RFC, RF1, RF2 pins	500 V
Digital pins	2000 V
Charged body model (CDM)	1250 V

1.4 Recommended operating conditions. 4/

Positive supply voltage (VDD)	+3.3 V
Negative supply voltage (VSS)	-3.3 V
Case temperature range (TC)	-55°C to +105°C

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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ For power derating versus frequency, see figure 4 and figure 5. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
- 3/ For 105°C operation, the power handling degrades from the TCASE = 85°C specification by 3 dB.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Power rating versus low frequency graph. The power rating versus low frequency graph shall be as shown in figure 4.

3.5.5 Power rating versus high frequency graph. The power rating versus high frequency graph shall be as shown in figure 5.

3.5.6 RFC, RF1, RF2 Interface schematic circuits. The RFC, RF1, RF2 interface schematic circuit shall be as shown in figure 6.

3.5.7 CTRL, EN Interface schematic circuits. The CTRL, EN interface schematic circuit shall be as shown in figure 7.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, TC	Device type	Limits		Unit
					Min	Max	
Frequency range			-55°C to +105°C	01	100	44,000	MHz
Insertion loss (IL)							
Between RFC and RF1/RF2		100 MHz to 18 GHz	+25°C	01	1.2 typical		dB
		18 GHz to 26 GHz			1.7 typical		
		26 GHz to 35 GHz			2.2 typical		
		35 GHz to 40 GHz			2.4 typical		
		40 GHz to 44 GHz <u>3/</u>			3.8 typical		
Return loss (RL)							
RFC and RF1/RF2 (on)		100 MHz to 18 GHz	+25°C	01	22 typical		dB
		18 GHz to 26 GHz			12 typical		
		26 GHz to 35 GHz			9 typical		
		35 GHz to 40 GHz			10 typical		
		40 GHz to 44 GHz <u>3/</u>			7 typical		
RFC and RF1/RF2 (off)		100 MHz to 18 GHz	+25°C	01	23 typical		dB
		18 GHz to 26 GHz			23 typical		
		26 GHz to 35 GHz			21 typical		
		35 GHz to 40 GHz			13 typical		
		40 GHz to 44 GHz <u>3/</u>			12 typical		
Isolation							
Between RFC and RF1/RF2		100 MHz to 18 GHz	+25°C	01	55 typical		dB
		18 GHz to 26 GHz			53 typical		
		26 GHz to 35 GHz			53 typical		
		35 GHz to 40 GHz			50 typical		
		40 GHz to 44 GHz			45 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _C	Device type	Limits		Unit
					Min	Max	
Isolation – continued.							
Between RF1 and RF2		100 MHz to 18 GHz	+25°C	01	63 typical		dB
		18 GHz to 26 GHz			60 typical		
		26 GHz to 35 GHz			60 typical		
		35 GHz to 40 GHz			63 typical		
		40 GHz to 44 GHz			55 typical		
Switching characteristics							
Rise and fall times	t _{RISE} , t _{FALL}	10% to 90% of RF output	+25°C	01	3 typical		ns
On and off time	t _{ON} , t _{OFF}	50% of triggered V _{CTRL} to 90% of RF output	+25°C	01	14 typical		ns
RF settling time 0.1 dB		50% of triggered V _{CTRL} to 0.1 dB of final RF output	+25°C	01	40 typical		ns
RF settling time 0.05 dB		50% of triggered V _{CTRL} to 0.05 dB of final RF output	+25°C	01	45 typical		ns
Input linearity		100 MHz to 40 GHz					
1 dB compression	P _{1dB}		+25°C	01	27 typical		dBm
Third order intercept	IP ₃	Two tone input power = 12 dBm each tone, Δf = 1 MHz	+25°C	01	53 typical		dBm
Supply current		VDD and VSS pins					
Positive	I _{DD}		+25°C	01	2 typical		μA
Negative	I _{SS}		+25°C	01	100 typical		μA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _C	Device type	Limits		Unit
					Min	Max	
Digital control inputs		CTRL and EN pins					
Low voltage	V _{INL}		-55°C to +105°C	01	0	0.8	V
High voltage	V _{INH}		-55°C to +105°C	01	1.2	3.3	V
Low and high current	I _{INL} , I _{INH}		+25°C	01	1 typical		μA
Recommended operating conditions							
Positive supply voltage	V _{DD}		-55°C to +105°C	01	3.15	3.45	V
Negative supply voltage	V _{SS}		-55°C to +105°C	01	-3.45	-3.15	V
Digital control voltage	V _{CTRL} , V _{EN}		-55°C to +105°C	01	0	V _{DD}	V
RF input power (P _{IN}) <u>4/</u>		f = 100 MHz to 40 GHz, T _{CASE} = +85°C <u>5/</u>					
Insertion loss path		RF signal is applied to RFC or through connected RF1/RF2	-55°C to +85°C	01		24	dBm
Isolation path		RF signal is applied to terminated RF1/RF2	-55°C to +85°C	01		24	dBm
Hot switching		RF signal is present at RFC while switching between RF1 and RF2	-55°C to +85°C	01		24	dBm

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V_{DD} = 3.3 V, V_{SS} = -3.3 V, CTRL pin voltage (V_{CTRL}) = EN pin voltage (V_{EN}) 0 V or V_{DD}, and T_{CASE} = 25°C in a 50 Ω system.
- 3/ Impedance matching on RF transmission lines improves high frequency performance. Refer to the manufacturer's data sheet for more information
- 4/ For power derating versus frequency, see figure 6 and figure 7. This power derating is applicable for insertion loss path, isolation path, and hot switching power specifications.
- 5/ For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

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Case X

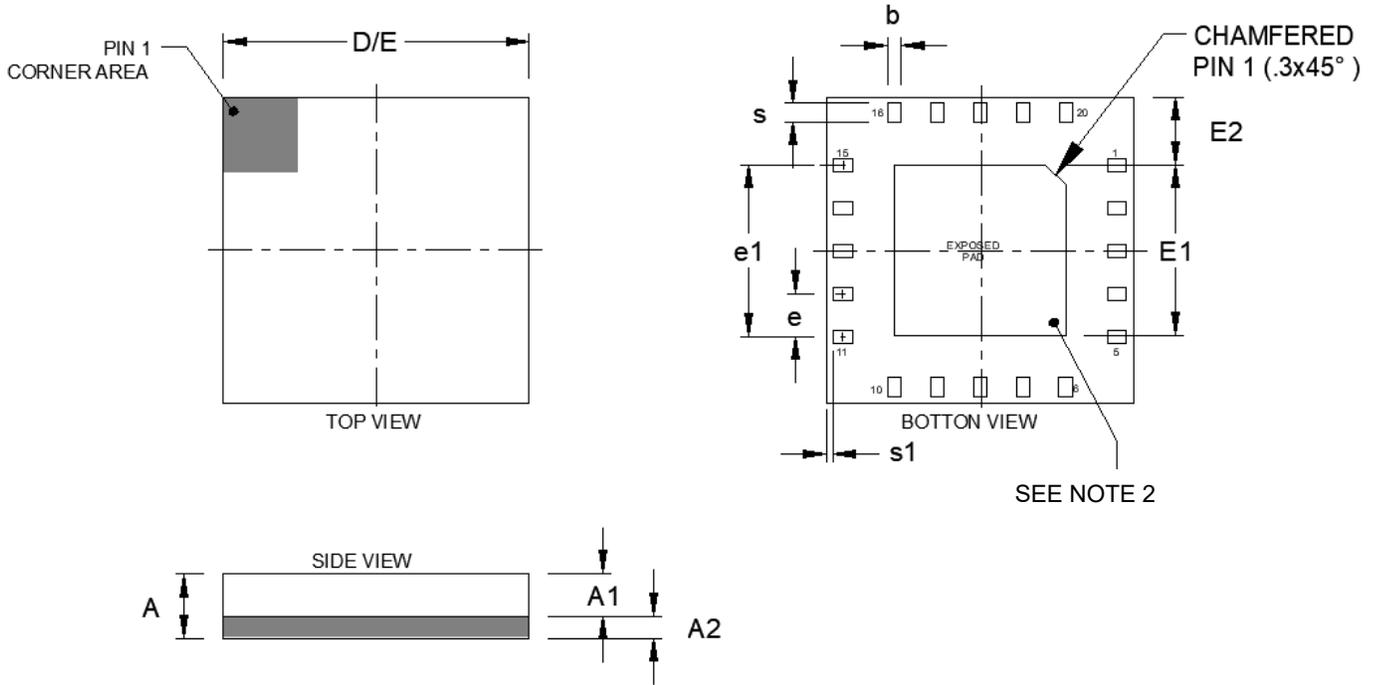


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/21601</p>
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Case X - continued

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.027	.028	.030	0.676	0.726	0.776
A1	.021 REF			0.530 REF		
A2	.006	.008	.009	0.156	0.196	0.236
b	.006	.008	.010	0.15	0.20	0.25
D/E	.114	.118	.122	2.90	3.00	3.10
E1	.055	.060	.063	1.40	1.50	1.60
E2	.029 REF			0.75 REF		
e	.016 BSC			0.40 BSC		
e1	.063 REF			1.60 REF		
s	.008	.010	.012	0.20	0.25	0.30
s1	.005 REF			0.13 REF		

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pads, refer to the pin configuration and function descriptions section of the manufacturer's data sheet.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
2	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
3	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω . No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See figure 6 for the interface schematic.
4	GND	Ground. These pins must be connected to the RF and dc ground of the printed circuit board (PCB).
5	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
6	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
7	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
8	RF1	RF1 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω . No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See figure 6 for the interface schematic.
9	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
10	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
11	VDD	Positive supply voltage.
12	CTRL	Control Input Voltage. See figure 7 for the interface schematic.
13	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
14	EN	Enable input voltage. See figure 7 for the interface schematic.
15	VSS	Negative supply voltage.
16	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
17	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
18	RF2	RF2 Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω . No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc. See figure 6 for the interface schematic.
19	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.
20	GND	Ground. These pins must be connected to the RF and dc ground of the PCB.

FIGURE 2. Terminal connections.

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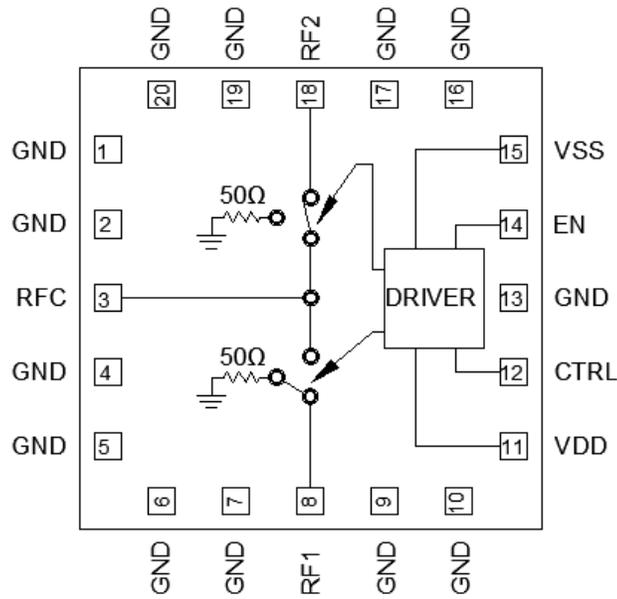


FIGURE 3. Functional block diagram.

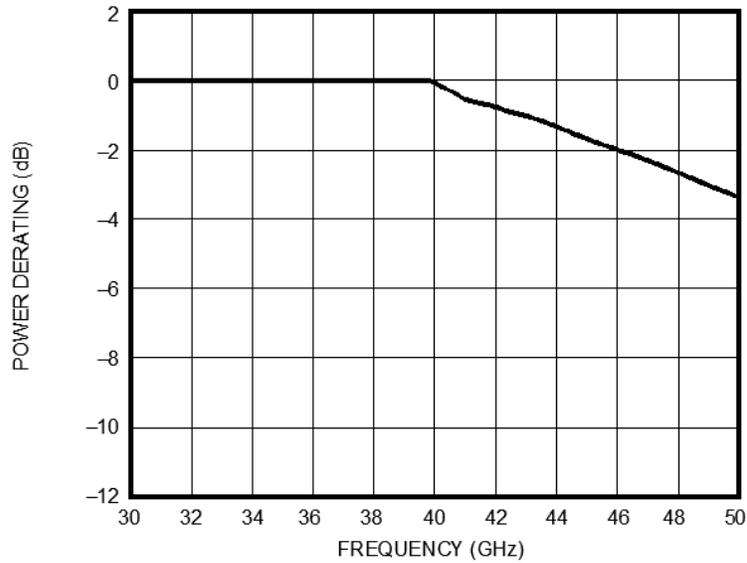


FIGURE 4. Power rating versus low frequency graph.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/21601</p>
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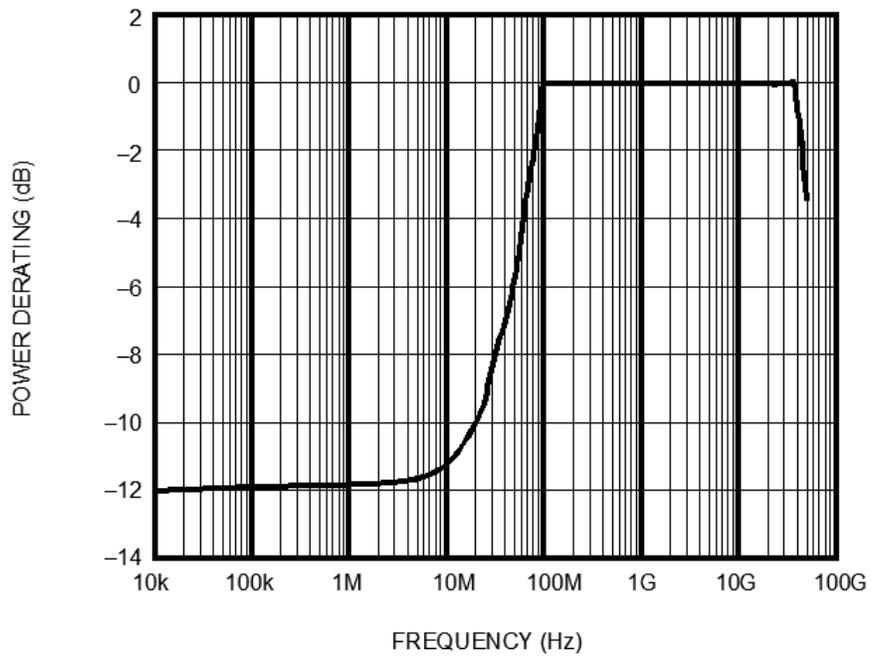


FIGURE 5. Power rating versus high frequency graph.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/21601</p>
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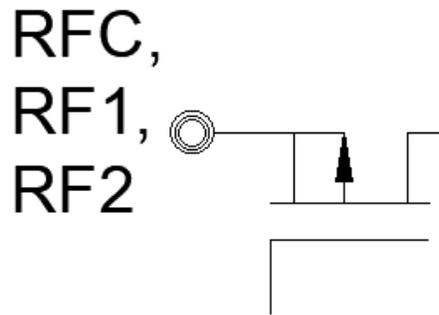


FIGURE 6. RFC, RF1, RF2 Interface schematic circuits

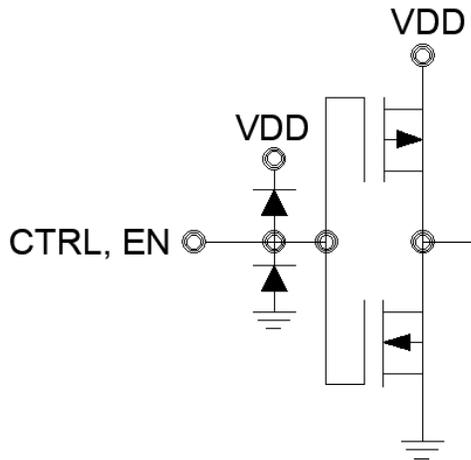


FIGURE 7. CTRL, EN Interface schematic circuits

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21601-01XE	24355	Cut tape, 500 units	6EP	ADRF5026SCCZ-EP
		Reel, 1500 units	6EP	ADRF5026SCCZ-EPR7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 20 Alpha Road
 Chelmsford, MA 01824-4123

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