Data Sheet

ADPD7008

Multimodal Sensor Front End

FEATURES

- Optical channel
  - 4 input channels with multiple operation modes for various sensor measurements
  - 4-channel processing with simultaneous sampling
  - 12 programmable time slots for synchronized sensor measurements
  - Flexible input multiplexing to support single-ended sensor measurements
  - 8 LED drivers, 2 of which can be driven simultaneously
  - Flexible sampling rate from 0.004 Hz to 9 kHz using internal oscillators
  - AC ambient light rejection: 78 dB up to 100 Hz
  - 400 mA total LED peak drive current
  - Individual ambient cancellation DAC at TIA input with 9-bit control up to 300 µA
  - Individual LED DC cancellation DAC at TIA input with 7-bit control up to 190 µA
- SPI communications supported
- 704-byte FIFO

APPLICATIONS

- Wearable health and fitness monitors: heart rate, heart rate variability, and saturation level of pulse oxygen
- Clinical patient monitors: small bed side patient, home portable patient, and small remote patient
- Industrial monitoring: particle, aerosol, and gas detection

GENERAL DESCRIPTION

The ADPD7008 is a highly integrated analog front end (AFE) designed for measuring various vital signals.

The optical channel is designed as an optical transceiver, stimulating up to eight light emitting diodes (LEDs) and measuring the return signal on up to four separate current inputs. The signal chain rejects signal offsets and corruption from asynchronous modulated interference, typically from ambient light, eliminating the need for optical filters or externally controlled DC cancellation circuitry.

The data output and functional configuration use a serial port interface (SPI) on the ADPD7008. The control circuitry includes flexible LED signaling and synchronous detection, digital filters, digital wave generators, and configurable filters.

The ADPD7008 is available in a 2.795 mm × 2.560 mm, 0.40 mm pitch, 36-ball WLCSP.

Rev. 0

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REVISION HISTORY

4/2024—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

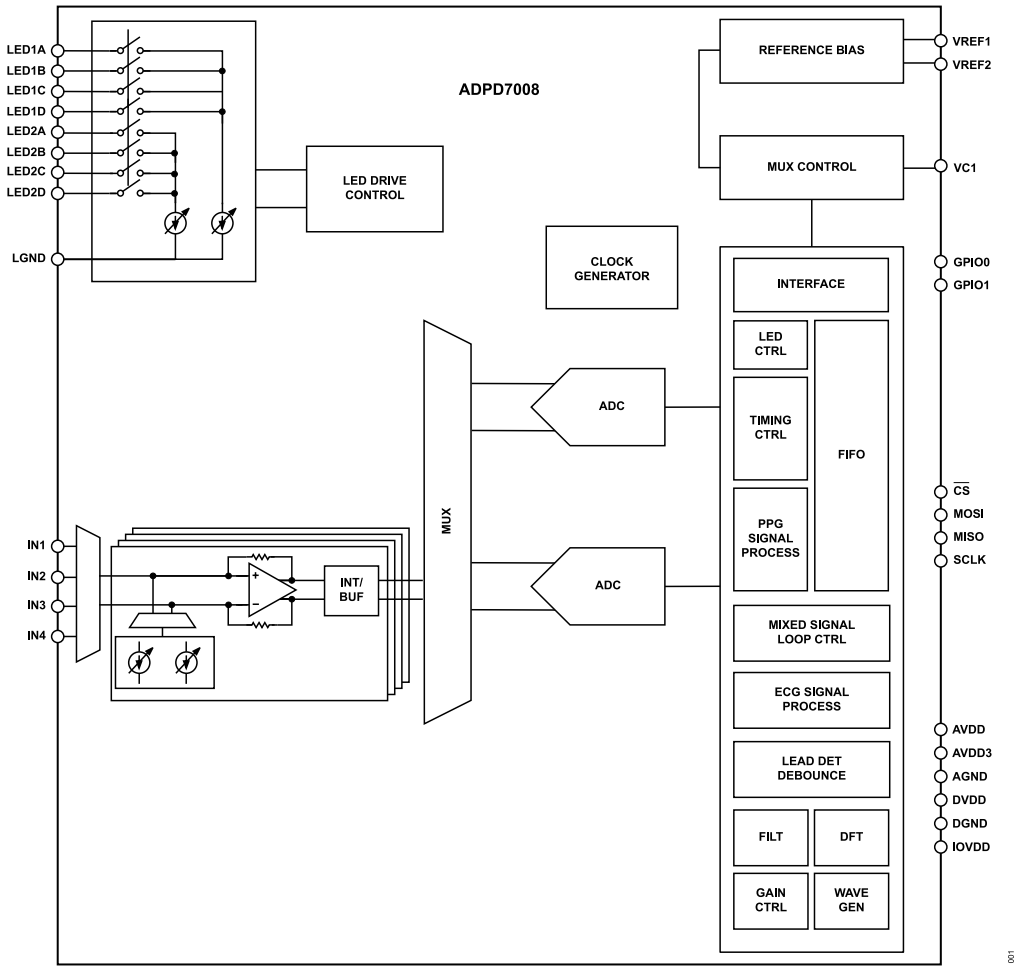

Figure 1. Functional Block Diagram

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Temperature and Power Specifications

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating Range	−40		+85	°C
Storage Range	−65		+150	°C
POWER SUPPLY VOLTAGES				
AVDD	1.7	1.8	1.9	V
AVDD3	2.7	3.3	3.6	V
DVDD	1.7	1.8	1.9	V
IOVDD	1.7	1.8	3.6	V

PERFORMANCE SPECIFICATION

AVDD = DVDD = IOVDD = 1.8 V, AVDD3 = 3.3 V, and T_A = 25°C, unless otherwise noted.

Table 2. Performance Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
DATA ACQUISTION					
Datapath Width				32	Bits
FIRST IN, FIRST OUT (FIFO) SIZE				704	Bytes
INTERNAL 960 kHz OSCILLATOR ACCURACY	Full temperature range (−40°C to +85°C)		±1		%
PHOTOPLETHYSMOGRAPHY (PPG) CHANNEL					
Transimpedance Amplifier (TIA) Gain		12.5		400	kΩ
DIGITAL INTEGRATION MODE					
Analog-to-Digital Converter (ADC) Resolution	TIA feedback resistor (R_F)				
	12.5 kΩ		5.84		nA/LSB
	25 kΩ		2.92		nA/LSB
	50 kΩ		1.46		nA/LSB
	100 kΩ		0.73		nA/LSB
	200 kΩ		0.365		nA/LSB
	400 kΩ		0.183		nA/LSB
ADC Saturation Level	TIA feedback resistor				
	12.5 kΩ		48		µA
	25 kΩ		24		µA
	50 kΩ		12		µA
	100 kΩ		6		µA
	200 kΩ		3		µA
	400 kΩ		1.5		µA
DC Ambient Light Rejection (ALR)					
ALR Range		0		300	µA
ALR Resolution			0.6		µA
LED DC Cancellation					
Range		0		190	µA
Resolution			1.48		µA
Dark Noise	Pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		1590		pA RMS

SPECIFICATIONS

Table 2. Performance Specifications (Continued)

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
	TIA gain = 25 kΩ		867		pA RMS
	TIA gain = 50 kΩ		425		pA RMS
	TIA gain = 100 kΩ		235		pA RMS
	TIA gain = 200 kΩ		140		pA RMS
	TIA gain = 400 kΩ		92		pA RMS
Signal-to-Noise Ratio (SNR)	White card reflection, pulse = 1, ADC sample = 20				
	TIA gain = 12.5 kΩ		90		dB
	TIA gain = 25 kΩ		90		dB
	TIA gain = 50 kΩ		88		dB
	TIA gain = 100 kΩ		87		dB
	TIA gain = 200 kΩ		85		dB
	TIA gain = 400 kΩ		82		dB
AC ALR	Up to 100 Hz		84		dB
DC Power Supply Rejection Ratio (PSRR)	At 75% full-scale (FS) input, optimal settings, all gains[1]		60		dB
LED DRIVER					
Peak Current per Driver	LED pulse enabled		200		mA
Peak Current, Total	Using multiple LED drivers simultaneously		400		mA
Current Step	High SNR mode		1.57		mA
	Low compliance mode		0.78		mA
Compliance Voltage	High SNR mode		400		mV
	Low compliance mode		200		mV
Power	AFE current only, 70% FS output data rate (ODR) = 25 Hz				
Standby	DVDD + AVDD		0.3		µA
Typical Heart Rate Monitor (HRM) Application	DVDD + AVDD		18.7		µA
SAMPLING RATE		0.004		9000	Hz

[1] DC PSRR = 20 × log((Signal(LSB)/NUM_INT_x/NUM_REPEAT_x × 0.146 mV/LSB)/V_{IN} (mV))

DIGITAL SPECIFICATIONS

IOVDD = 1.7 V to 3.6 V, unless otherwise noted.

Table 3. Digital Specifications

Parameter	Test Condition/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Voltage Level					
GPIOx, MISO, MOSI, SCLK, and $\overline{CS}$					
High		0.7 × IOVDD		IOVDD + 0.3	V
Low		−0.3		+0.3 × IOVDD	V
Input Current Level	All logic inputs				
High				10	µA
Low		−10			µA
Input Capacitance			2		pF
LOGIC OUTPUTS					
Output Voltage Level					
GPIOx and MISO					
High	2 mA high level output current	IOVDD – 0.5			V
Low	2 mA low level output current			0.5	V

SPECIFICATIONS

TIMING SPECIFICATIONS

Table 4. Timing Specifications

Parameter	Symbol	Test Condition/Comments	Min	Typ	Max	Unit
SPI PORT						
SCLK						
Frequency	f_{SCLK}				10	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		15			ns
Low	$t_{SCLKPWL}$		15			ns
$\overline{CS}$						
Setup Time	t_{CSS}	$\overline{CS}$ setup to SCLK rising edge	11			ns
Hold Time	t_{CSH}	$\overline{CS}$ hold from SCLK rising edge	5			ns
Pulse Width High	t_{CSPWH}	$\overline{CS}$ pulse width high	15			ns
MOSI						
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	5			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	5			ns
SWITCHING CHARACTERISTICS						
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge				
		Register 0x057 = 0x0050 (default)			21.5	ns
		Register 0x057 = 0x005F (maximum slew rate, maximum drive strength for SPI)			14	ns

Timing Diagram

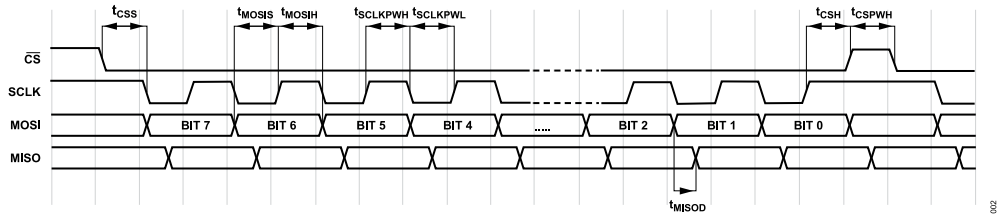

Figure 2. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
AVDD3 to AGND	−0.3 V to +3.9 V
DVDD to DGND	−0.3 V to +2.2 V
IOVDD to IOGND	−0.3 V to +3.9 V
GPIOx, MOSI, MISO, SCLK, $\overline{CS}$ to DGND	−0.3 V to +3.9 V
LEDxx to LGND	−0.3 V to +3.9 V
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CB-36-11[1]	42.15	0.98	°C/W

[1] The thermal resistance values are defined as per the JESD51-12 standard.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for ADPD7008

Table 7. ADPD7008, 36-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
CDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

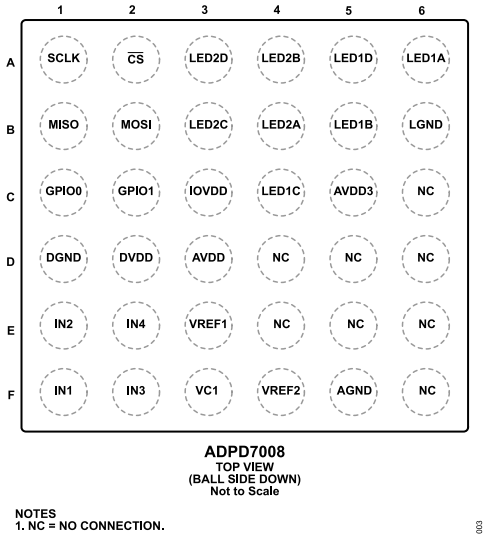

Figure 3. Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
D3	AVDD	Power	1.8 V Analog Power Supply.
C5	AVDD3	Power	3.3 V Analog Power Supply.
F5	AGND	Power	Analog Ground.
D2	DVDD	Power	1.8 V Digital Power Supply.
D1	DGND	Power	Digital Ground.
C3	IOVDD	Power	Input and Output Power Supply.
B6	LGND	Power	LED Ground.
E3	VREF1	Analog	ADC 1 Reference.
F4	VREF2	Analog	ADC 2 Reference.
F3	VC1	Analog	Output Voltage Source 1 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
F1	IN1	Analog	Current Input 1.
E1	IN2	Analog	Current Input 2.
F2	IN3	Analog	Current Input 3.
E2	IN4	Analog	Current Input 4.
A6	LED1A	Analog	LED Driver 1A.
B5	LED1B	Analog	LED Driver 1B.
C4	LED1C	Analog	LED Driver 1C.
A5	LED1D	Analog	LED Driver 1D.
B4	LED2A	Analog	LED Driver 2A.
A4	LED2B	Analog	LED Driver 2B.
B3	LED2C	Analog	LED Driver 2C.
A3	LED2D	Analog	LED Driver 2D.
E6	NC		No Connection.
F6	NC		No Connection.
E5	NC		No Connection.
E4	NC		No Connection.
C6	NC		No Connection.
D6	NC		No Connection.
D5	NC		No Connection.
D4	NC		No Connection.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type	Description
A2	$\overline{CS}$	Digital	SPI Chip Select Input.
A1	SCLK	Digital	SPI Clock Input.
B1	MISO	Digital	SPI Controller Input and Target Output.
B2	MOSI	Digital	SPI Controller Output and Target Input.
C1	GPIO0	Digital	General-Purpose Input and Output 0.
C2	GPIO1	Digital	General-Purpose Input and Output 1.

TYPICAL PERFORMANCE CHARACTERISTICS

DVDD = AVDD = 1.8 V, AVDD3 = 3.3 V, LGND = DGND = AGND = 0 V, and T_A = 25°C, unless otherwise noted.

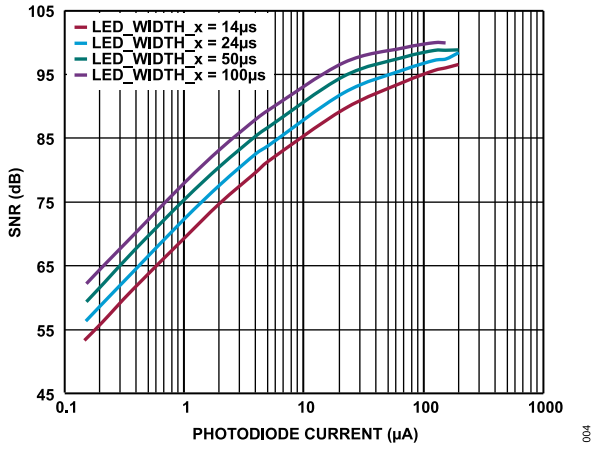

Figure 4. SNR vs. Photodiode Current, Number of Sequence Repeats = 1, TIA Gain = 100 kΩ

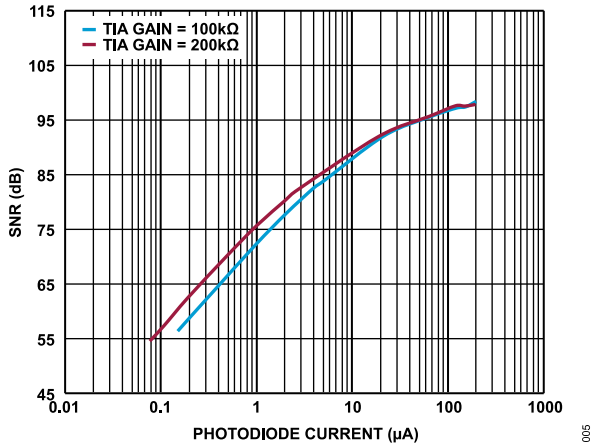

Figure 5. SNR vs. Photodiode Current, LED Width = 24 µs, Number of Sequence Repeats = 1

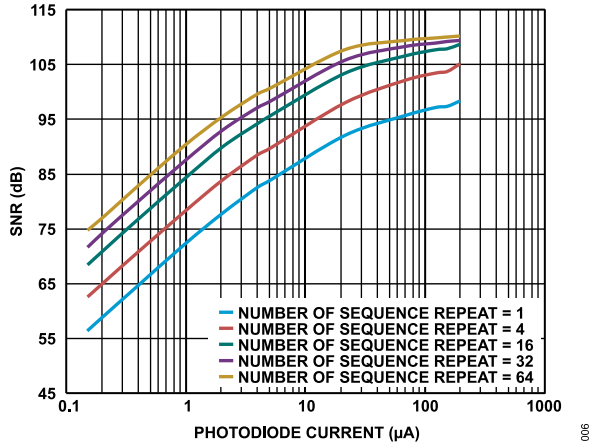

Figure 6. SNR vs. Photodiode Current, LED Width = 24 µs, TIA Gain = 100 kΩ

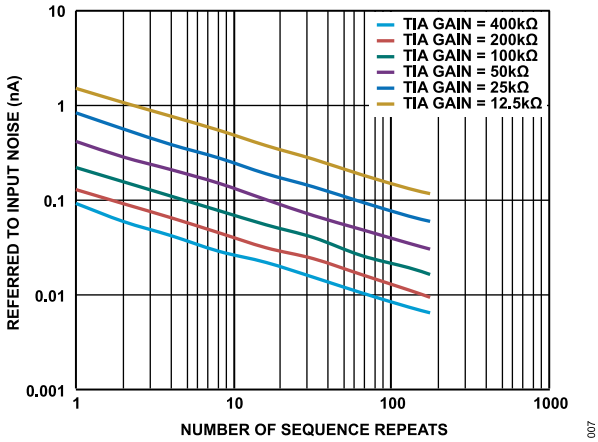

Figure 7. Referred to Input Noise vs. Number of Sequence Repeats

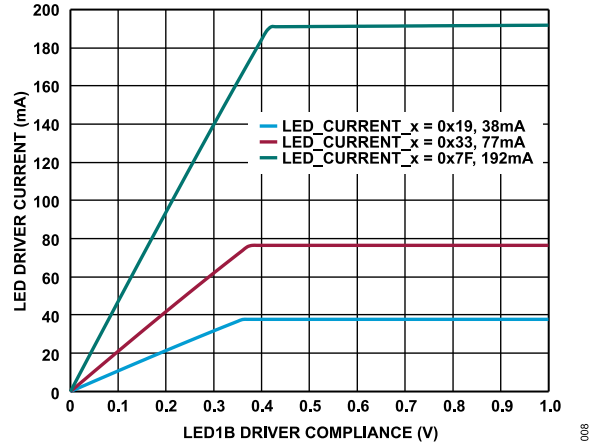

Figure 8. LED Driver Current vs. LED1B Driver Compliance, High SNR Mode

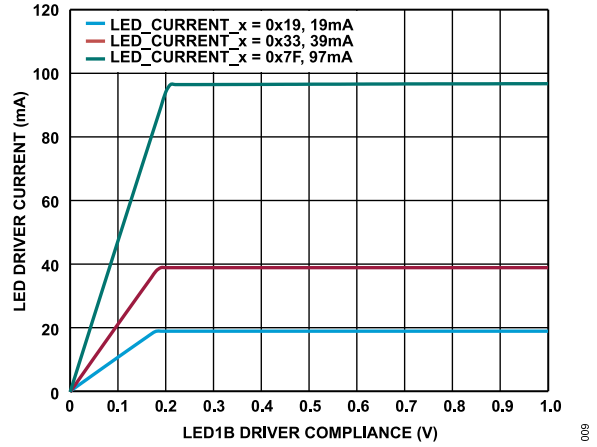

Figure 9. LED Driver Current vs. LED1B Driver Compliance, Low Compliance Mode

TYPICAL PERFORMANCE CHARACTERISTICS

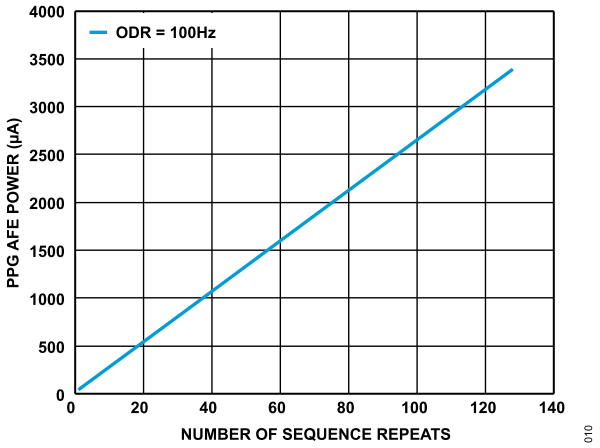

Figure 10. PPG AFE Power vs. Number of Sequence Repeats

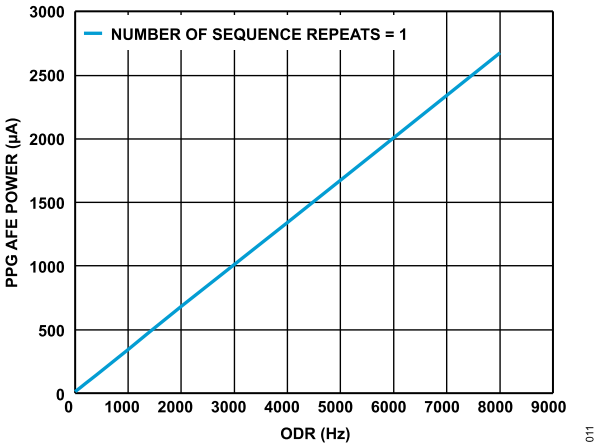

Figure 11. PPG AFE Power vs. ODR

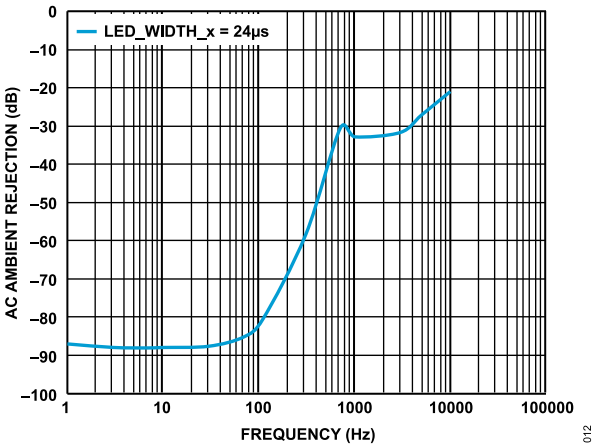

Figure 12. AC Ambient Rejection vs. Frequency

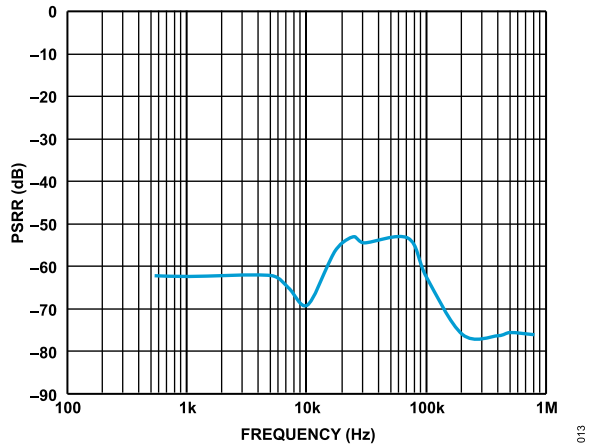

Figure 13. PSRR vs. Frequency, Photodiode Current = 8 µA

THEORY OF OPERATION

INTRODUCTION

The ADPD7008 is a vital signal monitoring AFE that comprises an optical measurement path (PPG) measurement path.

The PPG measurement path works as a transceiver that supports up to eight LEDs and four photodiode inputs. The current on the LEDs is programmable from two 7-bit LED drivers. The receiver path provides two high performance readout channels that can sample simultaneously and can be configured separately. Two high performance current DACs (IDACs) are implemented in each channel to provide first class ambient light suppression and large dynamic range in different application scenarios.

An internal state machine allows flexible control of this measurement path. The acquisition data can be stored in a 704-byte FIFO.

TIME SLOT OPERATION

An internal configurable controller handles the operation of the ADPD7008. This controller generates the timing needed to generate sampling regions comprising combinations of the three measurement paths and sleep periods. To facilitate the use of multiple signal chains, multiple time slots handle the access to different transmitters or receivers.

The system is characterized by the ODR, which determines the repetition periodicity of each enabled time slot. The enabled time slots are repeated at the time slot rate configured by the TIMESLOT_PERIOD_x bits.

There are 12 time slots (PPG_TSA to PPG_TSL) in the ADPD7008, as shown in Figure 14.

Each PPG time slot allows the creation of one or more LED pulses and modulate pulses, as well as the acquisition of the photodiode or other device current based on that stimulus. The operating parameters for each time slot are highly configurable.

Equation 1 determines the sampling rate (time slot rate), as follows:

$$Sampling\ Rate = Timer\ Clock\ Frequency\ (\text{Hz}) / TIMESLOT\_PERIODx \quad (1)$$

Table 9. Sources of Low Frequency Clock (LFCLK) and Timer Clock[1]

LFCLK	Timer Clock	ALT_CLOCKS	TM_CLK_GPIO_SEL
960 kHz Internal	960 kHz internal	0	N/A
960 kHz External	960 kHz external	1	N/A
960 kHz Internal	960 kHz internal	2	N/A
1 MHz External (Divided from 32 MHz)	1 MHz external (divided from 32 MHz)	3	N/A
960 kHz Internal	960 kHz external	4	1
960 kHz Internal	32 kHz external	4	0

[1] N/A means not applicable.

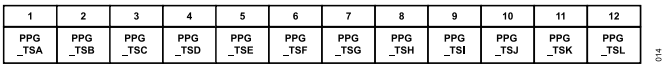

Figure 14. Time Slot Allocation

THEORY OF OPERATION

OPTICAL SIGNAL CHAIN

The optical signal path stimulates up to eight LEDs and measures the return signal on up to four separate current inputs. Twelve optical time slots enable 12 separate optical measurements per sampling period.

The analog inputs can be driven single-ended or in differential pairs. The four analog inputs can be multiplexed into a single channel or two independent channels, enabling simultaneous sampling of two sensors.

The optical signal chain consists of a TIA, an integrator that can also be configured as a buffer depending on the register setting, and an ADC. The digital block provides multiple operating modes, programmable timing, and block averaging.

Two independent LED drivers are provided that can each drive up to 200 mA. Two LED drivers can be enabled in any time slot and can be programmed from 1.57 mA to 200 mA monotonically, with a 7-bit register setting. The LED drivers enabled in any time slot can provide a combined maximum LED current of 400 mA.

When making optical measurements, ambient light rejection is automatic without the need of external control loops, dc current subtraction, or digital algorithms.

The LED driver is a current sink and is independent from the LED supply voltage and the LED type. The optical measurement path produces a high SNR for relatively low LED power, while greatly reducing the effect of ambient light on the measured signal.

Analog Signal Path

The analog signal path of the optical signal chain consists of four current inputs that can be configured as single-ended or differential pairs into one of four independent channels. The four channels can be sampled simultaneously for applications that require instantaneous sampling of four sensors.

Analog Input Multiplexer

The optical signal chain supports four analog input pins. Each input can be used as a single-ended input or as part of a differential pair. Figure 15 shows a single representation of the input switch matrix, which allows a programmable connection to the four optical channels. Each pair of inputs has a duplicate of this multiplexer: IN1 and IN2, and IN3 and IN4. The connections are programmable per time slot.

The PAIR12 and PAIR34 bits select whether the matching input pair is used as two single-ended inputs or as a differential pair. This selection is valid for all active time slots. The INP12_x and INP34_x bits specify whether the input pair is enabled during the corresponding time slot and, if enabled, which input is connected to which optical channel. Note that Channel 1 and Channel 2 support single-ended or differential inputs, while Channel 3 and Channel 4 only support a single-ended input.

The sleep conditions are used for any inputs that are not enabled. Sleep conditions are determined by the INP_SLEEP_12 and INP_SLEEP_34 bits, which specify the state for the input pairs during sleep and when the inputs are not active. Inputs are only considered active during the precondition and pulse regions for time slots where they are enabled.

Preconditioning of the sensor connected to the input is provided to set the operating point at the input before sampling. There are several different options for preconditioning determined by the PRECON_x bits. The PRECON_x bits are provided for each time slot to specify the precondition for enabled inputs or input pairs during the corresponding time slot. Preconditioning options include floating the inputs, VC1, an internal voltage reference signal for the TIA (TIA_VREF), a TIA input, and shorting the input pair. The preconditioning time at the start of each time slot is programmable using the PRE_WIDTH_x bits. The default preconditioning period is 8 µs.

The block diagram in Figure 15 shows the bias levels that can be switched into the input connections during sleep and preconditioning. These connections are not available during the sampling phase of a time slot in which the input is selected.

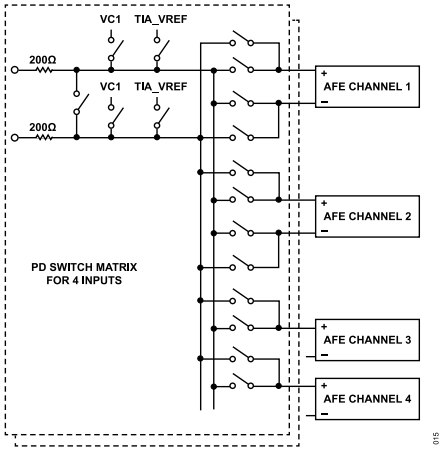

Figure 15. Switch Matrix Block Diagram

Ambient Light Cancellation

The ADPD7008 has three modes to perform ambient light cancellation, as follows:

- Coarse tuning only
- Coarse and fine tuning loop
- External microcontroller unit (MCU) control

Coarse tuning only mode and coarse and fine tuning loop mode are automatically controlled by the ADPD7008 without any software assistance. External MCU control mode allows tuning the ambient light rejection through an external algorithm.

Use the AMBIENT_CANCELLATION_x bits to choose the mode.

THEORY OF OPERATION

Coarse tuning mode works at the beginning of each PPG time slot. This mode measures the ambient light level and sets the ambient DAC code. This circuitry needs 48 µs to complete these activities and determine the baseline of the ambient DAC. Afterward, the PPG channel can start normal operation–for example, if in digital integration mode, the PPG receiver channel can start to take dark samples. This ambient baseline is used in the time slot if coarse tuning only mode is enabled.

If coarse and fine tuning loop mode is enabled, the coarse tuning circuit works the same way as in coarse tuning mode. However, the ambient DAC code updates after each dark sample measurement.

Select these two modes with the AMBIENT_CANCELLATION_x bits for system level design flexibility.

Coarse loop mode makes the measurement to find the accurate value of the ambient current. Then, the ambient DAC subtracts the ambient current at the beginning of the signal chain so that it does not corrupt the PPG signal measurement.

Both analog integration mode and digital integration mode can perform coarse loop ambient rejection.

The fine tuning loop updates the ambient information after each dark sample measurement. This feature is available only in digital integration mode.

The MCU mode allows the user to subtract the ambient current. The DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x bits are designed to allow the user to fill in the current ambient value, and the AFE then subtracts that value from the signal chain. DAC_AMBIENT_CH1_x and DAC_AMBIENT_CH2_x are 9-bit fields, with each LSB representing a 0.6 µA step in a 0 µA to 300 µA range.

LED DC Cancellation

Besides the ambient DAC, there is another IDAC at the input of each signal chain. This IDAC is used to subtract the unwanted dc component in the reflected LED to increase the dynamic range of the receiver channel.

These two IDACs are controlled by the MCU only. The DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x bits control the LED dc canceling, 7-bit IDAC with full scale.

The LED dc subtraction feature is available only for digital integration mode.

A certain amount of dc current can be subtracted from the AFE based on the top level optical and system design. DAC_LED_DC_CH1_x and DAC_LED_DC_CH2_x are 7-bit fields, with each LSB representing a 1.5 µA step in a 0 µA to 190 µA range.

LED Drivers

The optical path has two LED drivers, each of which is brought out to four LED driver outputs, providing a total of eight LED output drivers. The device can drive up to two LEDs simultaneously, one from each driver pair. The LED output driver is a current sink. Figure 16 shows an example of a single LED driver output pair.

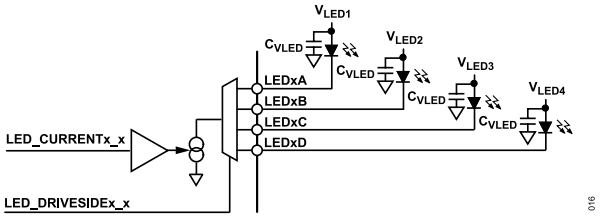

Figure 16. LED Driver Output Pair (C_{VLED} Are the Bypass Capacitors)

The LED driver output pins (LED1A, LED2A, LED1B, LED2B, LED1C, LED2C, LED1D, and LED2D) have a maximum allowable pin voltage of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LED driver output pins must not be confused with the supply voltages of the LEDs. V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LED output driver pins are connected to the cathode of the external LEDs. The compliance voltage is the amount of headroom voltage at the LED driver pins, measured with respect to ground, required to maintain the programmed LED current levels. The compliance voltage is a function of the current required.

FIFO

The FIFO is never written with partial packets of data. If there is not enough room for the data that is written to the FIFO for all enabled time slots and any selected status bytes, no data is written from any of the time slots during that period and the INT_FIFO_OFLOW status bit is set.

The order of samples written to the FIFO (if selected) is dark data followed by lit data. Table 10 shows the byte order for multibyte words.

Table 10. Byte Order for FIFO Writes

Size	Byte Order (After Shift)
8	[7:0]
16	[15:8], [7:0]
24	[23:16], [15:8], [7:0]
32	[31:24], [23:16], [15:8], [7:0]

The FIFO size is 704 bytes. When the FIFO is empty, a read operation returns 0xFF, and the INT_FIFO_UFLOW status bit is set.

PPG Data Format

At the end of each time slot, the selected data is written to the FIFO. The packet can include 0-, 8-, 16-, 24-, or 32-bit data for each of the dark data, signal data, or lit data values. The bit alignment of the data written to the FIFO is selectable with a shift of 0 bits to 31 bits, with saturation provided. Lower bits are ignored.

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The DARK_SIZE_x, LIT_SIZE_x and SIGNAL_SIZE_x bits select the number of bytes of each field to be written from 0 bytes to 4 bytes. When set to 0, no data is written for that data type. The DARK_SHIFT_x, LIT_SHIFT_x, and SIGNAL_SHIFT_x bits select the number bits to shift the output data to the right before writing the FIFO. If there are any significant bits at more significant bit positions than those selected, the data written to the FIFO is saturated.

The order of samples written to the FIFO (if selected) is signal data followed by dark data and then lit data. If both channels are enabled, all selected Channel 1 data values are written to the FIFO first, followed by the Channel 2 data.

For example, in modes that use dark data, the eight upper bits of the dark data can be stored with 24 appropriately selected bits from the signal data for each time slot. This method detects whether the ambient light is becoming large, while limiting the size of the amount of data transferred.

Figure 17 shows the PPG data format in the FIFO.

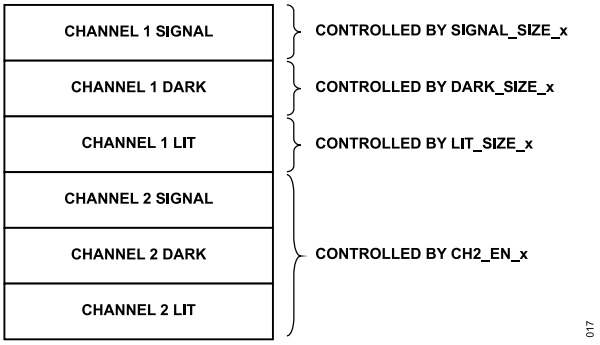

Figure 17. PPG Data Format

CLOCKING

Low Frequency Oscillator

A low frequency oscillator clocks the low speed state machine, which sets the time base used to control the sample timing, wake-up states, and overall operation. There are three options for low frequency oscillator generation. The first option is an internal 960 kHz oscillator. The second option is for the host to provide a low frequency oscillator externally. Finally, the low frequency oscillator can be generated by a divide by 32 of an external high frequency clock source at 32 MHz. When powering up the device, it is expected that the low frequency oscillator be enabled and left running continuously.

To operate with the on-chip low frequency oscillator, use the following writes. Set the OSC_960K_EN bit to 1 to turn on the internal oscillator. The internal 960 kHz clock frequency is set using the 10-bit OSC_960K_FREQ_ADJ bits.

If higher timing precision is required than can be provided by the on-chip low frequency oscillator, the low frequency oscillator can be driven directly from an external source provided on a GPIOx input. To enable an external low frequency clock, use the following writes. Enable one of the GPIOx inputs using the GPIO_PIN_CFGx bits. Next, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input to be used for the external low frequency oscillator. Set the ALT_CLOCKS bits to 0x1 to select an external low frequency oscillator.

In a third method, an external 32 MHz clock is used for both the high frequency clock and to be divided down to generate the low frequency clock. To use this method, follow the previous instructions for an external low frequency clock but set the ALT_CLOCKS bits to 0x3, and a divide by 32 used to generate the low frequency clock so that a 1 MHz clock is generated from the external 32 MHz clock.

For this low frequency, after power-on, the 960 kHz trim code in fuse of the ADPD7008 automatically loads, resulting in this 960 kHz clock being highly accurate. This operation is automatically handled by the chip, and the user must not take any additional steps.

High Frequency Oscillator

A 32 MHz high frequency oscillator is generated internally or can be provided externally. This high frequency clock clocks the high speed state machine, which controls the AFE operations during the time slots, such as LED timing and integration times.

The high frequency oscillator can be internally generated by setting the ALT_CLOCKS bits to 0x0 or 0x1. When selected, the internal 32 MHz oscillator is enabled automatically by the low speed state machine during the appropriate wake-up time or during the 32 MHz oscillator calibration routine.

The high frequency oscillator can also be driven from an external source. To provide an external 32 MHz high frequency oscillator, enable one of the GPIO inputs using the GPIO_PIN_CFGx bits. Then, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input for the external high frequency oscillator. Finally, write 0x2 or 0x3 to the ALT_CLOCKS bits to select an external high frequency oscillator. Writing 0x2 provides only the high frequency oscillator from the external source, whereas writing 0x3 generates both the low frequency oscillator and high frequency oscillator from the external 32 MHz source. When using an external 32 MHz oscillator, it must be kept running continuously for proper device operation.

TIME STAMP OPERATION

The time stamp feature is useful for calibrating the low frequency oscillator as well as providing the host with timing information during time slot operation. Timestamping is supported by the use of any GPIO as a time stamp request input, the CAPTURE_TIMESTAMP bit to enable capture of the time stamp trigger, a time counter running in the low frequency oscillator domain, and two output registers. The output bits include TIMESTAMP_COUNT_x, which holds the number of low frequency oscillator cycles between time stamp triggers, and TIMESTAMP_SLOT_DELTA, which holds

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the number of low frequency oscillator cycles remaining to the next time slot start.

The setup for using the time stamp operation is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Configure a GPIO to support the time stamp input using the appropriate GPIO_PIN_CFG_x bits. Select the matching GPIOx to provide the time stamp using the TIMESTAMP_ GPIO bits.
3. Configure the ADPD7008 for operation and enable the low frequency oscillator.
4. If the TIMESTAMP_SLOT_DELTA function is desired, start the time slot operation by placing the device in go mode using the OP_MODE bit (see Table 11). For low frequency oscillator calibration, it is only required that the low frequency oscillator is enabled. The device does not have to be in go mode for low frequency oscillator calibration.

Use the following procedure to capture the time stamp:

1. Set the CAPTURE_TIMESTAMP bit to 1 to enable the capture of the time stamp on the next rising edge of the selected GPIOx input.
2. The host provides the initial time stamp trigger on the selected GPIOx at an appropriate time.
3. The CAPTURE_TIMESTAMP bit is cleared when the timestamp signal is captured unless the TIMESTAMP_ ALWAYS_EN bit is set, in which case, the capture of the time stamp is always enabled. Reenable the capture if necessary.
4. The host provides a subsequent time stamp trigger on the selected GPIO at an appropriate time.
5. The number of low frequency oscillator cycles that occurred between time stamp triggers can be read from the TIMESTAMP_COUNT_x bits.

The host must continue to handle the FIFO data normally during time stamp processing.

If using a dedicated pin for a time stamp that does not have transitions other than the time stamp, set the TIMESTAMP_ ALWAYS_EN bit to avoid automatic clearing of the CAPTURE_ TIMESTAMP bit. This setting removes the need to enable the time stamp capture each time.

The host can also use TIMESTAMP_SLOT_DELTA to determine when the next time slot occurs. TIMESTAMP_SLOT_DELTA can determine the arrival time of the samples currently in the FIFO.

The time stamp trigger is edge sensitive and can be set to either trigger on the rising edge (default) or falling edge using TIMESTAMP_INV.

Low Frequency Oscillator Calibration

The time stamp circuitry can calibrate the 960 kHz low frequency oscillator circuit by adjusting the frequency to match the timing of the time stamp triggers. Simply compare the TIMESTAMP_COUNT_x value in low frequency oscillator cycles to the actual time stamp trigger period and adjust the OSC_960K_FREQ_ADJ value accordingly.

High Frequency Oscillator Calibration

The high frequency oscillator is calibrated by comparing multiples of its cycles with multiple cycles of the low frequency oscillator, which is calibrated to the system time. Calibration of the low frequency oscillator precedes calibration of the high frequency oscillator. The method for calibrating the high frequency oscillator is as follows:

1. Set OSC_CAL_ENABLE = 1 to enable the oscillator calibration circuitry.
2. Write 1 to the OSC_32M_CAL_START bit.
3. The ADPD7008 automatically powers up the high frequency oscillator.
4. The device automatically waits for the high frequency oscillator to be stable.
5. An internal counter automatically counts the number of 32 MHz high frequency oscillations that occur during 128 cycles of the 960 kHz low frequency oscillator.
6. The OSC_32M_CAL_COUNT bits update with the final count.
7. The 32 MHz oscillator automatically powers down following calibration unless time slots are active.
8. The device resets the OSC_32M_CAL_START bit indicating the count has updated.

The OSC_32M_FREQ_ADJ bits adjust the frequency of the 32 MHz oscillator to the desired frequency. When using an external low frequency oscillator, the 32 MHz oscillator calibration is performed with respect to the externally provided low frequency oscillator.

When the calibrations of the low frequency and high frequency oscillators are complete, set CLK_CAL_ENA = 0 to disable the clocking of the oscillator calibration circuitry to reduce the power consumption. CLK_CAL_ENA defaults to 0 so that the calibration circuitry is disabled by default.

EXECUTION MODES

A state machine in the low frequency oscillator clock domain controls sleep times, wake-up cycles, and the start of time slot operations. The low frequency oscillator serves as the time base for all time slot operations, controls the sample rates, and clocks the low frequency state machine. This state machine controls all operations and is controlled by the OP_MODE bit.

Table 11. OP_MODE Bit Setting Descriptions

OP_MODE Setting	Mode	Description
000	Standby	All operations stopped. Time slot actions reset. Low power standby state.
001	Go	Transitioning to this state from standby mode starts time slot operations.

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Table 11. OP_MODE Bit Setting Descriptions (Continued)

OP_MODE Setting	Mode	Description
011	ADC test mode	This mode goes through the normal wake-up sequence and then does continuous ADC cycles based on the PPG Time Slot A setting
101	Repeat selected time slots without sleep	This mode does one normal wake-up sequence and then cycles through the enabled time slot sequences without going to sleep between.
111	Reserved	Reserved.

At power-up and following any subsequent reset operations, the ADPD7008 is in standby mode. The user can write 0 to the OP_MODE bit to immediately stop operations and return to standby mode.

The time slots are enabled by the PPG_TIMESLOT_EN bit in the OPMODE register (see Register 0x010 in Table 15).

Set PPG_TIMESLOT_EN to a certain value to enable the corresponding PPG time slot.

After enabling the desired time slots, set the OP_MODE bit to 1 to start the chip operation.

Register writes that affect operating modes cannot occur during go mode. The user must enter standby mode before changing the control registers. Standby mode resets the digital portion of the ADC, all of the pulse generators, and the state machine.

When OP_MODE is set to 1, the device immediately starts the first wake-up sequence and time slot operations unless using an external synchronization trigger. If using an external synchronization trigger, the device enters the sleep state before the first wake-up and time slot regions begin.

HOST INTERFACE

The ADPD7008 uses an SPI to communicate with other devices. The device also provides numerous FIFO, error, and threshold status bits, each of which can be provided by an interrupt function from a GPIO, read from status registers, or appended as optional status bytes at the end of a FIFO packet.

Interrupt Status Bits

FIFO Threshold Interrupt

The FIFO threshold interrupt status bit, INT_FIFO_TH, is set when the number of bytes in the FIFO exceeds the value stored in the FIFO_TH register. The INT_FIFO_TH bit is cleared automatically when a FIFO read reduces the number of bytes below the value in the FIFO_TH register, which allows the user to set an appropriate data size for their host needs.

The INT_FIFO_TH bit does not trigger if the FIFO byte count exceeds the threshold in the middle of any write of complete data. Instead, the INT_FIFO_TH bit is set at the next write to the FIFO.

For example, if only PPG TSA is running, it only writes 4-byte lit data to the FIFO. Figure 18 shows the data in the FIFO.

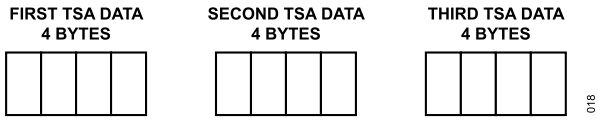

Figure 18. FIFO Threshold Interrupt Example

If the threshold is set as 4, the interrupt triggers at the beginning of the second TSA data write to the FIFO. If the threshold is set as 5, 6, or 7, the INT_FIFO_TH bit does not trigger until the write of the third TSA data. This method can help prevent any partial data read from the FIFO.

Clearing Interrupt Status Bits

All status bits are set regardless of whether the status bit is routed to one of the interrupt outputs, Interrupt X or Interrupt Y. The status bits are independent of the interrupt enable bits. The status bits are always set by the corresponding event. The interrupt bits stay set until they are either manually or automatically cleared.

The user can manually clear a given interrupt by writing a 1 to the matching interrupt status bit. In addition, the data interrupt status bits can be configured to clear automatically. When the INT_ACLEAR_FIFO bit is set, the appropriate interrupt status bit is automatically cleared when any matching FIFO register is read. Automatic clearing of the interrupt status bits removes the need to manually clear these interrupts.

Optional Status Bytes

There is an option to append each data packet with status bits. This option is useful for hosts that cannot spare an interrupt channel to service. The status bytes can each be individually selected in the FIFO_STATUS_BYTES register. Each bit in the FIFO_ STATUS_BYTES register enables a status byte that is appended to the data packet in the FIFO. If any bit in the FIFO_STATUS_ BYTES register is set to 1, the byte that is appended to the data packet contains the status bits.

The 4-bit sequence number cycles from 0 to 15 and is incremented with a wraparound every time the time slot sequence completes. This sequence number can also be made available bitwise on the GPIOx pins.

Interrupt Outputs, Interrupt X and Interrupt Y

The ADPD7008 supports two separate interrupt outputs, Interrupt X and Interrupt Y. Each interrupt has the option to be driven to any of the two GPIOx pins. The two different interrupt outputs can be generated for a host processor if desired. For example, the FIFO threshold interrupt, INT_FIFO_TH, can be routed to Interrupt X and used to drive the direct memory access (DMA) channel of the host, while the INT_FIFO_OFLOW and INT_FIFO_UFLOW interrupts

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can be routed to Interrupt Y and used to drive an additional host interrupt pin.

For each interrupt, there is an associated Interrupt X and Interrupt Y enable bit. See Table 16 for a full list of available interrupts that can be brought out on Interrupt X and Interrupt Y. The logic for the Interrupt X and Interrupt Y function is a logic AND of the status bit with its matching enable bit. All enabled status bits are then logically OR'ed to create the interrupt function. The enable bits do not affect the status bits.

General-Purpose I/Os

The ADPD7008 provides two general-purpose I/O pins: GPIO0 and GPIO1. These GPIOs can be used as previously described in the Interrupt Outputs, Interrupt X and Interrupt Y section for interrupt outputs or for providing external clock signals to the device. The GPIOs can also be used for many different control signals, as synchronization controls to external devices, as well as test signals that are useful during system debugging. All of the available signals that can be brought out on a GPIOx pin are listed in Table 16.

IOVDD Supply Voltage Consideration

The ADPD7008 can operate with IOVDD as low as 1.7 V and as high as 3.6 V. LOW_IOVDD_EN in Register 0x0057 is set to 0x1 for IOVDD lower than 3 V. 0x1 is the default value for this bit because the typical IOVDD value is 1.8 V.

If 3 V or higher is supplied for IOVDD, the LOW_IOVDD_EN bit must be set to 0x0 for proper operation.

SPI

The ADPD7008 contains an SPI port that operates synchronously with its input clocks.

The ADPD7008 has an internal power-on reset circuit that sets the device into a known idle state during the initial power-up. After the power-on reset is released, approximately 2 µs to 6 µs after the DVDD supply is active, there is an initialization state that sets the register default values. This initialization state lasts approximately 15 µs to 20 µs. The device can then be read and written through the SPI.

The registers are accessed using addresses within a 15-bit address space. Each address references a 15-bit register with one address reserved for the FIFO read accesses. For SPIs, reads and writes auto-increment to the next register if additional words are accessed as part of the same access sequence. This automatic address increment occurs for all addresses except the FIFO address, one less than the FIFO address and the last used address, which is 0x351. Reads from the FIFO address continue to access the next byte from the FIFO.

SPI Operations

The SPI single register write operation is shown in Figure 19. The first two bytes contain the 15-bit register address and specify that a write is requested. The remaining two bytes are the 16 data bits to write to the register. The register write occurs only when all 16 bits are shifted in prior to deassertion of the $\overline{CS}$ signal.

In addition, multiple registers can be written if additional 16-bit data is shifted in before deassertion of the $\overline{CS}$ signal. The register address automatically increments to the next register after each 16 bits of data.

The SPI single register read operation is shown in Figure 20. The first two bytes contain the 15-bit register address and specify that a read is requested. Register bits are shifted out starting with the MSB. In addition, multiple registers can be read if additional 16-bit data is shifted out prior to deassertion of the $\overline{CS}$ signal.

It is recommended that reading from the FIFO is performed byte wise. There is no requirement to read multiples of 16 bits.

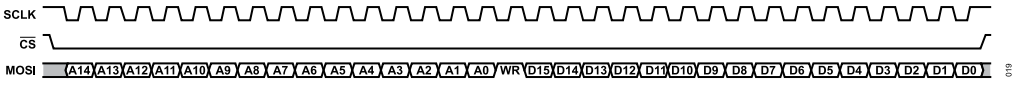

Figure 19. SPI Write Operation

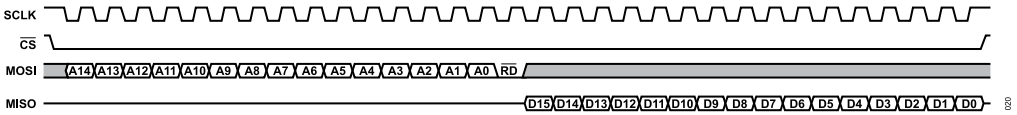

Figure 20. SPI Read Operation

APPLICATIONS INFORMATION

OPTICAL PATH

Digital Integration Mode

The ADPD7008 supports a digital integration mode in the optical path to accommodate sensors that require longer pulses. Digital integration mode allows the system to use a larger LED duty cycle, which can result in the highest achievable SNR levels.

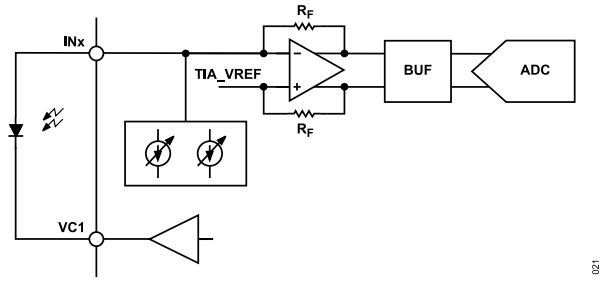

Figure 21. Signal Path for Digital Integration Mode

In digital integration mode, the integrator is configured as a buffer, resulting in the signal path shown in Figure 21. Digital integration regions are configured by the user and separated into lit and dark regions. The LED is pulsed in the lit region, and the LED is off in the dark region. ADC samples are taken at 1 µs intervals within the lit and dark regions and are then digitally integrated. The integration of the ADC samples from the dark region is subtracted from the integration of the ADC samples from the lit region, and the result is written into the relevant FIFO. Both signal and dark values can be written to the FIFO.

The ADPD7008 supports one-region and two-region digital integration modes. In one-region digital integration mode, an equal number of dark and lit samples are taken where all of the dark samples are taken in the dark region just before the lit region. One-region digital integration mode is shown in the timing diagram in Figure 22.

In two-region digital integration mode, an equal number of dark and lit samples are taken. However, the dark region is split such that half of the samples are taken in the dark region before the lit region, and the other half is taken in the dark region following the lit region. The two-region digital integration mode results in higher ambient light rejection than the one-region digital integration mode in situations with a varying ambient light level. A timing diagram for two-region digital integration mode is shown in Figure 23.

The signal data for one-region digital integration mode that reads from the FIFO follows:

$$Signal = (I_{PD} \times R_{TIA} \times TIA\_CONFIG \times BUF\_GAIN \times NUM\_INT\_x \times NUM\_REPEAT\_x)/(146\ \mu V/LSB) \quad (2)$$

where:
I_{PD} is the PD current.
TIA_CONFIG is the TIA configuration. BUF_*GAIN* is the buffer gain.

The signal data for two-region digital integration mode that reads from the FIFO follows:

$$Signal = ((I_{PD} \times R_{TIA} \times TIA\_CONFIG \times BUF\_GAIN \times NUM\_INT\_x \times NUM\_REPEAT\_x)/(146\ \mu V/LSB)) \times 2 \quad (3)$$

The AFE_PATH_CFG_x, TIA_GAIN_CHx_x, AFE_BUFFER_GAIN_x, and AFE_BUFFER_CAP_x bits must follow a certain combination in digital integration mode (both one-region mode and two-region mode). Table 12 shows the recommended settings of these bits. The TIA gain setting is independent of these settings.

Table 12. Bit Settings for AFE Path in Digital Integration Mode

Bit Name	Recommended Setting
AFE_PATH_CFG_x	0x28
TIA_GAIN_CHx_x	0x3
AFE_BUFFER_GAIN_x	0x3
AFE_BUFFER_CAP_x	0x1

The result of the configurations of the bits in Table 12 is the 1× TIA configuration with a buffer gain = 2.

Table 13 shows the relevant register settings for the digital integration modes of operation. The MIN_PERIOD_x bits must be set manually with the proper period because the minimum period is not automatically calculated in digital integration mode.

The recommended MIN_PERIOD_x setting for one-region digital integration mode is as follows:

$$MIN\_PERIOD\_x = NUM\_INT\_x \times 2 + (2 + t_D) \times 2$$

The recommended MIN_PERIOD_x setting for two-region digital integration mode is as follows:

$$MIN\_PERIOD\_x = NUM\_INT\_x \times 4 + t_D \times 2 + 6\ \mu s$$

The t_D value is the response time of the optical device. The 6 µs time is essential for the ambient fine loop update.

APPLICATIONS INFORMATION

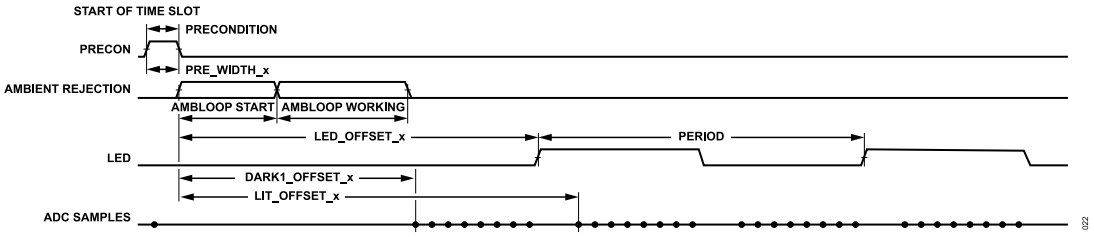

Figure 22. One-Region Digital Integration Mode Timing Diagram

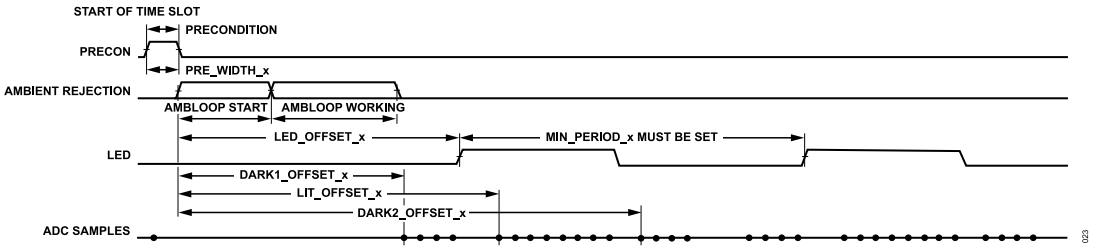

Figure 23. Two-Region Digital Integration Mode Timing Diagram

Table 13. Relevant Settings for Digital Integration Modes, for Example, for Time Slot A

Group	Time Slot A Register Address	Bit Field Name	Description
Signal Path Setup	0x0120, Bits[13:11]	SAMPLE_TYPE_A	Set to 0x2 for one-region digital integration mode. Set to 0x3 for two-region digital integration mode.
	0x0121, Bits[6:0]	AFE_PATH_CFG_A	Set to 0x28 for TIA, buffer, and ADC. Use 1x TIA configuration.
	0x0122, Bits[7:0]	INPxx_A	Enable desired inputs.
	0x0123, Bits[14:12]	PRECON_A	Set to 0x5 to precondition anode of photodiode to TIA_VREF.
	0x0123, Bits[1:0]	VC1_SELECT_A	Set to 0x2 to set ~215 mV reverse bias across photodiode.
	0x0124, Bits[5:0]	TIA_GAIN_CHx_A	Select TIA gain.
	0x0124, Bits[9:8]	AFE_TRIM_VREF_A	Set to 0x2 to set TIA_VREF = 0.8855 V.
	0x0124, Bits[12:11]	AFE_BUFFER_GAIN_A	Buffer gain selection. Set to 2 to select buffer gain = 2.
	0x125, Bits[13:12]	AFE_BUFFER_CAP_A	Buffer feedback capacitor selection. Set to 0x1 to 12.6 pF.
Timing	0x012A, Bits[15:8]	NUM_INT_A	Set to the number of desired ADC conversions in the dark and lit regions.
	0x012A, Bits[7:0]	NUM_REPEAT_A	Number of sequence repeats.
	0x012B, Bits[9:0]	MIN_PERIOD_A	Set the period. Automatic period calculation is not supported in digital integration mode.
	0x0138, Bits[8:0]	LIT_OFFSET_A	Set to the time of the first ADC conversion in the lit region.
	0x0139, Bits[6:0]	DARK1_OFFSET_A	Set to the time of the first ADC conversion in the Dark 1 region.
	0x0139, Bits[15:7]	DARK2_OFFSET_A	Set to the time of the first ADC conversion in the Dark 2 region. Only used in two-region digital integration mode.
LED Settings	0x0129, Bits[1:0]	LED_MODEx_A	Select LED mode.
	0x0129, Bits[7:4]	LED_DRIVESIDEx_A	Select LED for time slot used.
	0x0128, Bits[14:8], Bits[6:0]	LED_CURRENTx_A	Set LED current for selected LED.
	0x012C, Bits[7:0]	LED_OFFSET_A	Sets start time of first LED pulse in 1 µs increments.
	0x012C, Bits[15:8]	LED_WIDTH_A	Sets width of LED pulse in 1 µs increments.

APPLICATIONS INFORMATION

Timing Recommendations for Digital Integration Mode

When setting the timing for digital integration mode, it is important to place the ADC samples such that the signal being sampled is given time to settle before the sample being taken. Photodiode capacitance and the TIA settling time affect the settling time of the input signal.

If automatic ambient light rejection is on (AMBIENT_CANCELLATION_x is set to either 1 (01) or 2 (10) decimal), time is needed at the beginning of each time slot to enable the ambient rejection loop. The start-up time of this loop is 18 µs, and the working time of this loop is 30 µs.

The TIA_SAT_DET internal block must be turned on to speed up the TIA settling. Speeding up the TIA settling can help the TIA enter a normal working state quickly to make the automatic ambient rejection loop more accurate.

After the ambient loop completes, the first ADC sample of dark data can be enabled. The DARK1_OFFSET_x setting must be equal or larger than the ambient loop working time (48 µs).

Figure 24 shows an example of the proper placement of the ADC sampling edges.

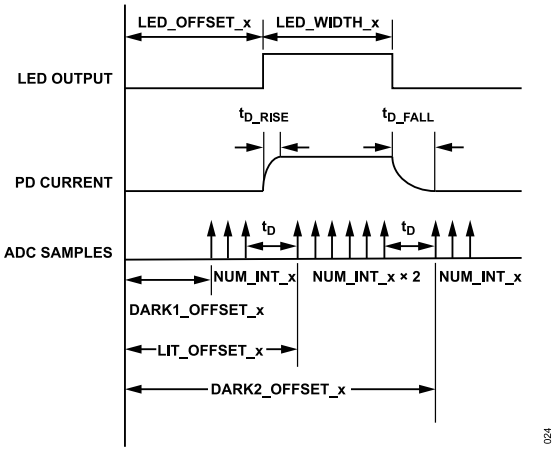

Figure 24. Proper Placement of ADC Sampling Edges in Digital Integration Mode

The recommended DARK1_OFFSET_x setting after the automatic ambient loop completes is 48 µs, or 10 µs if automatic ambient rejection is not turned on.

As shown in Figure 24, different optical devices, including the LED and photodiode, have different response times. t_{D_RISE} is the rising time of the photodiode current, and t_{D_FALL} is the falling time of the photodiode current. t_D is either t_{D_RISE} or t_{D_FALL}, depending on which one is bigger.

See the following equations to calculate the timing:

$$LED\_OFFSET\_x = DARK1\_OFFSET\_x + (NUM\_INT\_x + t_D - t_{D\_RISE}) \quad (4)$$

$$LIT\_OFFSET\_x = LED\_OFFSET\_x + t_{D\_RISE} \quad (5)$$

$$DARK2\_OFFSET\_x = LED\_OFFSET\_x + LED\_WIDTH\_x + t_D \quad (6)$$

These values must be characterized in the final application. These settings only apply to two-region digital integration mode.

Table 14. Empirical Values for Two-Region Digital Integration Mode

Optical Device	Green (µs)	Red (µs)	Infrared (µs)
LED_WIDTH_x	24	24	36
PERIOD_x	58	60	138
NUM_INT_x	10	9	13
LED_OFFSET_x	60	59	91
LIT_OFFSET_x	64	65	101
DARK1_OFFSET_x	48	48	48
DARK2_OFFSET_x	90	91	167
t_{D_RISE}	4	6	10
t_{D_FALL}	6	8	40

Optimizing Sampling Sequence

If the empirical value is not appropriate for the measurement, optimize the sampling sequence.

See the following reference method for sweeping the curve (this example is based on TSA Channel 1 in a dark environment):

1. Enable the following settings:
   - One-region digital integration mode
   - 1× TIA configuration
   - AFE_TRIM_VREF_A = 3
   - AMBIENT_CANCELLATION_A = 0
   - NUM_INT_A = 1
   - NUM_REPEAT_A = 1
   - DARK1_OFFSET_A = 10
   - LED_OFFSET_A = 20
   - LED_WIDTH_A = 80
   - LIT_OFFSET_A = 130
   - MIN_PERIOD_A = 160
2. Power on the optical devices and enable TSA Channel 1.
3. Collect about 100 lit data values (remove the first 10 data values) and calculate the mean value.
4. Sweep the LIT_OFFSET_A bit from 130 to 10 and reproduce the result from Step 3.
5. Plot the mean value of the lit data and LIT_OFFSET_A. The response time of the optical device (for example, OSRAM FIREFLY® CT DBLP31.12) is shown in Figure 25.

When collecting the lit data with the LIT_OFFSET_A bit changing, the data is lower than 16384 (unsaturated).

APPLICATIONS INFORMATION

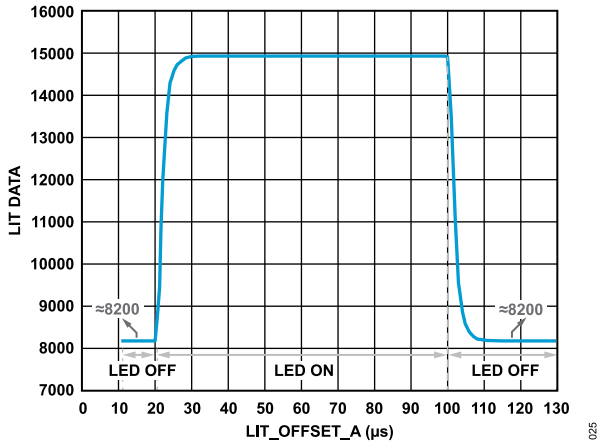

Figure 25. Timing of OSRAM FIREFLY CT DBLP31.12 (Green LED)

DESIGN GUIDE

The ADPD7008 is a vital sign monitoring AFE. The performance of the device can be adversely impacted by the PCB layout, especially for the analog input interfaces.

Power Rails

For the power supply, decouple the AVDD, AVDD3, DVDD, and IOVDD pins with a 0.1 µF or larger ceramic chip capacitor to the PCB ground plane placed near the power pins. It is recommended that all decoupling capacitors use individual vias to the PCB ground plane to avoid mutual impedance coupling between decoupled supplies when sharing vias.

Optical Channel

For the PPG channel, decouple the VREF1 pin and VREF2 pin to the PCB ground plane with a 1.0 µF ceramic capacitor. The voltage on the VREF1 pin and VREF2 pin is nominally 1.2 V. Therefore, a 6.3 V rated ceramic capacitor is adequate for this purpose. The most critical aspect of the PCB layout of the ADPD7008 is the handling of the IN1, IN2, IN3, and IN4 nodes. Because photodiode input is sensitive to noise, and any parasitic capacitive coupling to the pin can result in additional noise, it is recommended that the photodiode input trace in the layout be as short as possible and fully guarded by the ground plane.

For example, for a 6-layer stack design, place the chip in the top layer with the optical components in the bottom layer. Therefore, it is recommended to make the IN1, IN2, IN3, and IN4 trace length in the top short to avoid parasitic effects. In the bottom layer, the IN1, IN2, IN3, and IN4 traces and the photodiode anode are fully guarded with the ground shape and trace. VC1 and the photodiode cathode are also guarded with the ground plane. Layer 5 is filled with a ground plane for reference. Keep the analog input signals away from other digital or noisy signals.

REGISTER SUMMARY

Table 15. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x000	FIFO_STATUS	[15:8]	CLEAR_FIFO	INT_FIFO_UFLOW	INT_FIFO_OFLOW	INT_FIFO_TH	FIFO_INIT_DONE_STATUS	FIFO_BYTE_COUNT[10:8]			0x0000	R/W
		[7:0]	FIFO_BYTE_COUNT[7:0]									
0x001	INT_STATUS_TS1	[15:8]	RESERVED				INT_PPG_LEV0_L	INT_PPG_LEV0_K	INT_PPG_LEV0_J	INT_PPG_LEV0_I	0x0000	R/W
		[7:0]	INT_PPG_LEV0_H	INT_PPG_LEV0_G	INT_PPG_LEV0_F	INT_PPG_LEV0_E	INT_PPG_LEV0_D	INT_PPG_LEV0_C	INT_PPG_LEV0_B	INT_PPG_LEV0_A		
0x002	INT_STATUS_TS2	[15:8]	RESERVED				INT_PPG_LEV1_L	INT_PPG_LEV1_K	INT_PPG_LEV1_J	INT_PPG_LEV1_I	0x0000	R/W
		[7:0]	INT_PPG_LEV1_H	INT_PPG_LEV1_G	INT_PPG_LEV1_F	INT_PPG_LEV1_E	INT_PPG_LEV1_D	INT_PPG_LEV1_C	INT_PPG_LEV1_B	INT_PPG_LEV1_A		
0x006	FIFO_TH	[15:8]	RESERVED						FIFO_TH[9:8]		0x000C	R/W
		[7:0]	FIFO_TH[7:0]									
0x007	INT_ACLEAR	[15:8]	INT_ACLEAR_FIFO	RESERVED							0x8000	R/W
		[7:0]	RESERVED									
0x008	CHIP_ID	[15:8]	VERSION								0x00C6	R
		[7:0]	CHIP_ID									
0x009	OSC32M	[15:8]	RESERVED							OSC_32M_EFUSE_CTRL	0x0080	R/W
		[7:0]	OSC_32M_FREQ_ADJ									
0x00A	OSC32M_CAL	[15:8]	OSC_32M_CAL_START	OSC_32M_CAL_COUNT[14:8]							0x0000	R/W
		[7:0]	OSC_32M_CAL_COUNT[7:0]									
0x00B	OSC960K	[15:8]	CAPTURE_TIMESTAMP	RESERVED			OSC_960K_EFUSE_CTRL	OSC_CAL_ENABLE	OSC_960K_FREQ_ADJ[9:8]		0x0AB2	R/W
		[7:0]	OSC_960K_FREQ_ADJ[7:0]									
0x00D	TS_FREQ	[15:8]	TIMESLOT_PERIOD_L[15:8]								0x2580	R/W
		[7:0]	TIMESLOT_PERIOD_L[7:0]									
0x00E	TS_FREQH	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED	TIMESLOT_PERIOD_H								
0x00F	SYS_CTL	[15:8]	SW_RESET	RESERVED			LEAD_ON_MODE	ALT_CLOCKS			0x0000	R/W
		[7:0]	ALT_CLK_GPIO		LP_MODE_SLEEP	GO_SLEEP	RANDOM_SLEEP	TM_CLK_GPIO_SEL	OSC_960K_EN	RESERVED		
0x010	OPMODE	[15:8]	RESERVED								0x0000	R/W
		[7:0]	PPG_TIMESLOT_EN				RESERVED	OP_MODE				
0x011	STAMP_L	[15:8]	TIMESTAMP_COUNT_L[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_L[7:0]									
0x012	STAMP_H	[15:8]	TIMESTAMP_COUNT_H[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_H[7:0]									
0x013	STAMPDELTA	[15:8]	TIMESTAMP_SLOT_DELTA[15:8]								0x0000	R
		[7:0]	TIMESTAMP_SLOT_DELTA[7:0]									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x014	INT_ENABLE_XD	[15:8]	INTX_EN_FIFO_TH	INTX_EN_FIFO_UFLOW	INTX_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x015	INT_ENABLE_YD	[15:8]	INTY_EN_FIFO_TH	INTY_EN_FIFO_UFLOW	INTY_EN_FIFO_OFLOW	RESERVED					0x0000	R/W
		[7:0]	RESERVED									
0x01E	FIFO_STATUS_BYTES	[15:8]	RESERVED							ENA_STAT_LEVX	0x0100	R/W
		[7:0]	ENA_STAT_LEV1	ENA_STAT_LEV0	ENA_SEQ_NUM	RESERVED						
0x020	INPUT_SLEEP	[15:8]	RESERVED								0x0000	R/W
		[7:0]	INP_SLEEP_34				INP_SLEEP_12					
0x021	INPUT_CFG	[15:8]	RESERVED								0x0000	R/W
		[7:0]	RESERVED		VC1_SLEEP		RESERVED		PAIR34	PAIR12		
0x022	GPIO_CFG	[15:8]	GPIO_SLEW		GPIO_DRV		RESERVED			GPIO_PIN_CFG2, Bit 2	0x0000	R/W
		[7:0]	GPIO_PIN_CFG2[1:0]		GPIO_PIN_CFG1			GPIO_PIN_CFG0				
0x023	GPIO01	[15:8]	GPIOOUT1								0x0000	R/W
		[7:0]	GPIOOUT0									
0x025	GPIO_IN	[15:8]	RESERVED								0x0000	R
		[7:0]	RESERVED				GPIO_INPUT					
0x026	GPIO_EXT	[15:8]	RESERVED							GOUT_SLEEP	0x0000	R/W
		[7:0]	TIMESTAMP_INV	TIMESTAMP_ALWAYS_EN	TIMESTAMP_GPIO		RESERVED	EXT_SYNC_EN	EXT_SYNC_GPIO			
0x02F	FIFO_DATA	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x044	EFUSE	[15:8]	EFUSE_REFRESH	RESERVED							0x0005	R/W
		[7:0]	RESERVED					EFUSE_EN		EFUSE_REG_EN		
0x057	IO_ADJUST	[15:8]	RESERVED								0x0050	R/W
		[7:0]	RESERVED	LOW_IOVDD_EN	RESERVED		SPI_SLEW		SPI_DRV			
0x120	TS_CTRL_A	[15:8]	RESERVED		SAMPLE_TYPE_A			RESERVED	TIMESLOT_OFFSET_A[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_A[7:0]									
0x121	TS_PATH_A	[15:8]	PRE_WIDTH_A				AMBIENT_CANCELLATION_A		GOUT_A	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_A								
0x122	INPUTS_A	[15:8]	INP4_SEL_A		INP3_SEL_A		INP2_SEL_A		INP1_SEL_A		0x0000	R/W
		[7:0]	INP34_A				INP12_A					
0x123	CATHODE_A	[15:8]	RESERVED	PRECON_A			RESERVED		AFE_VREF_AMB_SEL_A		0x0200	R/W

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	VC1_AMB_SEL_A		VC1_PULSE_A		VC1_ALT_A		VC1_SEL_A			
0x124	AFE_TRIM_1_A	[15:8]	AFE_TIA_SAT_DETECT_EN_A	RESERVED		AFE_BUFFER_GAIN_A		VREF_PULSE_A	AFE_TRIM_VREF_A		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_A		TIA_GAIN_CH2_A			TIA_GAIN_CH1_A				
0x125	AFE_TRIM_2_A	[15:8]	RESERVED			AFE_BUFFER_CAP_A	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_A			TIA_GAIN_CH3_A				
0x126	AFE_DAC_1_A	[15:8]	DAC_AMBIENT_CH1_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_A, Bit 0	DAC_LED_DC_CH1_A								
0x127	AFE_DAC_2_A	[15:8]	DAC_AMBIENT_CH2_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_A, Bit 0	DAC_LED_DC_CH2_A								
0x128	LED_POW12_A	[15:8]	RESERVED	LED_CURRENT2_A							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_A								
0x129	LED_MODE_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_A		LED_DRIVESIDE1_A		RESERVED		LED_MODE2_A	LED_MODE1_A		
0x12A	COUNTS_A	[15:8]	NUM_INT_A								0x0101	R/W
		[7:0]	NUM_REPEAT_A									
0x12B	PERIOD_A	[15:8]	RESERVED	COARSE_LOOP_WIDTH_A	MOD_TYPE_A		RESERVED		MIN_PERIOD_A[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_A[7:0]									
0x12C	LED_PULSE1_A	[15:8]	LED_WIDTH_A								0x0210	R/W
		[7:0]	LED_OFFSET_A									
0x12D	AFE_DAC_3_A	[15:8]	DAC_AMBIENT_CH3_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_A, Bit 0	DAC_LED_DC_CH3_A								
0x12E	AFE_DAC_4_A	[15:8]	DAC_AMBIENT_CH4_A[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_A, Bit 0	DAC_LED_DC_CH4_A								
0x12F	THRESH0_A	[15:8]	RESERVED			THRESH0_SHIFT_A					0x0000	R/W
		[7:0]	THRESH0_VALUE_A									
0x130	MOD_PULSE_A	[15:8]	MOD_WIDTH_A								0x0001	R/W

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[7:0]	MOD_OFFSET_A									
0x131	PATTERN 1_A	[15:8]	LED_DISABLE_A				MOD_DISABLE_A				0x0000	R/W
		[7:0]	SUBTRACT_A				AFE_SWAP_A					
0x132	THRESH_ CFG_A	[15:8]	RESERVED					THRESH1_ DIR_A	THRESH1_TYPE_A		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_A	THRESH0_TYPE_A			
0x133	ADC_OFF 1_A	[15:8]	RESERVED		CH1_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_A[7:0]									
0x134	ADC_OFF 2_A	[15:8]	RESERVED		CH2_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_A[7:0]									
0x135	DATA1_A	[15:8]	DARK_SHIFT_A					DARK_SIZE_A			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_A					SIGNAL_SIZE_A				
0x136	DATA2_A	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_A					LIT_SIZE_A				
0x137	DECIMAT E_A	[15:8]	CHANNEL_EN_A		RESERVED			SUBSAMPLE_RATIO_A[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_A[3:0]				RESERVED					
0x138	DIGINT_LI T_A	[15:8]	RESERVED							LIT_OFFSE T_A, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_A[7:0]									
0x139	DIGINT_D ARK_A	[15:8]	DARK2_OFFSET_A[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_A, Bit 0	DARK1_OFFSET_A								
0x13A	ADC_OFF 3_A	[15:8]	RESERVED		CH3_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_A[7:0]									
0x13B	ADC_OFF 4_A	[15:8]	RESERVED		CH4_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_A[7:0]									
0x13C	THRESH1 _A	[15:8]	RESERVED			THRESH1_SHIFT_A					0x0000	R/W
		[7:0]	THRESH1_VALUE_A									
0x140	TS_CTRL_ B	[15:8]	RESERVED		SAMPLE_TYPE_B			RESERVED	TIMESLOT_OFFSET_B[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_B[7:0]									
0x141	TS_PATH_ B	[15:8]	PRE_WIDTH_B				AMBIENT_CANCELLATIO N_B		GOUT_B	RESERVED	0x4020	R/W
		[7:0]	RESERVE D	AFE_PATH_CFG_B								
0x142	INPUTS_B	[15:8]	INP4_SEL_B		INP3_SEL_B		INP2_SEL_B		INP1_SEL_B		0x0000	R/W
		[7:0]	INP34_B				INP12_B					
0x143	CATHODE _B	[15:8]	RESERVE D	PRECON_B			RESERVED		AFE_VREF_AMB_SEL_B		0x0200	R/W
		[7:0]	VC1_AMB_SEL_B		VC1_PULSE_B		VC1_ALT_B		VC1_SEL_B			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x144	AFE_TRIM_1_B	[15:8]	AFE_TIA_SAT_DETECT_EN_B	RESERVED		AFE_BUFFER_GAIN_B		VREF_PULSE_B	AFE_TRIM_VREF_B		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_B		TIA_GAIN_CH2_B			TIA_GAIN_CH1_B				
0x145	AFE_TRIM_2_B	[15:8]	RESERVED			AFE_BUFFER_CAP_B	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_B			TIA_GAIN_CH3_B				
0x146	AFE_DAC_1_B	[15:8]	DAC_AMBIENT_CH1_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_B, Bit 0	DAC_LED_DC_CH1_B								
0x147	AFE_DAC_2_B	[15:8]	DAC_AMBIENT_CH2_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_B, Bit 0	DAC_LED_DC_CH2_B								
0x148	LED_POW12_B	[15:8]	RESERVED	LED_CURRENT2_B							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_B								
0x149	LED_MODE_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_B		LED_DRIVESIDE1_B		RESERVED		LED_MODE2_B	LED_MODE1_B		
0x14A	COUNTS_B	[15:8]	NUM_INT_B								0x0101	R/W
		[7:0]	NUM_REPEAT_B									
0x14B	PERIOD_B	[15:8]	RESERVED	COARSE_LOOP_WIDTH_B	MOD_TYPE_B		RESERVED		MIN_PERIOD_B[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_B[7:0]									
0x14C	LED_PULSE1_B	[15:8]	LED_WIDTH_B								0x0210	R/W
		[7:0]	LED_OFFSET_B									
0x14D	AFE_DAC_3_B	[15:8]	DAC_AMBIENT_CH3_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_B, Bit 0	DAC_LED_DC_CH3_B								
0x14E	AFE_DAC_4_B	[15:8]	DAC_AMBIENT_CH4_B[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_B, Bit 0	DAC_LED_DC_CH4_B								
0x14F	THRESH0_B	[15:8]	RESERVED			THRESH0_SHIFT_B					0x0000	R/W
		[7:0]	THRESH0_VALUE_B									
0x150	MOD_PULSE_B	[15:8]	MOD_WIDTH_B								0x0001	R/W
		[7:0]	MOD_OFFSET_B									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x151	PATTERN 1_B	[15:8]	LED_DISABLE_B				MOD_DISABLE_B				0x0000	R/W
		[7:0]	SUBTRACT_B				AFE_SWAP_B					
0x152	THRESH_ CFG_B	[15:8]	RESERVED					THRESH1_ DIR_B	THRESH1_TYPE_B		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_B	THRESH0_TYPE_B			
0x153	ADC_OFF 1_B	[15:8]	RESERVED		CH1_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_B[7:0]									
0x154	ADC_OFF 2_B	[15:8]	RESERVED		CH2_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_B[7:0]									
0x155	DATA1_B	[15:8]	DARK_SHIFT_B					DARK_SIZE_B			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_B					SIGNAL_SIZE_B				
0x156	DATA2_B	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_B					LIT_SIZE_B				
0x157	DECIMAT E_B	[15:8]	CHANNEL_EN_B		RESERVED			SUBSAMPLE_RATIO_B[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_B[3:0]				RESERVED					
0x158	DIGINT_LI T_B	[15:8]	RESERVED							LIT_OFFSE T_B, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_B[7:0]									
0x159	DIGINT_D ARK_B	[15:8]	DARK2_OFFSET_B[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_B, Bit 0	DARK1_OFFSET_B								
0x15A	ADC_OFF 3_B	[15:8]	RESERVED		CH3_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_B[7:0]									
0x15B	ADC_OFF 4_B	[15:8]	RESERVED		CH4_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_B[7:0]									
0x15C	THRESH1 _B	[15:8]	RESERVED			THRESH1_SHIFT_B					0x0000	R/W
		[7:0]	THRESH1_VALUE_B									
0x160	TS_CTRL_ C	[15:8]	RESERVED		SAMPLE_TYPE_C			RESERVED	TIMESLOT_OFFSET_C[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_C[7:0]									
0x161	TS_PATH_ C	[15:8]	PRE_WIDTH_C				AMBIENT_CANCELLATIO N_C		GOUT_C	RESERVED	0x4020	R/W
		[7:0]	RESERVE D	AFE_PATH_CFG_C								
0x162	INPUTS_C	[15:8]	INP4_SEL_C		INP3_SEL_C		INP2_SEL_C		INP1_SEL_C		0x0000	R/W
		[7:0]	INP34_C				INP12_C					
0x163	CATHODE _C	[15:8]	RESERVE D	PRECON_C			RESERVED		AFE_VREF_AMB_SEL_C		0x0200	R/W
		[7:0]	VC1_AMB_SEL_C		VC1_PULSE_C		VC1_ALT_C		VC1_SEL_C			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x164	AFE_TRIM_1_C	[15:8]	AFE_TIA_SAT_DETECT_EN_C	RESERVED		AFE_BUFFER_GAIN_C		VREF_PULSE_C	AFE_TRIM_VREF_C		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_C		TIA_GAIN_CH2_C			TIA_GAIN_CH1_C				
0x165	AFE_TRIM_2_C	[15:8]	RESERVED			AFE_BUFFER_CAP_C	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_C			TIA_GAIN_CH3_C				
0x166	AFE_DAC_1_C	[15:8]	DAC_AMBIENT_CH1_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_C, Bit 0	DAC_LED_DC_CH1_C								
0x167	AFE_DAC_2_C	[15:8]	DAC_AMBIENT_CH2_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_C, Bit 0	DAC_LED_DC_CH2_C								
0x168	LED_POW12_C	[15:8]	RESERVED	LED_CURRENT2_C							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_C								
0x169	LED_MODE_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_C		LED_DRIVESIDE1_C		RESERVED		LED_MODE2_C	LED_MODE1_C		
0x16A	COUNTS_C	[15:8]	NUM_INT_C								0x0101	R/W
		[7:0]	NUM_REPEAT_C									
0x16B	PERIOD_C	[15:8]	RESERVED	COARSE_LOOP_WIDTH_C	MOD_TYPE_C		RESERVED		MIN_PERIOD_C[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_C[7:0]									
0x16C	LED_PULSE1_C	[15:8]	LED_WIDTH_C								0x0210	R/W
		[7:0]	LED_OFFSET_C									
0x16D	AFE_DAC_3_C	[15:8]	DAC_AMBIENT_CH3_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_C, Bit 0	DAC_LED_DC_CH3_C								
0x16E	AFE_DAC_4_C	[15:8]	DAC_AMBIENT_CH4_C[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_C, Bit 0	DAC_LED_DC_CH4_C								
0x16F	THRESH0_C	[15:8]	RESERVED			THRESH0_SHIFT_C					0x0000	R/W
		[7:0]	THRESH0_VALUE_C									
0x170	MOD_PULSE_C	[15:8]	MOD_WIDTH_C								0x0001	R/W
		[7:0]	MOD_OFFSET_C									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x171	PATTERN1_C	[15:8]	LED_DISABLE_C				MOD_DISABLE_C				0x0000	R/W
		[7:0]	SUBTRACT_C				AFE_SWAP_C					
0x172	THRESH_CFG_C	[15:8]	RESERVED					THRESH1_DIR_C	THRESH1_TYPE_C		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_C	THRESH0_TYPE_C			
0x173	ADC_OFF1_C	[15:8]	RESERVED		CH1_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_C[7:0]									
0x174	ADC_OFF2_C	[15:8]	RESERVED		CH2_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_C[7:0]									
0x175	DATA1_C	[15:8]	DARK_SHIFT_C					DARK_SIZE_C			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_C					SIGNAL_SIZE_C				
0x176	DATA2_C	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_C					LIT_SIZE_C				
0x177	DECIMATE_C	[15:8]	CHANNEL_EN_C		RESERVED			SUBSAMPLE_RATIO_C[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_C[3:0]				RESERVED					
0x178	DIGINT_LIT_C	[15:8]	RESERVED							LIT_OFFSET_C, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_C[7:0]									
0x179	DIGINT_DARK_C	[15:8]	DARK2_OFFSET_C[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_C, Bit 0	DARK1_OFFSET_C								
0x17A	ADC_OFF3_C	[15:8]	RESERVED		CH3_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_C[7:0]									
0x17B	ADC_OFF4_C	[15:8]	RESERVED		CH4_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_C[7:0]									
0x17C	THRESH1_C	[15:8]	RESERVED			THRESH1_SHIFT_C					0x0000	R/W
		[7:0]	THRESH1_VALUE_C									
0x180	TS_CTRL_D	[15:8]	RESERVED		SAMPLE_TYPE_D			RESERVED	TIMESLOT_OFFSET_D[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_D[7:0]									
0x181	TS_PATH_D	[15:8]	PRE_WIDTH_D				AMBIENT_CANCELLATION_D		GOUT_D	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_D								
0x182	INPUTS_D	[15:8]	INP4_SEL_D		INP3_SEL_D		INP2_SEL_D		INP1_SEL_D		0x0000	R/W
		[7:0]	INP34_D				INP12_D					
0x183	CATHODE_D	[15:8]	RESERVED	PRECON_D			RESERVED		AFE_VREF_AMB_SEL_D		0x0200	R/W
		[7:0]	VC1_AMB_SEL_D		VC1_PULSE_D		VC1_ALT_D		VC1_SEL_D			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x184	AFE_TRIM_1_D	[15:8]	AFE_TIA_SAT_DETECT_EN_D	RESERVED		AFE_BUFFER_GAIN_D		VREF_PULSE_D	AFE_TRIM_VREF_D		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_D		TIA_GAIN_CH2_D			TIA_GAIN_CH1_D				
0x185	AFE_TRIM_2_D	[15:8]	RESERVED			AFE_BUFFER_CAP_D	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_D			TIA_GAIN_CH3_D				
0x186	AFE_DAC_1_D	[15:8]	DAC_AMBIENT_CH1_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_D, Bit 0	DAC_LED_DC_CH1_D								
0x187	AFE_DAC_2_D	[15:8]	DAC_AMBIENT_CH2_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_D, Bit 0	DAC_LED_DC_CH2_D								
0x188	LED_POW12_D	[15:8]	RESERVED	LED_CURRENT2_D							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_D								
0x189	LED_MODE_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_D		LED_DRIVESIDE1_D		RESERVED		LED_MODE2_D	LED_MODE1_D		
0x18A	COUNTS_D	[15:8]	NUM_INT_D								0x0101	R/W
		[7:0]	NUM_REPEAT_D									
0x18B	PERIOD_D	[15:8]	RESERVED	COARSE_LOOP_WIDTH_D	MOD_TYPE_D		RESERVED		MIN_PERIOD_D[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_D[7:0]									
0x18C	LED_PULSE1_D	[15:8]	LED_WIDTH_D								0x0210	R/W
		[7:0]	LED_OFFSET_D									
0x18D	AFE_DAC_3_D	[15:8]	DAC_AMBIENT_CH3_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_D, Bit 0	DAC_LED_DC_CH3_D								
0x18E	AFE_DAC_4_D	[15:8]	DAC_AMBIENT_CH4_D[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_D, Bit 0	DAC_LED_DC_CH4_D								
0x18F	THRESH0_D	[15:8]	RESERVED			THRESH0_SHIFT_D					0x0000	R/W
		[7:0]	THRESH0_VALUE_D									
0x190	MOD_PULSE_D	[15:8]	MOD_WIDTH_D								0x0001	R/W
		[7:0]	MOD_OFFSET_D									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x191	PATTERN1_D	[15:8]	LED_DISABLE_D				MOD_DISABLE_D				0x0000	R/W
		[7:0]	SUBTRACT_D				AFE_SWAP_D					
0x192	THRESH_CFG_D	[15:8]	RESERVED					THRESH1_DIR_D	THRESH1_TYPE_D		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_D	THRESH0_TYPE_D			
0x193	ADC_OFF1_D	[15:8]	RESERVED		CH1_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_D[7:0]									
0x194	ADC_OFF2_D	[15:8]	RESERVED		CH2_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_D[7:0]									
0x195	DATA1_D	[15:8]	DARK_SHIFT_D					DARK_SIZE_D			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_D					SIGNAL_SIZE_D				
0x196	DATA2_D	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_D					LIT_SIZE_D				
0x197	DECIMATE_D	[15:8]	CHANNEL_EN_D		RESERVED			SUBSAMPLE_RATIO_D[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_D[3:0]				RESERVED					
0x198	DIGINT_LIT_D	[15:8]	RESERVED							LIT_OFFSET_D, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_D[7:0]									
0x199	DIGINT_DARK_D	[15:8]	DARK2_OFFSET_D[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_D, Bit 0	DARK1_OFFSET_D								
0x19A	ADC_OFF3_D	[15:8]	RESERVED		CH3_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_D[7:0]									
0x19B	ADC_OFF4_D	[15:8]	RESERVED		CH4_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_D[7:0]									
0x19C	THRESH1_D	[15:8]	RESERVED			THRESH1_SHIFT_D					0x0000	R/W
		[7:0]	THRESH1_VALUE_D									
0x1A0	TS_CTRL_E	[15:8]	RESERVED		SAMPLE_TYPE_E			RESERVED	TIMESLOT_OFFSET_E[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_E[7:0]									
0x1A1	TS_PATH_E	[15:8]	PRE_WIDTH_E				AMBIENT_CANCELLATION_E		GOUT_E	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_E								
0x1A2	INPUTS_E	[15:8]	INP4_SEL_E		INP3_SEL_E		INP2_SEL_E		INP1_SEL_E		0x0000	R/W
		[7:0]	INP34_E				INP12_E					
0x1A3	CATHODE_E	[15:8]	RESERVED	PRECON_E			RESERVED		AFE_VREF_AMB_SEL_E		0x0200	R/W
		[7:0]	VC1_AMB_SEL_E		VC1_PULSE_E		VC1_ALT_E		VC1_SEL_E			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1A4	AFE_TRIM_1_E	[15:8]	AFE_TIA_SAT_DETECT_EN_E	RESERVED		AFE_BUFFER_GAIN_E		VREF_PULSE_E	AFE_TRIM_VREF_E		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_E		TIA_GAIN_CH2_E			TIA_GAIN_CH1_E				
0x1A5	AFE_TRIM_2_E	[15:8]	RESERVED			AFE_BUFFER_CAP_E	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_E			TIA_GAIN_CH3_E				
0x1A6	AFE_DAC_1_E	[15:8]	DAC_AMBIENT_CH1_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_E, Bit 0	DAC_LED_DC_CH1_E								
0x1A7	AFE_DAC_2_E	[15:8]	DAC_AMBIENT_CH2_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_E, Bit 0	DAC_LED_DC_CH2_E								
0x1A8	LED_POW12_E	[15:8]	RESERVED	LED_CURRENT2_E							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_E								
0x1A9	LED_MODE_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_E		LED_DRIVESIDE1_E		RESERVED		LED_MODE2_E	LED_MODE1_E		
0x1AA	COUNTS_E	[15:8]	NUM_INT_E								0x0101	R/W
		[7:0]	NUM_REPEAT_E									
0x1AB	PERIOD_E	[15:8]	RESERVED	COARSE_LOOP_WIDTH_E	MOD_TYPE_E		RESERVED		MIN_PERIOD_E[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_E[7:0]									
0x1AC	LED_PULSE1_E	[15:8]	LED_WIDTH_E								0x0210	R/W
		[7:0]	LED_OFFSET_E									
0x1AD	AFE_DAC_3_E	[15:8]	DAC_AMBIENT_CH3_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_E, Bit 0	DAC_LED_DC_CH3_E								
0x1AE	AFE_DAC_4_E	[15:8]	DAC_AMBIENT_CH4_E[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_E, Bit 0	DAC_LED_DC_CH4_E								
0x1AF	THRESH0_E	[15:8]	RESERVED			THRESH0_SHIFT_E					0x0000	R/W
		[7:0]	THRESH0_VALUE_E									
0x1B0	MOD_PULSE_E	[15:8]	MOD_WIDTH_E								0x0001	R/W
		[7:0]	MOD_OFFSET_E									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1B1	PATTERN1_E	[15:8]	LED_DISABLE_E				MOD_DISABLE_E				0x0000	R/W
		[7:0]	SUBTRACT_E				AFE_SWAP_E					
0x1B2	THRESH_CFG_E	[15:8]	RESERVED					THRESH1_DIR_E	THRESH1_TYPE_E		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_E	THRESH0_TYPE_E			
0x1B3	ADC_OFF1_E	[15:8]	RESERVED		CH1_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_E[7:0]									
0x1B4	ADC_OFF2_E	[15:8]	RESERVED		CH2_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_E[7:0]									
0x1B5	DATA1_E	[15:8]	DARK_SHIFT_E					DARK_SIZE_E			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_E					SIGNAL_SIZE_E				
0x1B6	DATA2_E	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_E					LIT_SIZE_E				
0x1B7	DECIMATE_E	[15:8]	CHANNEL_EN_E		RESERVED			SUBSAMPLE_RATIO_E[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_E[3:0]				RESERVED					
0x1B8	DIGINT_LIT_E	[15:8]	RESERVED							LIT_OFFSET_E, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_E[7:0]									
0x1B9	DIGINT_DARK_E	[15:8]	DARK2_OFFSET_E[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_E, Bit 0	DARK1_OFFSET_E								
0x1BA	ADC_OFF3_E	[15:8]	RESERVED		CH3_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_E[7:0]									
0x1BB	ADC_OFF4_E	[15:8]	RESERVED		CH4_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_E[7:0]									
0x1BC	THRESH1_E	[15:8]	RESERVED			THRESH1_SHIFT_E					0x0000	R/W
		[7:0]	THRESH1_VALUE_E									
0x1C0	TS_CTRL_F	[15:8]	RESERVED		SAMPLE_TYPE_F			RESERVED	TIMESLOT_OFFSET_F[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_F[7:0]									
0x1C1	TS_PATH_F	[15:8]	PRE_WIDTH_F				AMBIENT_CANCELLATION_F		GOUT_F	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_F								
0x1C2	INPUTS_F	[15:8]	INP4_SEL_F		INP3_SEL_F		INP2_SEL_F		INP1_SEL_F		0x0000	R/W
		[7:0]	INP34_F				INP12_F					
0x1C3	CATHODE_F	[15:8]	RESERVED	PRECON_F			RESERVED		AFE_VREF_AMB_SEL_F		0x0200	R/W
		[7:0]	VC1_AMB_SEL_F		VC1_PULSE_F		VC1_ALT_F		VC1_SEL_F			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1C4	AFE_TRIM_1_F	[15:8]	AFE_TIA_SAT_DETECT_EN_F	RESERVED		AFE_BUFFER_GAIN_F		VREF_PULSE_F	AFE_TRIM_VREF_F		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_F		TIA_GAIN_CH2_F			TIA_GAIN_CH1_F				
0x1C5	AFE_TRIM_2_F	[15:8]	RESERVED			AFE_BUFFER_CAP_F	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_F			TIA_GAIN_CH3_F				
0x1C6	AFE_DAC_1_F	[15:8]	DAC_AMBIENT_CH1_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_F, Bit 0	DAC_LED_DC_CH1_F								
0x1C7	AFE_DAC_2_F	[15:8]	DAC_AMBIENT_CH2_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_F, Bit 0	DAC_LED_DC_CH2_F								
0x1C8	LED_POW12_F	[15:8]	RESERVED	LED_CURRENT2_F							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_F								
0x1C9	LED_MODE_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_F		LED_DRIVESIDE1_F		RESERVED		LED_MODE2_F	LED_MODE1_F		
0x1CA	COUNTS_F	[15:8]	NUM_INT_F								0x0101	R/W
		[7:0]	NUM_REPEAT_F									
0x1CB	PERIOD_F	[15:8]	RESERVED	COARSE_LOOP_WIDTH_F	MOD_TYPE_F		RESERVED		MIN_PERIOD_F[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_F[7:0]									
0x1CC	LED_PULSE1_F	[15:8]	LED_WIDTH_F								0x0210	R/W
		[7:0]	LED_OFFSET_F									
0x1CD	AFE_DAC_3_F	[15:8]	DAC_AMBIENT_CH3_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_F, Bit 0	DAC_LED_DC_CH3_F								
0x1CE	AFE_DAC_4_F	[15:8]	DAC_AMBIENT_CH4_F[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_F, Bit 0	DAC_LED_DC_CH4_F								
0x1CF	THRESH0_F	[15:8]	RESERVED			THRESH0_SHIFT_F					0x0000	R/W
		[7:0]	THRESH0_VALUE_F									
0x1D0	MOD_PULSE_F	[15:8]	MOD_WIDTH_F								0x0001	R/W
		[7:0]	MOD_OFFSET_F									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1D1	PATTERN1_F	[15:8]	LED_DISABLE_F				MOD_DISABLE_F				0x0000	R/W
		[7:0]	SUBTRACT_F				AFE_SWAP_F					
0x1D2	THRESH_CFG_F	[15:8]	RESERVED					THRESH1_DIR_F	THRESH1_TYPE_F		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_F	THRESH0_TYPE_F			
0x1D3	ADC_OFF1_F	[15:8]	RESERVED		CH1_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_F[7:0]									
0x1D4	ADC_OFF2_F	[15:8]	RESERVED		CH2_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_F[7:0]									
0x1D5	DATA1_F	[15:8]	DARK_SHIFT_F					DARK_SIZE_F			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_F					SIGNAL_SIZE_F				
0x1D6	DATA2_F	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_F					LIT_SIZE_F				
0x1D7	DECIMATE_F	[15:8]	CHANNEL_EN_F		RESERVED			SUBSAMPLE_RATIO_F[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_F[3:0]				RESERVED					
0x1D8	DIGINT_LIT_F	[15:8]	RESERVED							LIT_OFFSET_F, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_F[7:0]									
0x1D9	DIGINT_DARK_F	[15:8]	DARK2_OFFSET_F[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_F, Bit 0	DARK1_OFFSET_F								
0x1DA	ADC_OFF3_F	[15:8]	RESERVED		CH3_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_F[7:0]									
0x1DB	ADC_OFF4_F	[15:8]	RESERVED		CH4_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_F[7:0]									
0x1DC	THRESH1_F	[15:8]	RESERVED			THRESH1_SHIFT_F					0x0000	R/W
		[7:0]	THRESH1_VALUE_F									
0x1E0	TS_CTRL_G	[15:8]	RESERVED		SAMPLE_TYPE_G			RESERVED	TIMESLOT_OFFSET_G[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_G[7:0]									
0x1E1	TS_PATH_G	[15:8]	PRE_WIDTH_G				AMBIENT_CANCELLATION_G		GOUT_G	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_G								
0x1E2	INPUTS_G	[15:8]	INP4_SEL_G		INP3_SEL_G		INP2_SEL_G		INP1_SEL_G		0x0000	R/W
		[7:0]	INP34_G				INP12_G					
0x1E3	CATHODE_G	[15:8]	RESERVED	PRECON_G			RESERVED		AFE_VREF_AMB_SEL_G		0x0200	R/W
		[7:0]	VC1_AMB_SEL_G		VC1_PULSE_G		VC1_ALT_G		VC1_SEL_G			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1E4	AFE_TRIM_1_G	[15:8]	AFE_TIA_SAT_DETECT_EN_G	RESERVED		AFE_BUFFER_GAIN_G		VREF_PULSE_G	AFE_TRIM_VREF_G		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_G		TIA_GAIN_CH2_G			TIA_GAIN_CH1_G				
0x1E5	AFE_TRIM_2_G	[15:8]	RESERVED			AFE_BUFFER_CAP_G	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_G			TIA_GAIN_CH3_G				
0x1E6	AFE_DAC_1_G	[15:8]	DAC_AMBIENT_CH1_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_G, Bit 0	DAC_LED_DC_CH1_G								
0x1E7	AFE_DAC_2_G	[15:8]	DAC_AMBIENT_CH2_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_G, Bit 0	DAC_LED_DC_CH2_G								
0x1E8	LED_POW12_G	[15:8]	RESERVED	LED_CURRENT2_G							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_G								
0x1E9	LED_MODE_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_G		LED_DRIVESIDE1_G		RESERVED		LED_MODE2_G	LED_MODE1_G		
0x1EA	COUNTS_G	[15:8]	NUM_INT_G								0x0101	R/W
		[7:0]	NUM_REPEAT_G									
0x1EB	PERIOD_G	[15:8]	RESERVED	COARSE_LOOP_WIDTH_G	MOD_TYPE_G		RESERVED		MIN_PERIOD_G[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_G[7:0]									
0x1EC	LED_PULSE1_G	[15:8]	LED_WIDTH_G								0x0210	R/W
		[7:0]	LED_OFFSET_G									
0x1ED	AFE_DAC_3_G	[15:8]	DAC_AMBIENT_CH3_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_G, Bit 0	DAC_LED_DC_CH3_G								
0x1EE	AFE_DAC_4_G	[15:8]	DAC_AMBIENT_CH4_G[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_G, Bit 0	DAC_LED_DC_CH4_G								
0x1EF	THRESH0_G	[15:8]	RESERVED			THRESH0_SHIFT_G					0x0000	R/W
		[7:0]	THRESH0_VALUE_G									
0x1F0	MOD_PULSE_G	[15:8]	MOD_WIDTH_G								0x0001	R/W
		[7:0]	MOD_OFFSET_G									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1F1	PATTERN1_G	[15:8]	LED_DISABLE_G				MOD_DISABLE_G				0x0000	R/W
		[7:0]	SUBTRACT_G				AFE_SWAP_G					
0x1F2	THRESH_CFG_G	[15:8]	RESERVED					THRESH1_DIR_G	THRESH1_TYPE_G		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_G	THRESH0_TYPE_G			
0x1F3	ADC_OFF1_G	[15:8]	RESERVED		CH1_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_G[7:0]									
0x1F4	ADC_OFF2_G	[15:8]	RESERVED		CH2_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_G[7:0]									
0x1F5	DATA1_G	[15:8]	DARK_SHIFT_G					DARK_SIZE_G			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_G					SIGNAL_SIZE_G				
0x1F6	DATA2_G	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_G					LIT_SIZE_G				
0x1F7	DECIMATE_G	[15:8]	CHANNEL_EN_G		RESERVED			SUBSAMPLE_RATIO_G[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_G[3:0]				RESERVED					
0x1F8	DIGINT_LIT_G	[15:8]	RESERVED							LIT_OFFSET_G, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_G[7:0]									
0x1F9	DIGINT_DARK_G	[15:8]	DARK2_OFFSET_G[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_G, Bit 0	DARK1_OFFSET_G								
0x1FA	ADC_OFF3_G	[15:8]	RESERVED		CH3_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_G[7:0]									
0x1FB	ADC_OFF4_G	[15:8]	RESERVED		CH4_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_G[7:0]									
0x1FC	THRESH1_G	[15:8]	RESERVED				THRESH1_SHIFT_G				0x0000	R/W
		[7:0]	THRESH1_VALUE_G									
0x200	TS_CTRL_H	[15:8]	RESERVED		SAMPLE_TYPE_H			RESERVED	TIMESLOT_OFFSET_H[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_H[7:0]									
0x201	TS_PATH_H	[15:8]	PRE_WIDTH_H				AMBIENT_CANCELLATION_H		GOUT_H	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_H								
0x202	INPUTS_H	[15:8]	INP4_SEL_H		INP3_SEL_H		INP2_SEL_H		INP1_SEL_H		0x0000	R/W
		[7:0]	INP34_H				INP12_H					
0x203	CATHODE_H	[15:8]	RESERVED	PRECON_H			RESERVED		AFE_VREF_AMB_SEL_H		0x0200	R/W
		[7:0]	VC1_AMB_SEL_H		VC1_PULSE_H		VC1_ALT_H		VC1_SEL_H			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x204	AFE_TRIM_1_H	[15:8]	AFE_TIA_SAT_DETECT_EN_H	RESERVED		AFE_BUFFER_GAIN_H		VREF_PULSE_H	AFE_TRIM_VREF_H		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_H		TIA_GAIN_CH2_H			TIA_GAIN_CH1_H				
0x205	AFE_TRIM_2_H	[15:8]	RESERVED			AFE_BUFFER_CAP_H	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_H			TIA_GAIN_CH3_H				
0x206	AFE_DAC_1_H	[15:8]	DAC_AMBIENT_CH1_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_H, Bit 0	DAC_LED_DC_CH1_H								
0x207	AFE_DAC_2_H	[15:8]	DAC_AMBIENT_CH2_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_H, Bit 0	DAC_LED_DC_CH2_H								
0x208	LED_POW12_H	[15:8]	RESERVED	LED_CURRENT2_H							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_H								
0x209	LED_MODE_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_H		LED_DRIVESIDE1_H		RESERVED		LED_MODE2_H	LED_MODE1_H		
0x20A	COUNTS_H	[15:8]	NUM_INT_H								0x0101	R/W
		[7:0]	NUM_REPEAT_H									
0x20B	PERIOD_H	[15:8]	RESERVED	COARSE_LOOP_WIDTH_H	MOD_TYPE_H		RESERVED		MIN_PERIOD_H[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_H[7:0]									
0x20C	LED_PULSE1_H	[15:8]	LED_WIDTH_H								0x0210	R/W
		[7:0]	LED_OFFSET_H									
0x20D	AFE_DAC_3_H	[15:8]	DAC_AMBIENT_CH3_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_H, Bit 0	DAC_LED_DC_CH3_H								
0x20E	AFE_DAC_4_H	[15:8]	DAC_AMBIENT_CH4_H[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_H, Bit 0	DAC_LED_DC_CH4_H								
0x20F	THRESH0_H	[15:8]	RESERVED			THRESH0_SHIFT_H					0x0000	R/W
		[7:0]	THRESH0_VALUE_H									
0x210	MOD_PULSE_H	[15:8]	MOD_WIDTH_H								0x0001	R/W
		[7:0]	MOD_OFFSET_H									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x211	PATTERN 1_H	[15:8]	LED_DISABLE_H				MOD_DISABLE_H				0x0000	R/W
		[7:0]	SUBTRACT_H				AFE_SWAP_H					
0x212	THRESH_ CFG_H	[15:8]	RESERVED					THRESH1_ DIR_H	THRESH1_TYPE_H		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_H	THRESH0_TYPE_H			
0x213	ADC_OFF 1_H	[15:8]	RESERVED		CH1_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_H[7:0]									
0x214	ADC_OFF 2_H	[15:8]	RESERVED		CH2_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_H[7:0]									
0x215	DATA1_H	[15:8]	DARK_SHIFT_H					DARK_SIZE_H			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_H					SIGNAL_SIZE_H				
0x216	DATA2_H	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_H					LIT_SIZE_H				
0x217	DECIMAT E_H	[15:8]	CHANNEL_EN_H		RESERVED			SUBSAMPLE_RATIO_H[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_H[3:0]				RESERVED					
0x218	DIGINT_LI T_H	[15:8]	RESERVED							LIT_OFFSE T_H, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_H[7:0]									
0x219	DIGINT_D ARK_H	[15:8]	DARK2_OFFSET_H[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_H, Bit 0	DARK1_OFFSET_H								
0x21A	ADC_OFF 3_H	[15:8]	RESERVED		CH3_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_H[7:0]									
0x21B	ADC_OFF 4_H	[15:8]	RESERVED		CH4_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_H[7:0]									
0x21C	THRESH1 _H	[15:8]	RESERVED				THRESH1_SHIFT_H				0x0000	R/W
		[7:0]	THRESH1_VALUE_H									
0x220	TS_CTRL_ I	[15:8]	RESERVED		SAMPLE_TYPE_I			RESERVED	TIMESLOT_OFFSET_I[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_I[7:0]									
0x221	TS_PATH_ I	[15:8]	PRE_WIDTH_I				AMBIENT_CANCELLATIO N_I		GOUT_I	RESERVED	0x4020	R/W
		[7:0]	RESERVE D	AFE_PATH_CFG_I								
0x222	INPUTS_I	[15:8]	INP4_SEL_I		INP3_SEL_I		INP2_SEL_I		INP1_SEL_I		0x0000	R/W
		[7:0]	INP34_I				INP12_I					
0x223	CATHODE _I	[15:8]	RESERVE D	PRECON_I			RESERVED		AFE_VREF_AMB_SEL_I		0x0200	R/W
		[7:0]	VC1_AMB_SEL_I		VC1_PULSE_I		VC1_ALT_I		VC1_SEL_I			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x224	AFE_TRIM_1_I	[15:8]	AFE_TIA_SAT_DETECT_EN_I	RESERVED		AFE_BUFFER_GAIN_I		VREF_PULSE_I	AFE_TRIM_VREF_I		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_I		TIA_GAIN_CH2_I			TIA_GAIN_CH1_I				
0x225	AFE_TRIM_2_I	[15:8]	RESERVED			AFE_BUFFER_CAP_I	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_I			TIA_GAIN_CH3_I				
0x226	AFE_DAC_1_I	[15:8]	DAC_AMBIENT_CH1_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_I, Bit 0	DAC_LED_DC_CH1_I								
0x227	AFE_DAC_2_I	[15:8]	DAC_AMBIENT_CH2_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_I, Bit 0	DAC_LED_DC_CH2_I								
0x228	LED_POW12_I	[15:8]	RESERVED	LED_CURRENT2_I							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_I								
0x229	LED_MODE_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_I		LED_DRIVESIDE1_I		RESERVED		LED_MODE2_I	LED_MODE1_I		
0x22A	COUNTS_I	[15:8]	NUM_INT_I								0x0101	R/W
		[7:0]	NUM_REPEAT_I									
0x22B	PERIOD_I	[15:8]	RESERVED	COARSE_LOOP_WIDTH_I	MOD_TYPE_I		RESERVED		MIN_PERIOD_I[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_I[7:0]									
0x22C	LED_PULSE1_I	[15:8]	LED_WIDTH_I								0x0210	R/W
		[7:0]	LED_OFFSET_I									
0x22D	AFE_DAC_3_I	[15:8]	DAC_AMBIENT_CH3_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_I, Bit 0	DAC_LED_DC_CH3_I								
0x22E	AFE_DAC_4_I	[15:8]	DAC_AMBIENT_CH4_I[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_I, Bit 0	DAC_LED_DC_CH4_I								
0x22F	THRESH0_I	[15:8]	RESERVED			THRESH0_SHIFT_I					0x0000	R/W
		[7:0]	THRESH0_VALUE_I									
0x230	MOD_PULSE_I	[15:8]	MOD_WIDTH_I								0x0001	R/W
		[7:0]	MOD_OFFSET_I									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x231	PATTERN1_I	[15:8]	LED_DISABLE_I				MOD_DISABLE_I				0x0000	R/W
		[7:0]	SUBTRACT_I				AFE_SWAP_I					
0x232	THRESH_CFG_I	[15:8]	RESERVED					THRESH1_DIR_I	THRESH1_TYPE_I		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_I	THRESH0_TYPE_I			
0x233	ADC_OFF1_I	[15:8]	RESERVED		CH1_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_I[7:0]									
0x234	ADC_OFF2_I	[15:8]	RESERVED		CH2_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_I[7:0]									
0x235	DATA1_I	[15:8]	DARK_SHIFT_I					DARK_SIZE_I			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_I					SIGNAL_SIZE_I				
0x236	DATA2_I	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_I					LIT_SIZE_I				
0x237	DECIMATE_I	[15:8]	CHANNEL_EN_I		RESERVED			SUBSAMPLE_RATIO_I[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_I[3:0]				RESERVED					
0x238	DIGINT_LIT_I	[15:8]	RESERVED							LIT_OFFSET_I, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_I[7:0]									
0x239	DIGINT_DARK_I	[15:8]	DARK2_OFFSET_I[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_I, Bit 0	DARK1_OFFSET_I								
0x23A	ADC_OFF3_I	[15:8]	RESERVED		CH3_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_I[7:0]									
0x23B	ADC_OFF4_I	[15:8]	RESERVED		CH4_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_I[7:0]									
0x23C	THRESH1_I	[15:8]	RESERVED				THRESH1_SHIFT_I				0x0000	R/W
		[7:0]	THRESH1_VALUE_I									
0x240	TS_CTRL_J	[15:8]	RESERVED		SAMPLE_TYPE_J			RESERVED	TIMESLOT_OFFSET_J[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_J[7:0]									
0x241	TS_PATH_J	[15:8]	PRE_WIDTH_J				AMBIENT_CANCELLATION_J		GOUT_J	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_J								
0x242	INPUTS_J	[15:8]	INP4_SEL_J		INP3_SEL_J		INP2_SEL_J		INP1_SEL_J		0x0000	R/W
		[7:0]	INP34_J				INP12_J					
0x243	CATHODE_J	[15:8]	RESERVED	PRECON_J			RESERVED		AFE_VREF_AMB_SEL_J		0x0200	R/W
		[7:0]	VC1_AMB_SEL_J		VC1_PULSE_J		VC1_ALT_J		VC1_SEL_J			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x244	AFE_TRIM_1_J	[15:8]	AFE_TIA_SAT_DETECT_EN_J	RESERVED		AFE_BUFFER_GAIN_J		VREF_PULSE_J	AFE_TRIM_VREF_J		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_J		TIA_GAIN_CH2_J			TIA_GAIN_CH1_J				
0x245	AFE_TRIM_2_J	[15:8]	RESERVED			AFE_BUFFER_CAP_J	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_J			TIA_GAIN_CH3_J				
0x246	AFE_DAC_1_J	[15:8]	DAC_AMBIENT_CH1_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_J, Bit 0	DAC_LED_DC_CH1_J								
0x247	AFE_DAC_2_J	[15:8]	DAC_AMBIENT_CH2_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_J, Bit 0	DAC_LED_DC_CH2_J								
0x248	LED_POW12_J	[15:8]	RESERVED	LED_CURRENT2_J							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_J								
0x249	LED_MODE_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_J		LED_DRIVESIDE1_J		RESERVED		LED_MODE2_J	LED_MODE1_J		
0x24A	COUNTS_J	[15:8]	NUM_INT_J								0x0101	R/W
		[7:0]	NUM_REPEAT_J									
0x24B	PERIOD_J	[15:8]	RESERVED	COARSE_LOOP_WIDTH_J	MOD_TYPE_J		RESERVED		MIN_PERIOD_J[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_J[7:0]									
0x24C	LED_PULSE1_J	[15:8]	LED_WIDTH_J								0x0210	R/W
		[7:0]	LED_OFFSET_J									
0x24D	AFE_DAC_3_J	[15:8]	DAC_AMBIENT_CH3_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_J, Bit 0	DAC_LED_DC_CH3_J								
0x24E	AFE_DAC_4_J	[15:8]	DAC_AMBIENT_CH4_J[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_J, Bit 0	DAC_LED_DC_CH4_J								
0x24F	THRESH0_J	[15:8]	RESERVED			THRESH0_SHIFT_J					0x0000	R/W
		[7:0]	THRESH0_VALUE_J									
0x250	MOD_PULSE_J	[15:8]	MOD_WIDTH_J								0x0001	R/W
		[7:0]	MOD_OFFSET_J									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x251	PATTERN 1_J	[15:8]	LED_DISABLE_J				MOD_DISABLE_J				0x0000	R/W
		[7:0]	SUBTRACT_J				AFE_SWAP_J					
0x252	THRESH_ CFG_J	[15:8]	RESERVED					THRESH1_ DIR_J	THRESH1_TYPE_J		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_J	THRESH0_TYPE_J			
0x253	ADC_OFF 1_J	[15:8]	RESERVED		CH1_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_J[7:0]									
0x254	ADC_OFF 2_J	[15:8]	RESERVED		CH2_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_J[7:0]									
0x255	DATA1_J	[15:8]	DARK_SHIFT_J					DARK_SIZE_J			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_J					SIGNAL_SIZE_J				
0x256	DATA2_J	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_J					LIT_SIZE_J				
0x257	DECIMAT E_J	[15:8]	CHANNEL_EN_J		RESERVED			SUBSAMPLE_RATIO_J[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_J[3:0]				RESERVED					
0x258	DIGINT_LI T_J	[15:8]	RESERVED							LIT_OFFSE T_J, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_J[7:0]									
0x259	DIGINT_D ARK_J	[15:8]	DARK2_OFFSET_J[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_J, Bit 0	DARK1_OFFSET_J								
0x25A	ADC_OFF 3_J	[15:8]	RESERVED		CH3_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_J[7:0]									
0x25B	ADC_OFF 4_J	[15:8]	RESERVED		CH4_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_J[7:0]									
0x25C	THRESH1 _J	[15:8]	RESERVED				THRESH1_SHIFT_J				0x0000	R/W
		[7:0]	THRESH1_VALUE_J									
0x260	TS_CTRL_ K	[15:8]	RESERVED		SAMPLE_TYPE_K			RESERVED	TIMESLOT_OFFSET_K[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_K[7:0]									
0x261	TS_PATH_ K	[15:8]	PRE_WIDTH_K				AMBIENT_CANCELLATIO N_K		GOUT_K	RESERVED	0x4020	R/W
		[7:0]	RESERVE D	AFE_PATH_CFG_K								
0x262	INPUTS_K	[15:8]	INP4_SEL_K		INP3_SEL_K		INP2_SEL_K		INP1_SEL_K		0x0000	R/W
		[7:0]	INP34_K				INP12_K					
0x263	CATHODE _K	[15:8]	RESERVE D	PRECON_K			RESERVED		AFE_VREF_AMB_SEL_K		0x0200	R/W
		[7:0]	VC1_AMB_SEL_K		VC1_PULSE_K		VC1_ALT_K		VC1_SEL_K			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x264	AFE_TRIM_1_K	[15:8]	AFE_TIA_SAT_DETECT_EN_K	RESERVED		AFE_BUFFER_GAIN_K		VREF_PULSE_K	AFE_TRIM_VREF_K		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_K		TIA_GAIN_CH2_K			TIA_GAIN_CH1_K				
0x265	AFE_TRIM_2_K	[15:8]	RESERVED			AFE_BUFFER_CAP_K	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_K			TIA_GAIN_CH3_K				
0x266	AFE_DAC_1_K	[15:8]	DAC_AMBIENT_CH1_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_K, Bit 0	DAC_LED_DC_CH1_K								
0x267	AFE_DAC_2_K	[15:8]	DAC_AMBIENT_CH2_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_K, Bit 0	DAC_LED_DC_CH2_K								
0x268	LED_POW12_K	[15:8]	RESERVED	LED_CURRENT2_K							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_K								
0x269	LED_MODE_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_K		LED_DRIVESIDE1_K		RESERVED		LED_MODE2_K	LED_MODE1_K		
0x26A	COUNTS_K	[15:8]	NUM_INT_K								0x0101	R/W
		[7:0]	NUM_REPEAT_K									
0x26B	PERIOD_K	[15:8]	RESERVED	COARSE_LOOP_WIDTH_K	MOD_TYPE_K		RESERVED		MIN_PERIOD_K[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_K[7:0]									
0x26C	LED_PULSE1_K	[15:8]	LED_WIDTH_K								0x0210	R/W
		[7:0]	LED_OFFSET_K									
0x26D	AFE_DAC_3_K	[15:8]	DAC_AMBIENT_CH3_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_K, Bit 0	DAC_LED_DC_CH3_K								
0x26E	AFE_DAC_4_K	[15:8]	DAC_AMBIENT_CH4_K[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_K, Bit 0	DAC_LED_DC_CH4_K								
0x26F	THRESH0_K	[15:8]	RESERVED			THRESH0_SHIFT_K					0x0000	R/W
		[7:0]	THRESH0_VALUE_K									
0x270	MOD_PULSE_K	[15:8]	MOD_WIDTH_K								0x0001	R/W
		[7:0]	MOD_OFFSET_K									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x271	PATTERN1_K	[15:8]	LED_DISABLE_K				MOD_DISABLE_K				0x0000	R/W
		[7:0]	SUBTRACT_K				AFE_SWAP_K					
0x272	THRESH_CFG_K	[15:8]	RESERVED					THRESH1_DIR_K	THRESH1_TYPE_K		0x0000	R/W
		[7:0]	RESERVED					THRESH0_DIR_K	THRESH0_TYPE_K			
0x273	ADC_OFF1_K	[15:8]	RESERVED		CH1_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_K[7:0]									
0x274	ADC_OFF2_K	[15:8]	RESERVED		CH2_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_K[7:0]									
0x275	DATA1_K	[15:8]	DARK_SHIFT_K					DARK_SIZE_K			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_K					SIGNAL_SIZE_K				
0x276	DATA2_K	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_K					LIT_SIZE_K				
0x277	DECIMATE_K	[15:8]	CHANNEL_EN_K		RESERVED			SUBSAMPLE_RATIO_K[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_K[3:0]				RESERVED					
0x278	DIGINT_LIT_K	[15:8]	RESERVED							LIT_OFFSET_K, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_K[7:0]									
0x279	DIGINT_DARK_K	[15:8]	DARK2_OFFSET_K[8:1]								0x0086	R/W
		[7:0]	DARK2_OFFSET_K, Bit 0	DARK1_OFFSET_K								
0x27A	ADC_OFF3_K	[15:8]	RESERVED		CH3_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_K[7:0]									
0x27B	ADC_OFF4_K	[15:8]	RESERVED		CH4_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_K[7:0]									
0x27C	THRESH1_K	[15:8]	RESERVED			THRESH1_SHIFT_K					0x0000	R/W
		[7:0]	THRESH1_VALUE_K									
0x280	TS_CTRL_L	[15:8]	RESERVED		SAMPLE_TYPE_L			RESERVED	TIMESLOT_OFFSET_L[9:8]		0x1000	R/W
		[7:0]	TIMESLOT_OFFSET_L[7:0]									
0x281	TS_PATH_L	[15:8]	PRE_WIDTH_L				AMBIENT_CANCELLATION_L		GOUT_L	RESERVED	0x4020	R/W
		[7:0]	RESERVED	AFE_PATH_CFG_L								
0x282	INPUTS_L	[15:8]	INP4_SEL_L		INP3_SEL_L		INP2_SEL_L		INP1_SEL_L		0x0000	R/W
		[7:0]	INP34_L				INP12_L					
0x283	CATHODE_L	[15:8]	RESERVED	PRECON_L			RESERVED		AFE_VREF_AMB_SEL_L		0x0200	R/W
		[7:0]	VC1_AMB_SEL_L		VC1_PULSE_L		VC1_ALT_L		VC1_SEL_L			

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x284	AFE_TRIM_1_L	[15:8]	AFE_TIA_SAT_DETECT_EN_L	RESERVED		AFE_BUFFER_GAIN_L		VREF_PULSE_L	AFE_TRIM_VREF_L		0x02C9	R/W
		[7:0]	VREF_PULSE_VAL_L		TIA_GAIN_CH2_L			TIA_GAIN_CH1_L				
0x285	AFE_TRIM_2_L	[15:8]	RESERVED			AFE_BUFFER_CAP_L	RESERVED				0x0000	R/W
		[7:0]	RESERVED		TIA_GAIN_CH4_L			TIA_GAIN_CH3_L				
0x286	AFE_DAC_1_L	[15:8]	DAC_AMBIENT_CH1_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH1_L, Bit 0	DAC_LED_DC_CH1_L								
0x287	AFE_DAC_2_L	[15:8]	DAC_AMBIENT_CH2_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH2_L, Bit 0	DAC_LED_DC_CH2_L								
0x288	LED_POW12_L	[15:8]	RESERVED	LED_CURRENT2_L							0x0000	R/W
		[7:0]	RESERVED	LED_CURRENT1_L								
0x289	LED_MODE_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LED_DRIVESIDE2_L		LED_DRIVESIDE1_L		RESERVED		LED_MODE2_L	LED_MODE1_L		
0x28A	COUNTS_L	[15:8]	NUM_INT_L								0x0101	R/W
		[7:0]	NUM_REPEAT_L									
0x28B	PERIOD_L	[15:8]	RESERVED	COARSE_LOOP_WIDTH_L	MOD_TYPE_L		RESERVED		MIN_PERIOD_L[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_L[7:0]									
0x28C	LED_PULSE1_L	[15:8]	LED_WIDTH_L								0x0210	R/W
		[7:0]	LED_OFFSET_L									
0x28D	AFE_DAC_3_L	[15:8]	DAC_AMBIENT_CH3_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH3_L, Bit 0	DAC_LED_DC_CH3_L								
0x28E	AFE_DAC_4_L	[15:8]	DAC_AMBIENT_CH4_L[8:1]								0x0000	R/W
		[7:0]	DAC_AMBIENT_CH4_L, Bit 0	DAC_LED_DC_CH4_L								
0x28F	THRESH0_L	[15:8]	RESERVED			THRESH0_SHIFT_L					0x0000	R/W
		[7:0]	THRESH0_VALUE_L									
0x290	MOD_PULSE_L	[15:8]	MOD_WIDTH_L								0x0001	R/W
		[7:0]	MOD_OFFSET_L									

REGISTER SUMMARY

Table 15. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x291	PATTERN 1_L	[15:8]	LED_DISABLE_L				MOD_DISABLE_L				0x0000	R/W
		[7:0]	SUBTRACT_L				AFE_SWAP_L					
0x292	THRESH_ CFG_L	[15:8]	RESERVED					THRESH1_ DIR_L	THRESH1_TYPE_L		0x0000	R/W
		[7:0]	RESERVED					THRESH0_ DIR_L	THRESH0_TYPE_L			
0x293	ADC_OFF 1_L	[15:8]	RESERVED		CH1_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_L[7:0]									
0x294	ADC_OFF 2_L	[15:8]	RESERVED		CH2_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_L[7:0]									
0x295	DATA1_L	[15:8]	DARK_SHIFT_L					DARK_SIZE_L			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_L					SIGNAL_SIZE_L				
0x296	DATA2_L	[15:8]	RESERVED								0x0000	R/W
		[7:0]	LIT_SHIFT_L					LIT_SIZE_L				
0x297	DECIMAT E_L	[15:8]	CHANNEL_EN_L		RESERVED			SUBSAMPLE_RATIO_L[6:4]			0x0010	R/W
		[7:0]	SUBSAMPLE_RATIO_L[3:0]				RESERVED					
0x298	DIGINT_LI T_L	[15:8]	RESERVED							LIT_OFFSE T_L, Bit 8	0x0026	R/W
		[7:0]	LIT_OFFSET_L[7:0]									
0x299	DIGINT_D ARK_L	[15:8]	DARK2_OFFSET_L[8:1]								0x0086	R/W
		[7:0]	DARK2_O FFSET_L, Bit 0	DARK1_OFFSET_L								
0x29A	ADC_OFF 3_L	[15:8]	RESERVED		CH3_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH3_ADC_ADJUST_L[7:0]									
0x29B	ADC_OFF 4_L	[15:8]	RESERVED		CH4_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH4_ADC_ADJUST_L[7:0]									
0x29C	THRESH1 _L	[15:8]	RESERVED				THRESH1_SHIFT_L				0x0000	R/W
		[7:0]	THRESH1_VALUE_L									

REGISTER DETAILS

Table 16. Register Details

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x000	FIFO_STATUS	15	CLEAR_FIFO	Clear FIFO. Write a 1 to empty the FIFO while not operating, which resets the FIFO_BYTE_COUNT and also clears the FIFO overflow, FIFO underflow, and FIFO threshold interrupt status bits.	0x0	R0/W
		14	INT_FIFO_UFLOW	FIFO underflow error. This bit is set when the FIFO is read when it was empty. Write 1 to this bit to clear the interrupt, and it is also cleared when the FIFO is cleared by using the CLEAR_FIFO register.	0x0	R/W1C
		13	INT_FIFO_OFLOW	FIFO overflow error. This bit is set when data is not written to the FIFO due to lack of space. Write 1 to this bit to clear the interrupt, which is also cleared if the FIFO is cleared with the CLEAR_FIFO register bit.	0x0	R/W1C
		12	INT_FIFO_TH	FIFO_TH interrupt status. This bit is set during a FIFO write when the number of bytes in the FIFO exceeds the FIFO_TH register value. Write 1 to this bit to clear this interrupt. This bit can also be automatically cleared when the FIFO data register is read if the INT_ACLEAR_FIFO bit is set.	0x0	R/W1C
		11	FIFO_INIT_DONE_STATUS	FIFO initialization process is finished. Note that this field is a status bit and is not sent to interrupt. This bit is set after the FIFO self-initialization process.	0x0	R
		[10:0]	FIFO_BYTE_COUNT	Number of bytes in the FIFO. This field indicates the number of bytes in the FIFO.	0x0	R
0x001	INT_STATUS_TS1	[15:12]	RESERVED	Reserved.	0x0	R
		11	INT_PPG_LEV0_L	PPG Time Slot L Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot L.	0x0	R/W1C
		10	INT_PPG_LEV0_K	PPG Time Slot K Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot K.	0x0	R/W1C
		9	INT_PPG_LEV0_J	PPG Time Slot J Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot J.	0x0	R/W1C
		8	INT_PPG_LEV0_I	PPG Time Slot I Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot I.	0x0	R/W1C
		7	INT_PPG_LEV0_H	PPG Time Slot H Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot H.	0x0	R/W1C
		6	INT_PPG_LEV0_G	PPG Time Slot G Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot G.	0x0	R/W1C
		5	INT_PPG_LEV0_F	PPG Time Slot F Level 0 interrupt status. This bit is set during a data register update when the	0x0	R/W1C

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot F.		
		4	INT_PPG_LEV0_E	PPG Time Slot E Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot E.	0x0	R/W1C
		3	INT_PPG_LEV0_D	PPG Time Slot D Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot D.	0x0	R/W1C
		2	INT_PPG_LEV0_C	PPG Time Slot C Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot C.	0x0	R/W1C
		1	INT_PPG_LEV0_B	PPG Time Slot B Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot B.	0x0	R/W1C
		0	INT_PPG_LEV0_A	PPG Time Slot A Level 0 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 1 TIA saturates during Time Slot A.	0x0	R/W1C
0x002	INT_STATUS_TS2	[15:12]	RESERVED	Reserved.	0x0	R
		11	INT_PPG_LEV1_L	PPG Time Slot L Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot L.	0x0	R/W1C
		10	INT_PPG_LEV1_K	PPG Time Slot K Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot K.	0x0	R/W1C
		9	INT_PPG_LEV1_J	PPG Time Slot J Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot J.	0x0	R/W1C
		8	INT_PPG_LEV1_I	PPG Time Slot I Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot I.	0x0	R/W1C
		7	INT_PPG_LEV1_H	PPG Time Slot H Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot H.	0x0	R/W1C
		6	INT_PPG_LEV1_G	PPG Time Slot G Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot G.	0x0	R/W1C
		5	INT_PPG_LEV1_F	PPG Time Slot F Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot F.	0x0	R/W1C
		4	INT_PPG_LEV1_E	PPG Time Slot E Level 1 interrupt status. This bit is set during a data register update when the	0x0	R/W1C

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot E.		
		3	INT_PPG_LEV1_D	PPG Time Slot D Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot D.	0x0	R/W1C
		2	INT_PPG_LEV1_C	PPG Time Slot C Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot C.	0x0	R/W1C
		1	INT_PPG_LEV1_B	PPG Time Slot B Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot B.	0x0	R/W1C
		0	INT_PPG_LEV1_A	PPG Time Slot A Level 1 interrupt status. This bit is set during a data register update when the configured criteria is met. This bit is set when the Channel 2 TIA saturates during Time Slot A.	0x0	R/W1C
0x006	FIFO_TH	[15:10]	RESERVED	Reserved.	0x0	R
		[9:0]	FIFO_TH	FIFO interrupt generation threshold. Generate the FIFO interrupt during a FIFO write when the number of bytes in the FIFO exceeds this value.	0xC	R/W
0x007	INT_ACLEAR	15	INT_ACLEAR_FIFO	FIFO threshold Interrupt auto clear enabled. Set this bit to enable automatic clearing of the FIFO_TH interrupt each time the FIFO is read.	0x1	R/W
		[14:0]	RESERVED	Reserved.	0x0	R
0x008	CHIP_ID	[15:8]	VERSION	Mask version. R0 = 0x0.	0x0	R
		[7:0]	CHIP_ID	Chip ID.	0xC6	R
0x009	OSC32M	[15:9]	RESERVED	Reserved.	0x0	R
		8	OSC_32M_EFUSE_CTRL	Enables the high frequency oscillator frequency control from the eFuse bits. Write 0 to this bit to enable the frequency control from the OSC_32M_FREQ_ADJ bits.	0x0	R/W
		[7:0]	OSC_32M_FREQ_ADJ	High frequency oscillator frequency control. 0x000 is the lowest frequency, 0x0FF is the maximum frequency.	0x80	R/W
0x00A	OSC32M_CAL	15	OSC_32M_CAL_START	Start high frequency oscillator calibration cycle. Writing a 1 to this bit causes the high frequency oscillator calibration cycle to occur. It enables the oscillator, waits for it to start, and then counts the number 32 MHz cycles during either 128 (1 MHz) or 4 (32 kHz) low frequency cycles based on which one is selected. It updates the OSC_32M_CAL_COUNT bits with this count. The calibration circuit clears the OSC_32M_CAL_START bit when the calibration cycle completes. Silicon Version 0 counts 32 low frequency cycles if using the 32 kHz low frequency oscillator.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[14:0]	OSC_32M_CAL_COUNT	High frequency oscillator calibration count. This register contains the total number of 32 MHz cycles that occurred during the last high frequency oscillator calibration cycle.	0x0	R
0x00B	OSC960K	15	CAPTURE_TIMESTAMP	Enables time stamp capture. This bit is used to arm the time stamp capture function. When set, the next rising edge on the time stamp input (defaults to GPIO0) causes a time stamp capture. This bit is cleared when the time stamp occurs.	0x0	R/W
		[14:12]	RESERVED	Reserved.	0x0	R
		11	OSC_960K_EFUSE_CTRL	Enables the frequency oscillator frequency control from the eFuse bits. Write 0 to this bit to enable the frequency control from the OSC_960K_FREQ_ADJ bits.	0x1	R/W
		10	OSC_CAL_ENABLE	Enables clock calibration clocking. Writing a 1 to this bit enables the clocking of the low frequency and high frequency calibration circuits.	0x0	R/W
		[9:0]	OSC_960K_FREQ_ADJ	Low frequency oscillator frequency control. 0x000 is the lowest frequency, and 0x3FF is the maximum frequency.	0x2B2	R/W
0x00D	TS_FREQ	[15:0]	TIMESLOT_PERIOD_L	Lower 16 bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set as an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x2580	R/W
0x00E	TS_FREQH	[15:7]	RESERVED	Reserved.	0x0	R
		[6:0]	TIMESLOT_PERIOD_H	Upper seven bits of time slot period in low frequency oscillator cycles. The time slot rate is (timer clock frequency)/(TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 960 kHz clock. If the timer clock is set to be an external source from the GPIO, either 960 kHz or 32 kHz, TM_CLK_GPIO_SEL must be configured to match the real clock frequency.	0x0	R/W
0x00F	SYS_CTL	15	SW_RESET	Software Reset. Write 1 to this bit to assert a software reset. This resets the chip to its default values and stopping all analog front end operations. It does not reset the SPI (or optional I^2C) port. The write to this register completes normally.	0x0	R0/W
		[14:12]	RESERVED	Reserved.	0x0	R
		11	RESERVED	Reserved.	0x0	R
		[10:8]	ALT_CLOCKS	External clock select. 000: uses internal clocks. 001: uses GPIO for low frequency oscillator (960 kHz). Timer clock also uses this as source.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				010: uses GPIO for high frequency oscillator (32 MHz). 011: uses GPIO for high frequency oscillator (32 MHz), generate the low frequency oscillator (1 MHz) from the high frequency oscillator. 100: uses GPIO for timer clock, 32 kHz or 960 kHz.		
		[7:6]	ALT_CLK_GPIO	Alternate clock GPIO select. 00: uses GPIO0 for an alternate clock. 01: uses GPIO1 for an alternate clock. 10: reserved. 11: reserved.	0x0	R/W
		5	LP_MODE_SLEEP	Enable the low power mode during the sleep state. It is useful to reduce the power when the output data rate is slow.	0x0	R/W
		4	GO_SLEEP	Sleep before first time slot group on go. Set this bit to force a sleep period before the first sample when setting the device to run, which is especially useful for external sample triggers. 0: starts first time slot sequence on go. 1: sleep before first time slot sequence on go.	0x0	R/W
		3	RANDOM_SLEEP	Enables random sleep linear feedback shift register (LFSR). When enabled, the time slot wake up is varied ±7 cycles with the average being 0.	0x0	R/W
		2	TM_CLK_GPIO_SEL	Selects low frequency clock between 960 kHz and 32 kHz. Use this bit when ALT_CLOCKS is 3'b100. 0: uses the 32 kHz external source from the GPIO as the timer clock. 1: uses the 960 kHz external source from the GPIO as the timer clock.	0x0	R/W
		1	OSC_960K_EN	Enables low frequency oscillator. This bit turns on the 960 kHz low frequency oscillator, which must be left running during all operations using this oscillator.	0x0	R/W
		0	RESERVED	Reserved.	0x0	R
0x010	OPMODE	15	RESERVED	Reserved.	0x0	R
		14	RESERVED	Reserved.	0x0	R
		13	RESERVED	Reserved.	0x0	R
		[12:8]	RESERVED	Reserved.	0x0	R
		[7:4]	PPG_TIMESLOT_EN	PPG time slot enable control. 0000: no PPG time slot. 0001: PPG Time Slot Sequence A. 0010: PPG Time Slot Sequence AB. 0011: PPG Time Slot Sequence ABC. 0100: PPG Time Slot Sequence ABCD.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0101: PPG Time Slot Sequence ABCDE. 0110: PPG Time Slot Sequence ABCDEF. 0111: PPG Time Slot Sequence ABCDEFG. 1000: PPG Time Slot Sequence ABCDEFGH. 1001: PPG Time Slot Sequence ABCDEFGHI. 1010: PPG Time Slot Sequence ABCDEFGHIJ. 1011: PPG Time Slot Sequence ABCDEFGHIJK. 1100: PPG Time Slot Sequence ABCDEFGHIJKL.		
		3	RESERVED	Reserved.	0x0	R
		[2:0]	OP_MODE	Operating mode. Operating mode selection. 000: standby. 001: operate selected time slots. 011: ADC test mode. This mode goes through the normal wake-up sequence and then does continuous ADC cycles based on the PPG Time Slot A setting. 101: Repeat selected time slots without sleep. This mode does one normal wake-up sequence and then cycles through the enabled time slot sequences without going to sleep between. 111: Reserved.	0x0	R/W
0x011	STAMP_L	[15:0]	TIMESTAMP_COUNT_L	Count at last time stamp.	0x0	R
0x012	STAMP_H	[15:0]	TIMESTAMP_COUNT_H	Count at last time stamp.	0x0	R
0x013	STAMPDELTA	[15:0]	TIMESTAMP_SLOT_DELTA	Count remaining until next wake-up start.	0x0	R
0x014	INT_ENABLE_XD	15	INTX_EN_FIFO_TH	FIFO threshold interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status to the Interrupt Channel X function.	0x0	R/W
		14	INTX_EN_FIFO_UFLOW	FIFO underflow Interrupt enable for Interrupt Channel X. Write a 1 to this bit to enable drive of the FIFO underflow status to the Interrupt Channel X function.	0x0	R/W
		13	INTX_EN_FIFO_OFLOW	FIFO overflow interrupt enable for Interrupt Channel X. Write a 1 to this bit to enable drive of the FIFO overflow status to the Interrupt Channel X function.	0x0	R/W
		[12:0]	RESERVED	Reserved.	0x0	R
0x015	INT_ENABLE_YD	15	INTY_EN_FIFO_TH	FIFO threshold interrupt enable. Write a 1 to this bit to enable drive of the FIFO threshold status to the Interrupt Channel Y function.	0x0	R/W
		14	INTY_EN_FIFO_UFLOW	FIFO underflow interrupt enable for Interrupt Channel Y. Write a 1 to this bit to enable drive of the FIFO underflow status to the Interrupt Channel Y function.	0x0	R/W
		13	INTY_EN_FIFO_OFLOW	FIFO overflow Interrupt enable for Interrupt Channel Y. Write a 1 to this bit to enable drive of the FIFO overflow status to the Interrupt Channel Y function.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
		[12:0]	RESERVED	Reserved.	0x0	R
0x01E	FIFO_STATUS_BYTES	[15:10]	RESERVED	Reserved.	0x0	R
		9	RESERVED	Reserved.	0x0	R
		8	ENA_STAT_LEVX	Enables Level 0 and Level 1 interrupt status byte upper. This byte contains the interrupt status for Level Interrupt 0 and Level Interrupt 1 for PPG Time Slot I to Time Slot L.	0x0	R/W
		7	ENA_STAT_LEV1	Enables Level 1 interrupt status byte lower. This byte contains the interrupt status for Level Interrupt 1 for PPG Time Slot A to Time Slot H.	0x0	R/W
		6	ENA_STAT_LEV0	Enables Level 0 interrupt status byte lower. This byte contains the interrupt status for Level Interrupt 0 for PPG Time Slot A to Time Slot H.	0x0	R/W
		5	ENA_SEQ_NUM	Enables the 4-bit sequence number for the time slot sequence, which cycles from 0 to 15 and is incremented with wraparound every time the time slot sequence completes.	0x0	R/W
		[4:0]	RESERVED	Reserved.	0x0	R
0x020	INPUT_SLEEP	[15:8]	RESERVED	Reserved.	0x0	R
		[7:4]	INP_SLEEP_34	Input pair sleep state for Input 3 and Input 4. 0x0: both inputs float. 0x1: even and odd shorted together (floating short of differential). Only shorts if PAIR34 is 1. 0x2: both connected to Cathode 1 (also shorted together if configured as differential pair). 0x4: odd connected to Cathode 1. Even floating. 0x8: odd floating. Even connected to Cathode 1.	0x0	R/W
		[3:0]	INP_SLEEP_12	Input pair sleep state for Input 1 and Input 2. 0x0: both inputs float. 0x1: even and odd shorted together (floating short of differential). Only shorts if PAIR12 is 1. 0x2: both connected to Cathode 1 (also shorted together if configured as differential pair). 0x4: odd connected to Cathode 1. Even floating. 0x8: odd floating. Even connected to Cathode 1.	0x0	R/W
0x021	INPUT_CFG	[15:6]	RESERVED	Reserved.	0x0	R
		[5:4]	VC1_SLEEP	Cathode 1 sleep state. 0: cathode set to AVDD during sleep. 1: cathode set to GND during sleep. 10: cathode floating during sleep.	0x0	R/W
		[3:2]	RESERVED	Reserved.	0x0	R
		1	PAIR34	Input pair configuration. 0: uses as two single-ended inputs. 1: uses as a differential pair.	0x0	R/W
		0	PAIR12	Input pair configuration. 0: uses as two single-ended inputs. 1: used as a differential pair.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x022	GPIO_CFG	[15:14]	GPIO_SLEW	Slew control for GPIO pins. 0: slowest. 1: slow. 10: fastest. 11: fast.	0x0	R/W
		[13:12]	GPIO_DRV	Drive control for GPIO pins. 0: medium. 1: weak. 10: strong. 11: strong.	0x0	R/W
		[11:9]	RESERVED	Reserved.	0x0	R
		[8:6]	RESERVED	Reserved.	0x0	R
		[5:3]	GPIO_PIN_CFG1	GPIO1 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled Input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal. 101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.	0x0	R/W
		[2:0]	GPIO_PIN_CFG0	GPIO0 pin configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal. 101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.	0x0	R/W
0x023	GPIO01	[15:8]	GPIOOUT1	GPIO Pin 1 Output Select. 0x00: Output 0. 0x01: Output 1. 0x02: Interrupt X. 0x03: Interrupt Y. 0x08: LED1x amplifier enable. 0x09: LED2x amplifier enable. 0x0C: any LED amplifier enable. 0x0F: 32 MHz oscillator output divided by 64 (500 kHz). 0x10: time slot specific output pattern defined by GOUT_x and GOUT_SLEEP bits. 0x16: low frequency oscillator output. 0x17: 32 MHz oscillator output.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0x18: 32 MHz oscillator output divided by 32 (1 MHz). 0x20: Time Slot A active. 0x21: Time Slot B active. 0x22: Time Slot C active. 0x23: Time Slot D active. 0x24: Time Slot E active. 0x25: Time Slot F active. 0x26: Time Slot G active. 0x27: Time Slot H active. 0x28: Time Slot I active. 0x29: Time Slot J active. 0x2A: Time Slot K active. 0x2B: Time Slot L active. 0x31: Time Slot A LED pulse. 0x32: Time Slot B LED pulse. 0x33: Time Slot C LED pulse. 0x34: Time Slot D LED pulse. 0x35: Time Slot E LED pulse. 0x36: Time Slot F LED pulse. 0x37: Time Slot G LED pulse. 0x38: Time Slot H LED pulse. 0x39: Time Slot I LED pulse. 0x3A: Time Slot J LED pulse. 0x3B: Time Slot K LED pulse. 0x3C: Time Slot L LED pulse. 0x3F: Time Slot x LED pulse. 0x40: Time Slot A modulation pulse. 0x41: Time Slot B modulation pulse. 0x42: Time Slot C modulation pulse. 0x43: Time Slot D modulation pulse. 0x44: Time Slot E modulation pulse. 0x45: Time Slot F modulation pulse. 0x46: Time Slot G modulation pulse. 0x47: Time Slot H modulation pulse. 0x48: Time Slot I modulation pulse. 0x49: Time Slot J modulation pulse. 0x4A: Time Slot K modulation pulse. 0x4B: Time Slot L modulation pulse. 0x4F: Time Slot x modulation pulse. 0x50: output data cycle occurred in Time Slot A. 0x51: output data cycle occurred in Time Slot B. 0x52: output data cycle occurred in Time Slot C. 0x53: output data cycle occurred in Time Slot D. 0x54: output data cycle occurred in Time Slot E. 0x55: output data cycle occurred in Time Slot F. 0x56: output data cycle occurred in Time Slot G. 0x57: output data cycle occurred in Time Slot H. 0x58: output data cycle occurred in Time Slot I.		

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0x59: output data cycle occurred in Time Slot J. 0x5A: output data cycle occurred in Time Slot K. 0x5B: output data cycle occurred in Time Slot L. 0x5F: output data cycle occurred in any time slot.		
		[7:0]	GPIOOUT0	GPIO Pin 0 Output Select. Output options are identical to those described in the GPIOOUT1 bits.	0x0	R/W
0x025	GPIO_IN	[15:4]	RESERVED	Reserved.	0x0	R
		[3:0]	GPIO_INPUT	GPIO input value (if enabled).	0x0	R
0x026	GPIO_EXT	[15:9]	RESERVED	Reserved.	0x0	R
		8	GOUT_SLEEP	Time slot specific GPIO signal sleep value.	0x0	R/W
		7	TIMESTAMP_INV	Time stamp trigger invert. 0: time stamp trigger is rising edge. 1: time stamp trigger is falling edge.	0x0	R/W
		6	TIMESTAMP_ALWAYS_EN	Enables time stamp always on. When set, it does not automatically clear the CAPTURE_TIMESTAMP. This bit provides an always armed time stamp.	0x0	R/W
		[5:4]	TIMESTAMP_GPIO	Time stamp GPIO selection. 00: uses GPIO0 for time stamp (default). 01: uses GPIO1 for time stamp. 10: reserved. 11: reserved.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		2	EXT_SYNC_EN	External synchronization enabled. When enabled, use the GPIO selected by EXT_SYNC_GPIO to trigger samples rather than the period counter.	0x0	R/W
		[1:0]	EXT_SYNC_GPIO	External sync GPIO selection. 00: uses GPIO0 for external synchronization (default). 01: uses GPIO1 for external synchronization. 10: reserved. 11: reserved.	0x0	R/W
0x02F	FIFO_DATA	[15:0]	FIFO_DATA	FIFO data port.	0x0	R
0x044	EFUSE	15	EFUSE_REFRESH	Write 1 to this bit to assert a shadow register reset. It enables the eFuse auto refresh operation and cause shadow registers to update from fuses. The write to this register completes normally.	0x0	R0/W
		[14:3]	RESERVED	Reserved.	0x0	R
		[2:1]	EFUSE_EN	eFuse enable. 00: off (eFuse held in reset, and shadow register is also reset). 01: reserved. 10: standby (eFuse in low power state, and shadow register available). 11: on. Must have 32 MHz high frequency oscillator running. Transitions from 00 to 11 cause shadow registers to update from fuses. Must	0x2	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				be in on state to refresh, run built-in self test (BIST), or program. Off and standby states have lowest power. Must have 32 MHz high frequency oscillator operating for eFuse block to operate.		
		0	EFUSE_REG_EN	eFuse register access enable.	0x1	R/W
0x057	IO_ADJUST	[15:7]	RESERVED	Reserved.	0x0	R
		6	LOW_IOVDD_EN	Set to 0x0 if a IOVDD of 3 V or higher is used. Default value of 1 is used for a IOVDD lower than 3 V because the typical value of IOVDD is 1.8 V.	0x1	R/W
		[5:4]	RESERVED	Reserved.	0x1	R/W
		[3:2]	SPI_SLEW	Slew control for SPI pins. 0: slowest. 1: slow. 10: fastest. 11: fast.	0x0	R/W
		[1:0]	SPI_DRV	Drive control for SPI pins. 0: medium. 1: weak. 10: strong. 11: strong.	0x0	R/W
0x120	TS_CTRL_A	[15:14]	RESERVED	Reserved.	0x0	R
0x140 0x160 0x180 0x1A0 0x1C0 0x1E0 0x200 0x220 0x240	TS_CTRL_B TS_CTRL_C TS_CTRL_D TS_CTRL_E TS_CTRL_F TS_CTRL_G TS_CTRL_H TS_CTRL_I TS_CTRL_J	[13:11]	SAMPLE_TYPE_x	Time slot sampling type. 000: multiplexed one region digital integrate mode. 001: multiplexed two region digital integrate mode. 010: one region digital integrate mode. 011: two region digital integrate mode. 100: direct sample mode. 101: reserved. 110: reserved. 111: reserved.	0x2	R/W
0x260	TS_CTRL_K	10	RESERVED	Reserved.	0x0	R
0x280	TS_CTRL_L	[9:0]	TIMESLOT_OFFSET_x	Time Slot x offset in 64 × 960 kHz or 64 × (external 960 kHz) cycles.	0x0	R/W
0x121	TS_PATH_A	[15:12]	PRE_WIDTH_x	Precondition duration for this time slot. This value is in 2 µs increments. A value of 0 skips the precondition state.	0x4	R/W
0x141 0x161 0x181 0x1A1 0x1C1 0x1E1	TS_PATH_B TS_PATH_C TS_PATH_D TS_PATH_E TS_PATH_F TS_PATH_G	[11:10]	AMBIENT_CANCELLATION_x	Select the control type for the ambient cancellation DAC. 0: disables the ambient cancellation loop. 1: enables coarse and fine loop. 10: enables coarse loop only. 11: enables MCU control.	0x0	R/W
		9	GOUT_x	Time slot specific GPIO value for this time slot.	0x0	R/W
0x201	TS_PATH_H	[8:7]	RESERVED	Reserved.	0x0	R
0x221	TS_PATH_I	[6:0]	AFE_PATH_CFG_x	Bypass and input mux select. Integrator is either an integrator or buffer based on mode and AFE_INT_C_BUF for the active time slot.	0x20	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x241 0x261 0x281	TS_PATH_J TS_PATH_K TS_PATH_L			0x20: TIA, buffer, and ADC (2× TIA gain). 0x28: TIA buffer, and ADC (1× TIA gain). 0x35: buffer and ADC. 0x41: ADC.		
0x122	INPUTS_A	[15:14]	INP4_SEL_x	Input 4 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between Input 4 and Channel 3, and set Bit 1 to 1 to enable the connection between Input 4 and Channel 4.	0x0	R/W
0x142	INPUTS_B	[13:12]	INP3_SEL_x	IN3 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN3 and Channel 3, and set Bit 1 to 1 to enable the connection between IN3 and Channel 4.	0x0	R/W
0x162	INPUTS_C	[11:10]	INP2_SEL_x	IN2 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN2 and Channel 3, and set Bit 1 to 1 to enable the connection between IN2 and Channel 4.	0x0	R/W
0x182	INPUTS_D	[9:8]	INP1_SEL_x	IN1 to Channel 3 and Channel 4 enable. Set Bit 0 to 1 to enable the connection between IN1 and Channel 3, and set Bit 1 to 1 to enable the connection between IN1 and Channel 4.	0x0	R/W
0x1A2 0x1C2 0x1E2 0x202 0x222 0x242 0x262 0x282	INPUTS_E INPUTS_F INPUTS_G INPUTS_H INPUTS_I INPUTS_J INPUTS_K INPUTS_L	[7:4]	INP34_x	IN3 and IN4 input pair enabled. 0000: input pair disabled. IN3 and IN4 disconnected. 0001: IN3 connected to Channel 1 and IN4 disconnected. 0010: IN3 connected to Channel 2 and IN4 disconnected. 0011: IN4 connected to Channel 1 and IN3 disconnected. 0100: IN4 connected to Channel 2 and IN3 disconnected. 0101: IN3 connected to Channel 1 and IN4 connected to Channel 2. 0110: IN4 connected to Channel 1 and IN3 connected to Channel 2. 0111: IN3 and IN4 to Channel 1, single-ended or differentially based on PAIR34, and none to Channel 2. 1000: IN3 and IN4 connected to Channel 2, and single-ended or differentially based on PAIR34.	0x0	R/W
		[3:0]	INP12_x	IN1 and IN2 input pair enabled. 0000: input pair disabled. IN1 and IN2 disconnected. 0001: IN1 connected to Channel 1, and IN2 disconnected. 0010: IN1 connected to Channel 2, and IN2 disconnected. 0011: IN2 connected to Channel 1, and IN1 disconnected. 0100: IN2 connected to Channel 2, and IN1 disconnected. 0101: IN1 connected to Channel 1, and IN2 connected to Channel 2.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				0110: IN2 connected to Channel 1, and IN1 connected to Channel 2. 0111: IN1 and IN2 connected to Channel 1, and single-ended or differentially based on PAIR12. 1000: IN1 and IN2 connected to Channel 2, and single-ended or differentially based on PAIR12.		
0x123	CATHODE_A	15	RESERVED	Reserved.	0x0	R
0x143 0x163 0x183 0x1A3 0x1C3 0x1E3 0x203 0x223	CATHODE_B CATHODE_C CATHODE_D CATHODE_E CATHODE_F CATHODE_G CATHODE_H CATHODE_I	[14:12]	PRECON_x	Precondition value for enabled inputs during this time slot. 000: float inputs. 001: precondition to VC1. 010: reserved. 011: reserved. 100: precondition with TIA input. 101: precondition with TIA_VREF. 110: precondition by shorting differential pair.	0x0	R/W
0x243	CATHODE_J	[11:10]	RESERVED	Reserved.	0x0	R
0x263 0x283	CATHODE_K CATHODE_L	[9:8]	AFE_VREF_AMB_SEL_x	Voltage trim for reference buffer during the coarse ambient phase. 0: TIA_VREF = 0.8855 V, photodiode reverse bias = 600mV. 1: TIA_VREF = 0.8855 V, photodiode reverse bias = 400mV. 10: TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV. 11: TIA_VREF = 1.265 V.	0x2	R/W
		[7:6]	VC1_AMB_SEL_x	VC1 state during the coarse ambient phase. 0: AVDD. 1: TIA_VREF. 10: V_DELTA (TIA_VREF + photodiode reverse bias). 11: GND.	0x0	R/W
		[5:4]	VC1_PULSE_x	VC1 pulse control. 0: no pulsing. 1: alternate odd/even time slots. 10: pulse to alternate value using modulate pulse. 11: leave VC1 floating.	0x0	R/W
		[3:2]	VC1_ALT_x	VC1 alternate pulsed state for this time slot. 0: AVDD. 1: TIA_VREF. 10: V_DELTA. 11: GND.	0x0	R/W
		[1:0]	VC1_SEL_x	VC1 active state for this time slot. 0: AVDD. 1: TIA_VREF. 10: V_DELTA. 11: GND.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x124	AFE_TRIM1_A	15	AFE_TIA_SAT_DETECT_EN_x	Enable TIA saturation detection. Set to 1 to enable TIA saturation detection circuitry. Enables Channel 1 and also Channel 2 if Channel 2 is enabled.	0x0	R/W
0x144	AFE_TRIM1_B	[14:13]	RESERVED	Reserved.	0x0	R
0x164	AFE_TRIM1_C	[12:11]	AFE_BUFFER_GAIN_x	Buffer gain selection.	0x0	R/W
0x184	AFE_TRIM1_D			0: buffer gain = 1 (R_{FB}/R_{IN} = 200 kΩ/200 kΩ).		
0x1A4	AFE_TRIM1_E			1: buffer gain = 2 (R_{FB}/R_{IN} = 200 kΩ/100 kΩ).		
0x1C4	AFE_TRIM1_F			10: buffer gain = 1 (R_{FB}/R_{IN} = 100 kΩ/100 kΩ).		
0x1E4	AFE_TRIM1_G			11: buffer gain = 2 (R_{FB}/R_{IN} = 100 kΩ/50 kΩ).		
0x204	AFE_TRIM1_H	10	VREF_PULSE_x	Reference voltage (V_{REF}) pulse control.	0x0	R/W
0x224	AFE_TRIM1_I			0: no pulsing.		
0x244	AFE_TRIM1_J			1: pulse V_{REF} based on modulate pulse.		
0x264	AFE_TRIM1_K	[9:8]	AFE_TRIM_VREF_x	Voltage trim for reference buffer.	0x2	R/W
0x284	AFE_TRIM1_L			00: TIA_VREF = 0.8855 V, photodiode reverse bias = 600 mV.		
				01: TIA_VREF = 0.8855 V, photodiode reverse bias = 400 mV.		
				10: TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV.		
				11: TIA_VREF = 1.265 V.		
		[7:6]	VREF_PULSE_VAL_x	V_{REF} pulse alternate value.	0x3	R/W
				00: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 600 mV.		
				01: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 400 mV.		
				10: modulate TIA_VREF = 0.8855 V, photodiode reverse bias = 200 mV.		
				11: modulate TIA_VREF = 1.265 V.		
		[5:3]	TIA_GAIN_CH2_x	TIA resistor gain setting for Channel 2.	0x1	R/W
				0: 400 kΩ.		
				1: 200 kΩ.		
				10: 100 kΩ.		
				11: 50 kΩ.		
				100: 25 kΩ.		
				101: 12.5 kΩ.		
		[2:0]	TIA_GAIN_CH1_x	TIA resistor gain setting for Channel 1.	0x1	R/W
				0: 400 kΩ.		
				1: 200 kΩ.		
				10: 100 kΩ.		
				11: 50 kΩ.		
				100: 25 kΩ.		
				101: 12.5 kΩ.		
0x125	AFE_TRIM2_A	[15:13]	RESERVED	Reserved.	0x0	R
0x145	AFE_TRIM2_B	12	AFE_BUFFER_CAP_x	Buffer feedback capacitor selection.	0x0	R/W
0x165	AFE_TRIM2_C			0: 6.3 pF.		
0x185	AFE_TRIM2_D			1: 12.6 pF.		

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x1A5	AFE_TRIM2_E	[11:6]	RESERVED	Reserved.	0x0	R
0x1C5	AFE_TRIM2_F	[5:3]	TIA_GAIN_CH4_x	TIA resistor gain setting for Channel 4. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x0	R/W
0x1E5	AFE_TRIM2_G					
0x205	AFE_TRIM2_H					
0x225	AFE_TRIM2_I					
0x245	AFE_TRIM2_J					
0x265	AFE_TRIM2_K					
0x285	AFE_TRIM2_L					
		[2:0]	TIA_GAIN_CH3_x	TIA resistor gain setting for Channel 3. 000: 400 kΩ. 001: 200 kΩ. 010: 100 kΩ. 011: 50 kΩ. 100: 25 kΩ. 101: 12.5 kΩ.	0x0	R/W
0x126	AFE_DAC1_A	[15:7]	DAC_AMBIENT_CH1_x	Channel 1 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x146	AFE_DAC1_B	[6:0]	DAC_LED_DC_CH1_x	Channel 1 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x166	AFE_DAC1_C					
0x186	AFE_DAC1_D					
0x1A6	AFE_DAC1_E					
0x1C6	AFE_DAC1_F					
0x1E6	AFE_DAC1_G					
0x206	AFE_DAC1_H					
0x226	AFE_DAC1_I					
0x246	AFE_DAC1_J					
0x266	AFE_DAC1_K					
0x286	AFE_DAC1_L					
0x127	AFE_DAC2_A	[15:7]	DAC_AMBIENT_CH2_x	Channel 2 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x147	AFE_DAC2_B	[6:0]	DAC_LED_DC_CH2_x	Channel 2 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x167	AFE_DAC2_C					
0x187	AFE_DAC2_D					
0x1A7	AFE_DAC2_E					
0x1C7	AFE_DAC2_F					
0x1E7	AFE_DAC2_G					
0x207	AFE_DAC2_H					
0x227	AFE_DAC2_I					
0x247	AFE_DAC2_J					
0x267	AFE_DAC2_K					
0x287	AFE_DAC2_L					
0x128	LED_POW12_A	15	RESERVED	Reserved.	0x0	R
0x148	LED_POW12_B	[14:8]	LED_CURRENT2_x	LED current setting for the LED2A, LED2B, LED2C, or LED2D output. Set to 0 to disable.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.		
0x168	LED_POW12_C	7	RESERVED	Reserved.	0x0	R
0x188	LED_POW12_D	[6:0]	LED_CURRENT1_x	Led current setting for the LED1A, LED1B, LED1C, or LED1D output. Set to 0 to disable. Output current varies monotonically from 1.57 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x1A8	LED_POW12_E					
0x1C8	LED_POW12_F					
0x1E8	LED_POW12_G					
0x208	LED_POW12_H					
0x228	LED_POW12_I					
0x248	LED_POW12_J					
0x268	LED_POW12_K					
0x288	LED_POW12_L					
0x129	LED_MODE_A	[15:8]	RESERVED	Reserved.	0x0	R
0x149	LED_MODE_B	[7:6]	LED_DRIVESIDE2_x	Led output select for LED2x. 00: drives LED on Output LED2A. 01: drives LED on Output LED2B. 10: drives LED on Output LED2C. 11: drives LED on Output LED2D.	0x0	R/W
0x169	LED_MODE_C					
0x189	LED_MODE_D					
0x1A9	LED_MODE_E					
0x1C9	LED_MODE_F					
0x1E9	LED_MODE_G	[5:4]	LED_DRIVESIDE1_x	Led output select for LED1x. 00: drives LED on Output LED1A. 01: drives LED on Output LED1B. 10: drives LED on Output LED1C. 11: drives LED on Output LED1D.	0x0	R/W
0x209	LED_MODE_H					
0x229	LED_MODE_I					
0x249	LED_MODE_J					
0x269	LED_MODE_K					
0x289	LED_MODE_L	[3:2]	RESERVED	Reserved.	0x0	R
		1	LED_MODE2_x	Choose the operation mode of the LED2x. 0: high SNR mode. 1: low compliance mode.	0x0	R/W
		0	LED_MODE1_x	Choose the operation mode of the LED1x. 0: high SNR mode. 1: low compliance mode.	0x0	R/W
0x12A	COUNTS_A	[15:8]	NUM_INT_x	Number of ADC cycles or acquisition width. Number of analog integration cycles per ADC conversion or the acquisition width for digital integration. A setting of 0 is not allowed.	0x1	R/W
0x14A	COUNTS_B	[7:0]	NUM_REPEAT_x	Number of sequence repeats. Total number of pulses = NUM_INT_x × NUM_REPEAT_x. A setting of 0 is not allowed.	0x1	R/W
0x16A	COUNTS_C					
0x18A	COUNTS_D					
0x1AA	COUNTS_E					
0x1CA	COUNTS_F					
0x1EA	COUNTS_G					
0x20A	COUNTS_H					
0x22A	COUNTS_I					
0x24A	COUNTS_J					
0x26A	COUNTS_K					

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x28A	COUNTS_L					
0x12B	PERIOD_A	15	RESERVED	Reserved.	0x0	R
0x14B 0x16B 0x18B 0x1AB 0x1CB	PERIOD_B PERIOD_C PERIOD_D PERIOD_E PERIOD_F	14	COARSE_LOOP_WIDTH_x	The time duration for the coarse ambient cancellation loop. 0: 10 µs. 1: 20 µs.	0x0	R/W
0x1EB 0x20B 0x22B 0x24B	PERIOD_G PERIOD_H PERIOD_I PERIOD_J	[13:12]	MOD_TYPE_x	Modulation connection type. 00: TIA is continuously connected to the input after the precondition. No connection modulation. 01: float type operation. Pulse connection from the input to the TIA with modulate pulse, floating between pulses. 10: nonfloat type connection modulation. Pulse connection from the input to the TIA. Connect to the precondition value between pulses.	0x0	R/W
0x26B	PERIOD_K	[11:10]	RESERVED	Reserved.	0x0	R
0x28B	PERIOD_L	[9:0]	MIN_PERIOD_x	Minimum period for pulse repetition. Override for the automatically calculated period. Used in float type operations to set the float time of second and subsequent floats using the formula float = MIN_PERIOD_x − MOD_WIDTH_x.	0x0	R/W
0x12C	LED_PULSE1_A	[15:8]	LED_WIDTH_A	LED pulse width.	0x2	R/W
0x14C 0x16C 0x18C 0x1AC 0x1CC 0x1EC 0x20C 0x22C 0x24C 0x26C 0x28C	LED_PULSE1_B LED_PULSE1_C LED_PULSE1_D LED_PULSE1_E LED_PULSE1_F LED_PULSE1_G LED_PULSE1_H LED_PULSE1_I LED_PULSE1_J LED_PULSE1_K LED_PULSE1_L	[7:0]	LED_OFFSET_A	LED pulse offset.	0x10	R/W
0x12D	AFE_DAC3_A	[15:7]	DAC_AMBIENT_CH3_x	Channel 3 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x14D 0x16D 0x18D 0x1AD 0x1CD 0x1ED 0x20D 0x22D 0x24D	AFE_DAC3_B AFE_DAC3_C AFE_DAC3_D AFE_DAC3_E AFE_DAC3_F AFE_DAC3_G AFE_DAC3_H AFE_DAC3_I AFE_DAC3_J	[6:0]	DAC_LED_DC_CH3_x	Channel 3 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x26D	AFE_DAC3_K					
0x28D	AFE_DAC3_L					
0x12E	AFE_DAC4_A	[15:7]	DAC_AMBIENT_CH4_x	Channel 4 ambient cancellation DAC code, from 0 µA to 300 µA with 0.6 µA/LSB.	0x0	R/W
0x14E	AFE_DAC4_B	[6:0]	DAC_LED_DC_CH4_x	Channel 4 LED DC offset cancellation DAC code, from 0 µA to 190 µA with 1.5 µA/LSB. Set to 0 to disable.	0x0	R/W
0x16E	AFE_DAC4_C					
0x18E	AFE_DAC4_D					
0x1AE	AFE_DAC4_E					
0x1CE	AFE_DAC4_F					
0x1EE	AFE_DAC4_G					
0x20E	AFE_DAC4_H					
0x22E	AFE_DAC4_I					
0x24E	AFE_DAC4_J					
0x26E	AFE_DAC4_K					
0x28E	AFE_DAC4_L					
0x12F	THRESH0_A	[15:13]	RESERVED	Reserved.	0x0	R
0x14F	THRESH0_B	[12:8]	THRESH0_SHIFT_x	Shift for threshold compare Level Interrupt 0. Shift THRESH0_VALUE_x by this amount before comparing.	0x0	R/W
0x16F	THRESH0_C	[7:0]	THRESH0_VALUE_x	Value for threshold compare Level Interrupt 0.	0x0	R/W
0x18F	THRESH0_D					
0x1AF	THRESH0_E					
0x1CF	THRESH0_F					
0x1EF	THRESH0_G					
0x20F	THRESH0_H					
0x22F	THRESH0_I					
0x24F	THRESH0_J					
0x26F	THRESH0_K					
0x28F	THRESH0_L					
0x130	MOD_PULSE_A	[15:8]	MOD_WIDTH_x	Modulation pulse width. 0 = disable.	0x0	R/W
0x150	MOD_PULSE_B	[7:0]	MOD_OFFSET_x	Modulation pulse offset.	0x1	R/W
0x170	MOD_PULSE_C					
0x190	MOD_PULSE_D					
0x1B0	MOD_PULSE_E					
0x1D0	MOD_PULSE_F					
0x1F0	MOD_PULSE_G					
0x210	MOD_PULSE_H					
0x230	MOD_PULSE_I					
0x250	MOD_PULSE_J					
0x270	MOD_PULSE_K					
0x290	MOD_PULSE_L					
0x131	PATTERN1_A	[15:12]	LED_DISABLE_x	Four pulse LED disable pattern. Set to 1 to disable the LED pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x151	PATTERN1_B	[11:8]	MOD_DISABLE_x	Four pulse modulation disable pattern. Set to 1 to disable the modulation pulse in the matching	0x0	R/W

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
				position in a group of four pulses. The LSB maps to the first pulse.		
0x171	PATTERN1_C	[7:4]	SUBTRACT_x	Four pulse subtract pattern. Set to 1 to negate the math operation in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x191	PATTERN1_D	[3:0]	AFE_SWAP_x	Four pulse integration reverse pattern. Set to 1 to reverse the integrator positive or negative pulse order in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x1B1	PATTERN1_E					
0x1D1	PATTERN1_F					
0x1F1	PATTERN1_G					
0x211	PATTERN1_H					
0x231	PATTERN1_I					
0x251	PATTERN1_J					
0x271	PATTERN1_K					
0x291	PATTERN1_L					
0x132	THRESH_CFG_A	[15:11]	RESERVED	Reserved.	0x0	R
0x152	THRESH_CFG_B	10	THRESH1_DIR_x	Type of comparison for Level Interrupt 1. 0: set when less than the threshold. 1: set when more than the threshold.	0x0	R/W
0x172	THRESH_CFG_C					
0x192	THRESH_CFG_D					
0x1B2	THRESH_CFG_E	[9:8]	THRESH1_TYPE_x	Type of comparison for Level Interrupt 1. 0: off (no comparison). 1: compare to signal. 10: compare to lit. 11: compare to dark.	0x0	R/W
0x1D2	THRESH_CFG_F					
0x1F2	THRESH_CFG_G					
0x212	THRESH_CFG_H					
0x232	THRESH_CFG_I					
0x252	THRESH_CFG_J	[7:3]	RESERVED	Reserved.	0x0	R
0x272	THRESH_CFG_K	2	THRESH0_DIR_x	Type of comparison for Level Interrupt 0. 0: set when less than the threshold. 1: set when more than the threshold.	0x0	R/W
0x292	THRESH_CFG_L					
		[1:0]	THRESH0_TYPE_x	Type of comparison for Level Interrupt 0. 0: off (no comparison). 1: compare to signal. 10: compare to lit. 11: compare to dark.	0x0	R/W
0x133	ADC_OFF1_A	[15:14]	RESERVED	Reserved.	0x0	R
0x153	ADC_OFF1_B	[13:0]	CH1_ADC_ADJUST_x	Adjustment to the ADC value, which is subtracted from the ADC value for Channel 1.	0x0	R/W
0x173	ADC_OFF1_C					
0x193	ADC_OFF1_D					
0x1B3	ADC_OFF1_E					
0x1D3	ADC_OFF1_F					
0x1F3	ADC_OFF1_G					
0x213	ADC_OFF1_H					
0x233	ADC_OFF1_I					
0x253	ADC_OFF1_J					
0x273	ADC_OFF1_K					
0x293	ADC_OFF1_L					

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x134	ADC_OFF2_A	[15:14]	RESERVED	Reserved.	0x0	R/W
0x154	ADC_OFF2_B	[13:0]	CH2_ADC_ADJUST_x	Adjustment to the ADC value, which is subtracted from the ADC value for Channel 2.	0x0	R/W
0x174	ADC_OFF2_C					
0x194	ADC_OFF2_D					
0x1B4	ADC_OFF2_E					
0x1D4	ADC_OFF2_F					
0x1F4	ADC_OFF2_G					
0x214	ADC_OFF2_H					
0x234	ADC_OFF2_I					
0x254	ADC_OFF2_J					
0x274	ADC_OFF2_K					
0x294	ADC_OFF2_L					
0x135	DATA1_A	[15:11]	DARK_SHIFT_x	Dark data shift.	0x0	R/W
0x155	DATA1_B	[10:8]	DARK_SIZE_x	Dark data size.	0x0	R/W
0x175	DATA1_C	[7:3]	SIGNAL_SHIFT_x	Signal data shift.	0x0	R/W
0x195	DATA1_D	[2:0]	SIGNAL_SIZE_x	Signal data size.	0x3	R/W
0x1B5	DATA1_E					
0x1D5	DATA1_F					
0x1F5	DATA1_G					
0x215	DATA1_H					
0x235	DATA1_I					
0x255	DATA1_J					
0x275	DATA1_K					
0x295	DATA1_L					
0x136	DATA2_A	[15:8]	RESERVED	Reserved.	0x0	R
0x156	DATA2_B	[7:3]	LIT_SHIFT_x	Lit data shift.	0x0	R/W
0x176	DATA2_C	[2:0]	LIT_SIZE_x	Lit data size.	0x0	R/W
0x196	DATA2_D					
0x1B6	DATA2_E					
0x1D6	DATA2_F					
0x1F6	DATA2_G					
0x216	DATA2_H					
0x236	DATA2_I					
0x256	DATA2_J					
0x276	DATA2_K					
0x296	DATA2_L					
0x137	DECIMATE_A	[15:14]	CHANNEL_EN_x	Channel enable. 00: only Channel 1 enabled. 01: Channel 1 and Channel 2 enabled. 10: Channel 1, Channel 2, and Channel 3 enabled. 11: Channel 1, Channel 2, Channel 3, and Channel 4 enabled.	0x0	R/W
0x157	DECIMATE_B					
0x177	DECIMATE_C					
0x197	DECIMATE_D					
0x1B7	DECIMATE_E					

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x1D7	DECIMATE_F	[13:11]	RESERVED	Reserved.	0x0	R
0x1F7	DECIMATE_G	[10:4]	SUBSAMPLE_RATIO_x	Reduce the output data rate that is equal to (the timer clock frequency)/(TIMESLOT_PERIOD_x)/(SUBSAMPLE_RATIO_x).When this bit is set larger than 1, operate the time slot only once per (SUBSAMPLE_RATIO_x) time slot sequence. This subsampling aligns to other time slots using the same SUBSAMPLE_RATIO_x. It skips (SUBSAMPLE_RATIO_x − 1) times and then executes the time slot. Output data rate is the sample rate/(SUBSAMPLE_RATIO_x).	0x1	R/W
0x217	DECIMATE_H	[3:0]	RESERVED	Reserved.	0x0	R
0x237	DECIMATE_I					
0x257	DECIMATE_J					
0x277	DECIMATE_K					
0x297	DECIMATE_L					
0x138	DIGINT_LIT_A	[15:9]	RESERVED	Reserved.	0x0	R
0x158	DIGINT_LIT_B	[8:0]	LIT_OFFSET_x	Acquisition Window Lit Offset for Time Slot x.	0x26	R/W
0x178	DIGINT_LIT_C					
0x198	DIGINT_LIT_D					
0x1B8	DIGINT_LIT_E					
0x1D8	DIGINT_LIT_F					
0x1F8	DIGINT_LIT_G					
0x218	DIGINT_LIT_H					
0x238	DIGINT_LIT_I					
0x258	DIGINT_LIT_J					
0x278	DIGINT_LIT_K					
0x298	DIGINT_LIT_L					
0x139	DIGINT_DARK_A	[15:7]	DARK2_OFFSET_x	Acquisition window Dark Offset 2 for Time Slot x.	0x1	R/W
0x159	DIGINT_DARK_B	[6:0]	DARK1_OFFSET_x	Acquisition window Dark Offset 1 for Time Slot x.	0x6	R/W
0x179	DIGINT_DARK_C					
0x199	DIGINT_DARK_D					
0x1B9	DIGINT_DARK_E					
0x1D9	DIGINT_DARK_F					
0x1F9	DIGINT_DARK_G					
0x219	DIGINT_DARK_H					
0x239	DIGINT_DARK_I					
0x259	DIGINT_DARK_J					
0x279	DIGINT_DARK_K					
0x299	DIGINT_DARK_L					
0x13A	ADC_OFF3_A	[15:14]	RESERVED	Reserved.	0x0	R
0x15A	ADC_OFF3_B	[13:0]	CH3_ADC_ADJUST_x	Adjustment to ADC value, which is subtracted from the ADC value for Channel 3.	0x0	R/W
0x17A	ADC_OFF3_C					
0x19A	ADC_OFF3_D					
0x1BA	ADC_OFF3_E					

REGISTER DETAILS

Table 16. Register Details (Continued)

Reg	Name	Bits	Bit Name	Description	Reset	Access
0x1DA	ADC_OFF3_F					
0x1FA	ADC_OFF3_G					
0x21A	ADC_OFF3_H					
0x23A	ADC_OFF3_I					
0x25A	ADC_OFF3_J					
0x27A	ADC_OFF3_K					
0x29A	ADC_OFF3_L					
0x13B	ADC_OFF4_A	[15:14]	RESERVED	Reserved.	0x0	R
0x15B	ADC_OFF4_B	[13:0]	CH4_ADC_ADJUST_x	Adjustment to ADC value, which is subtracted from the ADC value for Channel 4.	0x0	R/W
0x17B	ADC_OFF4_C					
0x19B	ADC_OFF4_D					
0x1BB	ADC_OFF4_E					
0x1DB	ADC_OFF4_F					
0x1FB	ADC_OFF4_G					
0x21B	ADC_OFF4_H					
0x23B	ADC_OFF4_I					
0x25B	ADC_OFF4_J					
0x27B	ADC_OFF4_K					
0x29B	ADC_OFF4_L					
0x13C	THRESH1_A	[15:13]	RESERVED	Reserved.	0x0	R
0x15C	THRESH1_B	[12:8]	THRESH1_SHIFT_x	Shift for threshold compare Level Interrupt 1. Shift THRESH0_VALUE_x by this amount before comparing.	0x0	R/W
0x17C	THRESH1_C	[7:0]	THRESH1_VALUE_x	Value for threshold compare Level Interrupt 1.	0x0	R/W
0x19C	THRESH1_D					
0x1BC	THRESH1_E					
0x1DC	THRESH1_F					
0x1FC	THRESH1_G					
0x21C	THRESH1_H					
0x23C	THRESH1_I					
0x25C	THRESH1_J					
0x27C	THRESH1_K					
0x29C	THRESH1_L					

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CB-36-11	WLCSP	36-Ball Wafer Level Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

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ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPD7008BCBZR7	-40°C to +85°C	36-ball WLCSP (2.795 mm x 2.560 mm x 0.595 mm)	Reel, 1500	CB-36-11

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADPD7000Z	Evaluation Board

[1] Z = RoHS-Compliant Part.