High Survivability, Low Noise Amplifier, 1 GHz to 20 GHz

FEATURES

- High RF input power survivability: 36.5 dBm
- RBIAS drain current adjustment pin
- Gain: 15 dB from 8 GHz to 18 GHz
- Noise figure: 3 dB from 8 GHz to 18 GHz
- Extended operating temperature range: −55°C to +125°C
- RoHS compliant, 2 mm × 2 mm, 8-lead LFCSP

APPLICATIONS

- Telecommunications
- Satellite communications
- Military radar
- Civil radar
- Electronic warfare
- Test and measurement equipment

GENERAL DESCRIPTION

The ADL8109 is a 1 GHz to 20 GHz low noise amplifier (LNA) with 36.5 dBm RF input power survivability. The ADL8109 has a gain of 15 dB, an ouptut power for 1 dB compression (OP1dB) of 16 dBm, a typical output third-order intercept (OIP3) of 28 dBm, and a noise figure of 3 dB from 8 GHz to 18 GHz. This LNA operates on a 5 V supply voltage (V_{DD}) and has a nominal quiescent current (I_{DQ}) of 110 mA. The ADL8109 also features an RF input and output that are internally matched to 50 Ω.

The device is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead lead frame chip scale package [LFCSP] and is specified for operation from −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

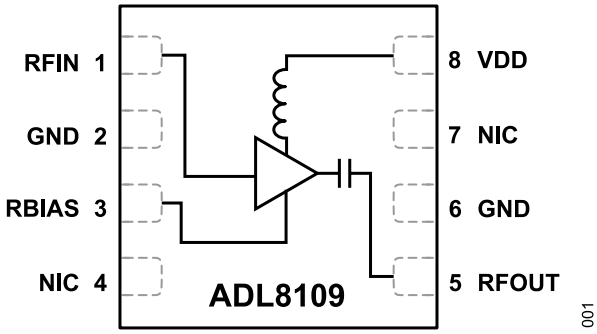

Figure 1. Functional Block Diagram

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REVISION HISTORY

9/2024—Rev. 0 to Rev. A

Replaced Figure 1 ... 1
Replaced Figure 13 and Figure 19 ... 7
Changes to Theory of Operation section and replaced Figure 53 ... 15
Changes to Applications Information section and replaced Figure 54 ... 16
Replaced Figure 55 ... 17

9/2024—Revision 0: Initial Version

SPECIFICATIONS

1 GHZ TO 8 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 110 mA, bias resistance (R_{BIAS}) = 274 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 1 GHz to 8 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		8	GHz	
GAIN	12.5	14.5		dB	
Gain Variation over Temperature		0.011		dB/°C	
NOISE FIGURE		3.5		dB	
RETURN LOSS					
Input (S11)		10		dB	
Output (S22)		21		dB	
OUTPUT					
OP1dB	14.5	16.5		dBm	
Saturated Output Power (P_{SAT})		19		dBm	
OIP3		28.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 0 dBm
Output Second-Order Intercept (OIP2)		35		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
Power-Added Efficiency (PAE)		10.5		%	Measured at P_{SAT}

8 GHZ TO 18 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 110 mA, R_{BIAS} = 274 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 8 GHz to 18 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		18	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.015		dB/°C	
NOISE FIGURE		3		dB	
RETURN LOSS					
S11		13		dB	
S22		20		dB	
OUTPUT					
OP1dB	14	16		dBm	
P_{SAT}		19		dBm	
OIP3		28		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		33.5		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
PAE		10		%	Measured at P_{SAT}

SPECIFICATIONS

18 GHZ TO 20 GHZ FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 110 mA, R_{BIAS} = 274 Ω, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 18 GHz to 20 GHz Frequency Range Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	18		20	GHz	
GAIN	13	15		dB	
Gain Variation over Temperature		0.018		dB/°C	
NOISE FIGURE		4.5		dB	
RETURN LOSS					
S11		13.5		dB	
S22		18		dB	
OUTPUT					
OP1dB	12.5	14.5		dBm	
P_{SAT}		17.5		dBm	
OIP3		26		dBm	Measurement taken at P_{OUT} per tone = 0 dBm
OIP2		47		dBm	Measurement taken at P_{OUT} per tone=0 dBm
PAE		7.5		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4. DC Specifications

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		110		mA
Amplifier Current (I_{DQ_AMP})		100		mA
RBIAS Current (I_{RBIAS})		10		mA
SUPPLY VOLTAGE				
V_{DD}	3	5	6	V

ABSOLUTE MAXIMUM RATINGS

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	7 V
RF Input Power (RFIN)	See Figure 2
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 17.51 mW/°C Above 85°C)	1.6 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 110 mA, Input Power (P_{IN}) = Off)	116.4°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

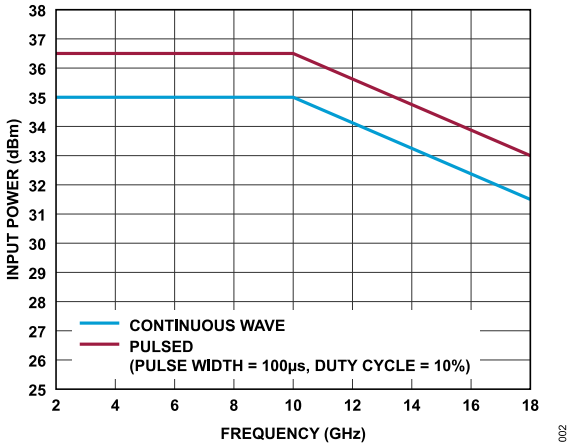

Figure 2. RF Input Power Absolute Maximum Ratings for Pulsed and Continuous Wave vs. Frequency, T_{CASE} = 85°C

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-8-30		
Quiescent, T_{CASE} = 25°C	48.2	°C/W
Worst Case,[1] T_{CASE} = 85°C	57.1	°C/W

[1] Worst case across all specified operating conditions.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8109

Table 7. ADL8109, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±400	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

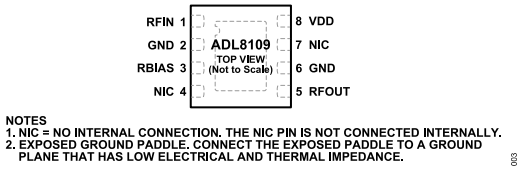

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. The RFIN pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. See Figure 5 for the interface schematic.
2, 6	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 7 for the interface schematic.
3	RBIAS	Bias setting resistor. Connect a resistor between RBIAS and VDD to set I_{DQ}. See Figure 54. and Table 9 for more details. See Figure 4 for the interface schematics.
4, 7	NIC	No Internal Connection. The NIC pin is not connected internally.
5	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 6 for the interface schematics.
8	VDD	Drain Bias. Connect this pin to the supply voltage. See Figure 6 for the interface schematic.
	EXPOSED PADDLE	Exposed Ground Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

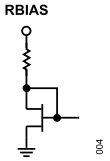

Figure 4. R_{BIAS} Interface Schematic

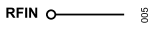

Figure 5. R_{FIN} Interface Schematic

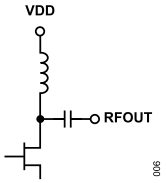

Figure 6. RFOUT/VDD Interface Schematic

Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

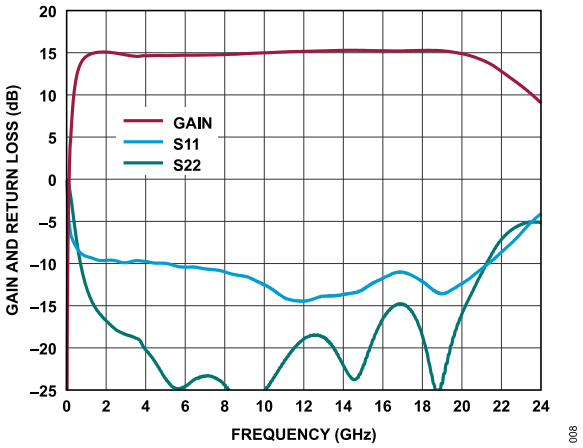

Figure 8. Gain and Return Loss vs. Frequency, 10 MHz to 24 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

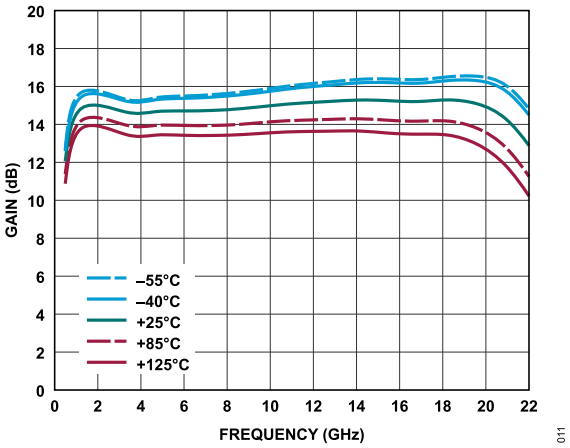

Figure 11. Gain vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

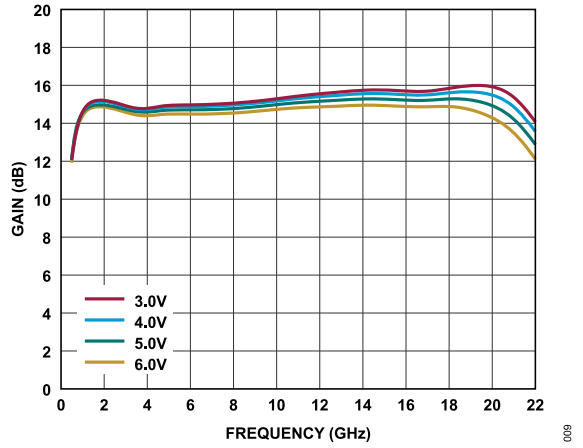

Figure 9. Gain vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

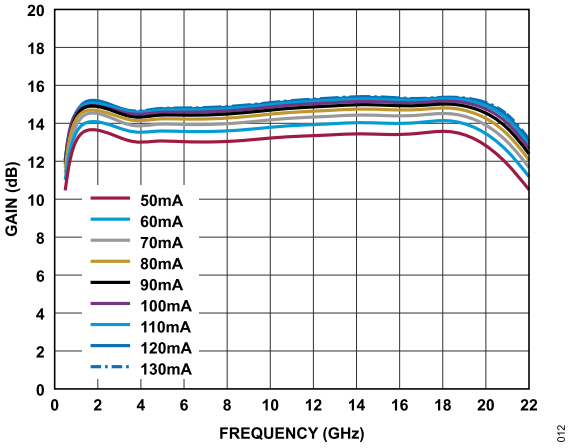

Figure 12. Gain vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

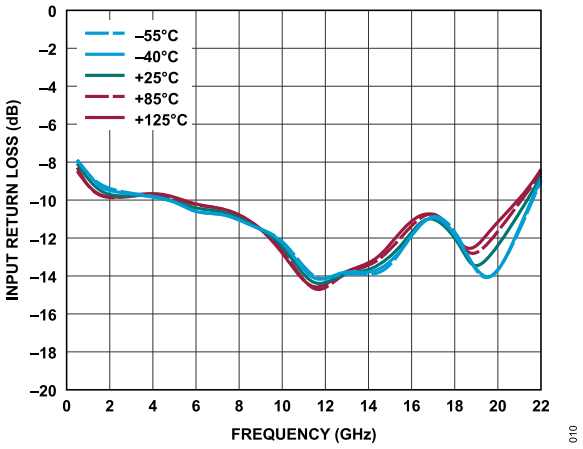

Figure 10. Input Return Loss vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

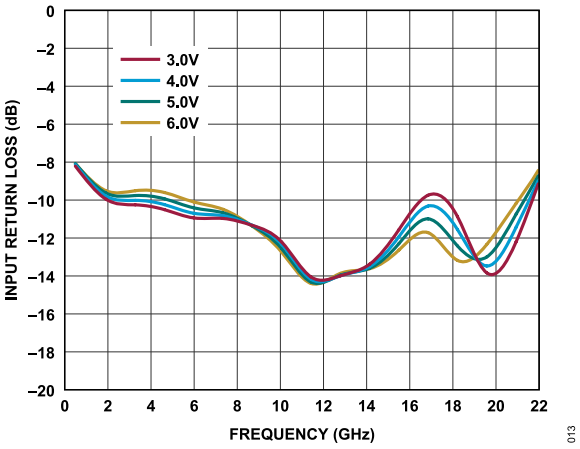

Figure 13. Input Return Loss vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

TYPICAL PERFORMANCE CHARACTERISTICS

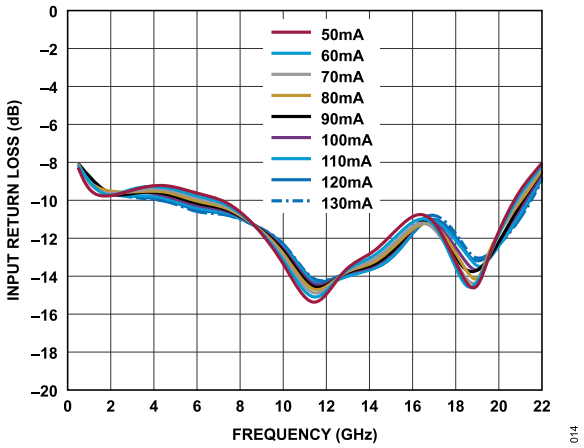

Figure 14. Input Return Loss vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz and V_{DD} = 5 V

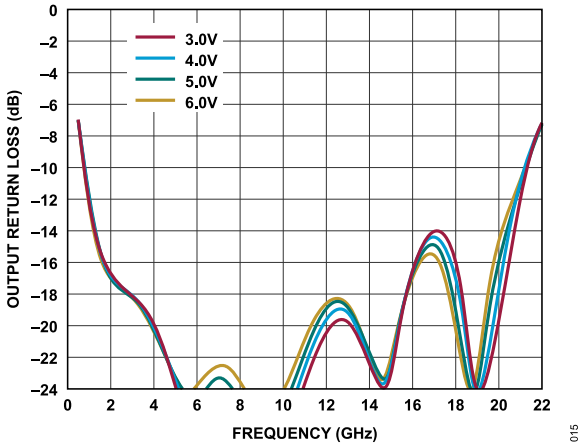

Figure 15. Output Return Loss vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz and I_{DQ} = 110 mA

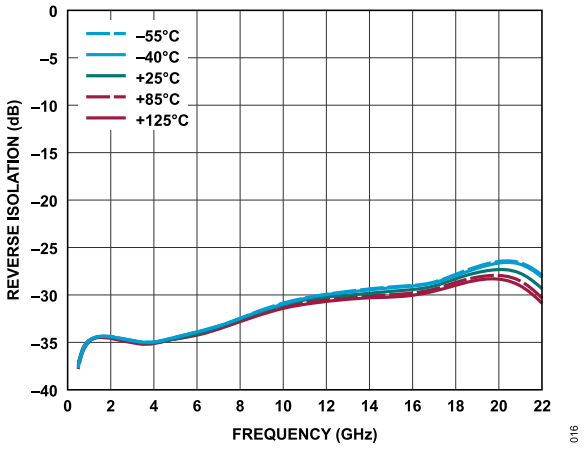

Figure 16. Reverse Isolation vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

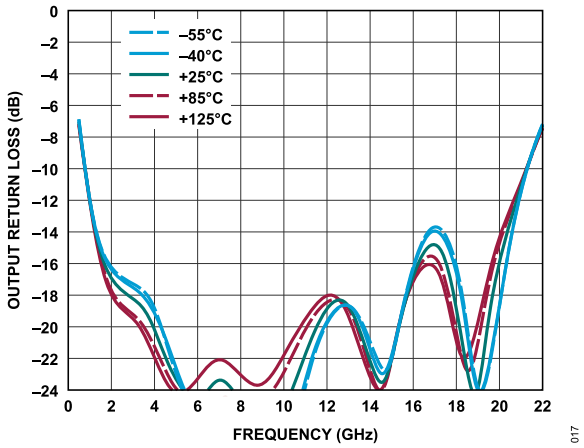

Figure 17. Output Return Loss vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

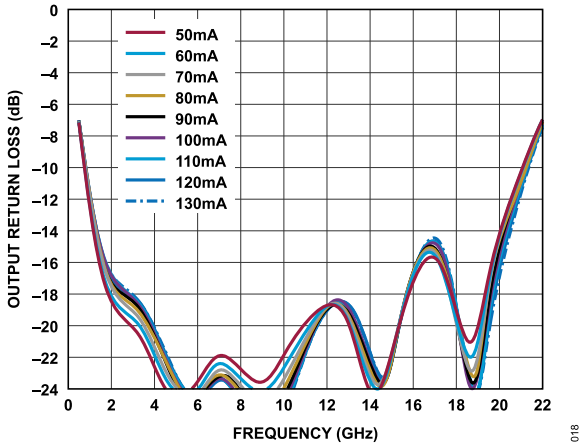

Figure 18. Output Return Loss vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

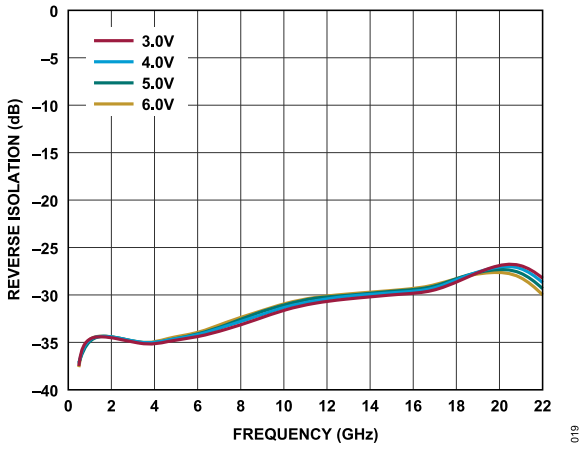

Figure 19. Reverse Isolation vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

TYPICAL PERFORMANCE CHARACTERISTICS

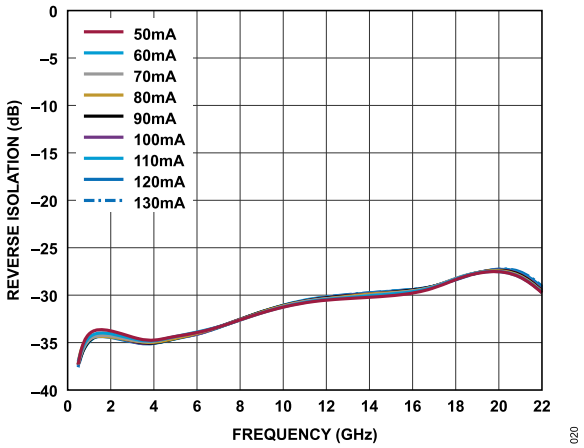

Figure 20. Reverse Isolation vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

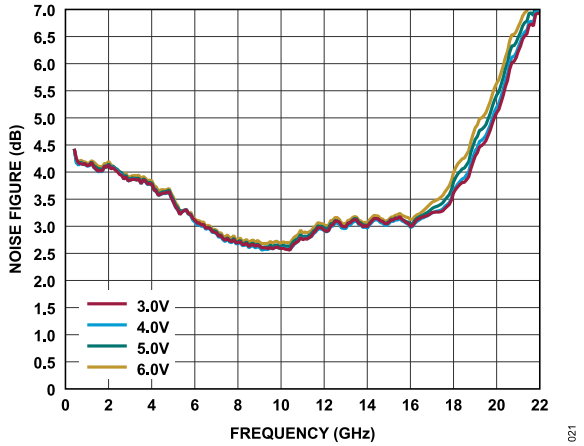

Figure 21. Noise Figure vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

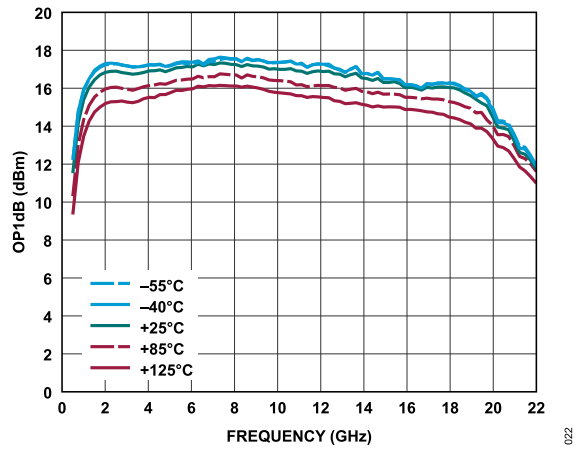

Figure 22. OP1dB vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

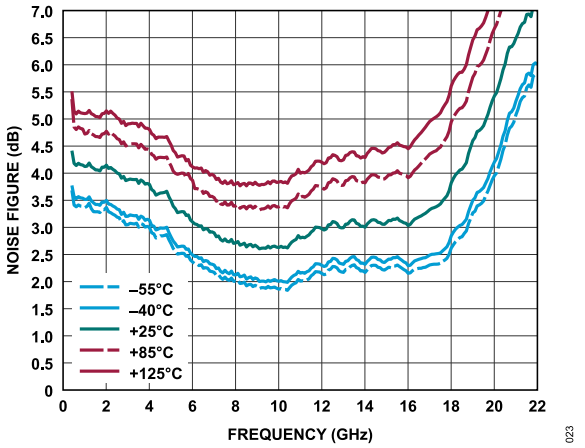

Figure 23. Noise Figure vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

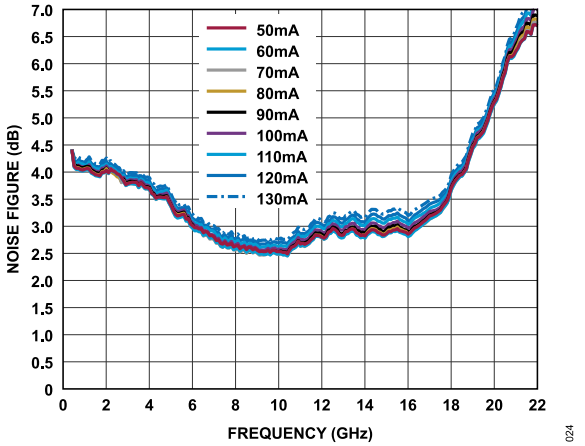

Figure 24. Noise Figure vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

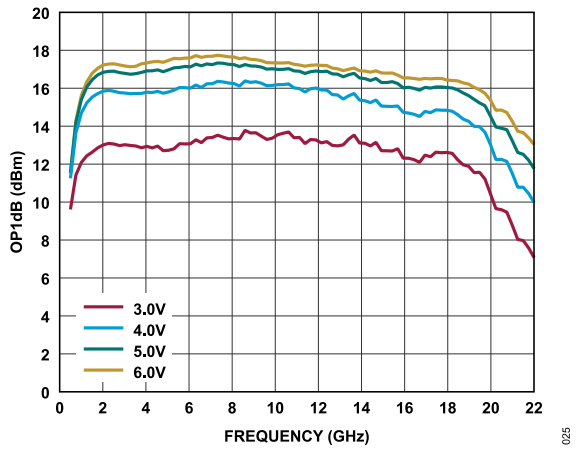

Figure 25. OP1dB vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

TYPICAL PERFORMANCE CHARACTERISTICS

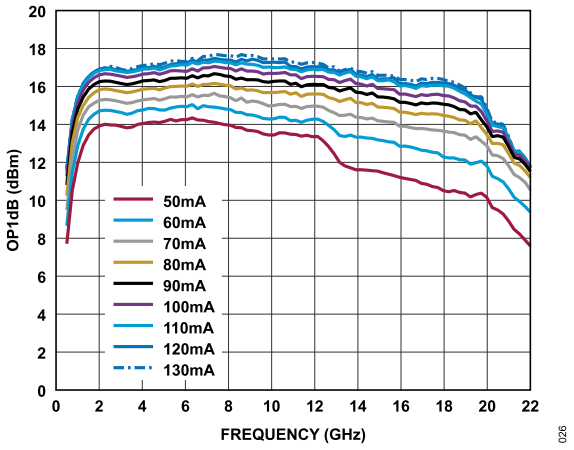

Figure 26. OP1dB vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

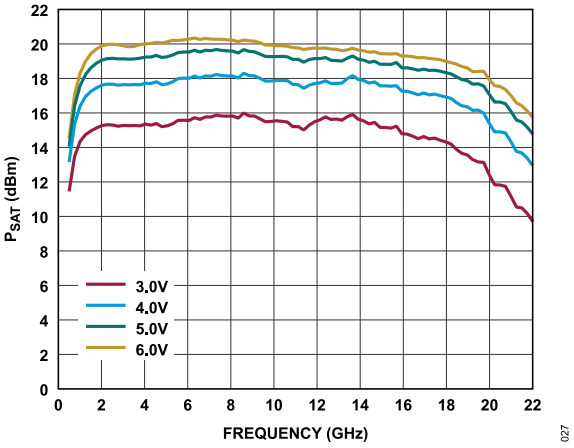

Figure 27. P_{SAT} vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

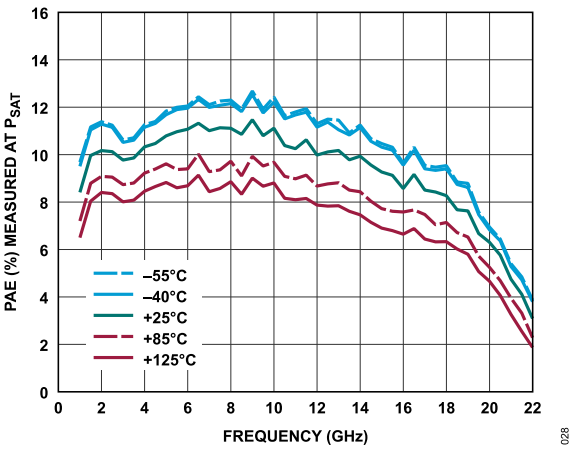

Figure 28. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

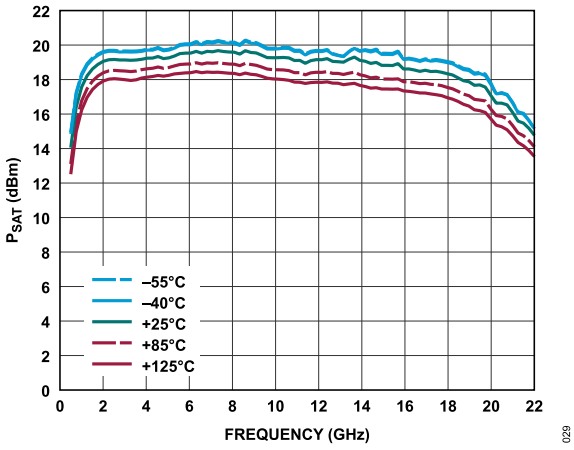

Figure 29. P_{SAT} vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

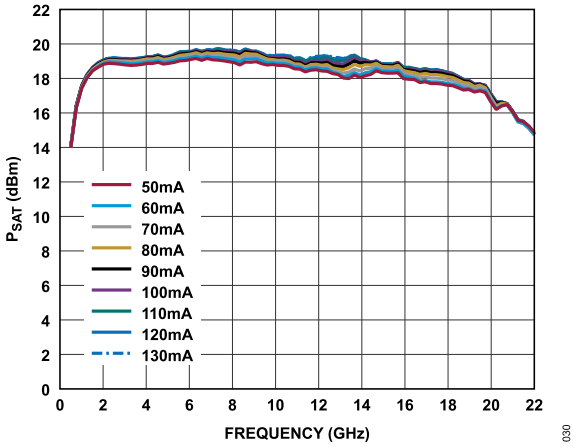

Figure 30. P_{SAT} vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

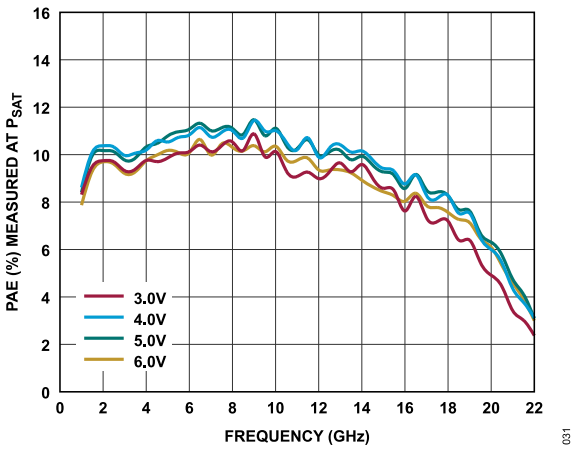

Figure 31. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

TYPICAL PERFORMANCE CHARACTERISTICS

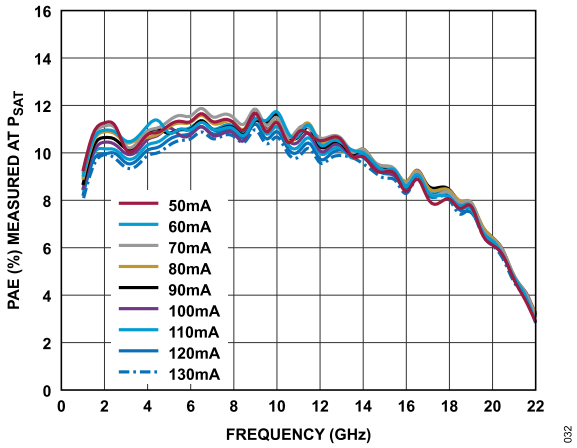

Figure 32. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

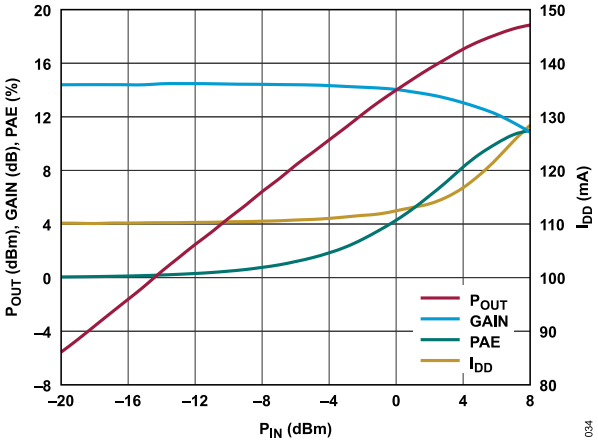

Figure 33. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 5 GHz, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

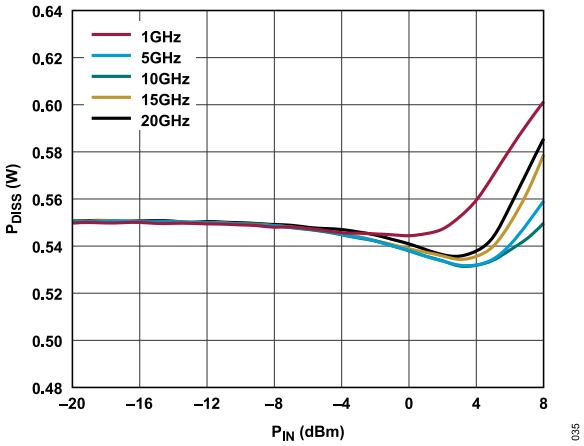

Figure 34. P_{DISS} vs. P_{IN} at Various Frequencies, T_{CASE} = 85°C, and V_{DD} = 5 V

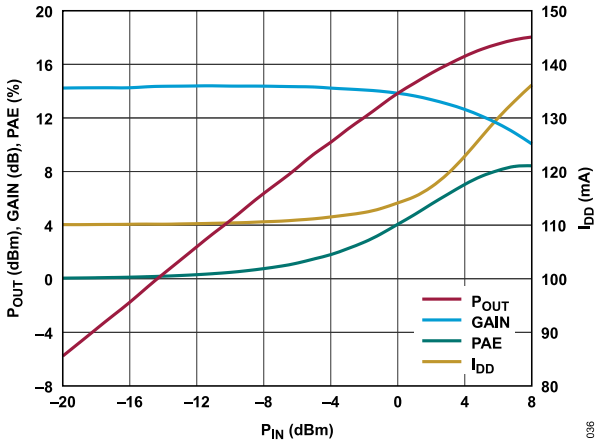

Figure 35. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 1 GHz, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

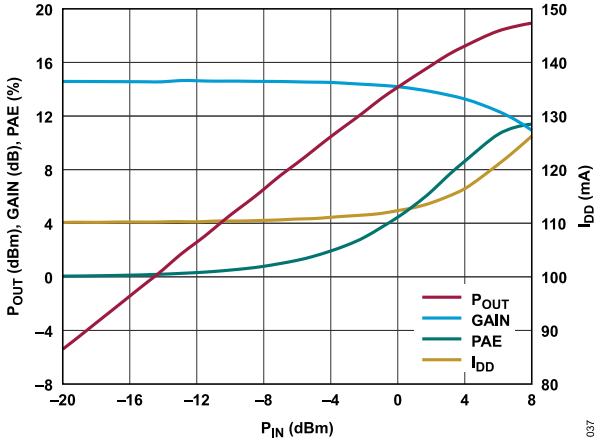

Figure 36. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 10 GHz, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

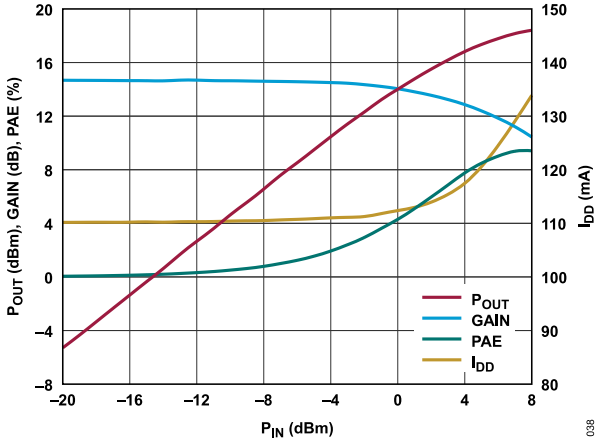

Figure 37. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 15 GHz, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

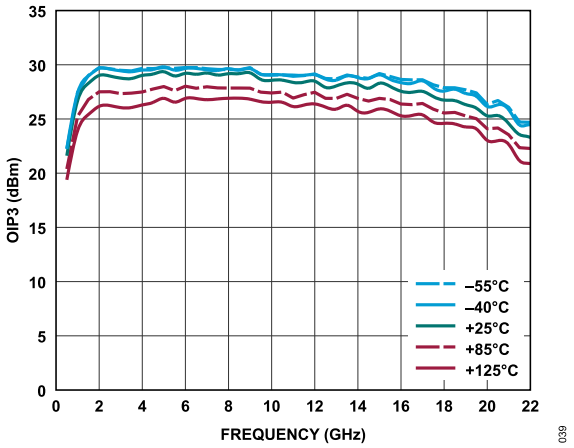

Figure 38. OIP3 vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

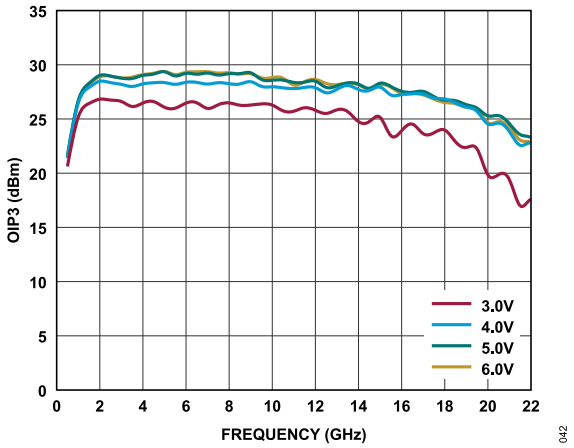

Figure 41. OIP3 vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

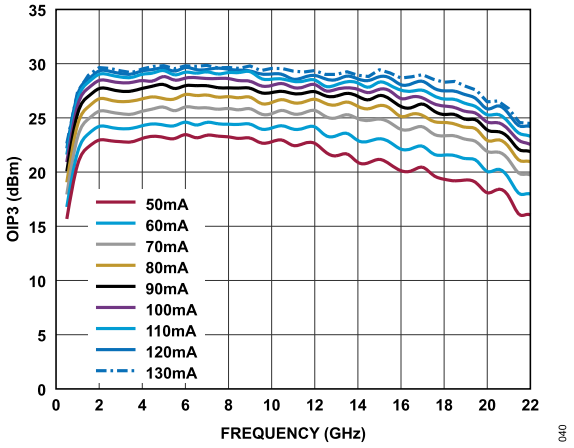

Figure 39. OIP3 vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

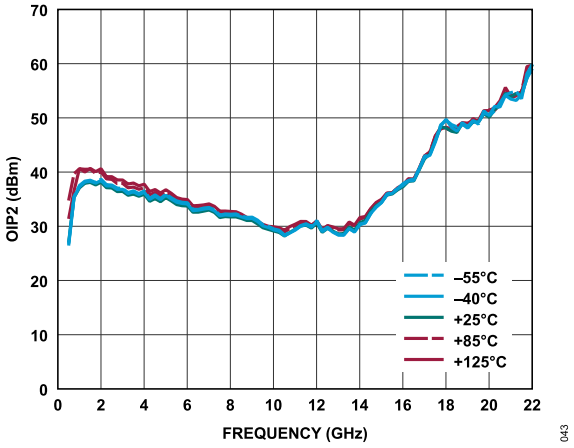

Figure 42. OIP2 vs. Frequency for Various Temperatures, 500 MHz to 22 GHz, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

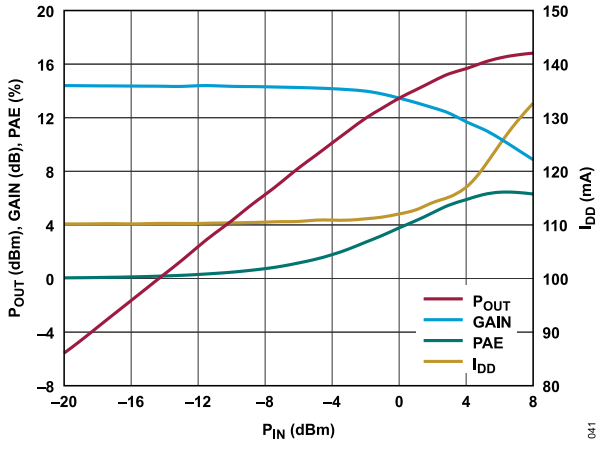

Figure 40. P_{OUT}, GAIN, PAE, and I_{DD} vs. P_{IN}, Power Compression at 20 GHz, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

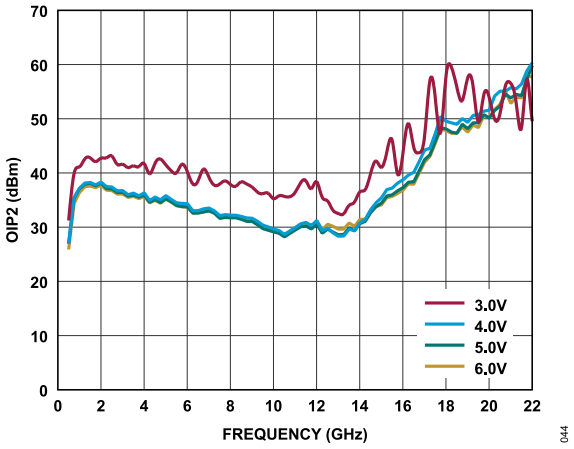

Figure 43. OIP2 vs. Frequency for Various Supply Voltages, 500 MHz to 22 GHz, and I_{DQ} = 110 mA

TYPICAL PERFORMANCE CHARACTERISTICS

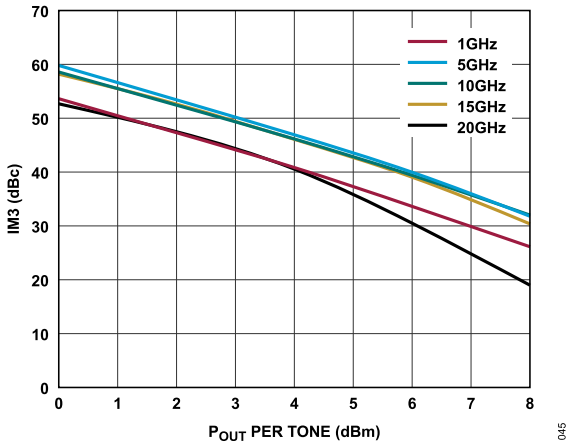

Figure 44. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 110 mA, and R_{BIAS} = 274 Ω

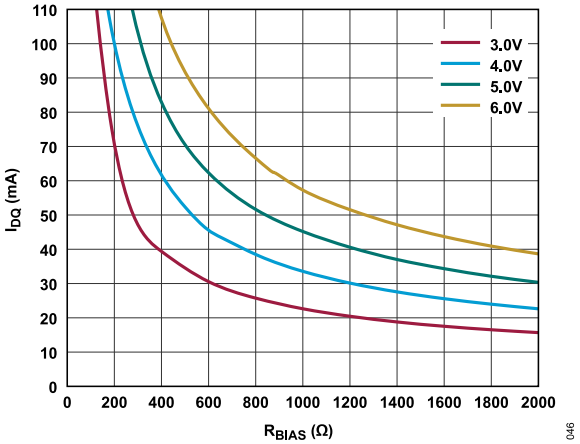

Figure 45. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 0 Ω to 2000 Ω

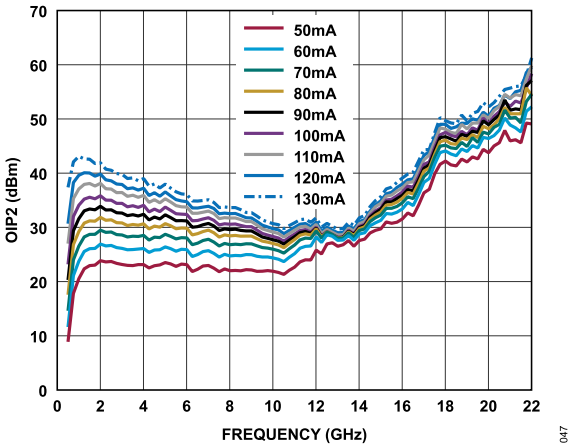

Figure 46. OIP2 vs. Frequency for Various I_{DQ}, 500 MHz to 22 GHz, and V_{DD} = 5 V

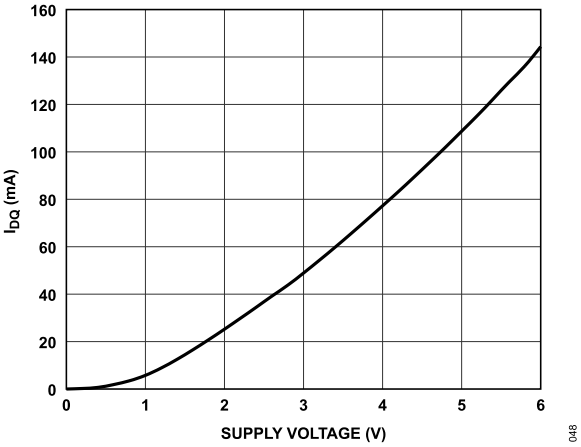

Figure 47. I_{DQ} vs. Supply Voltage, R_{BIAS} = 274 Ω

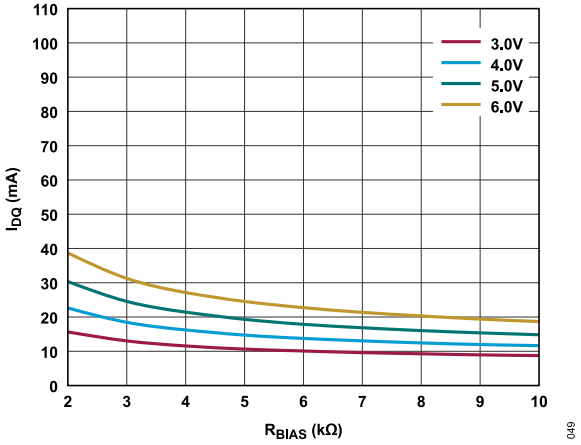

Figure 48. I_{DQ} vs. R_{BIAS} at Various Supply Voltages, 2 kΩ to 10 kΩ

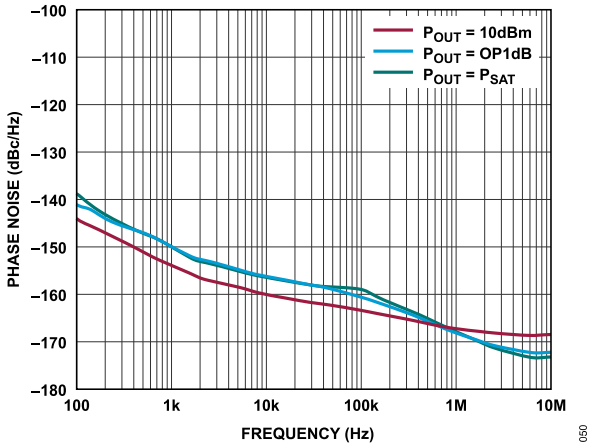

Figure 49. Phase Noise vs. Frequency at 5 GHz for Various P_{OUT} Values

TYPICAL PERFORMANCE CHARACTERISTICS

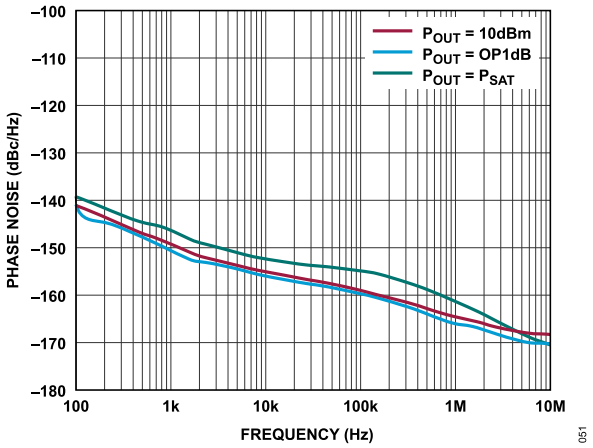

Figure 50. Phase Noise vs. Frequency at 10 GHz for Various P_{OUT} Values

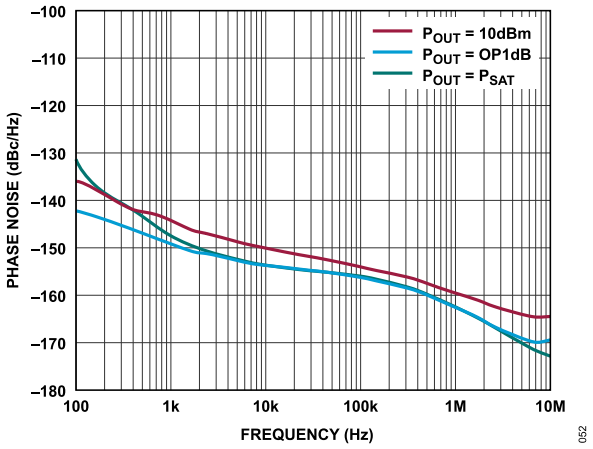

Figure 51. Phase Noise vs. Frequency at 15 GHz for Various P_{OUT} Values

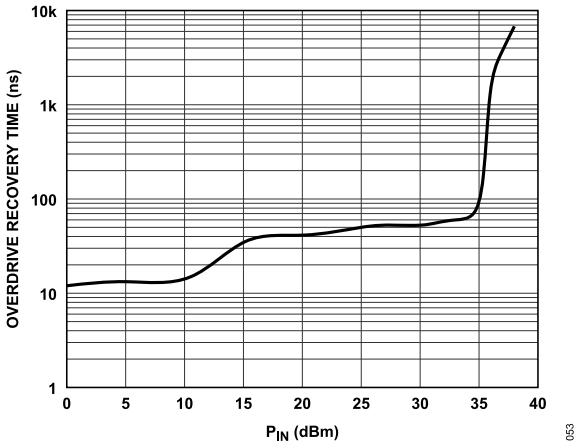

Figure 52. Overdrive Recovery Time vs. P_{IN} at 10 GHz, Recovery Time to within 90% of Small Signal Gain Value, V_{DD} = 5 V, and R_{BIAS} = 274 Ω

THEORY OF OPERATION

The ADL8109 is a wideband LNA with high RF input survivability that operates from 1 GHz to 20 GHz. A simplified block diagram is shown in Figure 53. The RFIN pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0 V DC. The RF output is AC-coupled. No external matching components are required. To adjust the I_{DQ}, connect a supply referenced external resistor to the RBIAS pin.

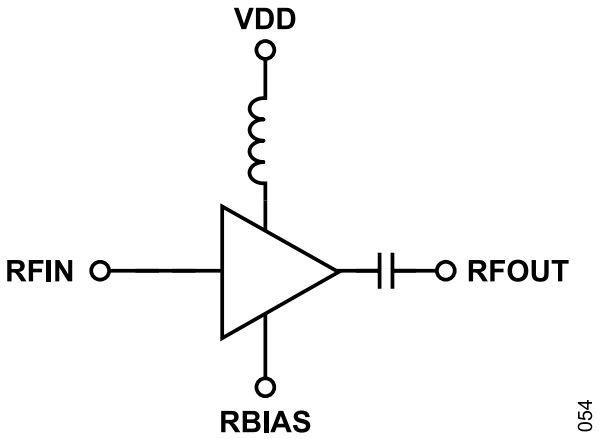

Figure 53. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8109 from 1 GHz to 20 GHz are shown in Figure 53. No external biasing inductor is required, allowing the 5 V supply to be connected to the VDD pin. It is recommended to use two 0.1 µF decoupling capacitors in parallel. The power supply decoupling capacitors shown in Figure 54 represent the configuration used to characterize and qualify the ADL8109.

The RF input is shown as DC-coupled. If the RF input is driven by a signal with a bias level that is not equal to 0 V, an external AC coupling capacitor should be used.

To set I_{DQ}, connect a resistor (R3) between the RBIAS pin and the bias resistance voltage (V_{RBIAS}) supply as shown in Figure 54. A default value of 274 Ω is recommended, which results in a nominal I_{DQ} of 110 mA. Table 9 shows how I_{DQ} and I_{DQ_AMP} vary vs. R_{BIAS}. The RBIAS pin also draws a current that varies with the value of R_{BIAS}. Table 9 shows the recommended R_{BIAS} values and their associated I_{DQ} values. Do not leave the RBIAS pin open.

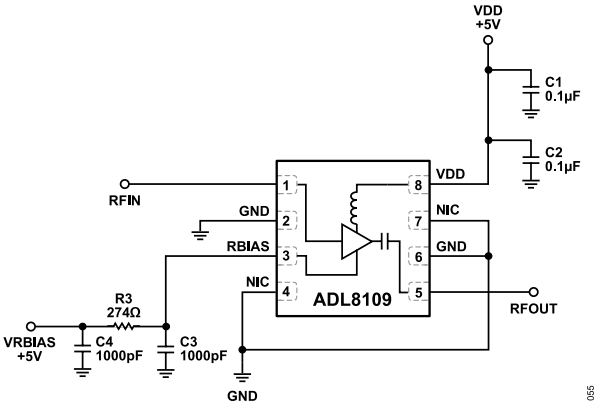

Figure 54. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

Correct sequencing of the DC and RF power is required to safely operate the ADL8109. During power-up, apply V_{DD} and V_{RBIAS} before the RF power is applied to RFIN. During power off, remove the RF power from RFIN before V_{RBIAS} and V_{DD} are powered off.

Table 9. Recommended Bias Resistor Values for Various I_{DQ} Values and V_{DD} = V_{RBIAS} = 5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
845	50	46	4
637	60	54.6	5.4
510	70	63.7	6.3
424	80	72.5	7.5
360	90	81.5	8.5
312	100	90.3	9.7
274	110	99.3	10.7
246	120	108.2	11.8
223	130	116.8	13.2

Table 10. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 110 mA

R_{BIAS} (Ω)	V_{DD} = V_{RBIAS}
69	3
168	4
274	5
391	6

USING RBIAS AS A FAST ENABLE AND DISABLE FUNCTION

By attaching an SPDT switch to the RBIAS pin, an enable and/or disable circuit can be implemented as shown in Figure 55. The ADG719 CMOS switch is used to connect the R_{BIAS} resistor to either the supply or the ground. When the R_{BIAS} resistor is connected to ground, the overall current consumption reduces to 4.73 mA with no RF signal present and 4.92 mA when the RF input level is −10 dBm.

Figure 56 shows a plot of the turn on and/or turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

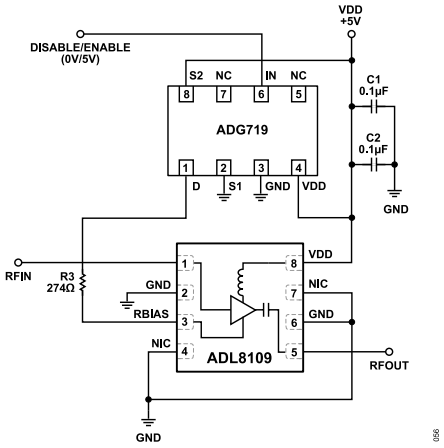

Figure 55. Fast Enable and Disable Circuit Using SPDT

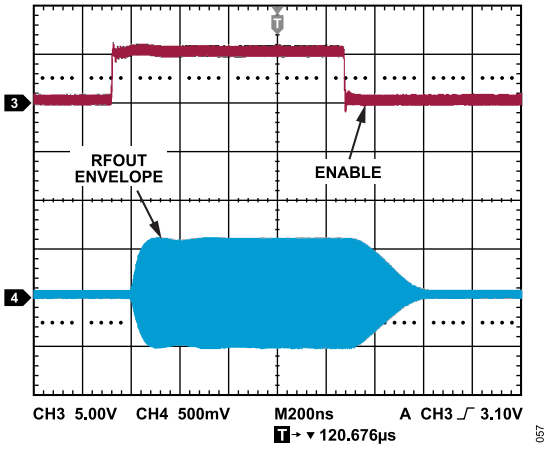

Figure 56. On and/or Off Response of the RF Output Envelope When the IN Pin of the ADG719 is Pulsed

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 57 shows a recommended power management circuit for the ADL8109. The LT8607 step-down regulator is used to step down a 12 V rail to 6.77 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 57 has an input voltage (V_{IN}) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.77 V regulator output of the LT8607 is set by the R2 and R3 resistors according to the following equation:

$$R2 = R3((V_{OUT}/0.778\ V) - 1) \quad (1)$$

where V_{OUT} is the output voltage.

The switching frequency is set to 2 MHz by the 18.2 kΩ resistor on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin according to the following equation:

$$V_{OUT} = 100\ \ \mu A \times R4 \quad (2)$$

The power good feedback (PGFB) resistors are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V.

The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, but adding resistors results in a bit more (5%) tolerance. Therefore, putting 5% between the output and the PGFB resistors works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 11 provides the recommended resistor values for operation from 6 V to 3 V.

Table 11. Recommended Resistor Values for the Various LDO Output Voltages

LDO Regulator V_{OUT} (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
6	60.4	620	30.1
5	49.9	442	30.1
4	40.2	301	30.1
3	30.1	255	30.1

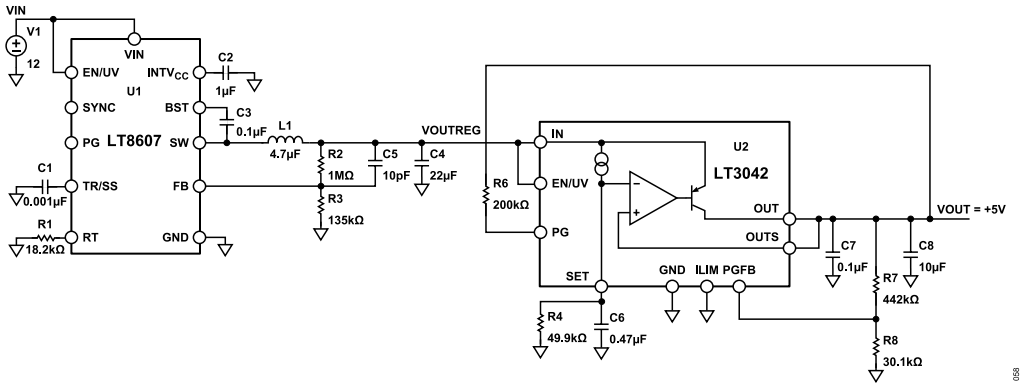

Figure 57. Recommended Power Management Circuit

OUTLINE DIMENSIONS

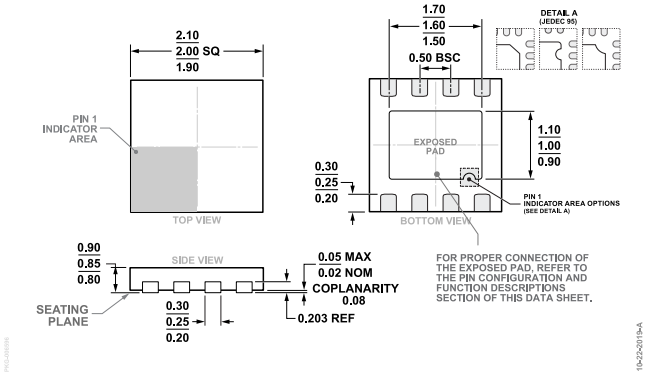

Figure 58. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8109ACPZN	−55°C to +125°C	8-Lead Lead LFCSP, 2 mm x 2 mm x 0.85	Tape, 1	CP-8-30
ADL8109ACPZN-R7	−55°C to +125°C	8-Lead Lead LFCSP, 2 mm x 2 mm x 0.85	Reel, 3000	CP-8-30

[1] Z = RoHS Compliant Part.

[2] The lead finish of ADL8109ACPZN and ADL8109ACPZN-R7 is nickel palladium gold.

EVALUATION BOARDS

Model[1]	Description
ADL8109-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.