Data Sheet

ADF5612

Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- RFOUT output frequency range: 7300MHz to 8500MHz
- PDIV_OUT and NDIV_OUT frequency range: 57MHz to 8500MHz
- Fractional-N synthesizer and Integer N synthesizer modes
- Typical PFD spurious: <−105dBc
- Integrated RMS jitter at 1kHz to 100MHz integration bandwidth: <40fs
- Normalized inband phase noise floor FOM
  - Integer mode: −232dBc/Hz
  - Fractional mode: −229dBc/Hz
- Maintains frequency lock over −40°C to +105°C (lock and leave)
- Low open-loop VCO phase noise
  - −115dBc/Hz typical at 100kHz offset (RFOUT at 7.3GHz)
- RFOUT power (typical): 6dBm
- Programmable divide by 1, 2, 4, 8, 16, 32, 64, or 128 output
- Programmable output power level
- Typical power dissipation: 1W
- 48-terminal, 7 mm × 7 mm LGA package: 49 mm^2

APPLICATIONS

- Military and defense
- Test equipment
- Clock generation
- Wireless infrastructure
- Satellite and very small aperture terminals (VSATs)
- Microwave radios

FUNCTIONAL BLOCK DIAGRAM

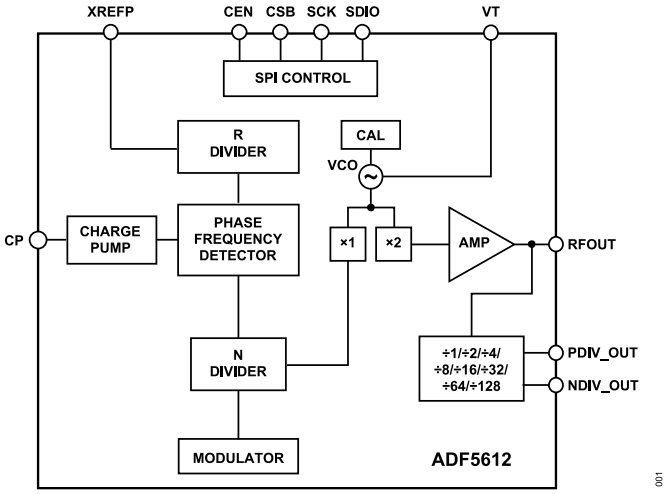

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADF5612 allows implementation of fractional-N or Integer N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference source. The wide-band microwave voltage controlled oscillator (VCO) design permits frequency operation from 7300MHz to 8500MHz at a single RF output. A series of frequency dividers with a differential frequency output allows operation from 57MHz to 8500MHz. Analog and digital power supplies for the PLL circuitry range from 3.15V to 3.45V, and the VCO supplies are between 4.75V and 5.25V.

The ADF5612 has an integrated VCO with a fundamental frequency of 3650MHz to 7300MHz. These frequencies are internally doubled and routed to the RFOUT pin. An additional differential output allows the doubled VCO frequency to be divided by 1, 2, 4, 8, 16, 32, 64, or 128, allowing the user to generate RF output frequencies as low as 57MHz. A simple 3-wire or 4-wire serial port interface (SPI) provides control of all on-chip registers. To conserve power, this divider block can be disabled when not needed through the SPI. Likewise, the output power for both the single-ended output and the differential output are programmable.

The integrated phase detector and Δ-Σ modulator, capable of operating at up to 100MHz, permit wide loop bandwidths and fast frequency tuning with a typical spurious level of −105dBc.

With a VCO open-loop phase noise at 100kHz offset of −115dBc/Hz at 7.3GHz RFOUT. The ADF5612 is equipped to minimize blocker effects and to improve receiver sensitivity and transmitter spectral purity. The low phase noise floor eliminates any contribution to modulator and mixer noise floor in transmitter applications.

Rev. 0

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REVISION HISTORY

2/2025—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 3.3V ± 5%, VDDLS, VPPCP, RVDD, VCCPD, VCCPS, and VCCHF = 3.3V ± 5%, VDD1, VDD2, and VDD3 = 3.3V ± 5%, VCOVCC = 5.0V ± 5%, and GND = 0V for the minimum and maximum specifications across the −40°C to +105°C temperature range, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RF OUTPUT CHARACTERISTICS						
RFOUT Frequency	f_{OUT}	7300		8500	MHz	
VCO Frequency at PLL Input	f_{VCO}	3650		7300	MHz	
PDIV_OUT and NDIV_OUT Frequency Range	f_{OUT_DIV}	57		8500	MHz	
OUTPUT POWER						
RFOUT Power	P_{RFOUT}		6		dBm	7300MHz to 8500MHz, RFOUT_PWR = 3
RFOUT Power Control Range			3		dB	Power range from RFOUT_PWR = 0 to 3
RFOUT Power Variation vs. Temperature			±1		dB	
RFOUT Power Variation vs. Frequency			±2		dB	
PDIV_OUT and NDIV_OUT Power	P_{O_DIV}		3		dBm	Single-ended, DIV_PWR = 3
			6		dBm	Differential, DIV_PWR = 3
PDIV_OUT and NDIV_OUT Control Range			9		dB	Single-ended, power range from DIV_PWR = 0 to 3
			9		dB	Differential, power range from DIV_PWR = 0 to 3
HARMONICS (RFOUT)						
½ Harmonic			−38		dBc	
1.5 Harmonic			−32		dBc	
Second Harmonic			−30		dBc	
2.5 Harmonic			−45		dBc	
Third Harmonic			−32		dBc	
HARMONICS (PDIV_OUT and NDIV_OUT)						
Single-Ended						
½ Harmonic			−35		dBc	Fundamental feed through
Second Harmonic			−32		dBc	Push-push feed through
Third Harmonic			−16		dBc	
Differential						
½ Harmonic			−35		dBc	Fundamental feed through
			−97		dBc	Push-push feed through
Second Harmonic			−38		dBc	
Third Harmonic			−12		dBc	
VCO Supply Pushing (VDD1)[1]			67		MHz/V	RFOUT (VT = 1.65V)
VCO Supply Pushing (VCOVCC)[1]			1.0		MHz/V	RFOUT (VT = 1.65V)
VCO Load Pulling (2.0:1)[2]			1.0		MHz p-p	RFOUT (VT = 1.65V)
VCO Frequency Drift			0.54		MHz/°C	RFOUT (VT = 1.65V), operating at 7.3GHz
REFERENCE INPUT CHARACTERISTICS						
XREFP Input Frequency	f_{REF}	10	50	350	MHz	Refer to the Reference Input section
XREFP Input Level		0.4		3.5	V p-p	Refer to the Reference Input section
XREFP Input Capacitance			6.9		pF	
14-Bit R Divider Range	R_{DIV}	1		16,383		All integers included
Input Current			150		µA	

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE DETECTOR						
Input Frequency	f_{PFD}					
Fractional Mode[3]				100	MHz	
Integer Mode				100	MHz	
CHARGE PUMP						
Output Current	I_{CP}		0.2 to 3.2		mA	Set by the CP_I bit fields, see Table 50
Charge Pump Gain Step Size			200		µA	
LOGIC INPUTS (CSB, SCK, AND SDIO)						
Input High Voltage	V_{INH}	1.2			V	
Input Low Voltage	V_{INL}			0.6	V	
Input Current	I_{IH}/I_{IL}			±1	µA	
Input Capacitance	C_{IN}		2		pF	
LOGIC INPUT (CE)						
Input High Voltage	V_{INH-3V}	1.8			V	
Input Low Voltage	V_{INL-3V}			0.8	V	
Input Current	I_{IH-3V}/I_{IL-3V}			±1	µA	
Input Capacitance	C_{IN-3V}		1		pF	
LOGIC OUTPUT (SDO AND SDIO)						
Output High Voltage (1.8V Mode)	V_{OH}	1.5	1.8		V	Output high current (I_{OH}) = 500µA, 1.8V output selected (default setting)
Output High Voltage (3.3V Mode)	V_{OH-3V}	$V_{3.3V}$ − 0.4			V	I_{OH} = 500µA, 3.3V output selected, set by the voltage on the DVDD pin
Output Low Voltage	V_{OL}			0.4	V	Output low current (I_{OL}) = 500µA
SDO High-Z Leakage	I_{ZH}/I_{ZL}			±1	µA	
POWER SUPPLY VOLTAGES						
3.3 V Supplies		3.15	3.3	3.45	V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD, VPPCP, VDDLS, VDD1, VDD2, and VDD3
5.0 V Supplies		4.75	5.0	5.25	V	VCOVCC
POWER DISSIPATION						
Typical Power Dissipation	P_{DIS}		1		W	f_{REF} = f_{PFD} = 100MHz, R_DIV = 1, I_{CP} = 3.2mA, RFOUT_PWR = 3, DIV_PWR = 3, RFOUT_DIV = divide by 128
POWER SUPPLY CURRENTS						f_{REF} = f_{PFD} = 100MHz, R_DIV = 1, I_{CP} = 3.2mA, RFOUT_PWR = 3, DIV_PWR = 0
AVDD			1		µA	3.3V
RVDD			3		mA	3.3V
VCCHF			<1		µA	3.3V
VCCPS			27		mA	3.3V
VCCPD			4		mA	3.3V
DVDD			3		mA	3.3V
VPPCP and VDDLS			3		mA	3.3V, grouped supply current for VPPCP and VDDLS
VDD1			6		mA	3.3V
VDD2			1		mA	3.3V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
VDD3			58		mA	Divide by 1
			71		mA	Divide by 2
			77		mA	Divide by 4
			81		mA	Divide by 8
			86		mA	Divide by 16
			88		mA	Divide by 32
			90		mA	Divide by 64
			92		mA	Divide by 128
VCOVCC			92		mA	5.0V
Power-Down						
PLL[4]			2.3		µA	Power down via the SPI and the PD_RDIV, PD_NDIV, PD_LD, PD_PFDCP, and PD_PFDNCLK bits, see Table 56 and Table 57
VCOVCC[5]			13		mA	Power down via the SPI and the PD_VCO and PD_ADC bits, see Table 56
Divider[5]			202		µA	Power down via the SPI and the PD_ODIV bit, see Table 57
VCO OPEN-LOOP PHASE NOISE						
RFOUT at 7.3GHz						
10kHz Offset			−92		dBc/Hz	
100kHz Offset			−115		dBc/Hz	
1MHz Offset			−135		dBc/Hz	
10MHz Offset			−155		dBc/Hz	
100MHz Offset			−168		dBc/Hz	
PLL						
Integer Boundary Spurs			−55		dBc	LOCKED bit = 1, f_{REF} = f_{PFD} = 100MHz, R_{DIV} = 1, see Figure 29
Phase Frequency Detector (PFD) Spurs			−105		dBc	LOCKED bit = 1, f_{REF} = 200MHz, f_{PFD} = 100MHz, R_{DIV} = 2, see Figure 30
Reference Spurs			−100		dBc	LOCKED bit = 1, f_{REF} = f_{PFD} = 100MHz, R_{DIV} = 1, see Figure 31
Normalized Inband Phase Noise Floor Figure of Merit (FOM)	L_{NORM}					Normalized to 1Hz
Floor Integer Mode	L_{NORM_INT}		−232		dBc/Hz	
Floor Fractional Mode	L_{NORM_FRAC}		−229		dBc/Hz	
Normalized 1/f Phase Noise Floor (Integer and Fractional Mode)	$L_{1/f}$		−268		dBc/Hz	
Integrated RMS Jitter			<40		fs	Integration bandwidth from 1kHz to 100MHz
VCO CHARACTERISTICS						
Tuning Sensitivity (RFOUT)	K_{VCO}		95 to 125		MHz/V	7300MHz to 8500MHz
Tune Port Capacitance			155		pF	
Auto Calibration Time			100		µs	Refer to the Total Autocalibration Time section
VCO OUTPUT DIVIDER						
VCO RF Divider Range		1		128		1, 2, 4, 6, 8, 16, 32, 64, or 128
VCO Supply Pushing (VCOVCC)[1]			0.7		MHz/V	PDIV_OUT and NDIV_OUT, divide by 1, VT = 1.65V
VCO Supply Pushing (VDD1)[5]			67		MHz/V	PDIV_OUT and NDIV_OUT, divide by 1, VT = 1.65V
Divided Reference Clock (DIV_RCLK) VCO Calibration Frequency				50	MHz	

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR						
ADC Clock Frequency			400		kHz	
RETURN LOSS						
RFOUT			5		dB	
PDIV_OUT (N > 1)			14		dB	
NDIV_OUT (N > 1)			14		dB	

[1] Pushing refers to a change in VCO frequency due to a change in the power supply voltage. To derive pushing at other divide ratios, divide the nominal pushing value by the divide ratio.

[2] Pulling refers to a change in VCO frequency due to a change in the load impedance.

[3] This maximum phase detector frequency can only be achieved if the minimum N value is respected. For example, in the case of fractional mode, the maximum phase detector frequency = $f_{VCO}/20$ or 100MHz, whichever is less.

[4] Reference disconnected.

[5] Some circuits remain on.

SPECIFICATIONS

SPI TIMING CHARACTERISTICS

AVDD = DVDD = 3.3V ± 5%, VCOVCC = 5V ± 5%, all voltages are with respect to GND, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. EPAD = 0V.

Table 2. SPI Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE (CSB, SCK, SDIO, AND SDO)						See Figure 2, Figure 3, and Figure 4
SCK Frequency	f_{SCK}			65	MHz	$f_{SCK} = 1/t_{SCK}$
SCK Pulse Width High	t_{HIGH}	7.6			ns	
SCK Pulse Width Low	t_{LOW}	7.6			ns	
SDIO Setup Time	t_{DS}	3			ns	
SDIO Hold Time	t_{DH}	3			ns	
SCK Fall Edge to SDIO Valid Prop Delay	t_{ACCESS_SDIO}	7.6			ns	
SCK Fall Edge to SDO Valid Prop Delay	t_{ACCESS_SDO}	7.6			ns	
CSB Rising Edge to SDIO High-Z	t_Z	7.6			ns	
CSB Falling Edge to SCLK Rise Setup Time	t_S	3			ns	
SCK Rising Edge to CSB Rise Hold Time	t_H	3			ns	

SPI TIMING DIAGRAMS

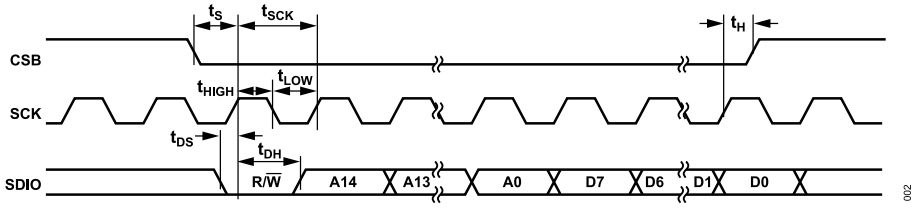

Figure 2. Write Timing Diagram

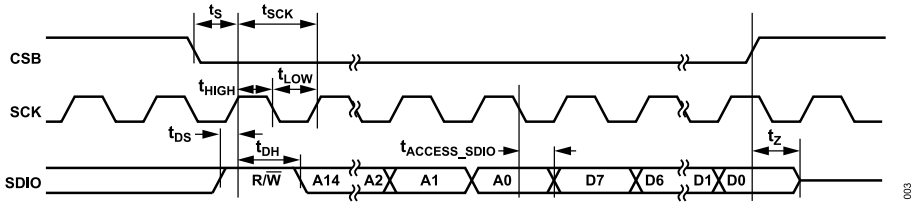

Figure 3. 3-Wire Read Timing Diagram (SDO_ACTIVE = 0)

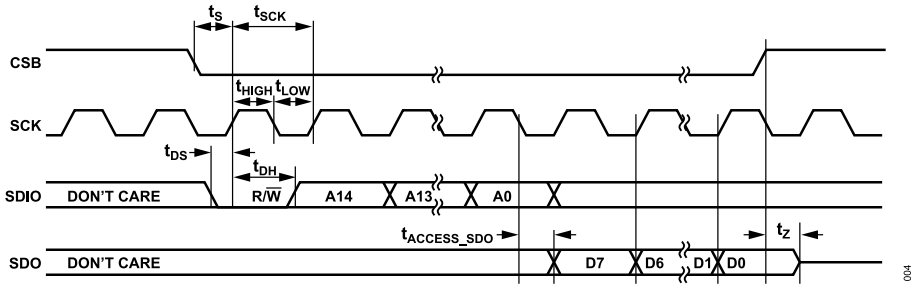

Figure 4. 4-Wire Read Timing Diagram (SDO_ACTIVE = 1)

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
$V_{3.3V}$ (AVDD, RVDD, VCCHF, VCCPS, VCCPD, DVDD, VPPCP, VDDLS, VDD1, VDD2, and VDD3) to GND	−0.3V to +3.6V
VCOVCC	−0.3V to +5.5V
XREFP	−0.3V to AVDD + 0.3V
Voltage on All Other Pins	−0.3V to $V_{3.3V}$ + 0.3V
Digital Outputs (SDO and SDIO)	5mA
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−55°C to +150°C
Maximum Junction	150°C
Reflow Soldering	
Peak	260°C
Time at Peak	30sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. $\theta_{JC\text{-}TOP}$ and $\theta_{JC\text{-}BOTTOM}$ are the junction-to-case thermal resistance top and bottom.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	Unit
CC-48-14	27.17	13.32	6.67	°C/W

[1] Thermal impedance simulated values are based on use of a 4-layer PCB with the thermal impedance paddle soldered to a ground plane.

TRANSISTOR COUNT

The transistor count for the ADF5612 is 2,300 (bipolar) and 140,270 (complementary metal-oxide semiconductor (CMOS)).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF5612

Table 5. ADF5612, 48-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	1500	1C
CDM	1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

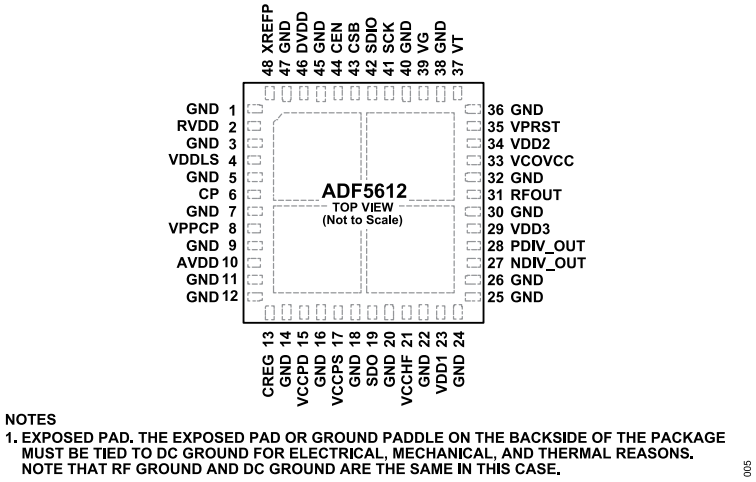

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 24 to 26, 30, 32, 36, 38, 40, 45, 47	GND	Negative Power Supply (Ground). Tie the GND pins directly to the ground pad.
2	RVDD	3.3V ± 5% Positive Power Supply for the Reference Circuitry. Short the RVDD pin to the other pins in the 3.3V power supply group.
4	VDDLS	3.3V ± 5% Typical Power Supply for the Charge Pump Digital Section. VDDLS must be equal to VPPCP.
6	CP	Charge Pump Output. When enabled, this output provides the positive and negative output current magnitude ($\pm I_{CP}$) to the external loop filter. The output of the loop filter is connected to the VT pin to drive the internal VCO. Place the first pole of the low-pass loop filter close to the CP pin if the loop filter path is electrically long.
8	VPPCP	3.3V ± 5% Typical Power Supply for Charge Pump. VPPCP must be equal to VDDLS.
10	AVDD	3.3V ± 5% Analog Supply. AVDD must be equal to DVDD.
13	CREG	Output of the On-Chip Regulator. Connect an external bypass decoupling capacitor of 220nF.
15	VCCPD	3.3V ± 5% Phase Detector Supply.
17	VCCPS	3.3V ± 5% Prescaler Supply.
19	SDO	Serial Data Output. Various other functions are available via an internal mulitplexer. In 3-wire mode (default mode), this three-state CMOS pin remains in a high impedance state. In 4-wire readback mode, the SDO pin presents data from the SPI during a read communication burst. When the CSB is de-asserted, SDO returns to a high impedance. Optionally, attach a resistor of >1kΩ to prevent a floating output. See the MUXOUT section for more details.
21	VCCHF	3.3V ± 5% Power Supply for PLL RF Section. Place a decoupling capacitor as close as possible to this pin.
23	VDD1	3.3V ± 5% Bias for VCO Digital Logic.
27	NDIV_OUT	Complementary Output of Differential Frequency Divider. N = 1, 2, 4, 8, 16, 32, 64, or 128. A DC block is required, and a broadband 100nF capacitor is recommended. Pin disabled upon power-up.
28	PDIV_OUT	Primary Output of Differential Frequency Divider. N = 1, 2, 4, 8, 16, 32, 64, or 128. A DC block is required, and a broadband 100nF capacitor is recommended. Pin disabled upon power-up.
29	VDD3	3.3V ± 5% Differential Output Divider Supply.
31	RFOUT	RF Output (7300MHz to 8500MHz). RFOUT has an internal DC block, and an external DC block with a 100nF capacitor is required.
33	VCOVCC	5.0V ± 5% VCO Power Supply.
34	VDD2	3.3V ± 5% VCO Calibration DAC Supply.
35	VPRST	Temperature Dependent, Calibration Preset. Decouple VPRST with a 470nF capacitor.
37	VT	VCO Tuning Port. Place the last pole of the low-pass filtered charge pump output close to the VT pin if the loop filter path is electrically long.
39	VG	Gate Voltage Bypassing. Decouple VG to GND with a low effective series resistance (ESR), 10 µF capacitor.
41	SCK	Serial Port Clock. This CMOS input clocks the serial port input data on its rising edge.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
42	SDIO	Serial Data Input/Output; CMOS Input and Output. When configured as an input, the SPI uses this CMOS input for data. In 3-wire mode (default mode), the SDIO pin outputs data from the SPI during a read communication burst.
43	CSB	Serial Port Chip Select. This CMOS input initiates a SPI communication burst when driven low, ending the burst when driven back high.
44	CEN	Chip Enable. This CMOS input enables the device when driven high. A logic low disables the device, putting the device in a full power-down state causing the register to reset.
46	DVDD	3.3V ± 5% Digital Power Supply. Retain bias to hold the PLL register contents when powering down the PLL.
48	XREFP	External Reference Input. For 50Ω match, AC couple to the XREFP pin using a low reactant capacitor value and add a 50Ω resistor to ground.
	EPAD	Exposed Pad. The exposed pad or ground paddle on the backside of the package must be tied to DC ground for electrical, mechanical, and thermal reasons. Note that RF ground and DC ground are the same in this case.

TYPICAL PERFORMANCE CHARACTERISTICS

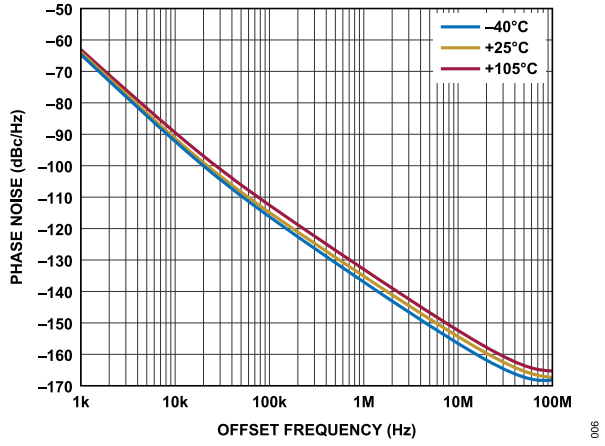

Figure 6. Open-Loop VCO Phase Noise at 8GHz RFOUT vs. Offset Frequency Across Various Temperatures

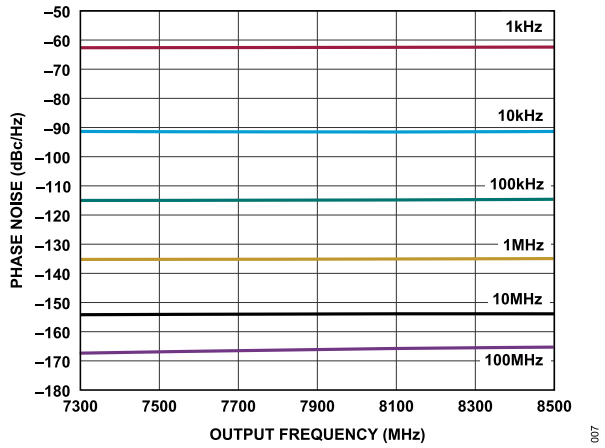

Figure 7. Open-Loop VCO Phase Noise vs. Output Frequency Across Various Offset Frequency

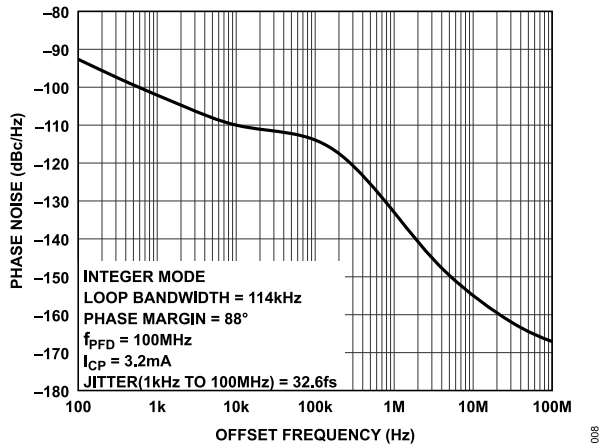

Figure 8. Closed-Loop Phase Noise vs. Offset Frequency at 8GHz RFOUT

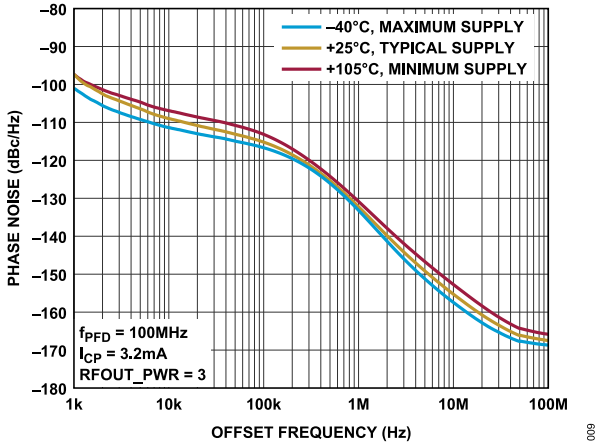

Figure 9. Closed-Loop Phase Noise at 7.3GHz RFOUT vs. Output Frequency Across Various Temperatures and Supplies

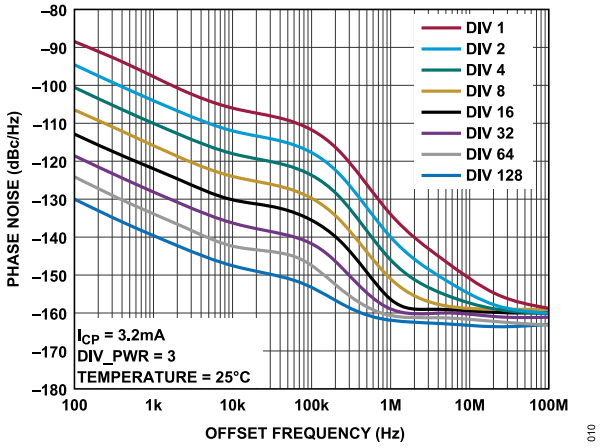

Figure 10. Closed Loop Phase Noise vs. Offset Frequency Across Various Output Divider Settings at 7.3GHz Fundamental Frequency

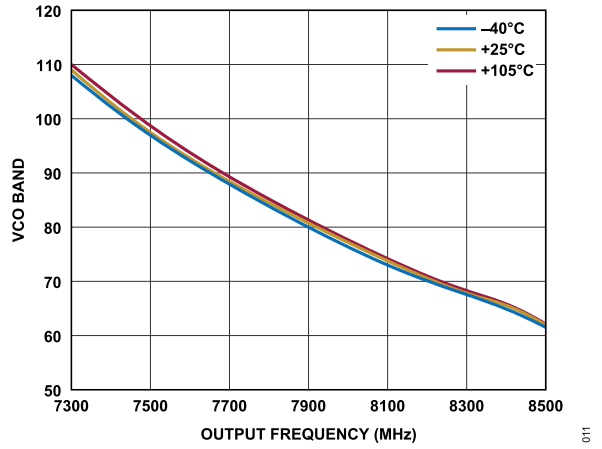

Figure 11. VCO Band vs. Output Frequency Across Various Temperatures, EN_AUTOCAL Enabled

TYPICAL PERFORMANCE CHARACTERISTICS

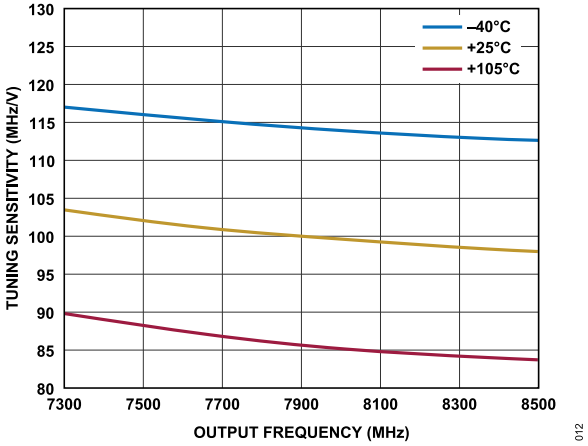

Figure 12. Tuning Sensitivity vs. Output Frequency Across Various Temperatures

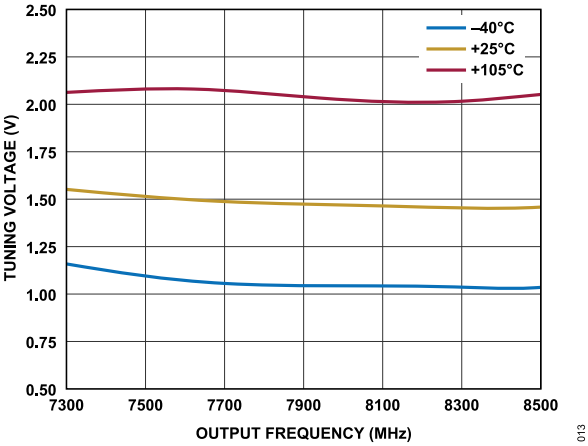

Figure 13. Tuning Voltage vs. Output Frequency after Calibration Across Various Temperatures

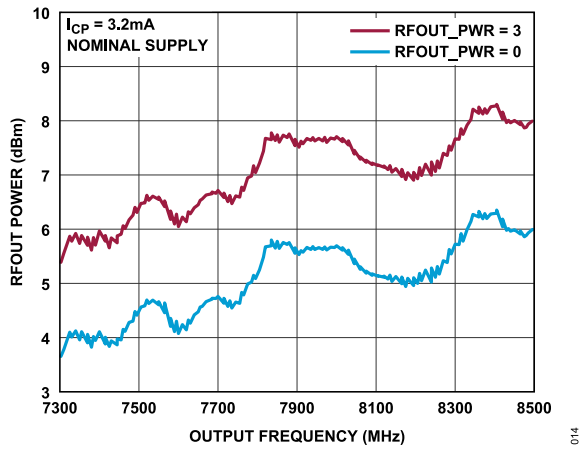

Figure 14. RFOUT Power vs. Output Frequency Across Various Power Settings, 25°C

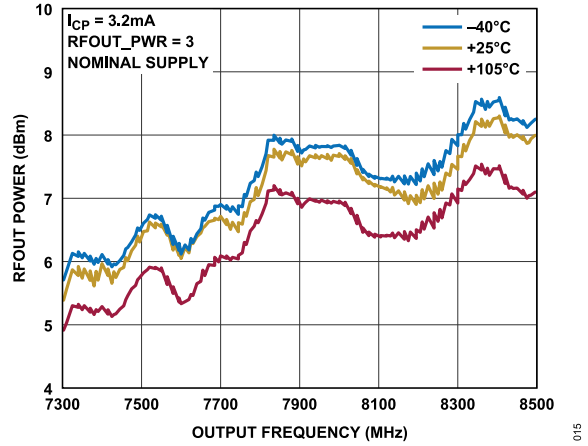

Figure 15. RFOUT Power vs. Output Frequency Across Various Temperatures

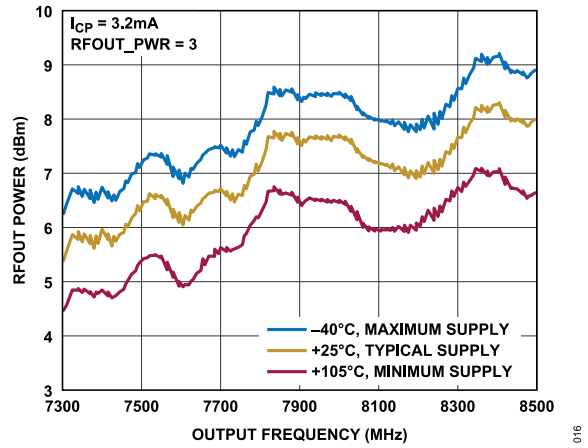

Figure 16. RFOUT Power vs. Output Frequency Across Various Temperatures and Supplies

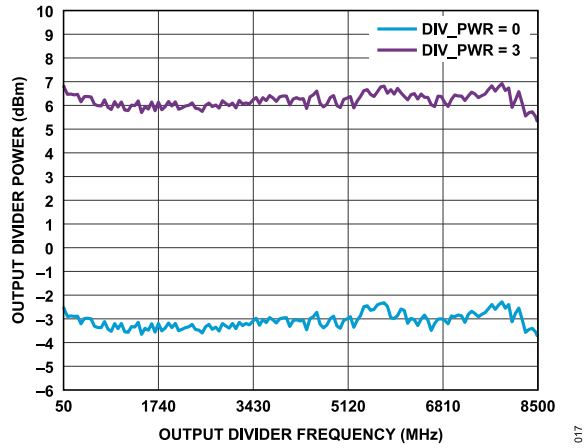

Figure 17. Differential Output Divider Power vs. Output Divider Frequency Across Various Power Settings, 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

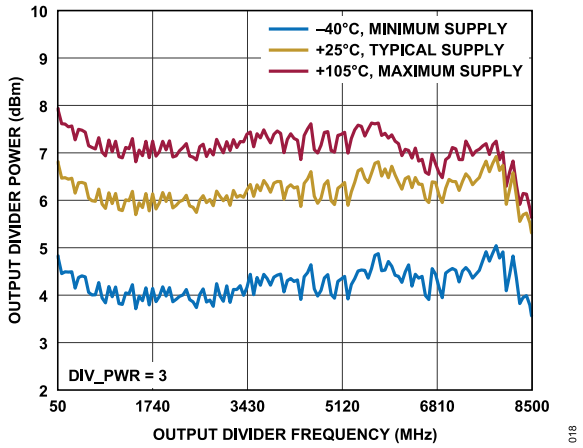

Figure 18. Differential Output Divider Power vs. Output Divider Frequency Across Various Temperatures and Supplies

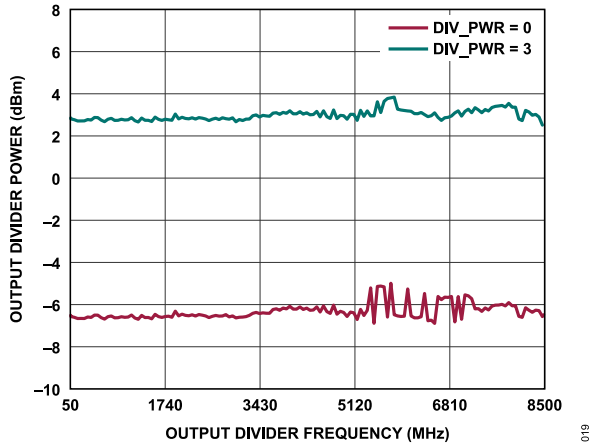

Figure 19. Single-Ended Output Divider Power vs. Output Divider Frequency Across Various Power Settings, 25°C

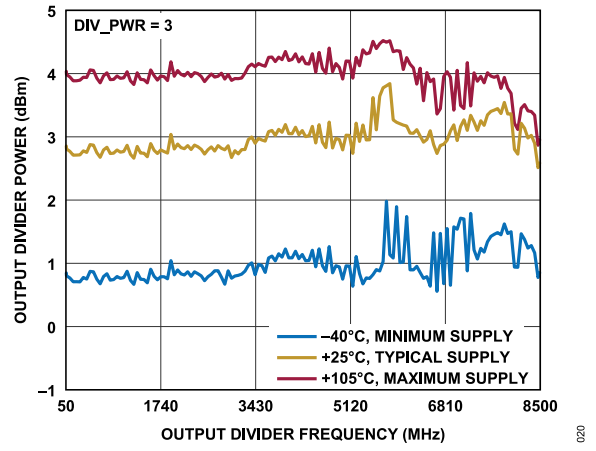

Figure 20. Single-Ended Output Divider Power vs. Output Divider Frequency Across Various Temperatures and Supplies

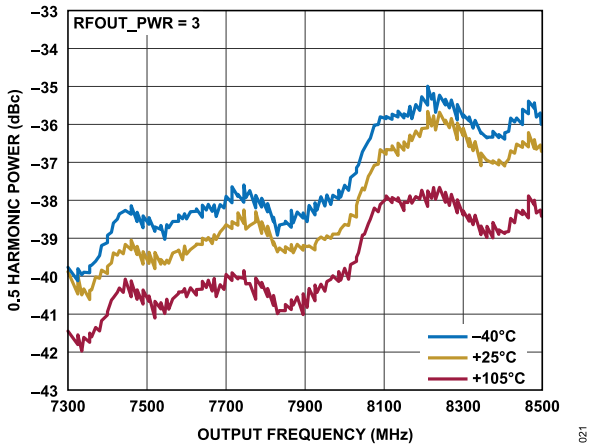

Figure 21. 0.5 Harmonic Power vs. Output Frequency Across Various Temperatures

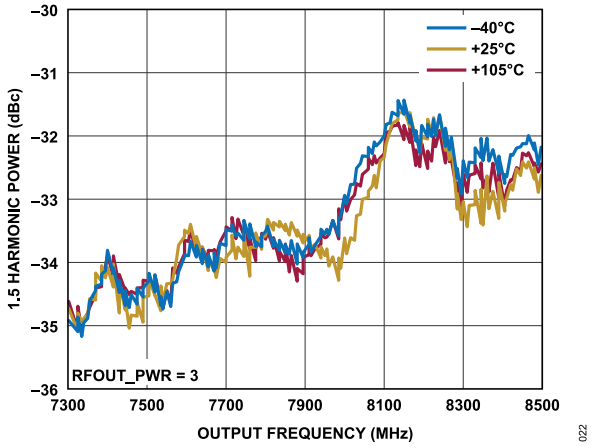

Figure 22. 1.5 Harmonic Power vs. Output Frequency Across Various Temperatures

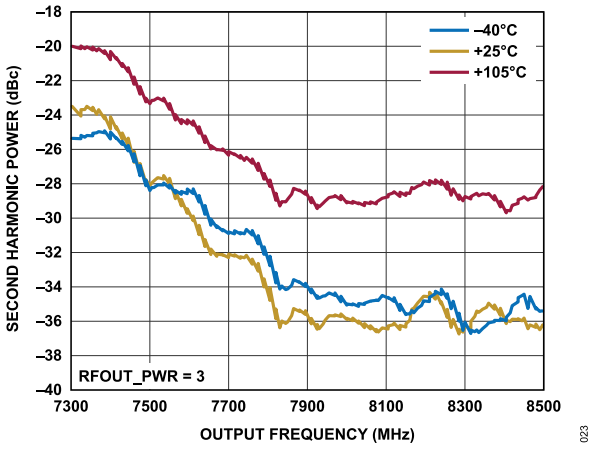

Figure 23. Second Harmonic Power vs. Output Frequency Across Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

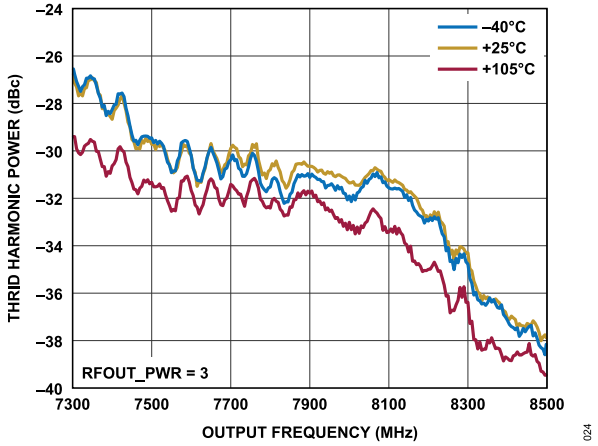

Figure 24. Third Harmonic Power vs. Output Frequency Across Various Temperatures

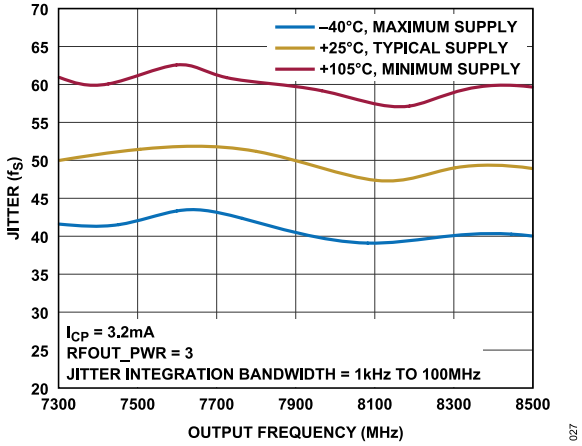

Figure 27. Jitter vs. Output Frequency Across Various Temperatures and Supplies, Fractional Mode

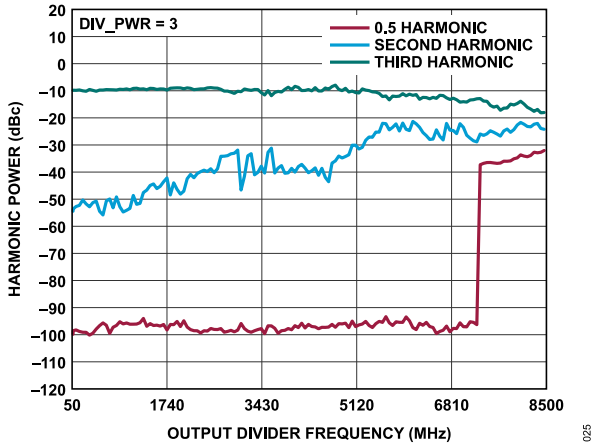

Figure 25. Harmonic Power vs. Output Divider Frequency at 25°C

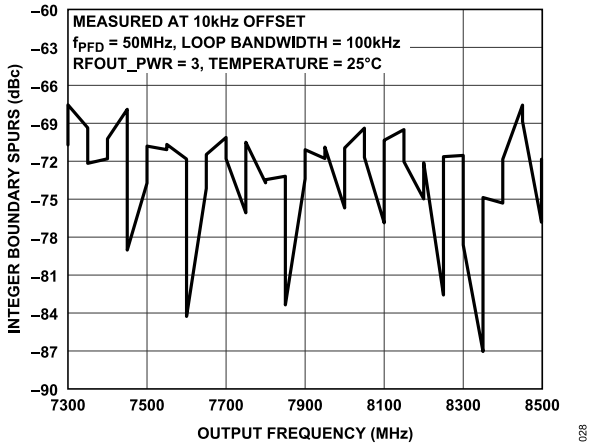

Figure 28. Integer Boundary Spurs vs. Output Frequency at 10kHz Offset

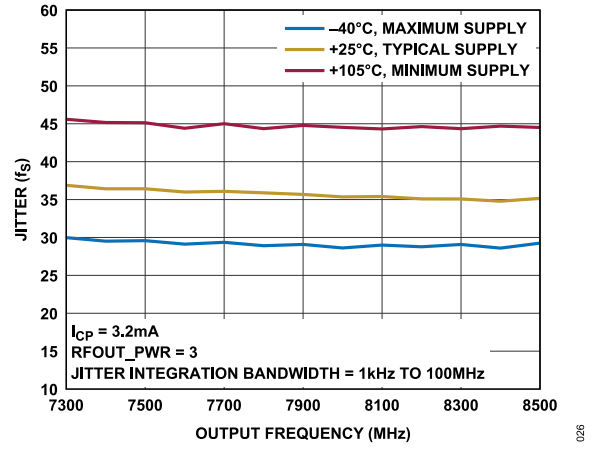

Figure 26. Jitter vs. Output Frequency Across Various Temperatures and Supplies, Integer Mode

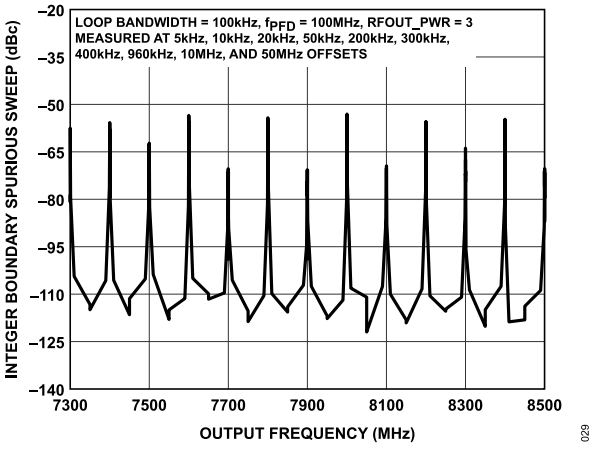

Figure 29. Worst Case Integer Boundary Spurious Sweep vs. Output Frequency at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

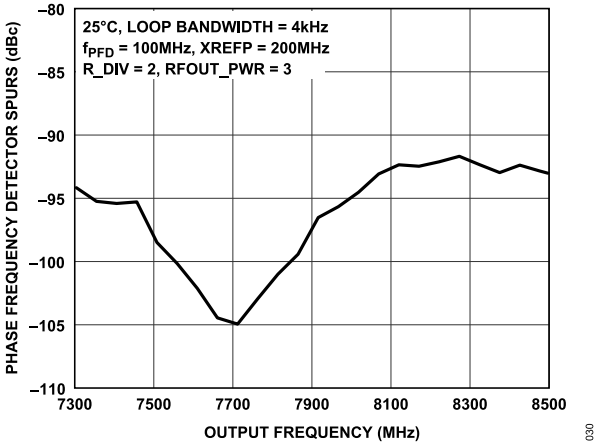

Figure 30. Phase Frequency Detector Spurs vs. Output Frequency

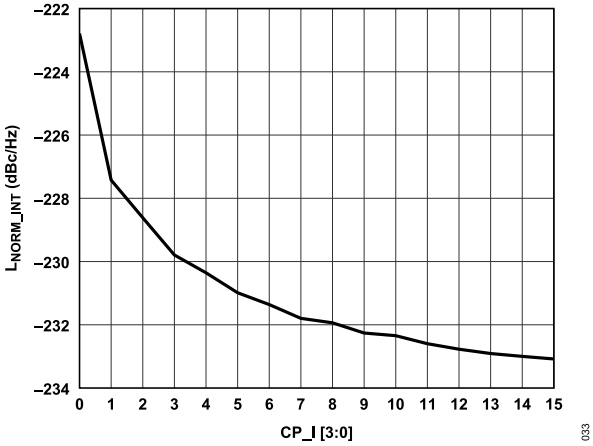

Figure 33. L_{NORM_INT} vs. CP_I[3:0] Settings, 25°C

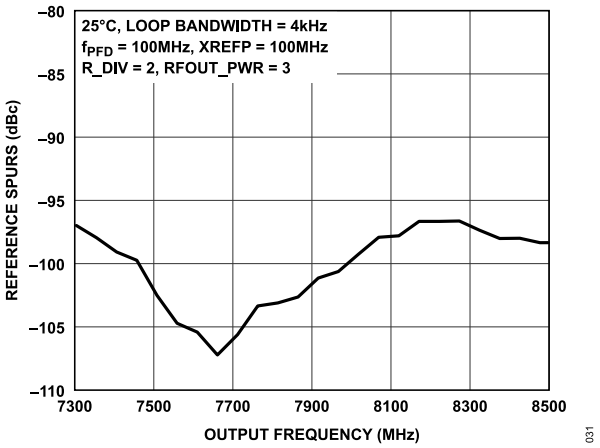

Figure 31. Reference Spurs vs. Output Frequency

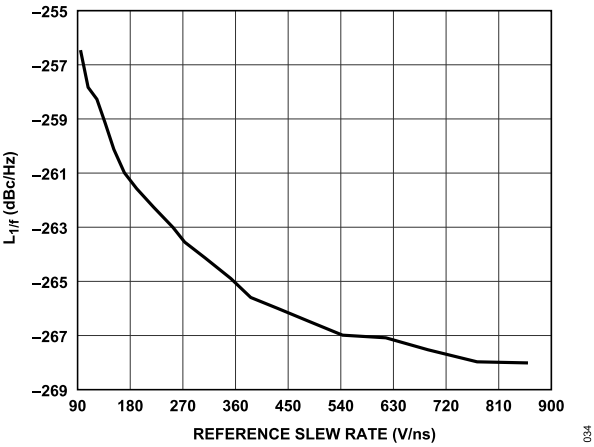

Figure 34. $L_{1/f}$ vs. Reference Slew Rate, 25°C

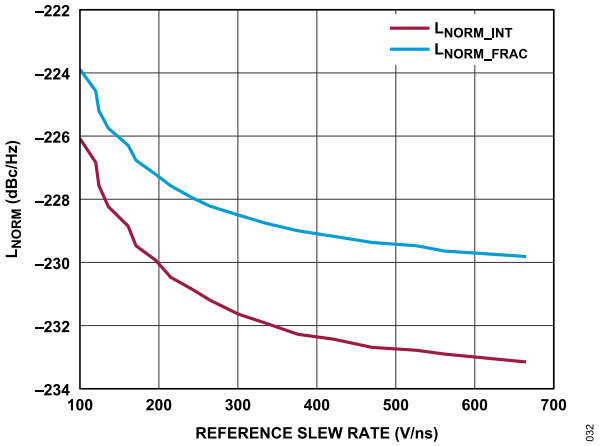

Figure 32. L_{NORM} vs. Reference Slew Rate at 25°C

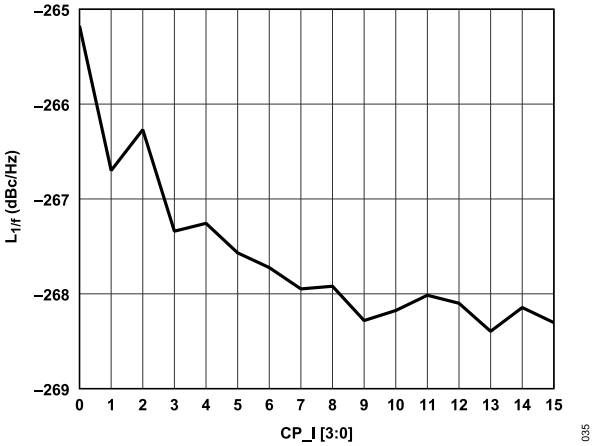

Figure 35. $L_{1/f}$ vs. CP_I[3:0] Settings, 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

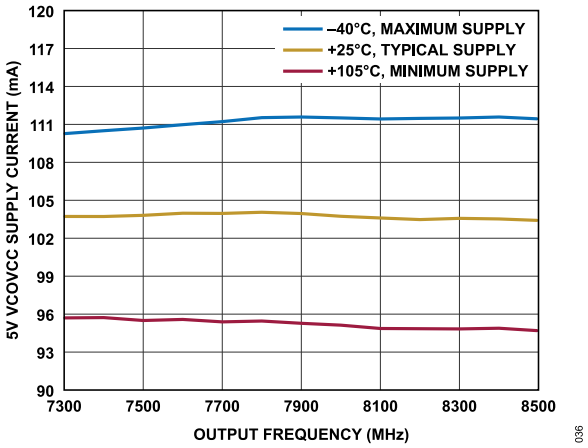

Figure 36. 5V VCOVCC Supply Current vs. Output Frequency Across Various Temperatures and Supplies

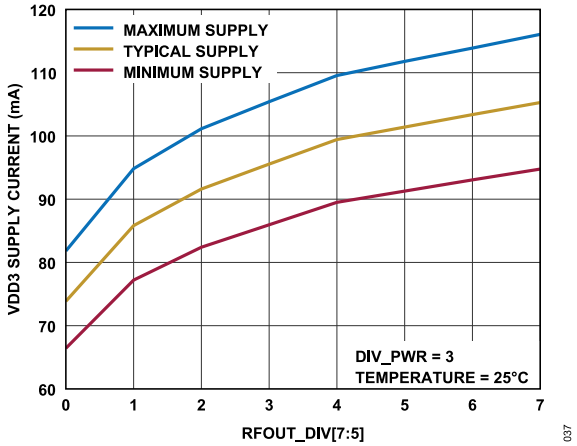

Figure 37. 3V VDD3 Supply Current vs. Output Divider Settings (RFOUT_DIV[7:5]) Across Various Supplies

THEORY OF OPERATION

INTRODUCTION

A PLL is a complex feedback system that can conceptually be considered a frequency multiplier. The system multiplies the reference frequency input at XREFP and outputs a higher frequency at RFOUT (single-ended output) or at PDIV_OUT or NDIV_OUT (differential output). The PFD, charge pump, output divider, feedback divider, VCO, and external loop filter form a feedback loop to accurately control the output frequency (see Figure 38). When operating in integer mode, the reference divider sets the frequency resolution. When operating in fractional mode, the fractional-N divider sets the frequency resolution.

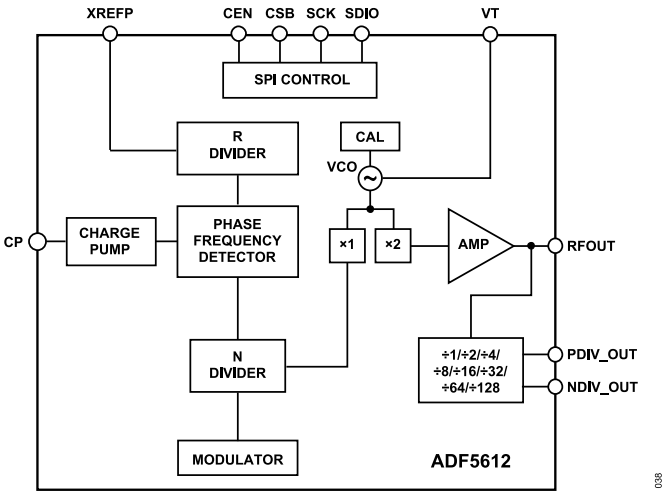

Figure 38. PLL Loop Diagram

OUTPUT FREQUENCY

When the loop is locked, the f_{VCO} (in Hz) produced at the output of the VCO is determined by the reference frequency (f_{REF}), reference division factor (R_DIV), and the N values given by the following equation:

$$f_{VCO} = f_{PFD} \times N \quad (1)$$

where the Feedback Counter N is given by the following:

$$N = N_{INT} + \left(\frac{FRAC1WORD + \frac{FRAC2WORD}{MOD2WORD}}{MOD1WORD} \right) \quad (2)$$

where:

INT is a 20-bit integer value.

FRAC1WORD is the numerator of the primary modulus (0 to 33554431).

FRAC2WORD is the numerator of the 24-bit auxiliary modulus (0 to 16777215).

MOD2WORD is the programmable, 24-bit auxiliary fractional modulus (2 to 16777215).

MOD1WORD is a 25-bit primary modulus with a fixed value of 2^{25} = 33554432

The f_{PFD} is expressed by the following:

$$f_{PFD} = \frac{f_{REF}}{R_{DIV}} \quad (3)$$

The output frequency, f_{RFOUT}, produced at the output channel RFOUT is given by the following:

$$f_{RFOUT} = 2 \times f_{VCO} \quad (4)$$

While the differential output frequency, f_{DIVOUT}, produced at PDIV_OUT and NDIV_OUT

is expressed by the following:

$$f_{DIVOUT} = \frac{2 \times f_{VCO}}{2^{RFOUT\_DIV}} \quad (5)$$

RFOUT_DIV refers to the clock output divider, which can divide the RFOUT from 1 to 128, following a power of 2 progression, see the RF Output Divider section.

Output Frequency Calculation Procedure

The following is a worked example for a fractional mode f_{RFOUT} using the formulas in the Output Frequency section.

For f_{RFOUT} = 7.954GHz and a channel spacing (f_{CHSP}) of 1Hz, where f_{REF} = f_{PFD} = 100MHz and the reference divider is set to divide by 1 (R_DIV = 1), the output frequency is within the fundamental VCO frequency range (f_{VCO}).

The steps to calculate all N-divider component values are outlined as follows:

1. Calculate the overall N value required based on the f_{RFOUT} and f_{PFD} provided as follows:

$$N = \frac{f_{RFOUT}}{2 \times f_{PFD}} \quad (6)$$

$$N = \frac{7.954GHz}{2 \times 100MHz} = 39.77 \quad (7)$$

2. Separate the N_{INT} and N_{FRAC} components as follows:

$$N_{INT} = INT(N) = 39 \quad (8)$$

$$N_{FRAC} = N - N_{INT} = 0.77 \quad (9)$$

3. Calculate the FRAC1WORD as follows:

$$N_{FRAC1WORD} = N_{FRAC} \times MOD1WORD \quad (10)$$

Where MOD1WORD is a fixed value of 2^{25} = 33554432.

$$N_{FRAC1WORD} = 0.77 \times 33554432 = 25836912.64 \quad (11)$$

$$FRAC1WORD = INT(N_{FRAC1WORD}) = 25836912 \quad (12)$$

THEORY OF OPERATION

FRAC2WORD and MOD2WORD are only required if $N_{FRAC1WORD}$ is not an integer number. If $N_{FRAC1WORD}$ is an integer, no further calculation is required. In this case, VAR_MOD_EN is set to 0 to disable FRAC2WORD and MOD2WORD.

4. Calculate the MOD2WORD as follows:

   a. Determine the remainder of the fractional word.

$$N_{REMAINDER} = N_{FRAC1WORD} - FRAC1WORD \quad (13)$$

$$N_{REMAINDER} = 25836912.64 - 25836912 = 0.64 \quad (14)$$

   b. Find the greatest common divisor (GCD) between f_{FPD} and MOD1WORD × f_{CHSP}.

$$GCD(MOD1WORD \times f_{CHSP}, f_{PFD}) \quad (15)$$

$$GCD(2^{25} \times 1, 100MHz) = 256 \quad (16)$$

   c. Calculate the initial MOD2WORD calculation as follows:

$$MOD2WORD_{INITIAL} = \frac{f_{PFD}}{GCD(MOD1WORD \times f_{CHSP}, f_{PFD})} \quad (17)$$

$$MOD2WORD_{INITIAL} = \frac{100MHz}{256} = 390625 \quad (18)$$

   d. Calculate the final MOD2WORD.

   To maximize frequency resolution, the final value of MOD2WORD is calculated by obtaining the highest integer multiple of the initial MOD2WORD, that is less than or equal to the $MOD2WORD_{MAX}$ as follows.

$$MOD2WORD = INT\left(\frac{MOD2WORD_{MAX}}{MO2WORD_{INITIAL}}\right) \times MOD2WORD_{INITIAL} \quad (19)$$

   Where $MOD2WORD_{MAX}$ is a fixed value of $2^{24} - 1$ = 16777215

$$MOD2WORD = INT\left(\frac{16777215}{390625}\right) \times 390625 \quad (20)$$

$$MOD2WORD = 42 \times 390625 = 16406250 \quad (21)$$

5. Calculate FRAC2WORD as follows:

$$FRAC2WORD = INT(N_{REMAINDER} \times MOD2WORD) \quad (22)$$

$$FRAC2WORD = INT(0.64 \times 16406250) \quad (23)$$

$$FRAC2WORD = 10500000 \quad (24)$$

6. Calculate the total N value using the original formula as follows:

$$N = N_{INT} + \frac{FRAC1WORD + \frac{FRAC2WORD}{MOD2WORD}}{MOD1WORD} \quad (25)$$

$$N = 39 + \frac{25836912 + \frac{10500000}{16406250}}{33554432} = 39.77 \quad (26)$$

7. Calculate the f_{RFOUT} frequency as follows:

$$f_{VCO} = f_{PFD} \times N \quad (27)$$

$$f_{RFOUT} = 2 \times f_{VCO} \quad (28)$$

$$f_{RFOUT} = 2 \times (f_{PFD} \times N) \quad (29)$$

$$f_{RFOUT} = 2 \times (100MHz \times 39.77) = 7.954GHz \quad (30)$$

CIRCUIT DESCRIPTION

RF Output Divider

The RFOUT_DIV (Register 0x022, Bits[7:5]) is a 3-bit divider used to divide the frequency seen at the output buffer. The divide ratio can be set from 1, 2, 4, 8, 16, 32, 64, or 128, offering a frequency range from 57MHz to 8500MHz. The divider output power can be set via the DIV_PWR bits (Register 0x022, Bits[2:0]). The RFOUT_DIV and output divider channels,NDIV_OUT and PDIV_OUT, can be disabled when not in use via the PD_ODIV bit (Register 0x028, Bit 1).

The RF output divider channels, NDIV_OUT and PDIV_OUT, can be either AC- or DC-coupled and terminated with a 100Ω resistor differentially as shown in Figure 39 and Figure 40. If a single-ended output is desired, each side of the output must be individually AC-coupled and terminated with a 50Ω resistor, see Figure 41. For AC-coupled applications, a series of 0.1µF capacitors must be connected to the RFOUT, PDIV_OUT, and NDIV_OUT pins as shown in Figure 42.

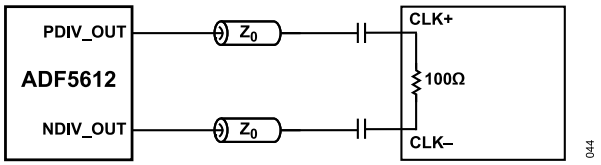

Figure 39. Common Clock Interface: Differential Clock with End Termination (Z_O = 50 Ω), AC-Coupled

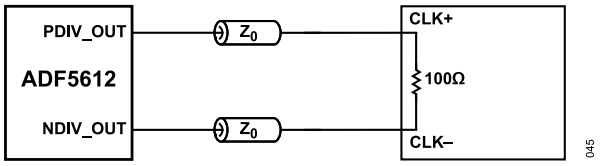

Figure 40. Common Clock Interface: Differential Clock with End Termination (Z_O = 50 Ω), DC-Coupled

THEORY OF OPERATION

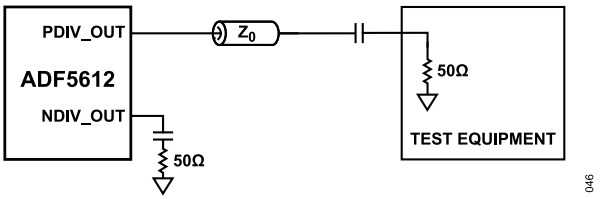

Figure 41. Common Clock Interface: Single-Ended Clock with End Termination (Z_O = 50 Ω)

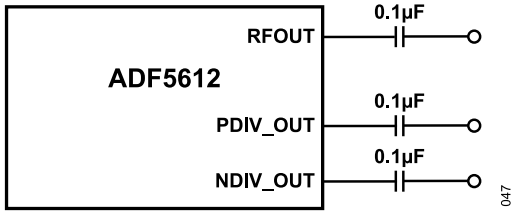

Figure 42. Output Interface Schematic

Feedback Divider (N)

The feedback divider provides a division ratio in the PLL feedback path. The division ratio consists of a 20-bit N_INT (Register 0x010 to Register 0x012), a 25-bit FRAC1WORD (Register 0x012 to Register 0x015), a 24-bit FRAC2WORD (Register 0x017 to Register 0x019), and a 24-bit MOD2WORD (Register 0x01A to Register 0x01C) bit field values that this divider comprises together with the fixed modulus MOD1WORD (2^{25}).

Reference Input

The reference signal of the PLL is input through XREFP, which operates as a single-ended input. This high impedance input is self biased and requires AC-coupling (refer to Figure 43 for a simplified schematic of the reference input stage). The reference signal input on the XREFP is enabled by configuring the PD_RDIV bit (Register 0x027, Bit 6) to 0. In this case, SW1 and SW2 are closed, and SW3 is open.

The slew rate of the input reference signal significantly affects the performance. The device is functional with signals as low as 0.4V p-p amplitude. However, to achieve optimal performance and the in-band phase noise performance of the ADF5612, apply a continuous sine-wave signal or a square-wave signal with a slew rate of at least 500V/µs. Achieving this slew rate with sinusoidal waves requires high amplitudes and may not be possible at low frequencies. For a frequency input of 10MHz, a square wave is required. A high performance square wave signal with a high slew rate is recommended as the reference input signal to achieve the best performance. See Figure 44 for reference input signal requirements and interfacing.

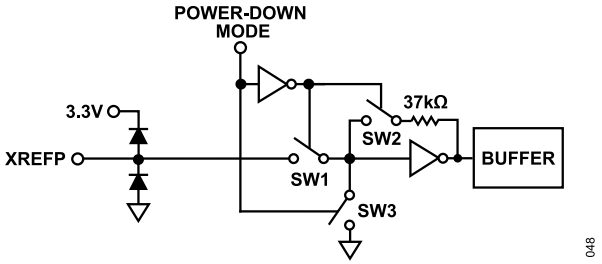

Figure 43. Reference Input Stage

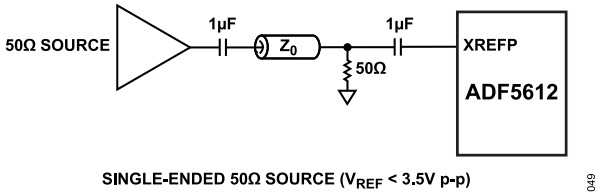

Figure 44. Reference Input Source

Reference Divider

The reference path R divider, R_DIV (Register 0x01F, Bits[7:0] and Register 0x20, Bits[5:0], respectively), is based on a 14-bit counter. This divider is used to reduce the frequency seen at the PFD, and its divide ratio (R) can be set to any integer from 1 to 16,383, inclusive. Use the R_DIV bits to directly program the R divide ratio.

Phase and Frequency Detector (PFD)

The PFD, in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the reference divider or reference doubler and feedback divider. These source and sink pulses are required to phase lock the loop, forcing a phase alignment at the inputs of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO. See Figure 45 for a simplified schematic of the PFD.

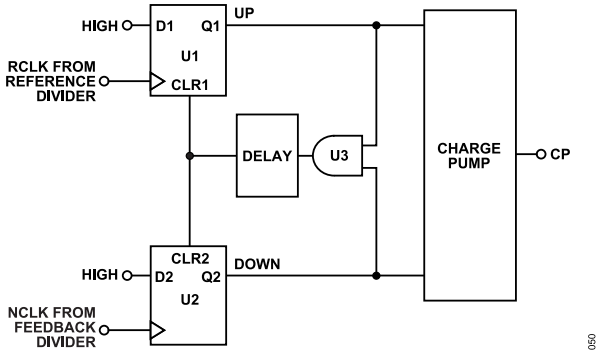

Figure 45. Simplified PFD Schematic

THEORY OF OPERATION

Charge Pump

The charge pump, controlled by the PFD, forces sink (down) or source (up) current pulses onto the CP pin, which must be connected to an appropriate loop filter. See Figure 46 for a simplified schematic of the charge pump.

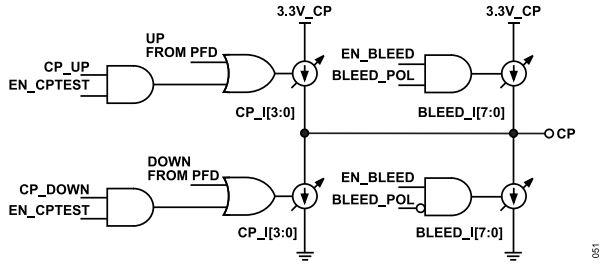

Figure 46. Simplified Charge Pump Schematic

The output current magnitude, I_{CP}, can be set from 0.2mA to 3.2mA using the CP_I bits (Register 0x021, Bits[3:0]). A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components, while a smaller I_{CP} can result in better spurious performance. See Table 7 for the charge pump programming values.

Table 7. CP Programming

CP_I, Bits[3:0]	I_{CP} (mA)
0	0.2
1	0.4
2	0.6
3	0.8
4	1
5	1.2
6	1.4
7	1.6
8	1.8
9	2
10	2.2
11	2.4
12	2.6
13	2.8
14	3
15	3.2

Charge Pump Test Mode

When the charge pump test mode EN_CPTEST bit (Register 0x02B, Bit 2) is set to 1, it allows the CP_UP and CP_DOWN bits (Register 0x02B, Bit 0 and Bit 1, respectively) to enforce a constant I_{CP} source or sink current, respectively, on the CP pin. These bits can be used as an aid to debug issues related to PLL during the hardware and software development phase of a project. For normal operation, set EN_CPTEST, CP_UP, and CP_DOWN to 0. See Table 8 for applicable charge pump test mode.

Table 8. Charge Pump Test Mode

EN_CPTEST	CP_UP	CP_DOWN	CP Pin State	Debug Test
1	0	0	High-Z	VCO open loop
1	1	0	~$V_{3.3V\_CP}$	Charge pump output voltage verification
1	0	1	~GND	Charge pump output voltage verification
0	0	0	Normal operation	Not applicable

Charge Pump Bleed Current Optimization

A small programmable constant charge pump current, known as bleed current, can be used to optimize the phase noise and fractional spurious signals in fractional mode, which also changes the propagation delay from the XREFP input pin to the RFOUT, PDIV_OUT, and NDIV_OUT output pins.

Configure the EN_BLEED bit (Register 0x01E, Bit 6) to 1 to enable the bleed current. If the BLEED_POL bit (Register 0x01E, Bit 0) is set to 1, a constant source current is applied to the CP pin. Conversely, if the BLEED_POL bit is adjusted to 0, a constant sink current is applied to the CP pin.

The 8-bit BLEED_I bits (Register 0x01D, Bits[7:0]) are used to optimize the spurious performance of the ADF5612. The bleed current, BLEED_I, is calculated and configured based on the required bleed time (t_{BLEED}) at a given VCO frequency, I_{CP}, and f_{PFD} as shown in the following equations:

$$t_{BLEED} = \frac{4}{2 \times VCO}$$

$$I_{BLEED} = t_{BLEED} \times f_{PFD} \times I_{CP}$$

$$BLEED\_I = \frac{I_{BLEED}}{3.125\mu A}$$

Lock Detector

The lock detector uses internal signals from the PFD to measure the phase difference between the output signal of the reference divider (RCLK) and the output signal of the feedback divider (NCLK) in Figure 45. This detector is enabled by configuring the PD_LD bit (Register 0x027, Bit 3) to 0, and both the EN_LOL and EN_LDWIN bits (Register 0x02A, Bit 5 and Bit 4, respectively) to 1. The output of the lock detector can be accessed either through the LOCKED bit (Register 0x048, Bit 0), or via the SDO pin (Pin 19) by setting the EN_MUXOUT bit (Register 0x02B, Bit 3) to 1 and programming the MUXOUT bits (Register 0x02B, Bits[7:4]) to 1 (LKDET).

The PFD RCLK and NCLK phase difference must be less than the phase difference lock window time, t_{LDWIN}, for a set number of PFD cycles before the lock detector output indicates the PLL has locked. The desired number of PFD cycles varies depending on whether the lock detect accuracy or speed is prioritized. See Table 9 to set

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the desired PFD cycles on the LD_COUNT bits (Register 0x029, Bits[4:0]). Five loop filter time constants can be used as an initial approximation of the needed number of PFD cycles, as shown in the following equation:

$$\text{PFD Cycles} = \left(\frac{5}{2 \times \pi \times \text{LFBW}}\right) \times f_{PFD}$$

where:

LFBW is the loop filter bandwidth

f_{PFD} is the PFD frequency

Table 9. LD_COUNT Programming

LD_COUNT[4:0]	PFD Cycles
0	27
1	35
2	51
3	67
4	99
5	131
6	195
7	259
8	387
9	515
10	771
11	1027
12	1539
13	2051
14	3075
15	4099
16	6147
17	8195
18	12291
19	16387
20	24579
21	32771

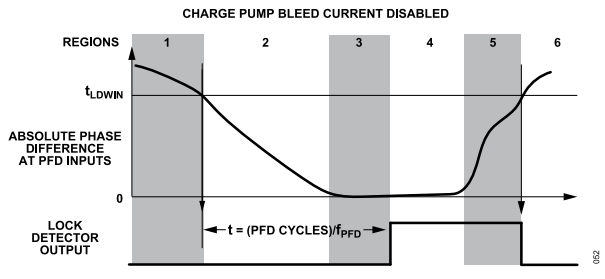

Figure 47. Lock Detector Timing, Bleed Current Disabled

Table 10. Lock Detector Timing, Bleed Current Disabled

Region	Absolute Phase Difference at PFD	Lock Detector State
1	$>t_{LDWIN}$	Low
2	$<t_{LDWIN}$	Low, counts PFD cycles
3	~0	Low, counts PFD cycles
4	~0	High, greater than or equal to the desired PFD cycle count
5	$<t_{LDWIN}$	High
6	$>t_{LDWIN}$	Low (immediately)

When the charge pump bleed current is enabled, a phase offset is applied to the PFD inputs. This phase offset, t_{IDEL}, is proportional to the amount of bleed current. Region 3 and Region 4 in Figure 47 and Figure 48 highlight the PFD phase difference the PLL settles to when the charge pump bleed current is disabled or enabled, respectively.

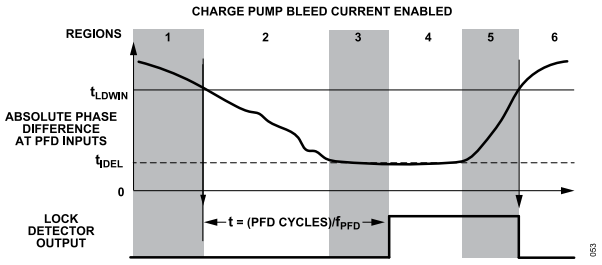

Figure 48. Lock Detector Timing, Bleed Current Enabled

For proper operation of the lock detector, the absolute value of t_{IDEL} must be less than t_{LDWIN}. The user sets the phase difference lock window time (t_{LDWIN}) for a valid lock condition on the LDWIN_PW bits (Register 0x029, Bits[7:5]). Configure the LDWIN_PW bits to 1 for integer mode and to 3 for fractional mode. All other bit field combinations are not applicable.

Table 11. LDWIN_PW Programming

LDWIN_PW [7:5]	Mode of Operation
001	Integer mode, 100MHz maximum PFD
011	Fractional mode, 100MHz maximum PFD, RF ≥ 3.65GHz

MUXOUT

The MUXOUT bits (Register 0x02B, Bits[7:4]) provide the user with access to various internal nodes. A common application of the MUXOUT bits is to serve as an extra lock status output or to debug PLL-related issues during the hardware and software development stages of a project. The MUXOUT bits and the SDO pin have a shared function on the SDO Pin (Pin 19). Refer to Table 12 to access the MUXOUT bits on the SDO pin. In 3-wire mode (SDO_ACTIVE = 0), set EN_MUXOUT (Register 0x2B, Bit 3) to 1 to output the MUXOUT data. In 4-wire mode (SDO_ACTIVE = 1), set EN_MUXOUT to 0 to allow SPI data to be read from the device during a SPI read operation. The CMOS_OV bit (Register 0x035, Bit 5) determines if the logic high level for the SDO or SDIO pins is 3.3V or 1.8V. See Table 12 for the different SDO pin configurations.

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Table 12. SDO Pin State

SDO_ACTIVE, Register 0x000, Bit 3	EN_MUXOUT	SDO Pin State
0	0	SDO pin inactive
0	1	MUXOUT signal
1	0	SDO data
1	1	MUXOUT signal

Temperature Sensor

The temperature sensor is composed of an 8-bit ADC, which measures the proportional to absolute temperature (PTAT) voltage with respect to the reference voltage (VREF) of a bandgap. The purpose of the temperature sensor is to measure changes in the die temperature and not the absolute junction temperature. The ADC clock can be generated from the reference clock (normal operation) or the SCK (test mode) that is configured in ADC_CLK_TEST_SEL bit (Register 0x037, Bit 0). Configuring the ADC_CLK_TEST_SEL to 1 (SCK) allows ADC conversion while all other blocks are inactive. In this configuration, the temperature of the chip is solely affected by the ADC. For normal operation, ADC_CLK_TEST_SEL set to 0. The maximum ADC clock frequency is 400kHz, and the ADC_CLK_DIV register (Register 0x036, Bits[7:0]) is used to set the division factor that divides the actual clock sent to the ADC.

To initialize ADC measurement, program the registers of the ADF5612 as shown in Table 13. An ADC conversion requires 17 clock cycles to complete. The ADC_BUSY readback bit (Register 0x048, Bit 2) monitors the conversion status. During a conversion, ADC_BUSY reads back to 1, and when the conversion is complete, ADC_BUSY reads back to 0. Measurements are then recorded in the 8-bit CHIP_TEMP register bit fields (Register 0x04A, Bits[7:0] and Register 0x04B, Bit 0). The value read back in Register 0x04A represents the junction temperature in degrees Celsius. The MSB (Bit 8) in Register 0x04B indicates positive or negative temperature, that is, when Bit 8 = 1, the temperature read back is negative.

Table 13. ADC Register Setup

Bit Fields	Value
EN_DNCLK, EN_ADC	1
EN_ADC_CLK, ADC_ST_CNV, and EN_ADC_CNV	1
PD_ADC	0

Double Buffering

Double buffering refers to a main and subordinate configuration for the bit fields detailed in Table 14.

Only the subordinate bit fields control the actual state of the ADF5612. When double buffering is enabled for a bit field, the SPI only writes to the main bit field. The subordinate bit field retains its previous value until a register write is sent to Register 0x010. After writing to Register 0x010, all the main bit fields are automatically loaded to their respective subordinate bit fields. Writing to Register 0x010 also starts the autocalibration of the VCO (see the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section), which allows the user to update several bit fields that change the output frequency of the ADF5612 and starts a new VCO calibration on the same register write. When double buffering is disabled, the SPI writes directly to the subordinate bit field.

Table 14. Double Buffer Enabled Bit Fields

Double Buffer Enabler Bits	Double Buffered Bit Fields
Not Applicable, Always Enabled	N_INT, R_DIV, FRAC1WORD, FRAC2WORD, MOD2WORD, CP_I
RFODIV_DB (Register 0x02C, Bit 7)	RFOUT_DIV
O_VCO_DB (Register 0x031, Bit 7)	M_VCO_CORE, M_VCO_BAND, M_VCO_BIAS
DEL_CTRL_DB (Register 0x033, Bit 7)	BLEED_I, BLEED_POL

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Serial Port

The SPI-compatible serial port provides control and monitoring functionality. The CMOS_OV bit (Register 0x035, Bit 5) determines if the logic high level for the SDO and SDIO SPI output pins is 3.3V or 1.8V. The SPI can be programmed to support several different configurations in Register 0x000 and Register 0x001. The SDO_ACTIVE bit (Register 0x000, Bit 3) determines if the serial port is configured as a 3-wire or 4-wire SPI (see the timing diagrams in Figure 2, Figure 3 and Figure 4.

The SPI register map can be programmed with single instructions, as shown in Figure 49 and Figure 50, or in streaming mode, as shown in Figure 51. Streaming mode allows for efficient data transfer read or write cycles to multiple registers. Streaming mode allows the user to program a bit stream composed of one register address in the instruction header and data for that register address, which is then followed by data in subsequent register addresses. The ADDRESS_ASCENSION bit (Register 0x000, Bit 2) determines if the subsequent register addresses are incremented or decremented. It is recommended to decrement the register addresses in streaming mode (ADDRESS_ASCENSION = 0). The reason for this recommendation is because REG0010 triggers the VCO calibration and loading of all double buffers and, therefore, must be the last SPI register written to. The SINGLE_INSTRUCTION bit (Register 0x001, Bit 7) disables streaming mode when it is set to 1. When SINGLE_INSTRUCTION is set to 0, streaming mode is enabled.

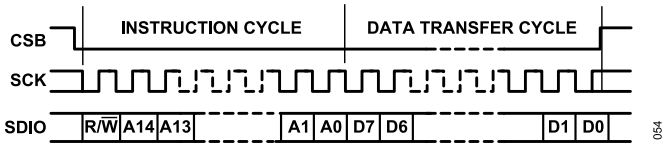

Figure 49. Serial Interface, MSB First (LSB_FIRST = 0)

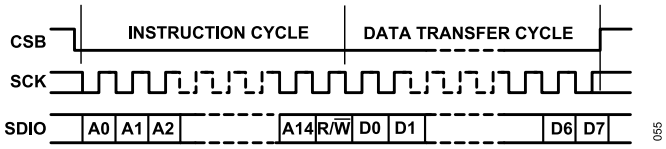

Figure 50. Serial Interface, LSB First (LSB_FIRST = 1)

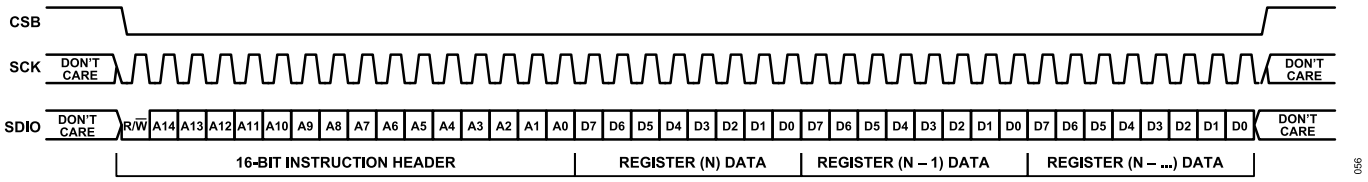

Figure 51. Serial Interface, Recommended Streaming Mode (SINGLE_INSTRUCTION = 0) with Decrementing Registers (ADDRESS_ASCENCION = 0)

APPLICATIONS INFORMATION

POWER-UP AND INITIALIZATION SEQUENCE

The following steps describe the recommended power-up and initialization sequence of the ADF5612:

1. Apply specified voltages to the 5V and 3.3V power supply pins. The ADF5612 is in full power-down mode at this point and SPI programming is not possible.
2. Set the CEN pin (Pin 44) to a logic high.
3. After waiting ≥200µs for all SPI register bits to settle to their power-on reset (POR) state, begin programming the SPI to configure the ADF5612 to a desired state. The following is the recommended SPI programming sequence:
   a. Set the SDO_ACTIVE bit (Register 0x000, Bit 3) and the CMOS_OV bit (Register 0d035, Bit 5) to a desired state for future readback operations.
   b. Program all required register addresses. The ordering of programming does not matter except to ensure that Register 0x010 is the last register write. There are several required reserved register field settings provided in Table 16 that are required for proper device operation.
4. The ADF5612 remains in power-down mode until the PD_ALL bit (Register 0x027, Bit 7) is programmed to 0.
5. A write to Register 0x010 starts a VCO autocalibration. At this point, the ADF5612 is fully operational, and new frequencies can be programmed as often as desired. The following steps are information for the PD_ALL bit and the CEN pin.
6. Setting PD_ALL to 1 powers down the ADF5612, retaining the latest programmed SPI settings and full SPI programming capability.
7. If only the state of PD_ALL was modified in Step 6, setting PD_ALL to 0 returns the ADF5612 to the frequency programmed in Step 5. After a 10µs wait, all circuit blocks are completely powered up internally. This 10µs wait does not include the frequency settling time associated with the loop filter bandwidth.
8. Toggling the CE pin level causes the ADF5612 to return to full power-down mode and return the SPI registers to the POR state (see Step 2 and Step 3).

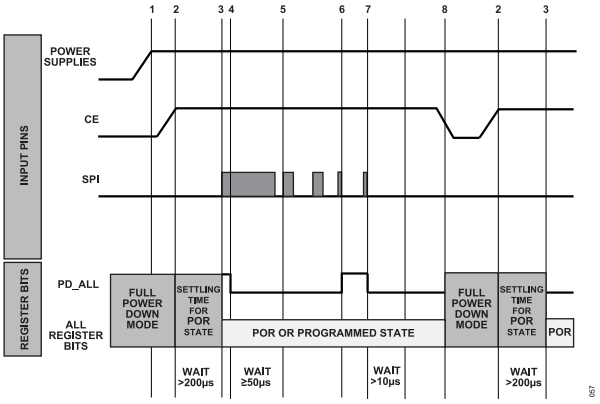

Figure 52. Power-Up and Initialization

Programming Procedure

There are two different methods to power up the ADF5612. The most commonly used method is provided in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section that is mandatory at the initial device power-up.

The method provided in the Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings section is an optional power-up procedure after the initial power-up.

Standard Power-Up and Initialization Sequence, Automatic VCO Calibration

The following standard power-up and initialization sequence is the recommended procedure to power up and program the ADF5612:

1. Follow Step 1 through Step 5 in the Power-Up and Initialization Sequence section.
2. It is optional to monitor the status of the VCO calibration bits, ADC_BUSY and FSM_BUSY (Register 0x048, Bit 2 and Bit 1, respectively). A VCO calibration is completed when ADC_BUSY transitions from high to low followed by FSM_BUSY transitioning from high to low.
3. After the VCO calibration is complete, disable the VCO calibration clocks by setting EN_DNCLK (Register 0x01E, Bit 4) = EN_ADC_CLK (Register 0x02C, Bit 3) = 0. Disabling the VCO calibration clocks reduces unwanted spurious content.
4. The PLL is locked when the lock detector sets the LOCKED bit (Register 0x48, Bit 0) to high.
5. When changing the frequency, take the following steps:
   a. Program only the modified registers.
   b. Write to Register 0x010 to start a new VCO autocalibration as the final step whether it is modified or not.

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Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings

For fast frequency hopping applications, a much shorter lock time is required. The ADF5612 can be manually programmed with predetermined calibration values to decrease the overall lock time by bypassing VCO calibration. The calibration values are first obtained by performing an autocalibration and reading back the corresponding band, core, and bias values for a given frequency. These values can then be manually programmed to the ADF5612 on subsequent device initializations. The values of the readbacks vary with each device due to process variation.

The following steps outline the procedure to perform a manual VCO calibration after initialization:

1. Perform an autocalibration with the target frequency required.
2. Record the VCO_CORE (Register 0x04D, Bit 7), VCO_BAND (Register 0x04D, Bits[6:0]), and VCO_BIAS (Register 0x049, Bits[2:0]).
3. On subsequent power-up and initialization sequences, program the override (O_VCO_CORE, O_VCO_BAND, and O_VCO_BIAS, Register 0x02D, Bit 0, Bit 1, and Bit 2, respectively) and manual VCO bits (M_VCO_CORE (Register 0x016 Bit 0), M_VCO_BAND (Register 0x016, Bits[7:1]), and M_VCO_BIAS (Register 0x015, Bits[7:5]) as documented in Table 15.
4. Program the fractional N-divider bit field values as required. See the Output Frequency section for calculations.
5. Program the N_INT value (Register 0x010) to program all of the manually calibrated values.
6. Repeat the sequence for each target frequency.

Table 15. Manually Programmed VCO Calibration Settings

Bit Fields	Value	Description
O_VCO_DB	0x1	Manually calibrated values are double buffered by programming N_INT.
EN_AUTOCAL	0x0	Disables autocalibration.
EN_DNCLK	0x0	Disables DIV_NCLK to the digital block.
EN_ADC_CLK	0x0	Disables the ADC clock.
O_VCO_CORE	0x1	Overrides the VCO core with value in M_VCO_CORE.
O_VCO_BAND	0x1	Overrides the VCO band with M_VCO_BAND.
O_VCO_BIAS	0x1	Overrides the VCO bias with M_VCO_BIAS.
M_VCO_CORE	Program with recorded values	Selects the VCO core when O_VCO_CORE = 1.
M_VCO_BAND	Program with recorded values	Selects the band within the core when O_VCO_BAND = 1.
M_VCO_BIAS	Program with recorded values	Selects the bias value used when O_VCO_BIAS = 1.
Configure Target Frequency Parameters	Program RFOUT	Sets the corresponding N_INT, FRAC1WORD, FRAC2WORD, and MOD2WORD. Ensure that Register 0x10 is the last write command.

LOOP FILTER DESIGN

A stable loop filter design requires care in selecting the loop filter components of the ADF5612. It is recommended to download and install ADIsimPLL for loop filter design and simulation. ADIsimPLL has an integrated tutorial for first time users and a help manual for more complex topics. There are also several ADIsimPLL training videos available on the ADIsimPLL web page. After a loop filter is designed and simulated, it is recommended to verify the new loop filter using the ADF5612 evaluation hardware. A full loop filter design tutorial is beyond the scope of this data sheet. However, some best practices are shown in the following list. ADIsimPLL aids in defining and simulating these parameters. Any significant change to these items requires a new loop filter design.

A stable loop filter must meet the following criteria:

- Loop filter phase margin > 45°
- Loop filter bandwidth < f_{PFD} ÷ 10

The desired loop filter bandwidth is determined by the following features of the ADF5612:

- I_{CP}
- K_{VCO}
- PFD frequency
- Reference input phase noise.
- Trade-off between minimizing jitter or settling time

The VT pin has an internal 155pF capacitor to GND that must be included in the loop filter design. ADIsimPLL takes this internal capacitance into account automatically.

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Loop Filter Layout Considerations

When designing the layout for the loop filter signal path on the PCB, use the following design recommendations to optimize performance and reduce potential spurious signals. Refer to the EV-ADF5612SD1Z PCB design files for an optimized example loop filter layout footprint. The default loop filter on this board has been designed for integer mode performance with f_{PFD} = 61.44MHz.

1. Place capacitors that are connected directly to the charge pump or VT voltage (V_{VT}) signals as close as possible to the corresponding device pin to ensure that the ground signals are close to the device ground.
2. Place charge pump, power supply decoupling capacitors as close as possible to the CP pin. Due to the limited available layout space, the charge pump, supply decoupling capacitors can be placed on the underside of the evaluation board.
3. Insert ground vias in the ground pads of shunt capacitors for optimal ground connections.
4. Reduce loop filter path length to ensure that the loop filter components are close to the device, with ground pads close to device ground.

VCO

The VCO subsystem consists of a switched capacitor, step tuned VCO, and an output stage. The topology of the VCO allows both fundamental and doubled frequency outputs. This arrangement allows the lower, fundamental frequency of the oscillator to be routed to the input of the PLL, which reduces the N counter of the PLL by a factor of 2. This reduction of the N counter results in not only a 3dB improvement in the close in-phase noise but also prevents residual phase noise degradation at offsets beyond 10MHz. The VCO tuning is a 2-step process consisting of band selection and fine tuning. During normal operation, autocalibration is enabled (EN_AUTOCAL, Register 0x1E, Bit 7), which allows the PLL finite state machine (FSM) to perform a binary search of the VCO bands (band selection). After the proper band is located, the charge pump output from the PLL takes control of the tuning port (VT) on the VCO and adjusts to the proper fundamental frequency (fine tuning) and is phase locked by the PLL.

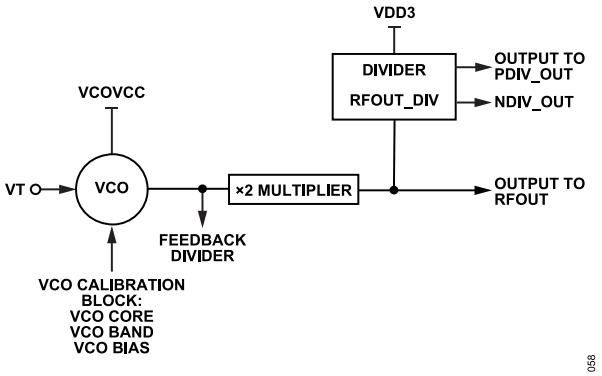

Figure 53. VCO and Clock Outputs

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VCO CALIBRATION

A VCO calibration is required to select the correct VCO core, VCO band, and VCO bias settings for a specific VCO frequency. This procedure assumes that the device is powered up, the desired reference frequency is present on the XREFP pin, and all other registers are programmed correctly. Figure 54 and Figure 55 are provided as visual aids for this procedure.

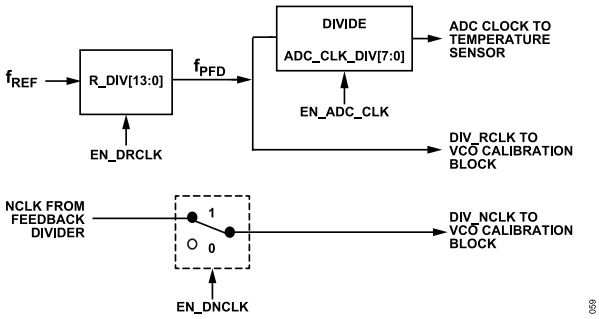

Figure 54. VCO Calibration Dividers

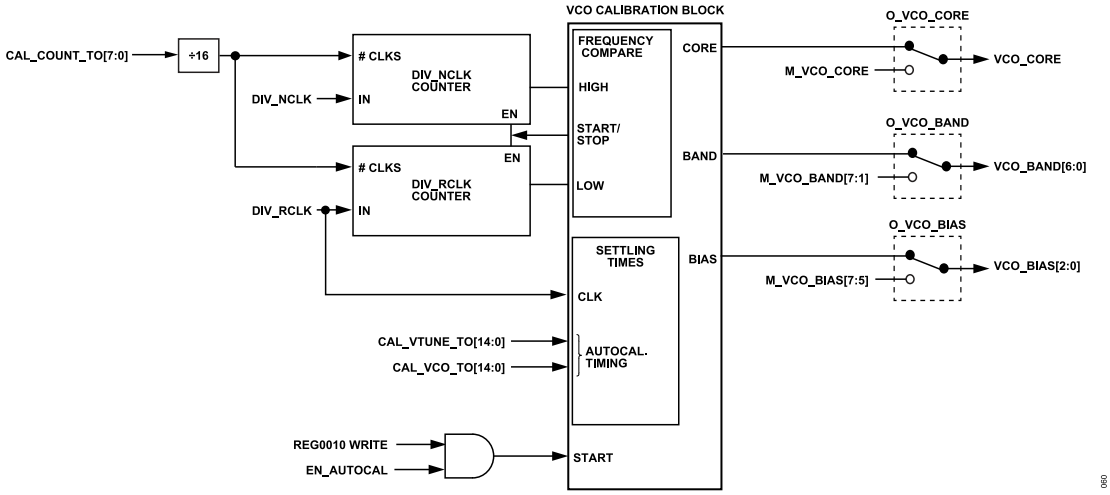

Figure 55. VCO Calibration Block

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The following calibration timeout bit fields must be programmed for autocalibration:

- CAL_VTUNE_TO (Register 0x030, Bits[7:0] and Register 0x031, Bits[6:0]): At the beginning of the calibration, VT is connected to the VPRST pin and is multiplexed to VT during VCO calibration. Calculate the CAL_VTUNE_TO as follows:

$$\text{CAL\_VTUNE\_TO} = \text{ceil}(\text{VTUNE\_CAL\_TIMEOUT} \times f_{PFD}) \quad (31)$$

  where VTUNE_CAL_TIMEOUT is a fixed value of 1µs. It is the time it takes for the VTUNE CAL to settle.
- CAL_COUNT_TO (Register 0x02F, Bits[7:0]): This bit field is used to calculate the target band decision timeout. During autocalibration, there are eight band decisions to be made to select the final band of operation for the selected frequency. CAL_COUNT_TO is used to program the time taken for each band decision. This time affects the calibration accuracy. Use the following equation to set the decision time of each band:

$$\text{CAL\_COUNT\_TO} \times 16 = \text{ceil}(\text{VCO\_BIT\_CAL\_TIMEOUT} \times f_{PFD}) \quad (32)$$

  where VCO_BIT_CAL_TIMEOUT is a fixed value of 8µs. It is the time it takes to make a VCO Core and Band decision.
- CAL_VCO_TO (Register 0x032, Bits[7:0] and Register 0x033, Bits[6:0]): This bit field is used to set the target VCO frequency settling timeout after each band decision. To set this time, use the following equation:

$$\text{CAL\_VCO\_TO} = \text{ceil}(\text{VCO\_CAL\_TIMEOUT} \times f_{PFD}) \quad (33)$$

  where VCO_CAL_TIMEOUT is a fixed value of 2µs. It is the time it takes for the frequency to settle after a band and VCO change.

To perform a VCO calibration, set up the following several registers as outlined in the following procedure:

1. Set DCLK_MODE.
2. Calculate and set the minimum required values for CAL_VTUNE_TO, CAL_VCO_TO, and CAL_COUNT_TO as per their corresponding formulas previously described in this section.
3. Set the N_INT, RFOUT_DIV, and R_DIV bits by programming Register 0x010 last. Any writes to Register 0x010 start the VCO autocalibration.
4. Monitor the FSM_BUSY bit (Register 0x048, Bit 3). The calibration is finished when the FSM_BUSY transitions from high to low.
5. After the VCO calibration is complete, disable the calibration clocks to limit unwanted spurious content by setting EN_ADC_CLK = EN_DNCLK = 0.

Total Autocalibration Time

Use each of the calibration timeout values to calculate the total autocalibration time as follows:

$$\text{Total Autocalibration Time} = \frac{\text{CAL\_VTUNE\_TO} + \text{No. of Cal Decisions} \times ((\text{CAL\_COUNT\_TO} \times 16) + \text{CAL\_VCO\_TO})}{f_{PFD}} \quad (34)$$

where No. of Cal Decisions is a fixed value = 8 that consists of one VCO decision and a seven band decision.

Refer to the VCO Calibration section to calculate for the CAL_VTUNE_TO, CAL_COUNT_TO, and CAL_VCO_TO.

REGISTER MAP

Table 16. ADF5612 Register Map

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	SOFT_RESET_R	LSB_FIRST_R	ADDRESS_ASCENSION_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDRESS_ASCENSION	LSB_FIRST	SOFT_RESET	0x00	R/W
0x001	SINGLE_INSTRUCTION	CSB_STALLING	MASTER_READBACK_CONTROL	RESERVED					0x00	R/W
0x002	RESERVED								0x00	R/W
0x003	RESERVED				CHIP_TYPE				0x00	R
0x004	PRODUCT_ID[7:0]								0x00	R
0x005	PRODUCT_ID[15:8]								0x00	R
0x006	RESERVED								0x00	R/W
0x007	RESERVED								0x00	R/W
0x008	RESERVED								0x00	R/W
0x009	RESERVED								0x00	R/W
0x00A	SCRATCHPAD								0x00	R/W
0x00B	SPI_REVISION								0x00	R
0x00C	VENDOR_ID[7:0]								0x56	R
0x00D	VENDOR_ID[15:8]								0x04	R
0x00E	RESERVED								0x00	R/W
0x00F	RESERVED								0x00	R/W
0x010	N_INT[7:0]								0x80	R/W
0x011	N_INT[15:8]								0x00	R/W
0x012	FRAC1WORD[3:0]				N_INT[19:16]				0x00	R/W
0x013	FRAC1WORD[11:4]								0x00	R/W
0x014	FRAC1WORD[19:12]								0x00	R/W
0x015	M_VCO_BIAS				FRAC1WORD[24:20]				0x00	R/W
0x016	M_VCO_BAND				M_VCO_CORE				0x00	R/W
0x017	FRAC2WORD[7:0]								0x00	R/W
0x018	FRAC2WORD[15:8]								0x00	R/W
0x019	FRAC2WORD[23:16]								0x00	R/W
0x01A	MOD2WORD[7:0]								0x01	R/W
0x01B	MOD2WORD[15:8]								0x00	R/W
0x01C	MOD2WORD[23:16]								0x00	R/W
0x01D	BLEED_I								0x00	R/W
0x01E	EN_AUTOCAL	EN_BLEED	DCLK_MODE	EN_DNCLK	RESERVED		1	BLEED_POL	0x00	R/W
0x01F	R_DIV[7:0]								0x01	R/W
0x020	RESERVED		R_DIV[13:8]						0x00	R/W
0x021	RESERVED	INT_MODE	RESERVED	EN_RCNTR	CP_I				0x00	R/W
0x022	RFOUT_DIV			RFOUT_PWR		DIV_PWR			0x00	R/W
0x023	1	1	1	1	1	1	1	1	0x00	R/W
0x024	1	1	1	1	1	1	1	1	0x00	R/W
0x025	0	1	1	1	1	1	1	1	0x00	R/W
0x026	RESERVED		VAR_MOD_EN	DITHER1_SCALE			EN_DITHER2	EN_DITHER1	0x00	R/W
0x027	PD_ALL	PD_RDIV	PD_NDIV	PD_VCO	PD_LD	PD_PFDCP	PD_ADC	PD_CALGEN	0x80	R/W
0x028	RESERVED						PD_PFDNCLK	PD_ODIV	0x01	R/W
0x029	LDWIN_PW			LD_COUNT					0x00	R/W
0x02A	0	1	EN_LOL	EN_LDWIN	RESERVED	RST_LD	ABPW_WD	RESERVED	0x00	R/W
0x02B	MUXOUT				EN_MUXOUT	EN_CPTEST	CP_DOWN	CP_UP	0x04	R/W

REGISTER MAP

Table 16. ADF5612 Register Map (Continued)

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02C	RFODIV_DB	RESERVED	RESERVED	RST_SYS	EN_ADC_CLK	RESERVED	CAL_CT_SEL	RESERVED	0x00	R/W
0x02D	RESERVED					O_VCO_BIAS	O_VCO_BAND	O_VCO_CORE	0x00	R/W
0x02E	RESERVED								0x00	R/W
0x02F	CAL_COUNT_TO								0x00	R/W
0x030	CAL_VTUNE_TO[7:0]								0x00	R/W
0x031	O_VCO_DB	CAL_VTUNE_TO[14:8]							0x00	R/W
0x032	CAL_VCO_TO[7:0]								0x00	R/W
0x033	DEL_CTRL_DB	CAL_VCO_TO[14:8]							0x00	R/W
0x034	RESERVED								0x00	R/W
0x035	RESERVED		CMOS_OV	RESERVED					0x00	R/W
0x036	ADC_CLK_DIV								0x00	R/W
0x037	EN_ADC_CNV	RESERVED					EN_ADC	ADC_CLK_TEST_SEL	0x00	R/W
0x038	RESERVED	1	0	0	1	1	1	0	0x00	R/W
0x039	RESERVED	0	1	0	0	0	1	0	0x00	R/W
0x03A	RESERVED								0x00	R/W
0x03B	RESERVED								0x00	R/W
0x03C	RESERVED								0x00	R/W
0x03D	RESERVED								0x00	R/W
0x03E	RESERVED								0x00	R/W
0x03F	0	1	0	1	0	1	0	0	0x00	R/W
0x040	RESERVED		1	0	1	0	1	1	0x00	R/W
0x041	RESERVED								0x00	R/W
0x042	RESERVED								0x00	R/W
0x043	RESERVED								0x00	R/W
0x044	RESERVED							ADC_ST_CNV	0x00	R/W
0x045	RESERVED								0x00	R/W
0x046	RESERVED								0x00	R/W
0x047	RESERVED								0x00	R/W
0x048	RESERVED					ADC_BUSY	FSM_BUSY	LOCKED	0x00	R
0x049	RESERVED					VCO_BIAS			0x00	R
0x04A	CHIP_TEMP[7:0]								0x00	R
0x04B	RESERVED							CHIP_TEMP[8]	0x00	R
0x04C	RESERVED								0x00	R
0x04D	VCO_CORE	VCO_BAND							0x00	R
0x04E	RESERVED								0x00	R
0x04F	VERSION								0x00	R
0x100	RESERVED		0	0	0	0	0	0	0x00	R/W
0x101	RESERVED		0	0	0	0	0	0	0x00	R/W
0x102	RESERVED		0	0	0	0	0	0	0x00	R/W
0x103	RESERVED		0	0	0	0	0	0	0x00	R/W
0x104	RESERVED		1	0	0	1	0	0	0x00	R/W
0x105	RESERVED		1	0	0	1	0	0	0x00	R/W
0x106	RESERVED		1	0	0	1	0	0	0x00	R/W
0x107	RESERVED		1	0	0	1	0	0	0x00	R/W

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: REG0000

Table 17. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Repeat of SOFT_RESET.	0x0	R/W
6	LSB_FIRST_R	Repeat of LSB_FIRST.	0x0	R/W
5	ADDRESS_ASCENSION_R	Repeat of ADDRESS_ASCENSION.	0x0	R/W
4	SDO_ACTIVE_R	Repeat of SDO_ACTIVE.	0x0	R/W
3	SDO_ACTIVE	Choose between 3-wire or 4-wire operation. 0: 3-wire. 1: 4-wire SPI (enables SDO and SDIO to become an input only).	0x0	R/W
2	ADDRESS_ASCENSION	Address Ascension When Streaming. 0: address auto-decrements when streaming. 1: address auto-increments when streaming.	0x0	R/W
1	LSB_FIRST	I/O Data Oriented LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
0	SOFT_RESET	Reset SPI Registers Except REG0000 to POR State. Self clearing reset. 0: normal operation. 1: soft reset.	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG0001

Table 18. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: SPI streaming enabled. 1: SPI streaming disabled.	0x0	R/W
6	CSB_STALLING	CSB Stalling.	0x0	R/W
5	MAIN_READBACK_CONTROL	Main/Subordinate Readback Control. 0: for double-buffered bit fields, readback subordinate register. 1: for double-buffered bit fields, readback main register.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x002, Reset: 0x00, Name: REG0002

Table 19. Bit Descriptions for REG0002

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x003, Reset: 0x00, Name: REG0003

Table 20. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type = 0x06.	0x0	R

Address: 0x004, Reset: 0x00, Name: REG0004

REGISTER DETAILS

Table 21. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID = 0x000B.	0x0	R

Address: 0x005, Reset: 0x00, Name: REG0005

Table 22. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID = 0x0000.	0x0	R

Address: 0x006, Reset: 0x00, Name: REG0006

Table 23. Bit Descriptions for REG0006

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x007, Reset: 0x00, Name: REG0007

Table 24. Bit Descriptions for REG0007

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x008, Reset: 0x00, Name: REG0008

Table 25. Bit Descriptions for REG0008

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x009, Reset: 0x00, Name: REG0009

Table 26. Bit Descriptions for REG0009

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x00A, Reset: 0x00, Name: REG000A

Table 27. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	SPI SCRATCHPAD.	0x0	R/W

Address: 0x00B, Reset: 0x00, Name: REG000B

Table 28. Bit Descriptions for REG000B

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REVISION	SPI Revision = 0x01.	0x0	R

Address: 0x00C, Reset: 0x56, Name: REG000C

Table 29. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor ID = 0x0456.	0x56	R

REGISTER DETAILS

Address: 0x00D, Reset: 0x04, Name: REG000D

Table 30. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor ID = 0x0456.	0x4	R

Address: 0x00E, Reset: 0x00, Name: REG000E

Table 31. Bit Descriptions for REG000E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x00F, Reset: 0x00, Name: REG000F

Table 32. Bit Descriptions for REG000F

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x010, Reset: 0x80, Name: REG0010

Table 33. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Access
[7:0]	N_INT[7:0]	20-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2. Double buffering always enabled.	0x80	R/W

Address: 0x011, Reset: 0x00, Name: REG0011

Table 34. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Access
[7:0]	N_INT[15:8]	20-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2. Double buffering always enabled.	0x0	R/W

Address: 0x012, Reset: 0x00, Name: REG0012

Table 35. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Access
[7:4]	FRAC1WORD[3:0]	25-Bit FRAC1 Word. Sets the FRAC1 value.	0x0	R/W
[3:0]	N_INT[19:16]	20-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2. Double buffering always enabled.	0x0	R/W

Address: 0x013, Reset: 0x00, Name: REG0013

Table 36. Bit Descriptions for REG0013

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[11:4]	25-Bit FRAC1 Word. Sets the FRAC1 value.	0x0	R/W

Address: 0x014, Reset: 0x00, Name: REG0014

Table 37. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[19:12]	25-Bit FRAC1 Word. Sets the FRAC1 value.	0x0	R/W

REGISTER DETAILS

Address: 0x015, Reset: 0x00, Name: REG0015

Table 38. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Access
[7:5]	M_VCO_BIAS	Selects the Bias Value Used When O_VCO_BIAS = 1. Used in manual VCO calibration together with the M_VCO_BAND and M_VCO_CORE.	0x0	R/W
[4:0]	FRAC1WORD[24:20]	25-Bit FRAC1 Word. Sets the FRAC1 value.	0x0	R/W

Address: 0x016, Reset: 0x00, Name: REG0016

Table 39. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Access
[7:1]	M_VCO_BAND	Selects band within core when O_VCO_BAND = 1. Used in manual VCO calibration together with M_VCO_BIAS and M_VCO_CORE. 127 = lowest frequency, and 0 = highest frequency.	0x0	R/W
0	M_VCO_CORE	Selects VCO core when O_VCO_CORE = 1. Used in manual VCO calibration together with M_VCO_BAND and M_VCO_BIAS. 0: VCO 0 highest frequency. 1: VCO 1 lowest frequency.	0x0	R/W

Address: 0x017, Reset: 0x00, Name: REG0017

Table 40. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[7:0]	24-Bit FRAC2 Word. Sets the FRAC2 value.	0x0	R/W

Address: 0x018, Reset: 0x00, Name: REG0018

Table 41. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[15:8]	24-Bit FRAC2 Word. Sets the FRAC2 value.	0x0	R/W

Address: 0x019, Reset: 0x00, Name: REG0019

Table 42. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[23:16]	24-Bit FRAC2 Word. Sets the FRAC2 value.	0x0	R/W

Address: 0x01A, Reset: 0x01, Name: REG001A

Table 43. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[7:0]	24-Bit MOD2 Word. Sets the MDO2 value.	0x1	R/W

Address: 0x01B, Reset: 0x00, Name: REG001B

Table 44. Bit Descriptions for REG001B

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[15:8]	24-Bit MOD2 Word. Sets the MDO2 value.	0x0	R/W

Address: 0x01C, Reset: 0x00, Name: REG001C

REGISTER DETAILS

Table 45. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[23:16]	24-Bit MOD2 Word. Sets the MDO2 value.	0x0	R/W

Address: 0x01D, Reset: 0x00, Name: REG001D

Table 46. Bit Descriptions for REG001D

Bits	Bit Name	Description	Reset	Access
[7:0]	BLEED_I	Bleed Current = BLEED_I × 3.125µA.	0x0	R/W

Address: 0x01E, Reset: 0x00, Name: REG001E

Table 47. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Access
7	EN_AUTOCAL	Enable VCO Calibration. 0: VCO calibration disabled. 1: VCO calibration enabled.	0x0	R/W
6	EN_BLEED	Enable Bleed Current. 0: bleed current disabled. 1: bleed current enabled.	0x0	R/W
5	DCLK_MODE	Divide RCLK and NCLK Frequency by 2 During VCO Calibration. 0: disables frequency reduction. 1: enables frequency reduction.	0x0	R/W
4	EN_DNCLK	Enable DIV_NCLK to the Digital Block. 0: DIV_NCLK off. 1: DIV_NCLK on.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R/W
1	REG1E_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	BLEED_POL	Bleed Polarity. 0: current sink. 1: current source.	0x0	R/W

Address: 0x01F, Reset: 0x01, Name: REG001F

Table 48. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Access
[7:0]	R_DIV[7:0]	14-Bit R-Divider.	0x1	R/W

Address: 0x020, Reset: 0x00, Name: REG0020

Table 49. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
[5:0]	R_DIV[13:8]	14-Bit R-Divider.	0x0	R/W

Address: 0x021, Reset: 0x00, Name: REG0021

Table 50. Bit Descriptions for REG0021

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Table 50. Bit Descriptions for REG0021 (Continued)

Bits	Bit Name	Description	Reset	Access
6	INT_MODE	Integer Mode Enabler. 0: fractional mode. 1: integer mode.	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
4	EN_RCNTR	Enables the reference clock to digital. 0: disables RCNTR. 1: enables RCNTR.	0x0	R/W
[3:0]	CP_I	Charge Pump Current. 0000: 0.2mA. 0001: 0.4mA. 0010: 0.6mA. 0011: 0.8mA. 0100: 1mA. 0101: 1.2mA. 0110: 1.4mA. 0111: 1.6mA. 1000: 1.8mA. 1001: 2mA. 1010: 2.2mA. 1011: 2.4mA. 1100: 2.6mA. 1101: 2.8mA. 1110: 3mA. 1111: 3.2mA.	0x0	R/W

Address: 0x022, Reset: 0x00, Name: REG0022

Table 51. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Access
[7:5]	RFOUT_DIV	RF Output Divider. 000: Divide by 1. 001: Divide by 2. 010: Divide by 4. 011: Divide by 8. 100: Divide by 16. 101: Divide by 32. 110: Divide by 64. 111: Divide by 128.	0x0	R/W
[4:3]	RFOUT_PWR	Sets the output power level for RFOUT.	0x0	R/W
[2:0]	DIV_PWR	Sets the output power level for RFOUT_DIV.	0x0	R/W

Address: 0x023, Reset: 0x00, Name: REG0023

Table 52. Bit Descriptions for REG0023

Bits	Bit Name	Description	Reset	Access
7	REG23_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG23_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG23_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

REGISTER DETAILS

Table 52. Bit Descriptions for REG0023 (Continued)

Bits	Bit Name	Description	Reset	Access
4	REG23_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG23_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG23_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG23_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG23_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x024, Reset: 0x00, Name: REG0024

Table 53. Bit Descriptions for REG0024

Bits	Bit Name	Description	Reset	Access
7	REG24_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG24_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG24_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG24_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG24_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG24_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG24_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG24_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x025, Reset: 0x00, Name: REG0025

Table 54. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
7	REG25_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG25_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG25_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG25_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG25_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG25_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG25_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG25_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x026, Reset: 0x00, Name: REG0026

Table 55. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
5	VAR_MOD_EN	Enables auxiliary Σ-Δ modulator. 0: normal operation. 1: enables auxiliary Σ-Δ modulator.	0x0	R/W
[4:2]	DITHER1_SCALE	Selects the LSB position for Dither 1.	0x0	R/W
1	EN_DITHER2	Dither applied to second accumulator.	0x0	R/W
0	EN_DITHER1	Dither applied to first accumulator.	0x0	R/W

Address: 0x027, Reset: 0x80, Name: REG0027

REGISTER DETAILS

Table 56. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Access
7	PD_ALL	Main Power Down. 0: normal operation. 1: power down.	0x1	R/W
6	PD_RDIV	Powers down the R-divider. 0: normal operation. 1: power down R-divider.	0x0	R/W
5	PD_NDIV	Powers down the N-divider. 0: normal operation. 1: power down N-divider.	0x0	R/W
4	PD_VCO	Powers down the VCO. 0: normal operation. 1: power down VCO.	0x0	R/W
3	PD_LD	Powers down the lock detector. 0: normal operation. 1: power down the lock detector.	0x0	R/W
2	PD_PFDCP	Powers down the PFD charge pump. 0: normal operation. 1: power down the PDF charge pump.	0x0	R/W
1	PD_ADC	Powers down the temperature ADC. 0: normal operation. 1: power down ADC.	0x0	R/W
0	PD_CALGEN	Powers down the VTUNE calibration DAC. 0: normal operation. 1: power down the VTUNE calibration DAC.	0x0	R/W

Address: 0x028, Reset: 0x01, Name: REG0028

Table 57. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R/W
1	PD_PFDNCLK	Powers down the NCLK going to the PFD. 0: disables NCLK. 1: enables NCLK.	0x0	R/W
0	PD_ODIV	Powers down the output divider. 0: enables RFOUT_DIV. 1: disables RFOUT_DIV.	0x1	R/W

Address: 0x029, Reset: 0x00, Name: REG0029

Table 58. Bit Descriptions for REG0029

Bits	Bit Name	Description	Reset	Access
[7:5]	LDWIN_PW	Lock Detector Pulse Window Width. 001: integer PLL, 100MHz maximum PFD. 011: fractional PLL, 100MHz maximum PFD, RF > = 3.65GHz.	0x0	R/W
[4:0]	LD_COUNT	Number of PFD Cycles Before LD Goes High.	0x0	R/W

Address: 0x02A, Reset: 0x00, Name: REG002A

REGISTER DETAILS

Table 59. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	REG2A_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG2A_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	EN_LOL	Enables loss of lock detector. 0: disables loss of lock detector. 1: enables loss of lock detector.	0x0	R/W
4	EN_LDWIN	Enables the lock detector pulse window. 0: lock detector pulse window disabled. 1: lock detector pulse window enabled.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	RST_LD	Resets the lock detector to the unlocked state. 0: resets to inactive. 1: resets to active.	0x0	R/W
1	ABPW_WD	PFD Antibacklash Pulse Width.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x02B, Reset: 0x04, Name: REG002B

Table 60. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Access
[7:4]	MUXOUT	Selects test signal to MUXOUT. 0000: High-Z. 0001: LKDET. 0010: Low. 0011: SDMCLK/2. 0100: RCLK/2. 0101: NCLK/2. 0110: ADC_BUSY. 0111: Low. 1000: High. 1001: VCOCAL RBAND/2. 1010: VCOCAL NBAND/2. 1011: high. 1100: high. 1101: high. 1110: high. 1111: analog test.	0x0	R/W
3	EN_MUXOUT	Enables MUXOUT to SDO. 0: disables MUXOUT. 1: enables MUXOUT.	0x0	R/W
2	EN_CPTEST	Enables charge pump force up or down test mode. 0: charge pump force up or down test mode off (normal operation). 1: charge pump force up or down test mode on.	0x1	R/W
1	CP_DOWN	Forces pump down charge pump test mode. 0: forces pump down off. 1: forces pump down on.	0x0	R/W
0	CP_UP	Forces pump up charge pump test mode. 0: forces pump up off. 1: forces pump up on.	0x0	R/W

REGISTER DETAILS

Address: 0x02C, Reset: 0x00, Name: REG002C

Table 61. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Access
7	RFODIV_DB	Enables double buffering for the RFOUT_DIV bit field. 0: RFOUT_DIV not double buffered. 1: RFOUT_DIV double buffered.	0x0	R/W
6	RESERVED	Reserved	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
4	RST_SYS	Resets digital except SPI and registers to a POR state. 0: resets to inactive. 1: reset to active.	0x0	R/W
3	EN_ADC_CLK	Enables the ADC clock. 0: disables ADC clock. 1: enables ADC clock.	0x0	R/W
2	RESERVED	Reserved.	0x0	R/W
1	CAL_CT_SEL	Decreases by 1 the number of DIV_RCLK cycles used in the VCO calibration.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x02D, Reset: 0x00, Name: REG002D

Table 62. Bit Descriptions for REG002D

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R/W
2	O_VCO_BIAS	Overrides the VCO bias with M_VCO_BIAS. 0: VCO bias select from the VCO calibration state machine. 1: VCO bias select from M_VCO_BIAS.	0x0	R/W
1	O_VCO_BAND	Overrides the VCO band with M_VCO_BAND. 0: VCO band code from VCO calibration state machine. 1: VCO band code from M_VCO_BAND.	0x0	R/W
0	O_VCO_CORE	Overrides the VCO core with M_VCO_CORE. 0: VCO core select from VCO calibration state machine. 1: VCO core select from M_VCO_CORE.	0x0	R/W

Address: 0x02E, Reset: 0x00, Name: REG002E

Table 63. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x02F, Reset: 0x00, Name: REG002F

Table 64. Bit Descriptions for REG002F

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_COUNT_TO	Time for Each VCO Calibration Decision. CAL_COUNT_TO = ceil(8µs × f_{PFD})/16.	0x0	R/W

Address: 0x030, Reset: 0x00, Name: REG0030

REGISTER DETAILS

Table 65. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_VTUNE_TO[7:0]	Time for VCO Calibration VTUNE CAL-DAC Settling. CAL_VTUNE_TO = ceil(1µs × f_{PFD}).	0x0	R/W

Address: 0x031, Reset: 0x00, Name: REG0031

Table 66. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Access
7	O_VCO_DB	M_VCO_CORE, M_VCO_BAND, M_VCO_BIAS Doubled Buffered. 0: core, bias, and band not double buffered. 1: core, bias, and band double buffered.	0x0	R/W
[6:0]	CAL_VTUNE_TO[14:8]	Time for VCO Calibration VTUNE CAL-DAC Settling. CAL_VTUNE_TO = ceil(1µs × f_{PFD}).	0x0	R/W

Address: 0x032, Reset: 0x00, Name: REG0032

Table 67. Bit Descriptions for REG0032

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_VCO_TO[7:0]	Time for VCO Calibration Band/Core Settling. CAL_VCO_TO = ceil(2µs × f_{PFD}).	0x0	R/W

Address: 0x033, Reset: 0x00, Name: REG0033

Table 68. Bit Descriptions for REG0033

Bits	Bit Name	Description	Reset	Access
7	DEL_CTRL_DB	Delay That Controls Double Buffered. BLEED_I, BLEED_POL Double Buffered 0: not double buffered. 1: double buffered.	0x0	R/W
[6:0]	CAL_VCO_TO[14:8]	Time for VCO Calibration Band/Core Settling. CAL_VCO_TO = ceil(2µs × f_{PFD}).	0x0	R/W

Address: 0x034, Reset: 0x00, Name: REG0034

Table 69. Bit Descriptions for REG0034

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R/W

Address: 0x035, Reset: 0x00, Name: REG0035

Table 70. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
5	CMOS_OV	Logic High Voltage for SDO, SDIO. 0: 1.8V logic. 1: 3.3V logic.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x036, Reset: 0x00, Name: REG0036

Table 71. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CLK_DIV	ADC CLK Frequency = f_{PFD}/((ADC_CLK_DIV × 4) + 2).	0x0	R/W

Address: 0x037, Reset: 0x00, Name: REG0037

REGISTER DETAILS

Table 72. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Access
7	EN_ADC_CNV	Enables ADC conversion. 0: no ADC conversion. 1: performs the ADC conversion on R0x10 write if ADC is enabled.	0x0	R/W
[6:2]	RESERVED	Reserved.	0x0	R/W
1	EN_ADC	Enables ADC. 0: ADC disabled. 1: ADC enabled.	0x0	R/W
0	ADC_CLK_TEST_SEL	Selects ADC clock source. 0: uses RCLK as ADC clock source. 1: uses SPI SCK as ADC clock source.	0x0	R/W

Address: 0x038, Reset: 0x00, Name: REG0038

Table 73. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
6	REG38_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG38_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG38_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG38_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG38_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG38_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG38_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x039, Reset: 0x00, Name: REG0039

Table 74. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
6	REG39_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG39_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG39_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG39_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG39_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG39_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG39_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x03A, Reset: 0x00, Name: REG003A

Table 75. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x03B, Reset: 0x00, Name: REG003B

Table 76. Bit Descriptions for REG003B

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Address: 0x03C, Reset: 0x00, Name: REG003C

Table 77. Bit Descriptions for REG003C

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x03D, Reset: 0x00, Name: REG003D

Table 78. Bit Descriptions for REG003D

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x03E, Reset: 0x00, Name: REG003E

Table 79. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x03F, Reset: 0x00, Name: REG003F

Table 80. Bit Descriptions for REG003F

Bits	Bit Name	Description	Reset	Access
7	REG3F_RSV7	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
6	REG3F_RSV6	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
5	REG3F_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG3F_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG3F_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG3F_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG3F_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG3F_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x040, Reset: 0x00, Name: REG0040

Table 81. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
5	REG40_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG40_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG40_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG40_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG40_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG40_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x041, Reset: 0x00, Name: REG0041

Table 82. Bit Descriptions for REG0041

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x042, Reset: 0x00, Name: REG0042

REGISTER DETAILS

Table 83. Bit Descriptions for REG0042

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x043, Reset: 0x00, Name: REG0043

Table 84. Bit Descriptions for REG0043

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x044, Reset: 0x00, Name: REG0044

Table 85. Bit Descriptions for REG0044

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_ST_CNV	Writes this bit to start an ADC conversion.	0x0	R/W

Address: 0x045, Reset: 0x00, Name: REG0045

Table 86. Bit Descriptions for REG0045

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R

Address: 0x046, Reset: 0x00, Name: REG0046

Table 87. Bit Descriptions for REG0046

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[15:8]	Reserved.	0x0	R

Address: 0x047, Reset: 0x00, Name: REG0047

Table 88. Bit Descriptions for REG0047

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[23:16]	Reserved.	0x0	R

Address: 0x048, Reset: 0x00, Name: REG0048

Table 89. Bit Descriptions for REG0048

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	ADC_BUSY	1 = ADC conversion in progress.	0x0	R
1	FSM_BUSY	1 = VCO calibration in progress.	0x0	R
0	LOCKED	Lock Detector Output.	0x0	R

Address: 0x049, Reset: 0x00, Name: REG0049

Table 90. Bit Descriptions for REG0049

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	VCO_BIAS	VCO bias is selected.	0x0	R

REGISTER DETAILS

Address: 0x04A, Reset: 0x00, Name: REG004A

Table 91. Bit Descriptions for REG004A

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_TEMP[7:0]	Temperature Measured by the ADC. Bit 8 = Sign bits, Bits[7:0] = magnitude.	0x0	R

Address: 0x04B, Reset: 0x00, Name: REG004B

Table 92. Bit Descriptions for REG004B

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CHIP_TEMP[8]	Temperature Measured by the ADC. Bit 8 = Sign bits, Bits[7:0] = magnitude.	0x0	R

Address: 0x04C, Reset: 0x00, Name: REG004C

Table 93. Bit Descriptions for REG004C

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x04D, Reset: 0x00, Name: REG004D

Table 94. Bit Descriptions for REG004D

Bits	Bit Name	Description	Reset	Access
7	VCO_CORE	VCO core is selected.	0x0	R
[6:0]	VCO_BAND	VCO band is selected.	0x0	R

Address: 0x04E, Reset: 0x00, Name: REG004E

Table 95. Bit Descriptions for REG004E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x04F, Reset: 0x00, Name: REG004F

Table 96. Bit Descriptions for REG004F

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	Chip Version.	0x0	R

Address: 0x100, Reset: 0x00, Name: REG0100

Table 97. Bit Descriptions for REG0100

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG100_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG100_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG100_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG100_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG100_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG100_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x101, Reset: 0x00, Name: REG0101

REGISTER DETAILS

Table 98. Bit Descriptions for REG0101

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG101_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG101_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG101_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG101_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG101_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG101_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x102, Reset: 0x00, Name: REG0102

Table 99. Bit Descriptions for REG0102

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG102_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG102_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG102_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG102_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG102_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG102_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x103, Reset: 0x00, Name: REG0103

Table 100. Bit Descriptions for REG0103

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG103_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG103_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG103_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG103_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG103_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG103_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x104, Reset: 0x00, Name: REG0104

Table 101. Bit Descriptions for REG0104

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG104_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG104_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG104_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG104_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG104_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG104_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x105, Reset: 0x00, Name: REG0105

REGISTER DETAILS

Table 102. Bit Descriptions for REG0105

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG105_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG105_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG105_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG105_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG105_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG105_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x106, Reset: 0x00, Name: REG0106

Table 103. Bit Descriptions for REG0106

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG106_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG106_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG106_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG106_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG106_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG106_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

Address: 0x107, Reset: 0x00, Name: REG0107

Table 104. Bit Descriptions for REG0107

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	REG107_RSV5	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
4	REG107_RSV4	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
3	REG107_RSV3	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
2	REG107_RSV2	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
1	REG107_RSV1	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W
0	REG107_RSV0	Reserved. Table 16 (the register map) provides the reserved register settings.	0x0	R/W

OUTLINE DIMENSIONS

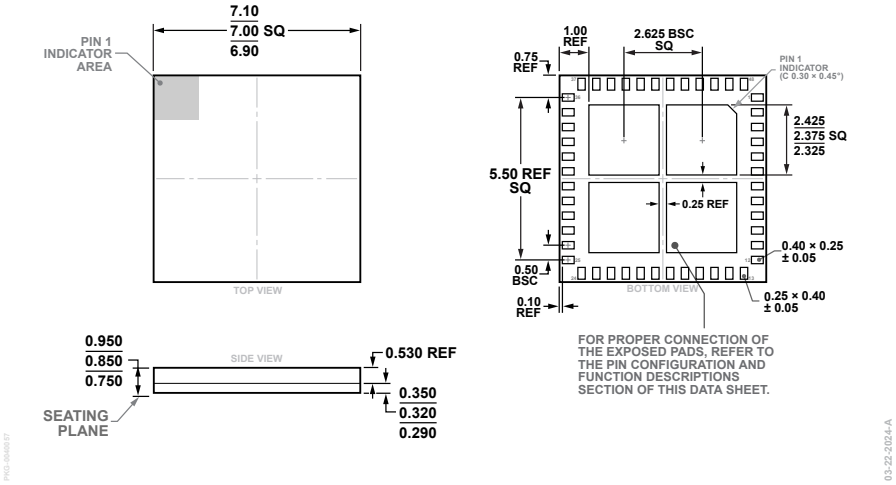

Figure 56. 48-Terminal Land Grid Array [LGA]
(CC-48-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADF5612CCCZ	−40°C to +105°C	48-Terminal Land Grid Array [LGA]	Tray	CC-48-14
ADF5612CCCZ-RL7	−40°C to +105°C	48-Terminal Land Grid Array [LGA]	Reel	CC-48-14

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 105. Evaluation Boards

Model[1]	Description
EV-ADF5612SD1Z	Evaluation Board

[1] Z = RoHS-Compliant Part.