Data Sheet

ADAU1797A

High-Performance Audio Codec with Integrated HiFi 3z and FastDSP Cores

FEATURES

- FastDSP™ audio processing engine
  - Low latency at sample rates up to 768kHz
  - Supports up to 128 instructions
- Tensilica® HiFi 3z DSP with TIE accelerators
  - Quad MAC/cycle and 1024kB total memory
  - 2-way SIMD IEEE floating point multiplier
  - Supports both 50MHz and 200MHz modes
- 5µs group delay (analog input to amp output)
  - 768kHz sample rate (FastDSP bypass mode)
- Three low power 24-bit ADC record channels
  - 104dB SNR, -91dB THD+N, 0.6mW (PGA on)
  - Flexible differential or single-ended inputs
  - 2.35µV_{RMS} A-Wt. input-referred noise (PGA_GAIN = 18dB, single-ended)
- Ten digital microphone (DMIC) input channels
  - Two clock outputs (384kHz to 6.144MHz)
- Mono low power 24-bit DAC playback channel
  - 113dB SNR, -93dB THD+N, 1.4mW P_Q
  - High-efficiency, low-noise, Class-D amplifier
- Two high-performance PDM output channels
  - Supports 3.072MHz or 6.144MHz clock rates
- Two 32-bit I^2S/TDM serial audio data ports
  - Sync clock frequencies from 8kHz to 768kHz
  - Two full-duplex, 4-channel ASRCs
- Supports low power, single-supply mode (1.8V)
  - Integrated LDO or switch-cap regulator
  - Digital I/O supports 1.2V or 1.8V logic levels
- Digital Control and Communication interfaces
  - I^2C/SPI control and I^3C combined interfaces
  - Master QSPI, UART, and JTAG interfaces
  - Supports self-boot from QSPI Flash/EEPROM
- Multi-purpose I/O pins for GPIO/IRQ support
- Updated Self-Boot supporting a wider range of QSPI flash devices

APPLICATIONS

- True wireless stereo (TWS) ANC headphones
- Over-ear stereo ANC headphones
- VR and AR headsets and wearable devices
- Hearing assist and PSAP devices
- Soundbar and smart speaker systems
- Gaming devices and tablets

GENERAL DESCRIPTION

The device is a low power, high-performance audio codec that provides three analog input channels, ten DMIC input channels, two PDM output channels, and one high-efficiency Class-D amplifier output channel.

The device features a low power HiFi 3z audio DSP core and a low-latency FastDSP core. The audio DSP cores paired with high-fidelity audio data converters are ideal for applications like noise cancellation, transparency, personal sound amplification, and voice processing.

When operating in low-power mode, the DSP cores are optimized for small form factor applications such as true wireless stereo (TWS) headphones. In this mode, the device delivers the right level of processing power while still minimizing power consumption to extend play time.

The device has the flexibility to also support applications requiring additional processing capability such as over-ear headphones, VR and AR headsets, wearables, hearing assist, and PSAP devices. In high-performance mode, the HiFi 3z core is boosted from 50MHz to 200MHz, and the FastDSP supports double the number of instructions (up from 64 to 128). This increased processing capability can either be used to offload cycles from the host processor or enable a lower-cost host processor without requiring an additional external audio DSP or MCU.

The device supports a -40°C to +85°C temperature range and is available in a space-saving 77-ball WLCSP package (0.4mm pitch, 3.24mm × 4.83mm).

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FUNCTIONAL BLOCK DIAGRAM

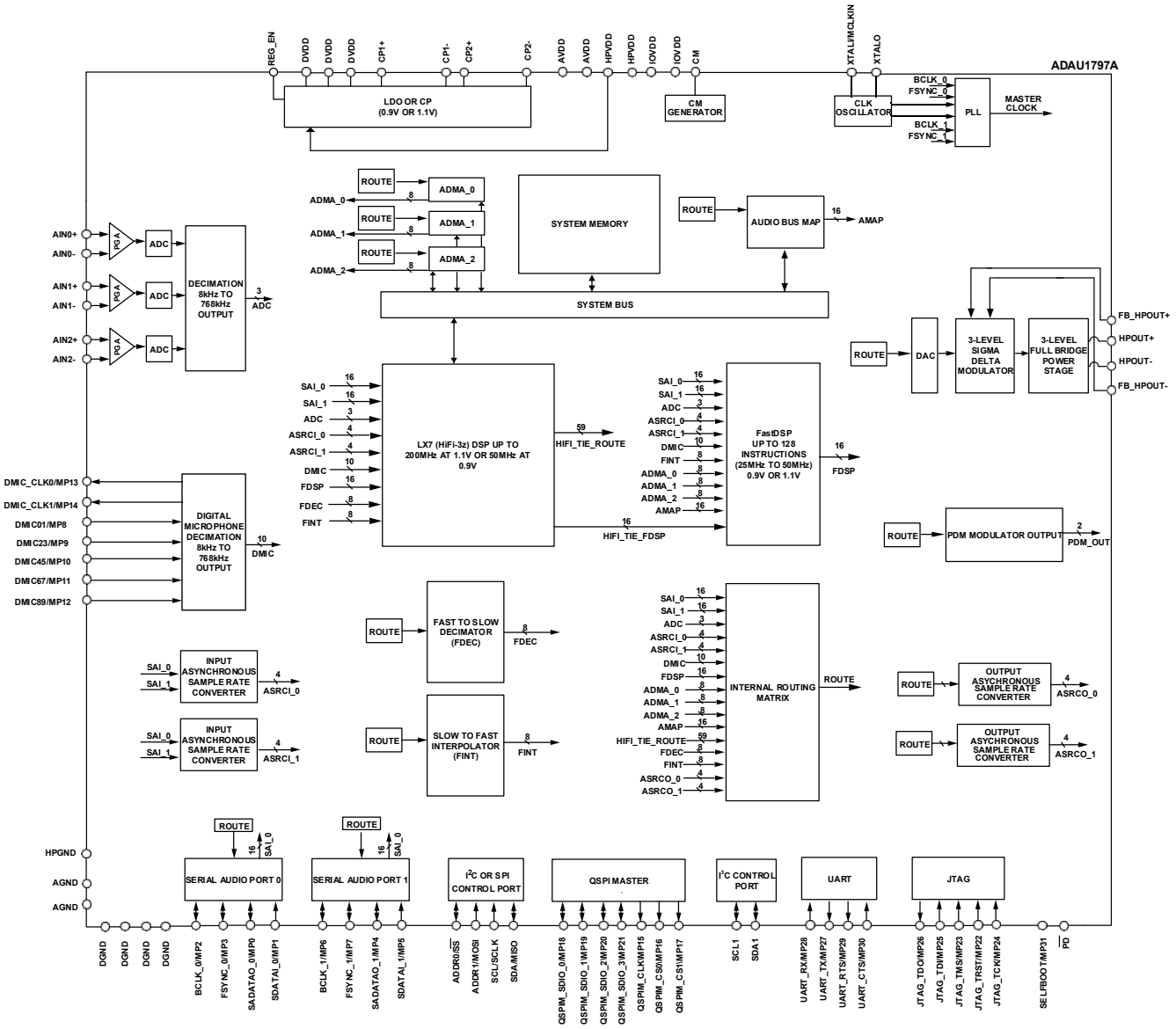

Figure 1. Top Level Block Diagram

REVISION HISTORY

7/2024—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Electrical Characteristics

(Supply voltages V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V (external), Supply bypass C_{AVDD} = C_{HPVDD} = C_{IOVDD} = 2.2µF + 2 x 0.1µF and C_{DVDD} = 2.2µF + 3 x 0.1µF, Master clock = 24.576MHz, Serial audio data port sample rate = 48kHz, Audio data word width = 24-bits, Headphone amplifier load = 16Ω +33µH, default analog power modes, AC measurement bandwidth = 20Hz to 20kHz, Ambient temperature (T_A) = -40°C to +85°C with typical values at +25°C unless otherwise noted, see the *System Block Diagram* for other external component values.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE RANGE							
AVDD Voltage	V_{AVDD}			1.7	1.8	1.98	V
AVDD Undervoltage Trip Point					1.55		V
HPVDD Voltage	V_{HPVDD}			1.7	1.8	1.98	V
HPVDD Undervoltage Trip Point					1.55		V
DVDD Voltage	V_{DVDD}	Integrated supply	HIFI_SPEED = 0	0.85	0.9	0.99	V
		External supply	HIFI_SPEED = 0	0.85	0.9	1.21	
		Integrated or external supply	HIFI_SPEED = 1	1.05	1.1	1.21	
IOVDD Voltage	V_{IOVDD}			1.1	1.8	1.98	V
ANALOG-TO-DIGITAL CONVERTERS (ADCs)							
ADC Resolution					24		Bits
Digital Volume Step					0.375		dB
Digital Volume Range				-71		+24	dB
Digital Volume Ramp Rate					4.5		dB/ms
ANALOG INPUT RESISTANCE (AINPx/AINNx R_{IN})							
Input Disabled					≥1		MΩ
Direct ADC Input Mode					21		kΩ
Programmable Gain Amplifier Input Mode		Differential input mode	-9dB attenuation		33.7		kΩ
			0dB gain		22.5		
			6dB gain		15		
			28.5dB gain		1.5		
		Single-ended or pseudo-diff. input mode	-9dB attenuation		26.5		
			0dB gain		15		
			6dB gain		9.2		
			28.5dB gain		0.9		

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
SINGLE-ENDED OR PSEUDO-DIFFERENTIAL LINE INPUT MODE (DIRECT TO ADC INPUT)							
Full-Scale Input Voltage		Input level for a 0dBFS output			0.64		V_{RMS}
					1.8		V_{P-P}
Dynamic Range[1]		A-weighted filter, f_{IN} = 1kHz, -60dBFS output	Normal operation mode (default)		100		dB
			Extreme power-saving mode		96		
		Unweighted filter, f_{IN} = 1kHz, -60dBFS output	Normal operation mode (default)		97		
			Extreme power-saving mode		93		
Signal-to-Noise Ratio (SNR)[2]		Normal operation mode	A-weighted filter		100		dB
			Unweighted filter		97		
THD+N Level[3]		f_{IN} = 1kHz, -1dBFS output, normal operation mode			-87		dBFS
Interchannel Gain Mismatch					0.04		dB
Offset Error					±0.1		mV
Gain Error					±0.2		dB
Interchannel Isolation		C_{CM} = 10µF			100		dB
Power Supply Rejection Ratio (PSRR)		C_{CM} = 10µF, 100mV_{P-P} signal	f_{IN} = 1kHz		70		dB
			f_{IN} = 10kHz		50		
DIFFERENTIAL LINE INPUT MODE (DIRECT TO ADC INPUT)							
Full-Scale Input Voltage		Input level for a 0dBFS output			1.08		V_{RMS}
					3.05		V_{P-P}
Dynamic Range[1]		A-weighted filter, f_{IN} = 1kHz, -60dBFS output	Normal operation mode (default)		106		dB
			Extreme power-saving mode		100		
			Normal operation mode (default)		103		

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
		Unweighted filter, f_{IN} = 1kHz, -60dBFS output	Extreme power-saving mode		97		
Signal-to-Noise Ratio (SNR)[2]		Normal operation mode	A-weighted filter		106		dB
			Unweighted filter		103		
THD+N Level[3]		f_{IN} = 1kHz, -1dBFS output, normal operation mode			-93		dBFS
CMRR					60		dB
Interchannel Gain Mismatch					0.04		dB
Offset Error					±0.1		mV
Gain Error					±0.2		dB
Interchannel Isolation		C_{CM} = 10µF			100		dB
Power Supply Rejection Ratio (PSRR)		C_{CM} = 10µF, 100mV_{P-P} signal	f_{IN} = 1kHz		70		dB
			f_{IN} = 10kHz		50		
SINGLE-ENDED OR PSEUDO-DIFFERENTIAL PGA INPUT MODE (PGA ENABLED)							
Full-Scale Input Voltage		Input level for a 0dBFS output			0.54		V_{RMS}
					1.53		V_{P-P}
Dynamic Range[1]		A-weighted filter, f_{IN} = 1kHz, -60dBFS output, +6dB PGA gain	Normal operation mode (default)		99		dB
			Extreme power-saving mode		98		
		Unweighted filter, f_{IN} = 1kHz, -60dBFS output, +6dB PGA gain	Normal operation mode (default)		96		
			Extreme power-saving mode		94		
Signal-to-Noise Ratio (SNR)[2]		+6dB PGA gain, normal operation mode	A-weighted filter		98		dB
			Unweighted filter		95		
THD+N Level[3]		f_{IN} = 1kHz, -1dBFS output, +6dB PGA gain, normal operation mode			-90		dBFS

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Input-Referred Noise		Single-ended mode, PGA_GAIN = 0dB	A-weighted filter		5.4		μV_{RMS}
		Single-ended mode, PGA_GAIN = 6dB	A-weighted filter		3.77		
		Single-ended mode, PGA_GAIN = 18dB	A-weighted filter		2.35		
		Pseudo-differential mode, PGA_GAIN = 0dB	A-weighted filter		5.09		
		Pseudo-differential mode, PGA_GAIN = 6dB	A-weighted filter		3.46		
		Pseudo-differential mode, PGA_GAIN = 18dB	A-weighted filter		2.01		
PGA Gain Range				-9		+29.25	dB
PGA Gain Step Size					0.75		dB
PGA Gain Variation with 0dB Setting					0.05		dB
PGA Gain Variation with +24dB Setting					0.15		dB
Interchannel Gain Mismatch					0.005		dB
Offset Error					±0.1		mV
Gain Error					±0.2		dB
Interchannel Isolation		C_{CM} = 10µF			100		dB
Power Supply Rejection Ratio (PSRR)		C_{CM} = 10µF, 100mV_{P-P} signal, f_{IN} = 1kHz			70		dB
DIFFERENTIAL PGA INPUT MODE (PGA ENABLED)							
		Input level for a 0dBFS output			1.08		V_{RMS}

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Full-Scale Input Voltage					3.05		V_{P-P}
Dynamic Range[1]		A-weighted filter, f_{IN} = 1kHz, -60dBFS output, 0dB PGA gain	Normal operation mode		104		dB
		A-weight(RMS)ed filter, f_{IN} = 1kHz, -60dBFS output, 0dB PGA gain	Extreme power-saving mode		100		
		Unweighted filter, f_{IN} = 1kHz, -60dBFS output, 0dB PGA gain	Normal operation mode		100		
			Extreme power-saving mode		97		
Signal-to-Noise Ratio (SNR)[2]		0dB PGA gain, normal operation mode	A-weighted filter		103		dB
			Unweighted filter		100		
THD+N Level[3]		f_{IN} = 1kHz, -1dBFS output, 0dB PGA gain, normal operation mode			-93		dBFS
Input-Referred Noise		Differential mode, PGA_GAIN = 0dB	A-weighted filter		7.37		$µV_{RMS}$
		Differential mode, PGA_GAIN = 6dB	A-weighted filter		4.73		
		Differential mode, PGA_GAIN = 18dB	A-weighted filter		2.30		
PGA Gain Range				-6		+30	dB
PGA Gain Step Size					0.75		dB
PGA Gain Variation With 0dB Setting					0.05		dB
PGA Gain Variation With +24dB Setting					0.15		dB
CMRR		1kHz input frequency			60		dB

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Interchannel Gain Mismatch					0.005		dB
Offset Error					±0.1		mV
Gain Error					±0.2		dB
Interchannel Isolation		C_{CM} = 10µF			100		dB
Power Supply Rejection Ratio (PSRR)		C_{CM} = 10µF, 100mV_{P-P} signal, f_{IN} = 1kHz			70		dB
DIGITAL-TO-ANALOG CONVERTER (DAC)							
DAC Resolution					24		Bits
Digital Volume Step					0.375		dB
Digital Volume Range				-71		+24	dB
Digital Volume Ramp Rate					4.5		dB/ms
DIFFERENTIAL HEADPHONE OUTPUT							
Full-Scale Output Voltage		0dBFS input to analog output channel, 16Ω load			1.15		V_{RMS}
Dynamic Range[1]		A-weighted filter, f_{IN} = 1kHz, -60dBFS input			113		dB
		Unweighted filter, f_{IN} = 1kHz, -60dBFS input			110		
Signal-to-Noise Ratio (SNR)[2]		A-weighted filter			113		dB
		Unweighted filter			110		
Output Noise		A-weighted filter, zero code digital input			2.57		$µV_{RMS}$
THD+N Level[3]		-2dBFS, 16Ω load			-90		dBV
THD+N Ratio		32Ω load	P_{OUT} = 1mW		-83		dB
			P_{OUT} = 30mW		-90		
		24Ω load, P_{OUT} = 40mW			-90		
		16Ω load, P_{OUT} = 60mW			-90		
Headphone Output Power		HPVDD = 1.8V, <0.1% THD+N ratio	32Ω load		40		mW
		HPVDD = 1.8V, <0.1% THD+N ratio	24Ω load		54		
			16Ω load		80		

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Gain Error					±2.5		%
DC Offset					±0.1		mV
Pop-Click Level		A-weighted peak transient voltage			0.5		mV_P
Peak Output Current						350	mA
Minimum Load Resistance				6			Ω
Minimum Load Inductance				5			µH
Maximum Load Capacitance		From HPOUTP or HPOUTN to GND or HPVDD				470	pF
Power Efficiency		55mW into a 16Ω load			90		%
PSRR		100mV_{P-P} signal	f_{IN} = 1kHz		89		dB
			f_{IN} = 10kHz		75		
COMMON MODE REFERENCE							
Output					0.85		V
Source Impedance					5		kΩ
PHASED-LOCKED LOOP (PLL)							
Input Frequency		After input prescale		0.9		2.1	MHz
Output Frequency				195.5	196.608	198	MHz
Fractional Limits		Fractional mode, fraction portion (N/M ratio)		0.1		0.9	
Integer Limits		Fractional mode, integer portion		2		256	
Input Pre-Divide				1		32	
Lock Time		1.024MHz input				1	ms
PLL Bypass XTAL Frequency					49.152		MHz
INTEGRATED LDO REGULATOR							
Line Regulation					1.1		mV/V
Load Regulation					0.3		mV/mA
INTEGRATED SWITCHED-CAP REGULATOR							
Line Regulation		V_{HPVDD} = 1.8V, see *Figure 47* for full HPVDD range			5		mV/V
Load Regulation					0.3		mV/mA
CRYSTAL AMPLIFIER							
Jitter					270	500	ps

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Frequency Range				0.9		50	MHz
Load Capacitance						20	pF
DIGITAL INPUT AND OUTPUT							
Input Voltage High	V_{IH}			0.7 × V_{IOVDD}			V
Input Voltage Low	V_{IL}					0.3 × V_{IOVDD}	V
Input Leakage High	I_{IH}	V_{IOVDD} = 1.8V	V_{IH} = 1.1V			10	µA
Input Leakage Low	I_{IL}	V_{IOVDD} = 1.8V	V_{IL} = 0.45V			10	µA
Output Voltage High	V_{OH}			0.71 × V_{IOVDD}	0.83 × V_{IOVDD}		V
Output High Current Drive Strength	I_{OH}	Low output drive strength			1		mA
		High output drive strength			3		
Output Voltage Low	V_{OL}				0.1 × V_{IOVDD}	0.3 × V_{IOVDD}	V
Output Low Current Drive Strength	I_{OL}	Low output drive strength			1		mA
		High output drive strength			3		
Input Capacitance						5	pF
SERIAL AUDIO DATA PORT DIGITAL INTERFACE CURRENT							
Digital Current (IOVDD)		Single serial audio data port disabled (SPTx), crystal oscillator enabled (24.576MHz) V_{IOVDD} = 1.8V			0.422		mA
		Single serial audio data port enabled (SPTx), crystal oscillator enabled (24.576MHz), 25pF line loads, V_{IOVDD} = 1.8V	Slave mode, f_S = 48kHz, f_{BCLK} = 3.072MHz		0.475		
			Slave mode, f_S = 192kHz, f_{BCLK} = 12.288MHz		0.481		
			Master mode, f_S = 48kHz, f_{BCLK} = 3.072MHz		0.697		
			Master mode, f_S = 192kHz, f_{BCLK} = 12.288MHz		1.336		

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PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
ADC INPUT TO DAC OUTPUT SIGNAL PATH						
Pass-Band Ripple		DC to 20kHz Bandwidth, f_S = 192kHz, ADCxx_FCOMP = 1, DAC_FCOMP = 1			±0.02	dB
Group Delay[4]		f_S = 192kHz		15.7		µs
		f_S = 384kHz		8.2		
		f_S = 768kHz		5.7		
ASYNCHRONOUS SAMPLE RATE CONVERTERS						
Pass-Band Frequency		f_{LRCLK} < 63kHz			0.475 x f_S	kHz
		63kHz ≤ f_{LRCLK} < 112kHz			0.4286 x f_S	
		112kHz ≤ f_{LRCLK}			0.4286 x f_S	
Audio-Band Ripple		20Hz to 20kHz bandwidth	-0.1		+0.1	dB
Sample Rate Frequency Range		Input and output ASRCs	7		224	kHz
Dynamic Range[1]		ASRCIx_LPM or ASRCOx_LPM = 0		130		dB
		ASRCIx_LPM or ASRCOx_LPM = 1		130		
		ASRCIx_LPM_II or ASRCOx_LPM_II = 1		130		
THD+N Level[3, 6]		ASRCIx_LPM or ASRCOx_LPM = 0		-130	-120	dBFS
		ASRCIx_LPM or ASRCOx_LPM = 1		-120	-110	
		ASRCIx_LPM_II or ASRCOx_LPM_II = 1		-115	-90	
Startup Lock-On Time					25	ms
PULSE DENSITY MODULATION (PDM) OUTPUTS						
Dynamic Range[1]		A-weighted filter		126		dB
THD+N Level[3]		-6dBFS input level		-125		dBFS
Group Delay[5]		f_S = 384kHz, f_{PDM_CLK} = 6.144MHz		7.5		µs
		f_S = 768kHz, f_{PDM_CLK} = 6.144MHz		4.9		
MASTER CLOCK TIMING SPECIFICATIONS						
Master Clock Period	t_{MP}	900kHz to 49.152MHz input clock frequency	0.0203		1.11	µs
SERIAL AUDIO DATA PORT TIMING SPECIFICATIONS						

(Supply voltages V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V (external), Supply bypass C_{AVDD} = C_{HPVDD} = C_{IOVDD} = 2.2µF + 2 x 0.1µF and C_{DVDD} = 2.2µF + 3 x 0.1µF, Master clock = 24.576MHz, Serial audio data port sample rate = 48kHz, Audio data word width = 24-bits, Headphone amplifier load = 16Ω +33µH, default analog power modes, AC measurement bandwidth = 20Hz to 20kHz, Ambient temperature (T_A) = -40°C to +85°C with typical values at +25°C unless otherwise noted, see the *System Block Diagram* for other external component values.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Nominal Bit Clock Frequency	f_{BCLK}	Maximum valid frequency	Slave mode		49.152		MHz
Nominal Bit Clock Frequency Range	f_{BCLK}	Maximum valid frequency	Master mode		24.576		MHz
		Minimum valid frequency	Slave mode		0.512		
			Master mode		2.048		
Bit Clock Low Pulse Width	t_{BL}	Master or slave mode		18			ns
Bit Clock High Pulse Width	t_{BH}	Master or slave mode		18			ns
Frame Sync Clock Frequency Range	f_{SYNC}	Maximum setting			768		kHz
		Minimum setting			8		
Frame Sync to Bit Clock Active Edge Setup Time	t_{LS}	Slave mode, setup time to bit clock active edge		3			ns
Bit Clock Active Edge to Frame Sync Hold Time	t_{LH}	Slave mode, hold time from bit clock active edge		5			ns
Data Input to Bit Clock Active Edge Setup Time	t_{SS}	Master or slave mode, setup time to bit clock active edge		3			ns
Bit Clock Active Edge to Data Input Hold Time	t_{SH}	Master or slave mode, hold time from bit clock active edge		10			ns
Bit Clock Inactive Edge to Frame Sync Edge Timing Skew	t_{TS}	Master mode				6	ns
Bit Clock Inactive Edge to Data Output Delay	t_{SOD}	Master or slave mode, delay until data output logic level change	V_{IOVDD} ≥ 1.62V	0		16	ns
		Master or slave mode, delay until data output level change	V_{IOVDD} ≥ 1.1V	0		32	

(Supply voltages V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V (external), Supply bypass C_{AVDD} = C_{HPVDD} = C_{IOVDD} = 2.2µF + 2 x 0.1µF and C_{DVDD} = 2.2µF + 3 x 0.1µF, Master clock = 24.576MHz, Serial audio data port sample rate = 48kHz, Audio data word width = 24-bits, Headphone amplifier load = 16Ω +33µH, default analog power modes, AC measurement bandwidth = 20Hz to 20kHz, Ambient temperature (T_A) = -40°C to +85°C with typical values at +25°C unless otherwise noted, see the *System Block Diagram* for other external component values.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Bit Clock Inactive Edge to Data Output Active	t_{SOTD}	Master or slave mode, delay until high-Z data output is active	0		16	ns
Bit Clock Inactive Edge to Data Output High-Z	t_{SOTX}	Master or slave mode, delay until active data output is high-Z	0		16	ns
I²C CONTROL PORT TIMING SPECIFICATIONS						
Serial Clock (SCL) Frequency	f_{SCL}				1	MHz
SCL Pulse Width High	t_{SCLH}		0.26			µs
SCL Pulse Width Low	t_{SCLL}		0.5			µs
SCL Setup Time for a Repeated Start Condition	t_{SCS}	Setup time from SCL rising to SDA falling	0.26			µs
SCL Hold Time for a Start Condition	t_{SCH}	Hold time from SDA falling to SCL falling	0.26			µs
SCL Setup Time for a Stop Condition	t_{BFT}	Setup time from SCL rising to SDA rising	0.5			µs
Serial Data (SDA) Setup Time	t_{DS}	SDA setup time to SCL rising	50			ns
Serial Data (SDA) Hold Time	t_{DH}	SDA hold time from SCL falling	0			ns
SCL and SDA Rise Time	t_{SCR}	400pF load			120	ns
SCL and SDA Fall Time	t_{SCF}	400pF load			120	ns
Bus Free Time Between Stop and Start Condition	t_{BUF}	Master mode	0.5			µs
I³C CONTROL PORT TIMING SPECIFICATIONS						
Maximum Serial Clock (SCL) Frequency	f_{SCL}	Master or slave mode		6.144		MHz
Maximum Serial Data (SDA) Rate	f_{SDA}	Master DDR mode		6.144		MHz
SCL Pulse Width High	t_{SCLH}	Slave mode	24			ns
SCL Pulse Width Low	t_{SCLL}	Slave mode	24			ns
SDA Input Setup Time		Slave mode	19			ns

(Supply voltages V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V (external), Supply bypass C_{AVDD} = C_{HPVDD} = C_{IOVDD} = 2.2µF + 2 x 0.1µF and C_{DVDD} = 2.2µF + 3 x 0.1µF, Master clock = 24.576MHz, Serial audio data port sample rate = 48kHz, Audio data word width = 24-bits, Headphone amplifier load = 16Ω +33µH, default analog power modes, AC measurement bandwidth = 20Hz to 20kHz, Ambient temperature (T_A) = -40°C to +85°C with typical values at +25°C unless otherwise noted, see the *System Block Diagram* for other external component values.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
	t_{DS}	Setup time from SDA edge to SCL rising edge	Master mode	10			
SDA Input Hold Time	t_{DH}	Slave mode		11			ns
SERIAL PERIPHERAL INTERFACE (SPI) PORT TIMING SPECIFICATIONS							
Serial Clock Frequency	f_{SCLK}					10	MHz
Serial Clock Pulse Width	t_{CCPL}	Low pulse		35			ns
	t_{CCPH}	High pulse		35			
Slave Select to Serial Clock Setup Time	t_{CLS}	Setup time to serial clock rising edge		5			ns
Serial Clock to Slave Select Hold Time	t_{CLH}	Hold time from serial clock rising		40			ns
Slave Select Pulse Width	t_{CLPH}	Minimum high pulse		10			ns
MOSI to Serial Clock Setup Time	t_{CDS}	Setup time to serial clock rising		10			ns
Serial Clock to MOSI Hold Time	t_{CDH}	Hold time from serial clock rising		10			ns
Serial Clock to MISO Data Delay Time	t_{COD}	Delay until MISO level change				30	ns
Slave Select to MISO High-Z Delay Time	t_{COTS}	Delay until MISO becomes high-Z				30	ns
QUAD-SPI (QSPI) MASTER PORT TIMING SPECIFICATIONS							
QSPI Clock Frequency	f_{SCLK}	QSPI output clock (QSPI_CLK) during self-boot				12.5	MHz
QSPI Data Input Setup Time	t_{CDS}	QSPI data input to clock rising edge setup time		10			ns
QSPI Data Input Hold Time	t_{CDH}	QSPI clock rising to data input edge hold time		10			ns
QSPI Data Output Delay Time	t_{COD}	QSPI data output delay from clock falling edge		1			ns
QSPI Data Output High-Z Delay Time	t_{CODS}	QSPI data output high-Z delay from chip select rising edge		1			ns
UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER (UART) PORT TIMING SPECIFICATIONS							

(Supply voltages V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V (external), Supply bypass C_{AVDD} = C_{HPVDD} = C_{IOVDD} = 2.2µF + 2 x 0.1µF and C_{DVDD} = 2.2µF + 3 x 0.1µF, Master clock = 24.576MHz, Serial audio data port sample rate = 48kHz, Audio data word width = 24-bits, Headphone amplifier load = 16Ω +33µH, default analog power modes, AC measurement bandwidth = 20Hz to 20kHz, Ambient temperature (T_A) = -40°C to +85°C with typical values at +25°C unless otherwise noted, see the *System Block Diagram* for other external component values.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
UART Baud Rate					3.125	Mbps
ACTIVE-LOW HARDWARE POWER-DOWN INPUT PIN TIMING SPECIFICATIONS						
Power-Down Input Assert Time	t_{RLPW}	Minimum time $\overline{PD}$ input must be asserted low to power down the device	20			ns
Power-Down Input Hardware Enable Time		REG_EN is pulled high, f_{MCLK} = 24.576MHz	15			ms
GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PIN TIMING SPECIFICATIONS						
GPIO (MPx) Input Latency	t_{GIL}	Time delay until MPx logic level is read internally			1.5 x $1/f_S$	µs
DIGITAL MICROPHONE INTERFACE TIMING SPECIFICATIONS						
DMIC Clock Output Fall Time	t_{CF}	2mA output drive strength, 25pF load			12	ns
DMIC Clock Output Rise Time	t_{CR}	2mA output drive strength, 25pF load			14	ns
DMIC Data Setup time	t_{SETUP}	Setup time from DMIC data edge to DMIC clock edge	10			ns
DMIC Data Hold Time	t_{HOLD}	Hold time from PDM clock edge to DMIC data edge	3			ns
PULSE DENSITY MODULATION (PDM) OUTPUT TIMING SPECIFICATIONS						
PDM Clock Frequency	f_{PDM_CLK}	PDM_RATE = 0		12.288		MHz
		PDM_RATE = 1		6.144		
		PDM_RATE = 2		3.072		
PDM Clock Output Fall Time	t_{CF}	2mA output drive strength, 25pF load			12	ns
PDM Clock Output Rise Time	t_{CR}	2mA output drive strength, 25pF load			14	ns
PDM Data Hold Time	t_{HOLD}	Delay time from PDM clock edge to PDM data change	35		46	ns

[1] Dynamic range is the ratio of the sum of the inband noise and harmonic power with a -60dBFS input signal level at 1kHz relative to the full-scale power level in decibels. Normal operating mode uses default settings, while extreme power saving mode changes ADCx_IBIAS to 0x1 and ADC_LP_MODE to 1.

[2] SNR is the ratio of the sum of all inband noise power with no input signal relative to the full-scale power level in decibels.

[3] THD+N level is the ratio of the sum of the inband harmonic power with the specified input signal level at 1kHz relative to either full-scale code (in dBFS) or a $1V_{RMS}$ reference level (in dBV).

[4] Group delay specified from analog input to Class-D amplifier output with FastDSP in bypass mode, ADCxx_FCOMP = 0, and DAC_FCOMP = 0. Point group delay values taken at f_{IN} = 1kHz, see the group delay *Typical Performance Characteristics* for the delay over the entire audio band.

[5] Group delay specified from input to the PDM output channels to the PDM output pins. Point group delay values taken at f_{IN} = 1kHz at the specified PDM sample rate.

[6] ASRC THD+N typical value is specified at f_{IN} = 1kHz and the maximum value is specified at f_{IN} = 20kHz.

Timing Diagrams

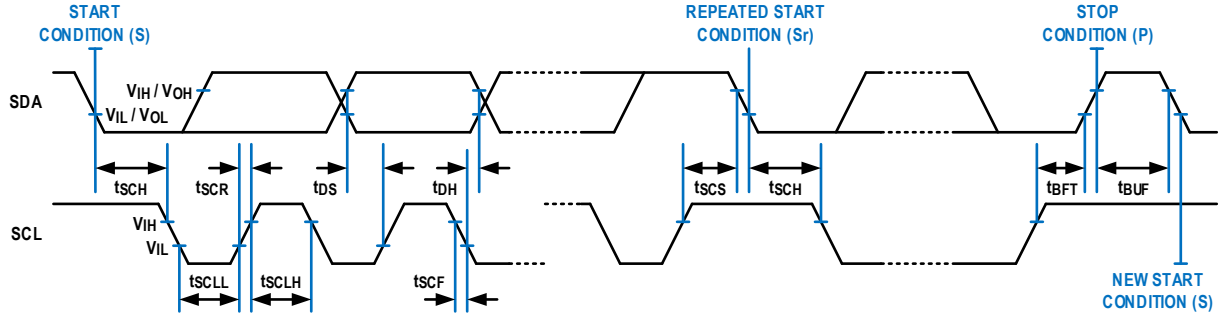


Figure 2. I²C Interface Slave Mode Timing Diagram

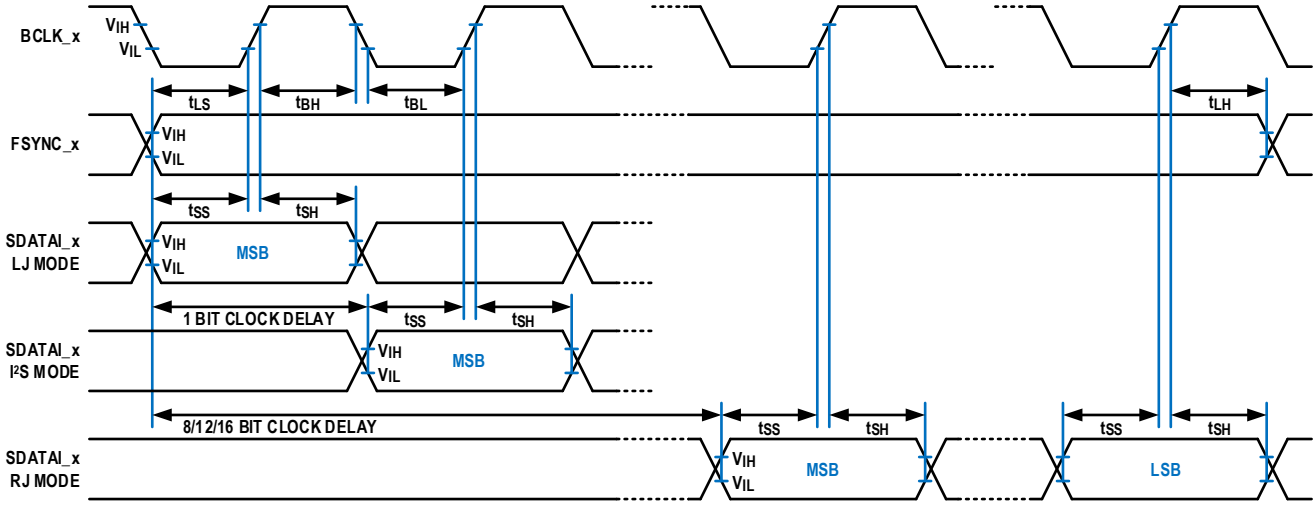


Figure 3. Serial Audio Data Port Input Timing (Slave Mode, Bit Clock Rising Active Edge)

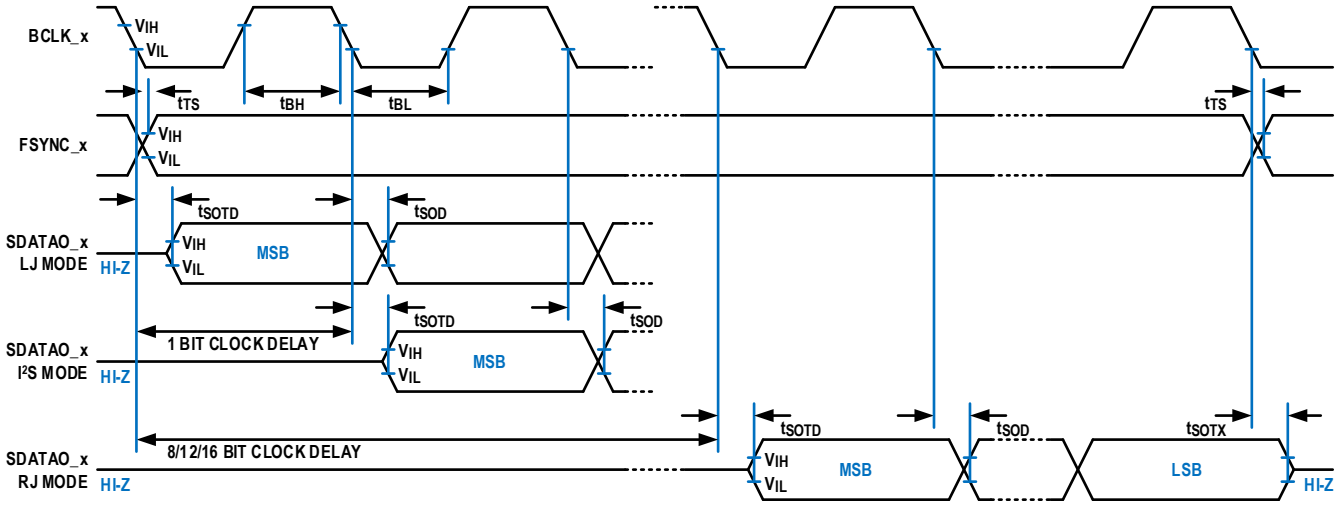


Figure 4. Serial Audio Data Port Output Timing (Master Mode, Bit Clock Rising Active Edge, Tristate Enabled)

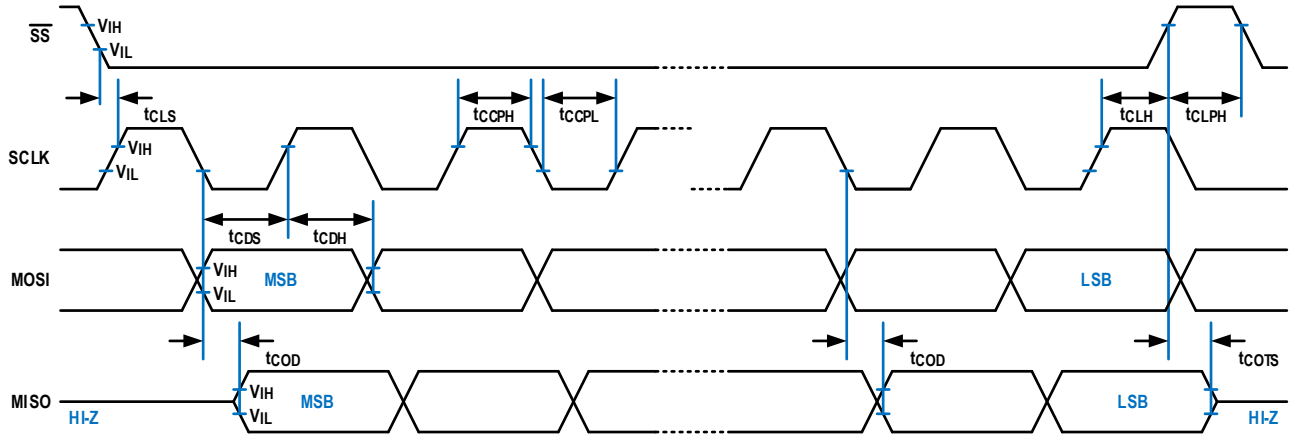


Figure 5. SPI Port Timing Diagram

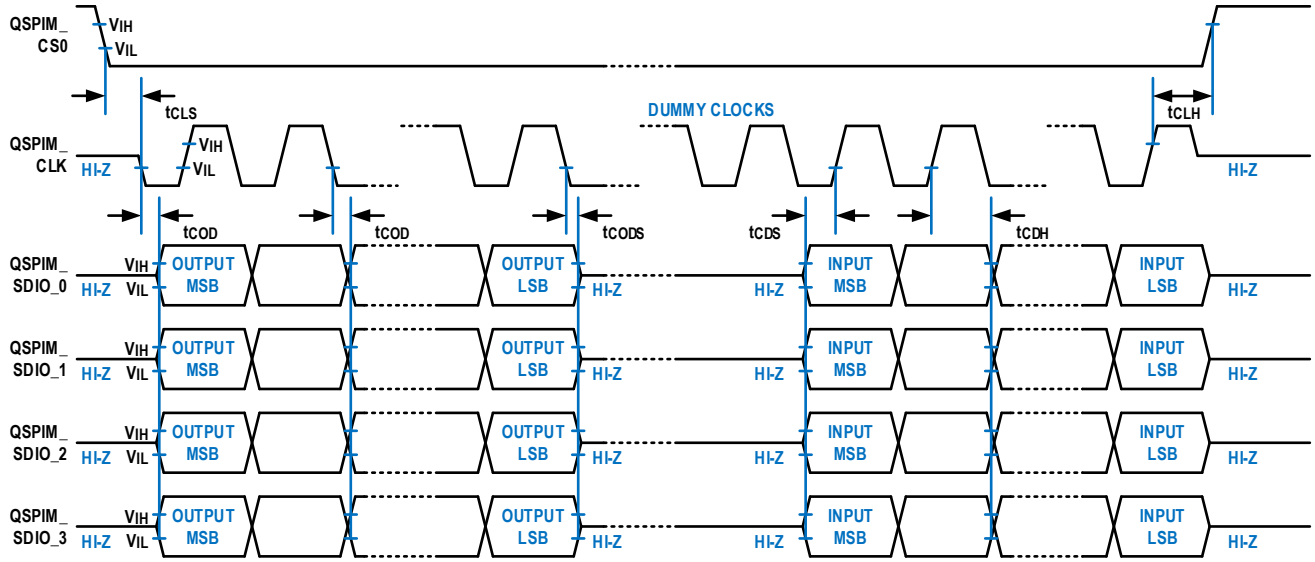


Figure 6. QSPI Master Port Timing Diagram (Default Settings with Tristate Idle)

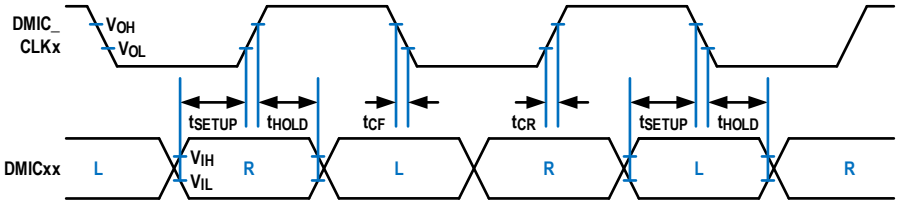


Figure 7. Digital Microphone Timing Diagram

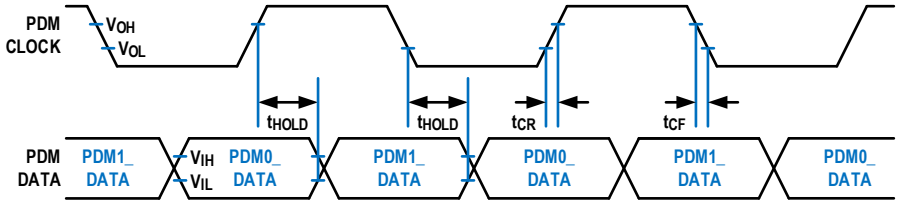


Figure 8. PDM Output Timing Diagram

Power Consumption Specifications

Device Power-Down Modes

Supplies externally connected at V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V, PLL and crystal oscillator disabled.

Table 2. Quiescent Power Consumption for Power-Down Mode Configurations

DEVICE STATE	CONDITIONS	TYPICAL AVDD CURRENT	TYPICAL HPVDD CURRENT	TYPICAL DVDD CURRENT	TYPICAL IOVDD CURRENT	UNIT
Hardware Power-Down	$\overline{PD}$ pin low	0.52	0.8	30.2	0.02	µA
Software Power-Down	$\overline{PD}$ pin high, POWER_EN = 0, no keep-alive modes enabled	1.08	1.35	31.17	0.02	µA
Software Power-Down with Common-Mode Keep Alive Set	$\overline{PD}$ pin high, POWER_EN = 0, CM_KEEP_ALIVE = 1, KEEP_MEM = 0	63.92	1.35	32.76	0.02	µA
Software Power-Down with Common-Mode, FastDSP/HiFi 3z Memory Keep Alive Set	$\overline{PD}$ pin high, POWER_EN = 0, CM_KEEP_ALIVE = 1, KEEP_MEM = 1	69.93	1.35	32.78	0.02	µA

Power Management Mode Configurations

Configuration models a typical active noise canceling (ANC) use case with different analog power mode settings. External supplies are V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V and V_{DVDD} = 0.9V. PLL enabled with f_{MCLK} = 24.576MHz (crystal amp enabled). 3 ADC inputs with PGAs in single-ended mode with channels 0 and 1 set to f_S = 384kHz and channel 2 set to f_S = 48kHz. 2 interpolator and decimator channels. FastDSP core at f_S = 384kHz, FDSP_SPEED = 0 (24.576MHz), and 64 instructions. HiFi 3z core disabled. All biquad filters are set to 27-bit precision. DAC to Class-D amp output channel set to f_S = 384kHz with a 16Ω load. Single serial audio data port in slave mode for input and output with 1 input and 2 output ASRC channels. Quiescent current state (zero code or no signal input to all audio channels).

Table 3. Quiescent Power Consumption Comparison for Power Management Modes

POWER MODE	POWER MANAGEMENT DEVICE SETTINGS	I_{DVDD} (mA)	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{IOVDD} (mA)	TOTAL POWER (mW)	ADC A-wt DR (dB)	ADC THD+N (dB)[1]	Class-D A-wt DR (dB)	Class-D THD+N (dB)[1]
Normal Power Mode	ADC_IBIAS: 0x000, ADC_LP_MODE: 0, DAC_IBIAS: 0x00, DAC_PWR_MODE: 0x00, ASRCI_LPM1: 0, ASRCI_LPM2: 0, PGA_IBIAS: 0, ASRCO_LPM1: 0, ASRCO_LPM2: 0	10.141	1.307	0.747	0.693	14.07	100.0	-90.0	110.0	-90.9
Power-Savings Mode	ADC_IBIAS: 0x010, ADC_LP_MODE: 1, DAC_IBIAS: 0x01, DAC_PWR_MODE: 0x01, ASRCI_LPM1: 1, ASRCI_LPM2: 0, PGA_IBIAS: 1, ASRCO_LPM1: 1, ASRCO_LPM2: 0	9.931	1.172	0.735	0.709	13.65	98.0	-86.3	112.4	-90.6
Extreme Power-Savings Mode	ADC_IBIAS: 0x001, ADC_LP_MODE: 1, DAC_IBIAS: 0x01, DAC_PWR_MODE: 0x10, ASRCI_LPM1: 0, ASRCI_LPM2: 1, PGA_IBIAS: 0x10, ASRCO_LPM1: 0, ASRCO_LPM2: 1	9.869	1.083	0.675	0.71	13.324	97.9	-85.6	112.4	-90.8

[1] THD+N ratio is measured at f_{IN} = 1kHz with a -1dBFS output for ADC input channels and at f_{IN} = 1kHz with 50mW into 16Ω for Class-D amplifier.

Typical Application Use Case Configurations

Supplies are externally connected at V_{AVDD} = V_{HPVDD} = V_{IOVDD} = 1.8V. PLL enabled with master clock = 24.576MHz (crystal oscillator enabled). PGAs enabled for ADC inputs with channels 0 and 1 set to Fs = 384kHz and channel 2 set to Fs = 48kHz. FastDSP core running at Fs = 384kHz and FDSP_SPEED = 0 (24.576MHz) if FDSP instructions < 64. Otherwise, FDSP_SPEED = 1. HiFi 3z core running at Fs = 48kHz. FDSP biquad filters are 54-bit precision. P-product biquad filters used in HiFi 3z. DAC to Class-D amp output channel is set to Fs = 48kHz with DAC_LPM = 1 and a headphone load of 16Ω. SPT0 and SPT1 are enabled, with clocks as inputs.

Table 4. Quiescent Power Consumption Comparison for Power Management Modes

DVDD (V)	DAC	ADC	DMIC	ASRCI/A SRCO	FINT/ FDEC	HiFi 3z MIPS	FastDSP Inst.	I_{DVDD} (mA)	I_{AVDD} (mA)	I_{HPVDD} (mA)	I_{IOVDD} (mA)	TOTAL POWER (mW)
0.9	1	0	0	1/0	0	0	0	4.196	0.071	0.747	0.492	**6.1344**
0.9	1	2	0	1/0	0	0	32	7.22	0.816	0.747	0.492	**10.197**
0.9	1	3	0	1/2	2/2	0	64	10.456	0.967	0.747	0.638	**13.644**
0.9	1	3	0	1/2	2/2	<1	32	8.829	0.967	0.747	0.638	**12.1797**
0.9	1	3	0	1/2	2/2	24	32	14.62	0.967	0.747	0.638	**17.3916**
0.9	1	3	0	1/2	2/2	40	64	20.7	0.967	0.747	0.638	**22.8636**
0.9	1	3	4	1/2	4/4	40	96	23.71	0.967	0.747	0.855	**25.9632**
0.9	1	3	4	1/2	4/4	40	128	26.29	0.967	0.747	0.855	**28.2852**
1.1	1	3	4	1/2	4/4	100	96	48.87	0.967	0.747	0.855	**58.3812**
1.1	1	3	4	1/2	4/4	100	128	52.41	0.967	0.747	0.855	**62.2752**

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C unless otherwise specified.

Table 5. Absolute Maximum Ratings

PARAMETER	RATING
Power Supply (AVDD, HPVDD IOVDD)	-0.3V to +1.98V
Digital Supply (DVDD)	-0.3V to +1.98V
Input Current (Except Supply Pins)	±20mA
Analog Input Voltage (Signal Pins)	-0.3V to V_{AVDD} + 0.3V
Digital Input Voltage (Signal Pins)	-0.3V to V_{IOVDD} + 0.3V
Operating Temperature Range (Case)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required. θ_{JA} and θ_{JC} are determined using JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 6. Thermal Resistance

PACKAGE TYPE	θ_{JA}[1]	θ_{JC}[1]	UNIT
CB-77-1	17	0.3	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with two thermal vias. See JEDEC JESD-51.

Electrostatic Discharge (ESD)

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD-protected area-only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Table 7. ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	3A
CDM	±1000	C5

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

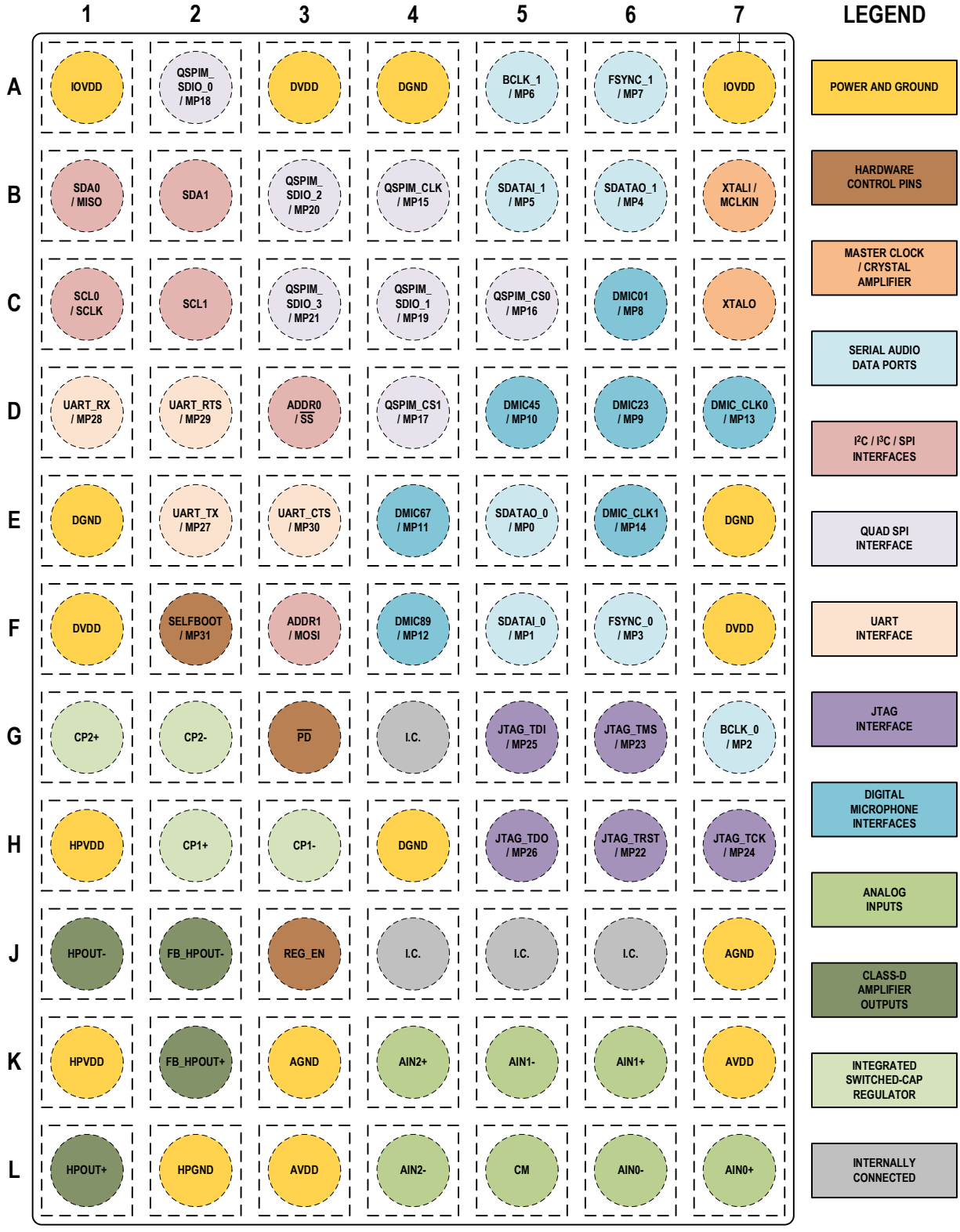


Figure 9. Top View Ball Configuration (View from Top-Side)

Table 8. Pin Function Descriptions

PIN	NAME	DESCRIPTION	Type
A1	IOVDD	Digital Input and Output Pin Supply. The digital output pins are supplied from IOVDD, and this pin sets the highest input voltage seen on the digital input pins. The current draw of this pin is variable because the current is dependent on the loads of the digital outputs. Decouple each IOVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
A2	QSPIM_ SDIO_0 / MP18	Quad Master SPI Data I/O (QSPIM_SDIO_0) or Multipurpose I/O 18	D_IO
A3	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
A4	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
A5	BCLK_1 / MP6	Serial Audio Data Port 1 Bit Clock or Multipurpose I/O 6	D_IO
A6	FSYNC_1 / MP7	Serial Audio Port 1 Frame Sync/Left Right Clock (FSYNC_1) or Multipurpose I/O 7	D_IO
A7	IOVDD	Digital Input and Output Pin Supply. The digital output pins are supplied from IOVDD, and this pin sets the highest input voltage seen on the digital input pins. The current draw of this pin is variable because the current is dependent on the loads of the digital outputs. Decouple each IOVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
B1	SDA0/MISO	I^2C Data 0 I/O (SDA0) or SPI Data Output (MISO). In I^2C mode, this pin is a bidirectional open-drain input. The line connected to this pin must have a 2.0kΩ pullup resistor. In SPI mode, the SPI data output is used for reading back registers and memory locations. This pin is tri-stated when an SPI read is not active.	D_IO
B2	SDA1	I^2C/I^3C Master Data 1 I/O	D_IO
B3	QSPIM_ SDIO_2 / MP20	Quad Master SPI Data I/O 2 (QSPIM_SDIO2) or Multipurpose I/O 20	D_IO
B4	QSPIM_ CLK / MP15	Quad Master SPI Clock (QSPIM_CLK) or Multipurpose I/O 15	D_IO
B5	SDATAI_1 / MP5	Serial Audio Port 1 Input Data (SDATAI_1) or Multipurpose I/O 5	D_IO
B6	SDATAO_1 / MP4	Serial Audio Port 1 Output Data (SDATAO_1) or Multipurpose I/O 4	D_IO
B7	XTALI / MCLKIN	Crystal Clock Input (XTALI)/Master Clock Input (MCLKIN)	D_IN

C1	SCL0 / SCLK	I^2C Clock 0 (SCL0) or SPI Clock (SCLK). In I^2C mode, this pin is an open-collector input. When the device is in self-boot mode, this pin is an open-collector output (I^2C master). In I^2C mode, the line connected to this pin must have a 2.0kΩ pullup resistor. In SPI mode, this pin is the SPI Clock. This pin can either run continuously or be gated off between SPI transactions.	D_IN
C2	SCL1	I^2C/I^3C Master Clock Output	D_O
C3	QSPIM_ SDI0_3 / MP21	Quad Master SPI Data I/O 3 (QSPIM_SDIO3) or Multipurpose I/O 21	D_IO
C4	QSPIM_ SDIO_1 / MP19	Quad Master SPI Data I/O 1 (QSPIM_SDIO1) or Multipurpose I/O 19	D_IO
C5	QSPIM_CS0 / MP16	Quad Master SPI Chip Select 0 (QSPIM_CS0) or Multipurpose I/O 16	D_IO
C6	DMIC01 / MP8	Digital Microphone Stereo Input 0 and 1 (DMIC01) or Multipurpose I/O 8	D_IO
C7	XTALO	Crystal Clock Amp Output. This pin is the output of the crystal amplifier. Do not use this pin to provide a clock to other ICs in the system.	A_OUT
D1	UART_RX / MP28	UART Port Data Receiver Input (UART_RX) or Multipurpose I/O 28	D_IO
D2	UART_RTS / MP29	UART Port Flow Control Ready to Send Output (UART_RTS) or Multipurpose I/O 29	D_IO
D3	ADDR0 / $\overline{SS}$	I^2C Address 0 (ADDR0) or SPI Latch Signal ($\overline{SS}$). In I^2C mode, ADDR0 and ADDR1 are used to select one of four I^2C address options. In SPI mode, this pin must go low at the beginning of a transaction and high at the end of a transaction. Each SPI transaction may take a different number of SCLK cycles to complete, depending on the address and read/write bit that is sent at the beginning of the SPI transaction.	D_IN
D4	QSPIM_CS1 / MP17	Quad Master SPI Chip Select 1 (QSPIM_CS1) or Multipurpose I/O 17	D_IO
D5	DMIC45 / MP10	Digital Microphone Stereo Input 4 and 5 (DMIC45) or Multipurpose I/O 10	D_IO
D6	DMIC23 / MP9	Digital Microphone Stereo Input 2 and 3 (DMIC23) or Multipurpose I/O 9	D_IO
D7	DMIC_CLK0 / MP13	Digital Microphone Clock Output 0 (DMIC_CLK0) or Multipurpose I/O 13	D_IO
E1	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
E2	UART_TX / MP27	UART Port Data Transmit Output (UART_TX) or Multipurpose I/O 27	D_IO

E3	UART_CTS / MP30	UART Port Flow Control Clear to Send Input (UART_CTS) or Multipurpose I/O 30	D_IO
E4	DMIC67 / MP11	Digital Microphone Stereo Input 6 and 7 (DMIC67) or Multipurpose I/O 11	D_IO
E5	SDATAO_0 / MP0	Serial Audio Port 0 Output Data (SDATAO_0) or Multipurpose I/O 0	D_IO
E6	DMIC_CLK1 / MP14	Digital Microphone Clock Output 1 (DMIC_CLK1) or Multipurpose I/O 14	D_IO
E7	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
F1	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
F2	SELFBOOT / MP31	Self-Boot Select or Multipurpose I/O 31. Connect this pin to IOVDD through a 100kΩ resistor at power-up to enable the self-boot mode. This pin also outputs the buffered Crystal Oscillator clock by default at the start-up. Otherwise, set this pin to DGND through a 100kΩ resistor. Once the power-up is completed, this pin can be re-configured as Multipurpose I/O 31.	D_IN
F3	ADDR1 / MOSI	I^2C Address 1 (ADDR1) or SPI Data Input (MOSI). In I^2C mode, ADDR0 and ADDR1 are used to select one of four I^2C address options. In SPI mode, the SPI data input is used for writing registers and memory locations.	D_IN
F4	DMIC89 / MP12	Digital Microphone Stereo Input 8 and 9 (DMIC89) or Multipurpose I/O 12	D_IO
F5	SDATAI_0 / MP1	Serial Audio Port 0 Input Data (SDATAI_0)/Multipurpose I/O 1	D_IO
F6	FSYNC_0 / MP3	Serial Audio Port 0 Frame Sync/Left Right Clock (FSYNC_0) or Multipurpose I/O 3	D_IO
F7	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
G1	CP2+	Switched-Cap Regulator Capacitor 2 Positive Connection. Connect a 1µF capacitor between CP2+ and CP2-.	PWR
G2	CP2-	Switched-Cap Regulator Capacitor 2 Negative Connection. Connect a 1µF capacitor between CP2+ and CP2-.	PWR
G3	$\overline{\text{PD}}$	Active Low Power-Down Input. All digital and analog circuits are powered down. The external pulldown resistor to DGND is recommended on this pin to hold the device in power-down mode if the input signal from the system micro-controller is floating while power is applied to the supply pins.	D_IN
G4	I.C.	Internally Connected. Connect to DGND.	DGND

G5	JTAG_TDI / MP25	JTAG Debug Port Data Input (JTAG_TDI) or Multipurpose I/O 25	D_IO
G6	JTAG_TMS / MP23	JTAG Debug Port Master Select (JTAG_TMS) or Multipurpose I/O 23	D_IO
G7	BCLK_0 / MP2	Serial Audio Port 0 Bit Clock (BCLK_0) or Multipurpose I/O 2	D_IO
H1	HPVDD	Headphone Amplifier 1.8V Analog Power Supply. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs. Decouple each HPVDD input to HPGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor to provide the peak current necessary for low frequency signals.	PWR
H2	CP1+	Switched-Cap Regulator Capacitor 1 Positive Connection. Connect a 1µF capacitor between CP1+ and CP1-.	PWR
H3	CP1-	Switched-Cap Regulator Capacitor 1 Negative Connection. Connect a 1µF capacitor between CP1+ and CP1-.	PWR
H4	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
H5	JTAG_TDO / MP26	JTAG Debug Port Data Output (JTAG_TDO) or Multipurpose I/O 26	D_IO
H6	JTAG_TRST / MP22	JTAG Debug Port Reset (JTAG_TRST) or Multipurpose I/O 22	D_IO
H7	JTAG_TCK / MP24	JTAG Debug Port Clock (JTAG_TCK) or Multipurpose I/O 24	D_IO
J1	HPOUT-	Headphone Output Inverted	A_OUT
J2	FB_HPOUT-	Headphone Output Inverted Feedback Signal. Connect close to the inverted side of the headphone load after any filtering components.	A_IN
J3	REG_EN	Regulator Enable. Tie this pin to HPVDD to enable the internal DVDD regulator and tie this pin to ground to disable the regulator.	A_IN
J4	I.C.	Internally Connected. Leave this pin unconnected.	DNC
J5		Internally Connected. Connect to DGND.	DGND
J6		Internally Connected. Leave this pin unconnected.	DNC
J7	AGND	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
K1	HPVDD	Headphone Amplifier 1.8V Analog Power Supply. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs. Decouple each HPVDD input to HPGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor to provide the peak current necessary for low frequency signals.	PWR
K2	FB_HPOUT+	Headphone Output Noninverted Feedback Signal. Connect close to the noninverted side of the headphone load after any filtering components.	A_IN

K3	AGND	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
K4	AIN2+	Analog Input ADC2 Non-Inverting Input	A_IN
K5	AIN1-	Analog Input ADC1 Inverting Input	A_IN
K6	AIN1+	Analog Input ADC1 Non-Inverting Input	A_IN
K7	AVDD	1.8V Analog Supply. Decouple each AVDD input to AGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
L1	HPOUT+	Headphone Output Noninverted	A_OUT
L2	HPGND	Headphone Amplifier and Regulator Ground	PWR
L3	AVDD	1.8V Analog Supply. Decouple each AVDD input to AGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
L4	AIN2-	Analog Input ADC2 Inverting Input	A_IN
L5	CM	Common-Mode Reference Output. The CM output is fixed at 0.85V nominal. Connect a 10µF and 0.1µF decoupling capacitor between this pin and AGND to reduce crosstalk between the ADC channels. The material of the capacitors is not critical. This pin can supply a reference bias to external analog circuits as long as they are not drawing current from the CM output (Example: high impedance input of an external amplifier).	A_OUT
L6	AIN0-	Analog Input ADC0 Inverting Input	A_IN
L7	AIN0+	Analog Input ADC0 Non-Inverting Input	A_IN

TYPICAL PERFORMANCE CHARACTERISTICS

See the *Specifications* table for the overall global conditions.

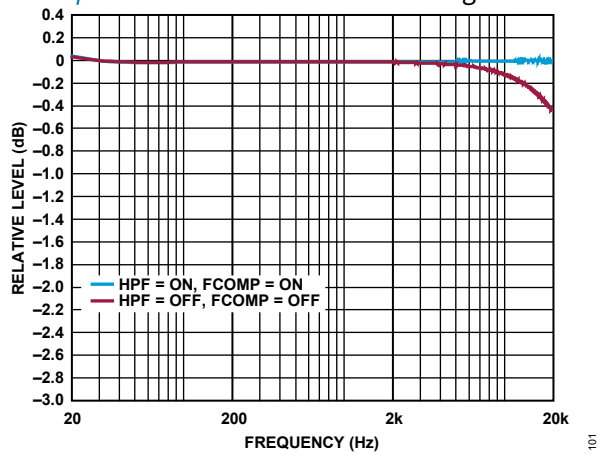


Figure 10. Frequency Response, Fs = 48kHz, -20dBV Input, Signal Path = AINx to SDATAO_x, No PGA

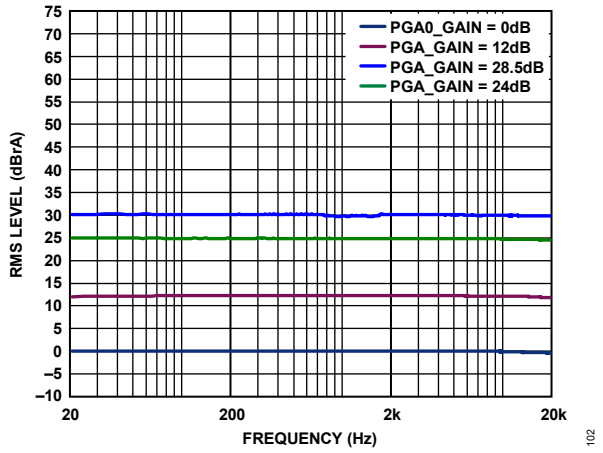


Figure 11. Frequency Response, Fs = 48kHz, Signal Path = AINx to SDATAO_x

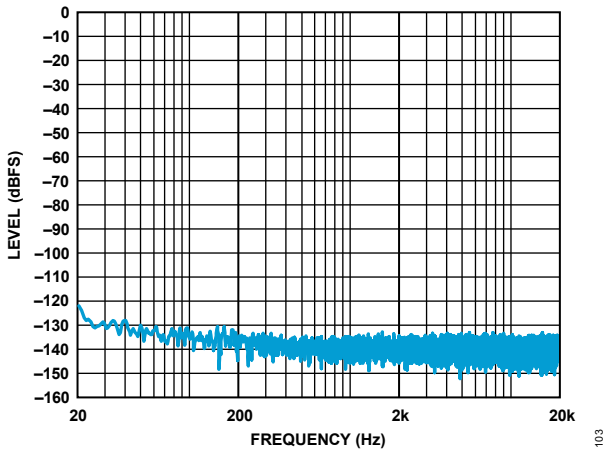


Figure 12. FFT, No Signal, Fs = 48kHz, Signal Path = AINx to SDATAO_x, No PGA

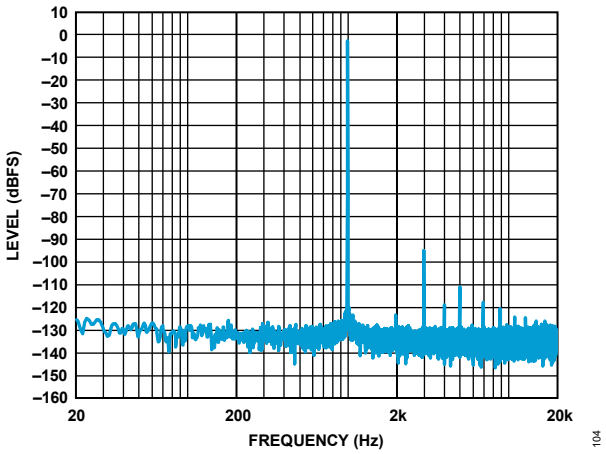


Figure 13. FFT, -7dBV Input, Fs = 48kHz, Signal Path = AINx to SDATAO_x, No PGA

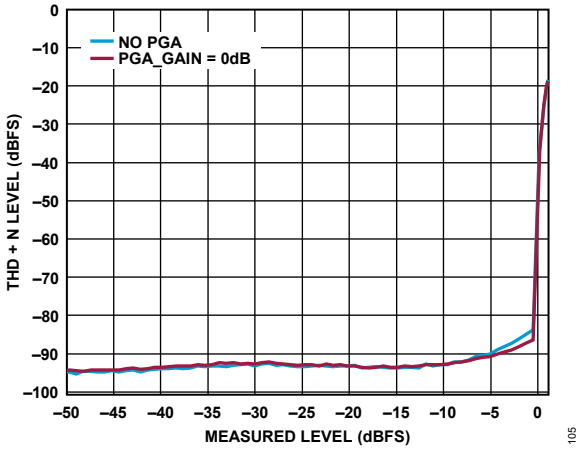


Figure 14. THD + N Level vs. Amplitude, Fs = 48kHz, Signal Path = AINx to SDATAO_x

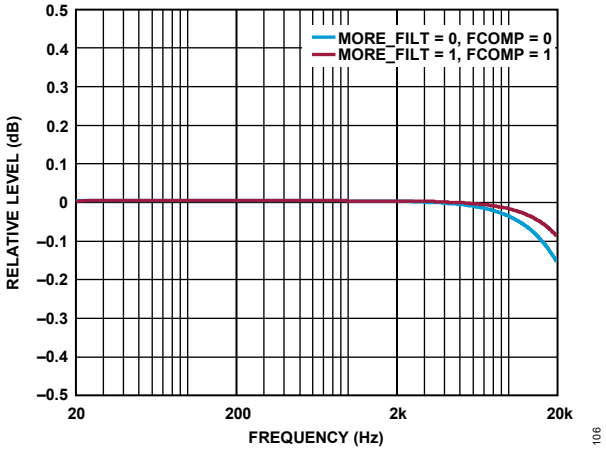


Figure 15. Frequency Response, Fs = 48kHz, Signal Path = SDATAI_x to PDMOUT

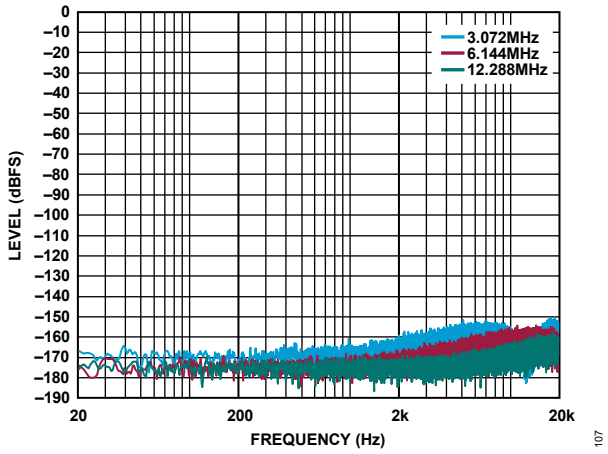


Figure 16. FFT, No Signal, Fs = 48kHz, Signal Path = SDATAI_x to FDSP to PDMOUT

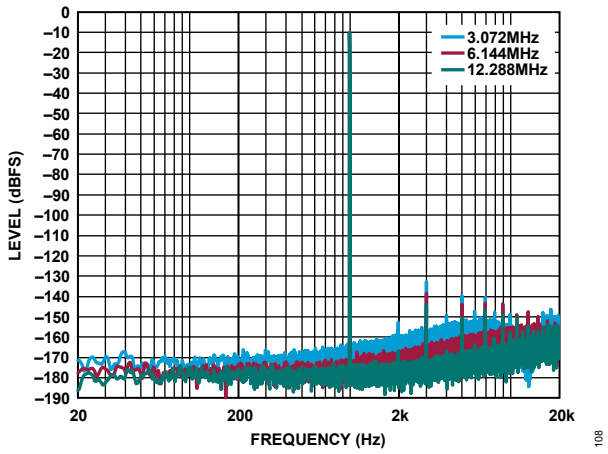


Figure 17. FFT, -10dBFS input, Fs = 48kHz, Signal Path = SDATAI_x to FDSP to PDMOUT

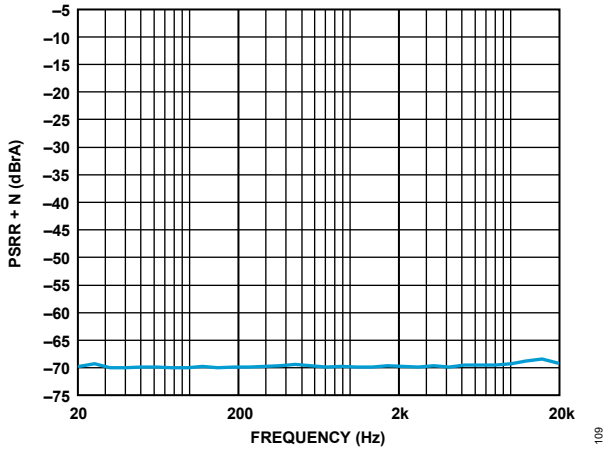


Figure 18. PSRR + N, Signal Path = AINx to SDATAO_x, Fs = 48kHz, 100mVp-p Ripple on AVDD, No PGA

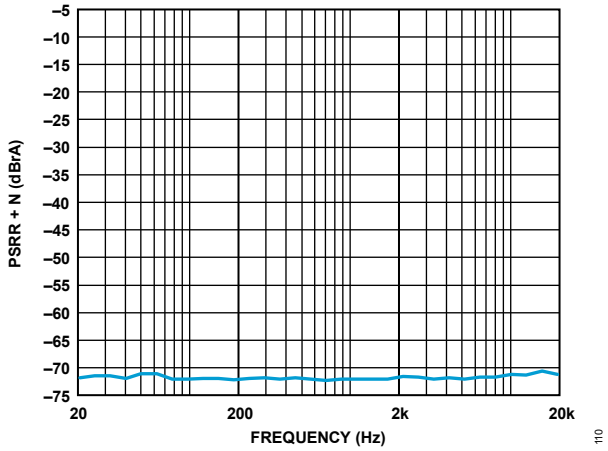


Figure 19. PSRR + N, Signal Path = AINx to SDATAO_x, Fs = 48kHz, 100mVp-p Ripple on AVDD, PGA = 0dB Gain

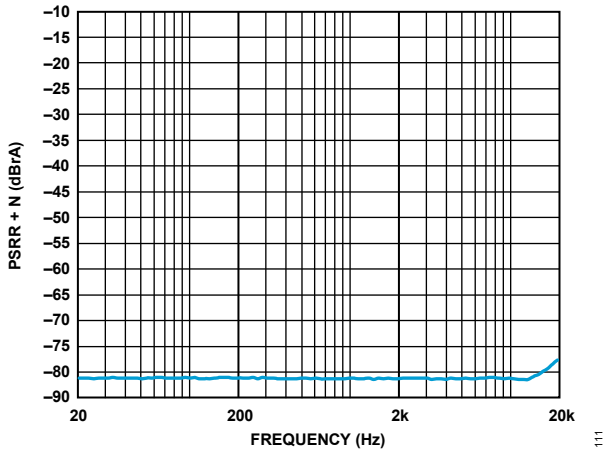


Figure 20. PSRR + N, Signal Path = SDATAI_x to HPOUT, Fs = 48kHz, 100mVp-p Ripple on HPVDD

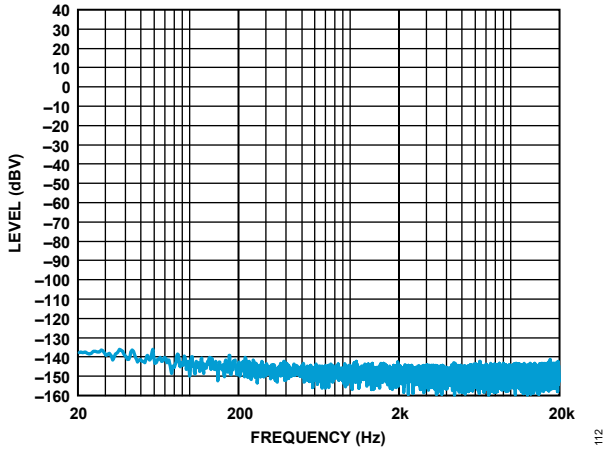


Figure 21. FFT, No Signal, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT, 16Ω Load

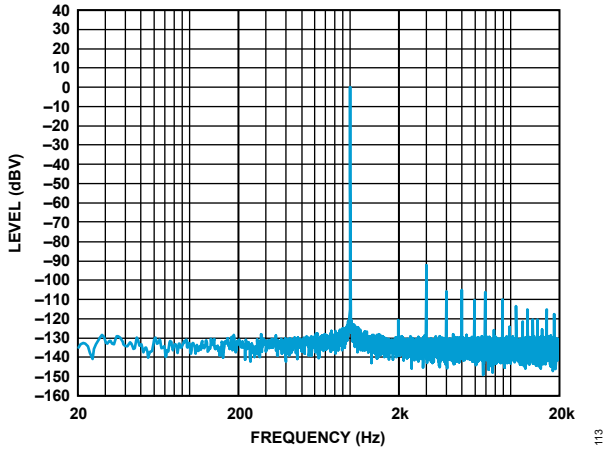


Figure 22. FFT, -1dBFS Input, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT, 32Ω Load

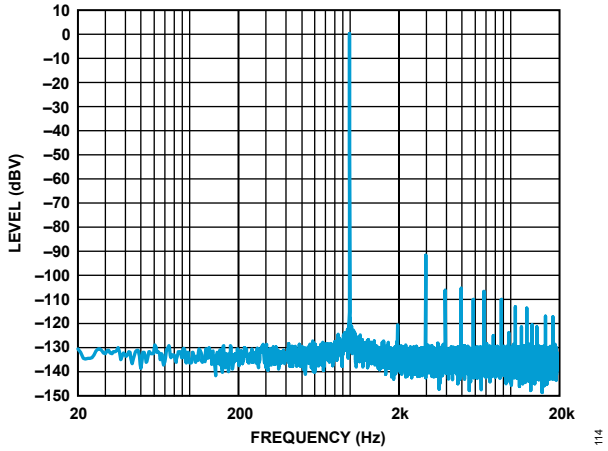


Figure 23.FFT, -1dBFS Input, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT, 24Ω Load

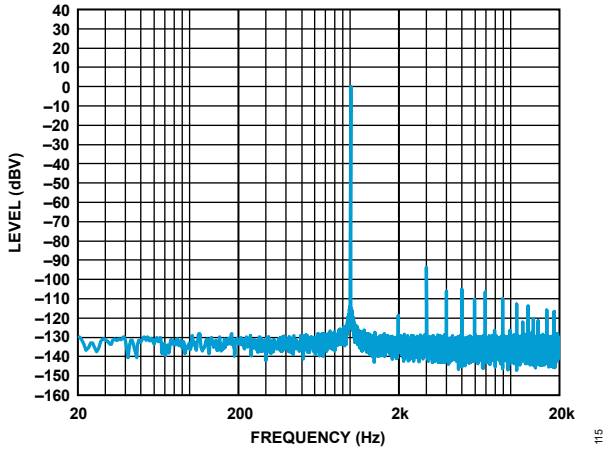


Figure 24. FFT, -1dBFS input, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT, 16Ω Load

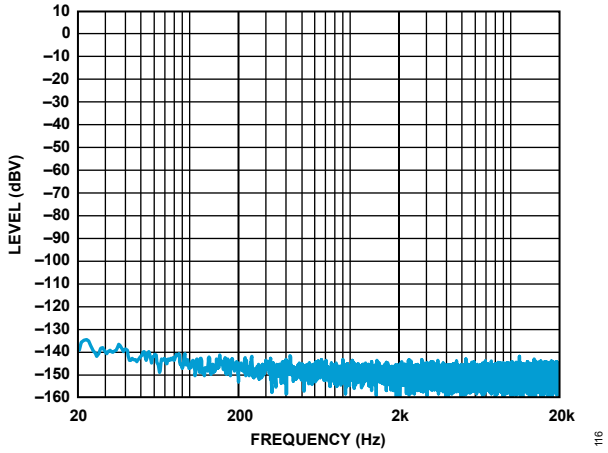


Figure 25. FFT, No Signal, Fs = 768kHz, Signal Path = SDATAI_x to FINT to FDSP to HOUT, 16Ω Load

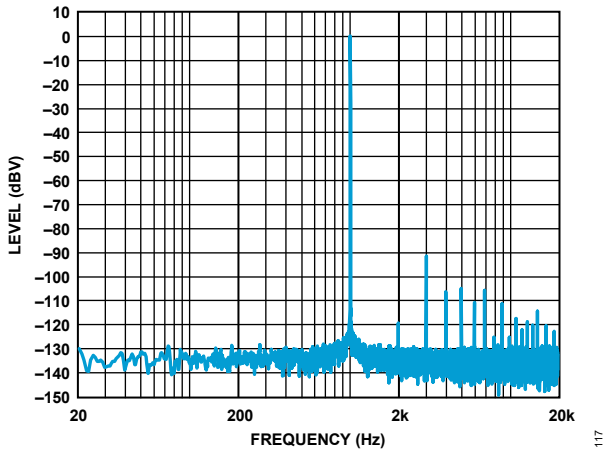


Figure 26. FFT, -1dBFS Input, Fs = 768kHz, Signal Path = SDATAI_x to FINT to FDSP to HOUT, 16Ω Load

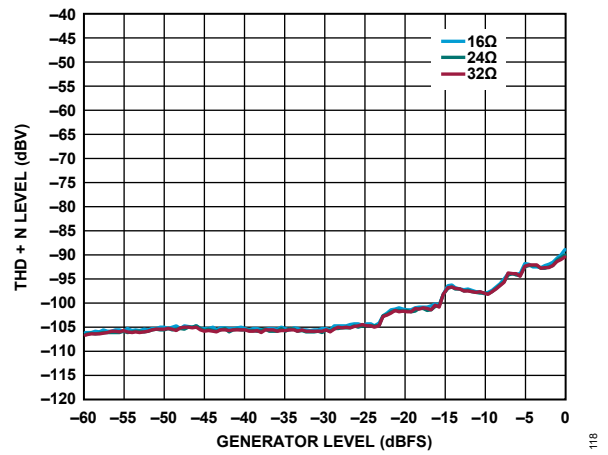


Figure 27. THD + N Level vs. Input Amplitude, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT

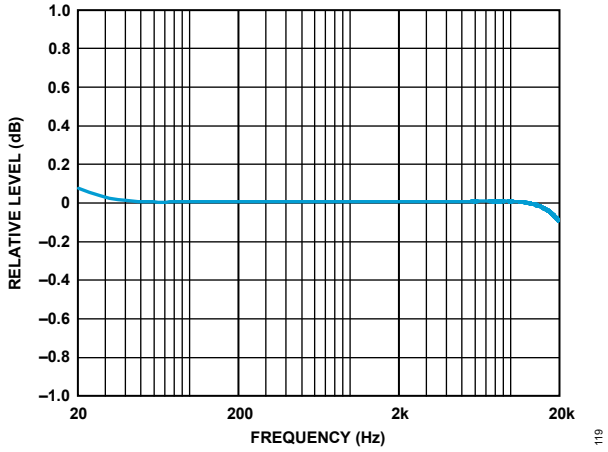


Figure 28. Relative Level vs. Frequency, Fs = 48kHz, Signal Path = SDATAI_x to HPOUT, 16Ω Load

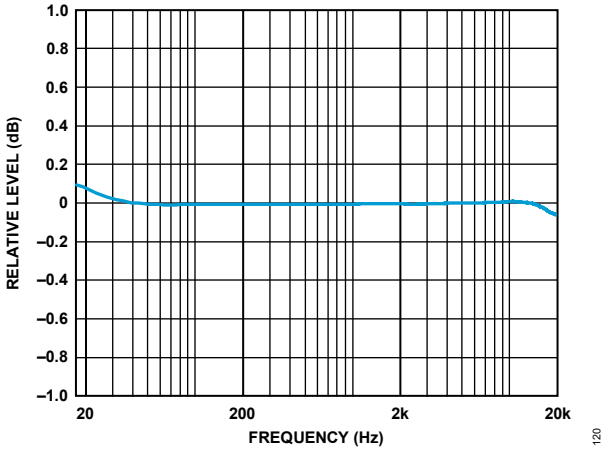


Figure 29. Relative Level vs. Frequency, Fs = 768kHz, Signal Path = SDATAI_x to FINT to FDSP to HPOUT, 16Ω Load

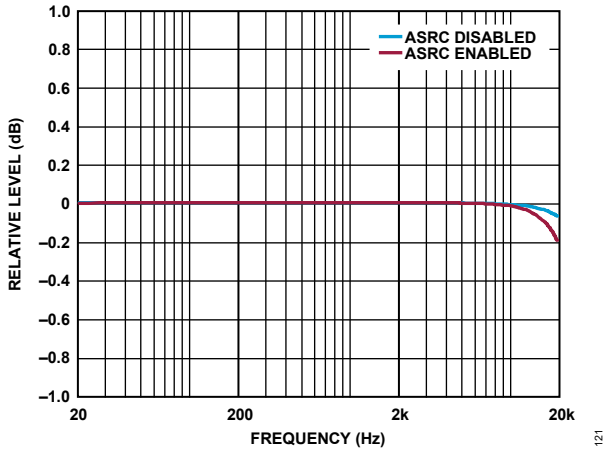


Figure 30. Relative Level vs. Frequency, Fs = 48kHz Except FDSP = 768kHz, Signal Path = SDATAI_x to ASRCI to FINT to FDSP to FDEC to ASRCO to SDATAO_x

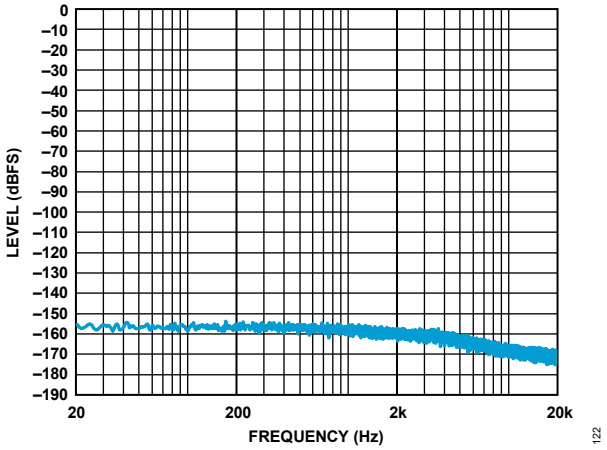


Figure 31. FFT, No Signal, Fs = 48kHz Except FDSP = 768kHz, Signal Path = SDATAI_x to ASRCI to FINT to FDSP to FDEC to ASRCO to SDATAO_x

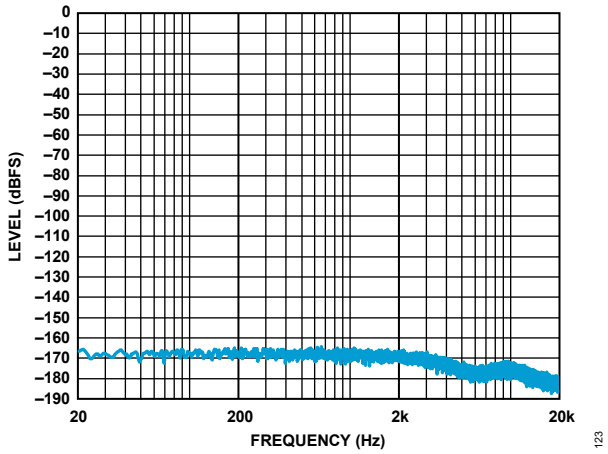


Figure 32. FFT, No Signal, Fs = 48kHz Except FDSP = 768kHz, Signal Path = SDATAI_x to FINT to FDSP to FDEC to SDATAO_x

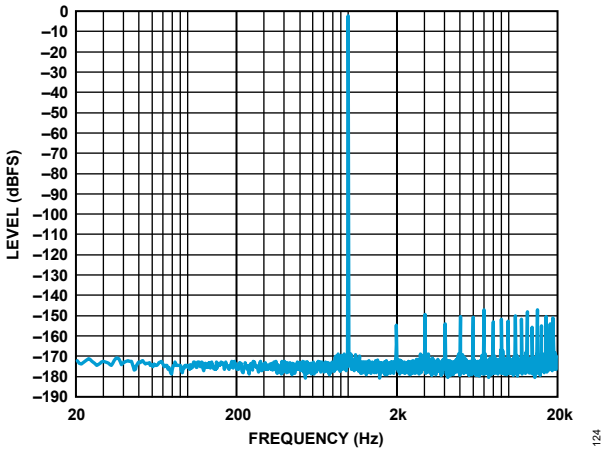


Figure 33. FFT, -1dBFS, Fs = 48kHz Except FDSP = 768kHz, Signal Path = SDATAI_x to ASRCI to FINT to FDSP to FDEC to ASRCO to SDATAO_x

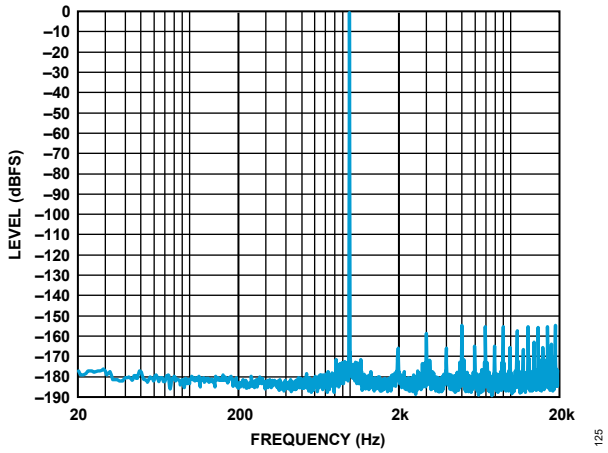


Figure 34. FFT, -1dBFS, Fs = 48kHz Except FDSP = 768kHz, Signal Path = SDATAI_x to FINT to FDSP to FDEC to SDATAO_x

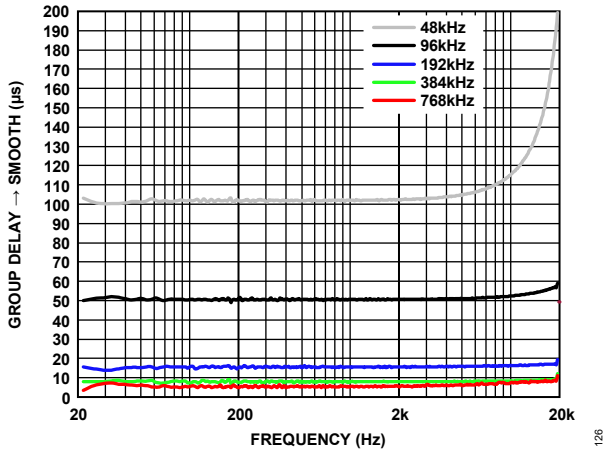


Figure 35. Group Delay vs. Frequency, Fs = 48kHz to 768kHz, Signal Path = AINx to FDSP to HPOUT

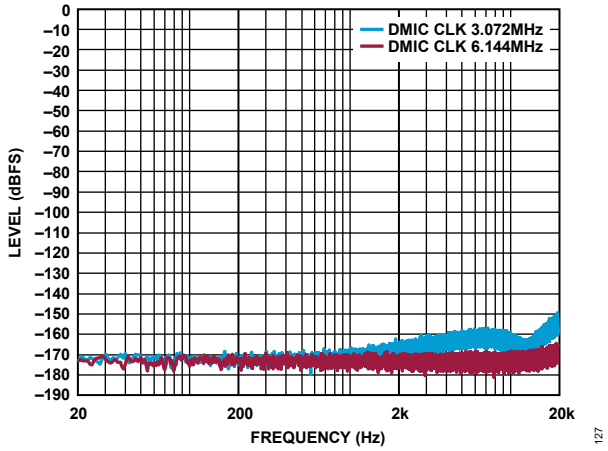


Figure 36. FFT, No Signal, Fs = 48kHz, Signal Path = DMICxx to SDATAO_x

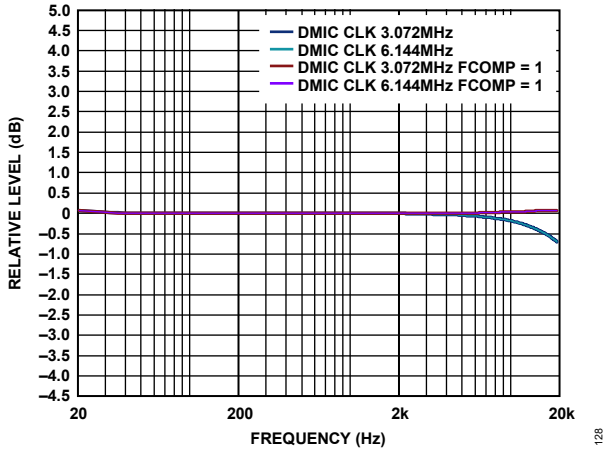


Figure 37. Relative Level vs. Frequency, Fs = 48kHz, Signal Path = DMICxx to SDTAO_x

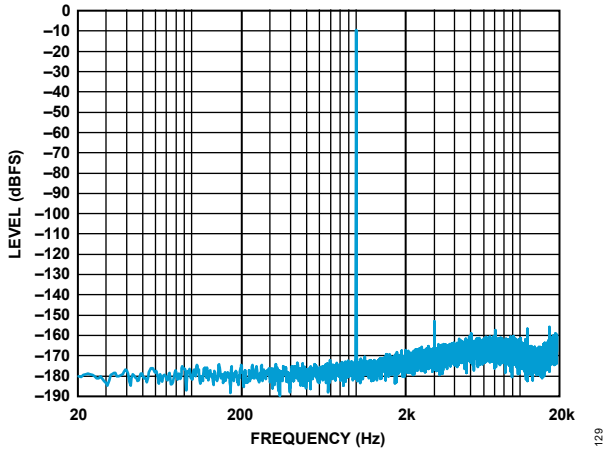


Figure 38. FFT, -10dBFS Input, DMIC_CLKx = 3.072MHz, Fs = 48kHz, Signal Path = DMICx to SDATAO_x

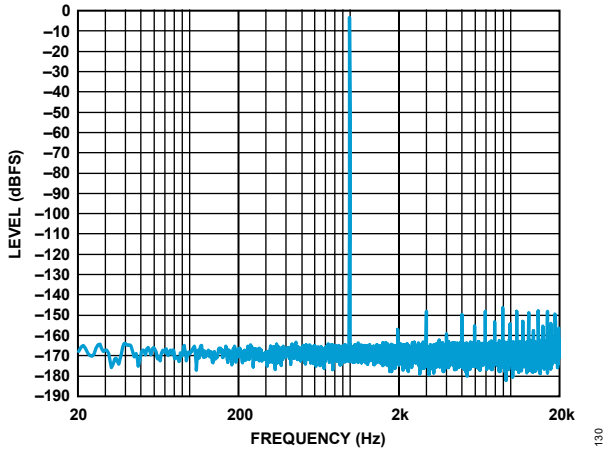


Figure 39. FFT, -10dBFS Input, DMIC_CLKx = 6.144MHz, Fs = 48kHz, Signal Path = DMICx to SDATAO_x

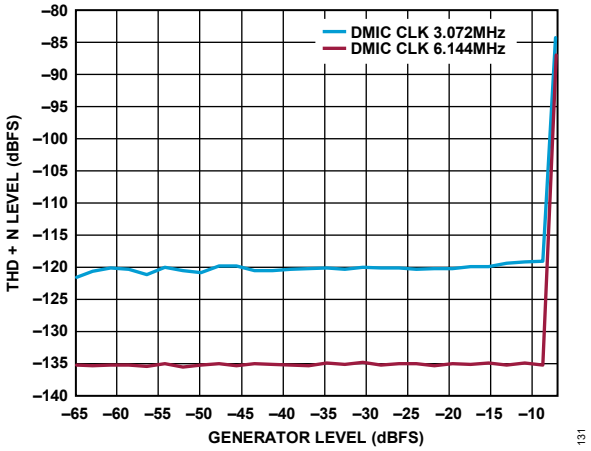


Figure 40. THD + N Level vs. Amplitude, -10dBFS, Fs = 48kHz, Signal Path = DMICxx to SDATAO_x

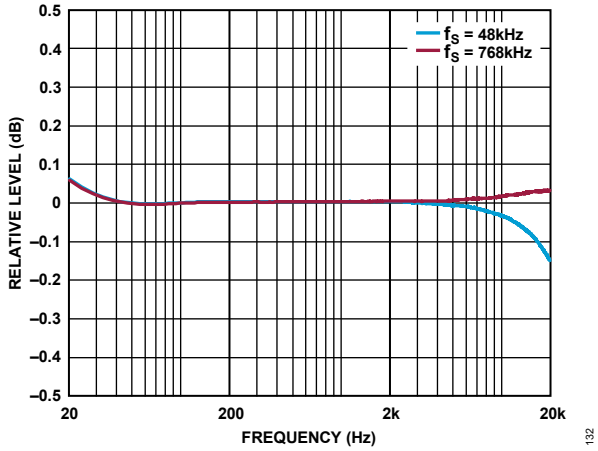


Figure 41. Relative Level vs. Frequency, Signal Path = AINx to HPOUT, 16Ω Load

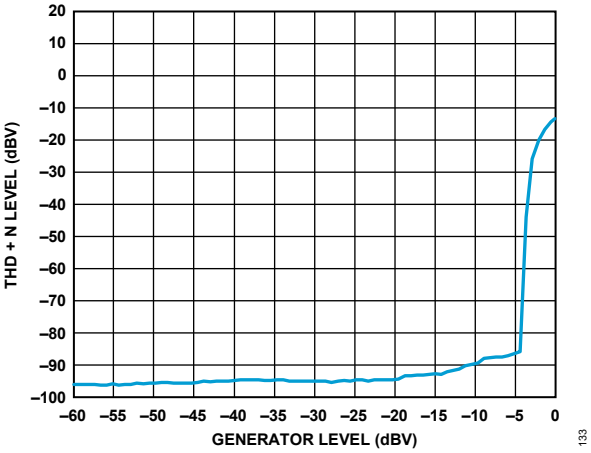


Figure 42. THD + N Level vs. Amplitude, Fs = 48kHz to 768kHz, Signal Path = AINx to HPOUT, 16Ω Load

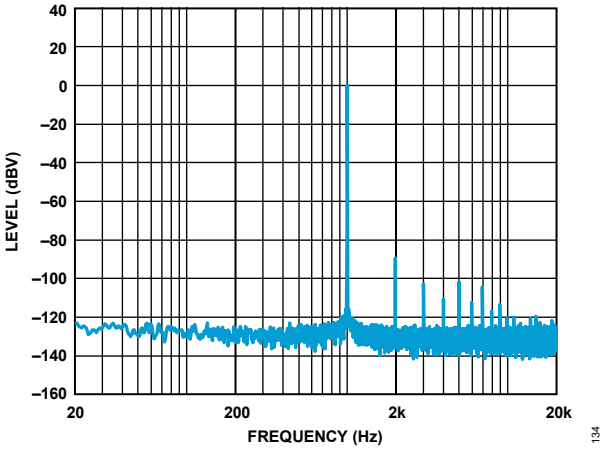


Figure 43. FFT, -7dBV Input, Fs = 48kHz to 768kHz, Signal Path = AINx to HPOUT, 16Ω Load

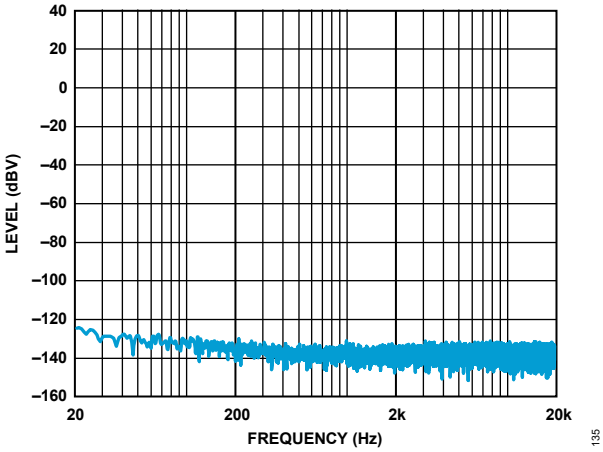


Figure 44. FFT, No Signal, Fs = 48kHz to 768kHz, Signal Path = AINx to HPOUT, 16Ω Load

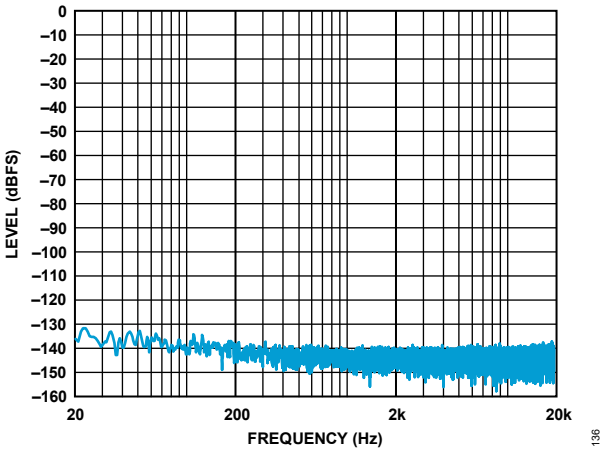


Figure 45. FFT, No Signal, Fs = 48kHz, Signal Path = AINx to SDATAO_x, No PGA (ADC Differential Mode)

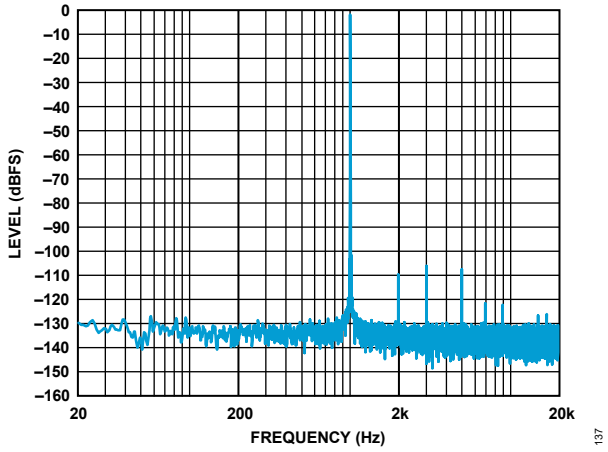


Figure 46. FFT, -1dBV Input, Fs = 48kHz, Signal Path = AINx to SDATAO_x, No PGA (ADC Differential Mode)

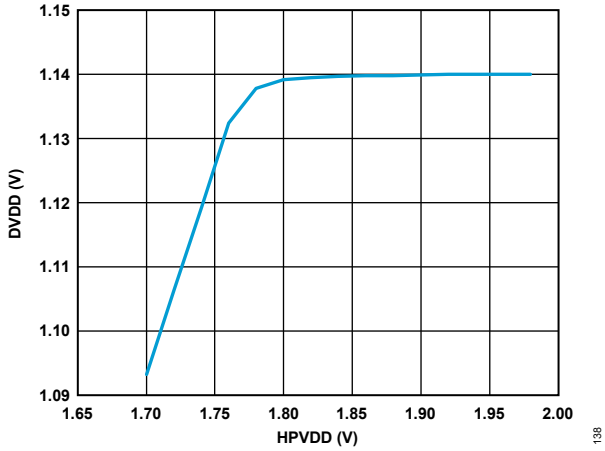


Figure 47. Integrated Switched-Cap DVDD Line Regulation vs. HPVDD Operating Range

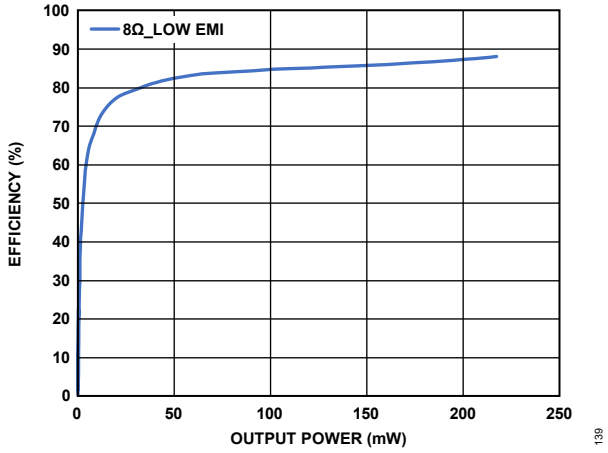


Figure 48. Efficiency, Signal Path = SPTx to HPOUT, 8Ω Load

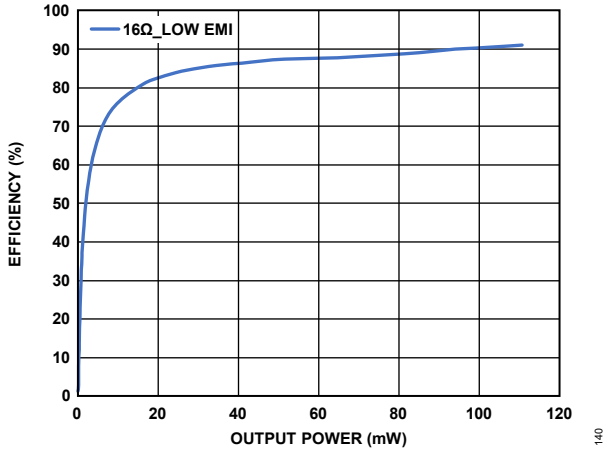


Figure 49. Efficiency, Signal Path = SPTx to HPOUT, 16Ω Load

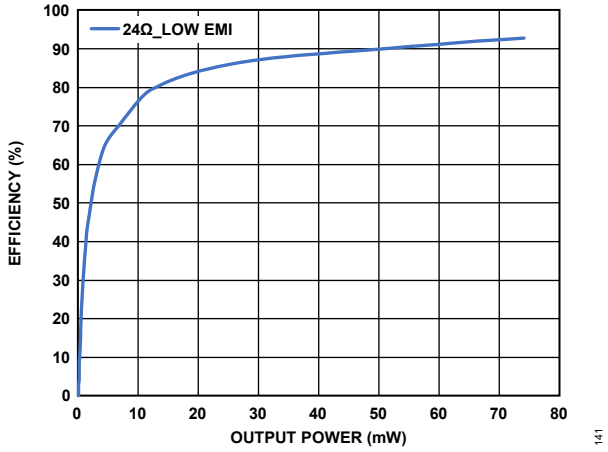


Figure 50. Efficiency, Signal Path = SPTx to HPOUT, 24Ω Load

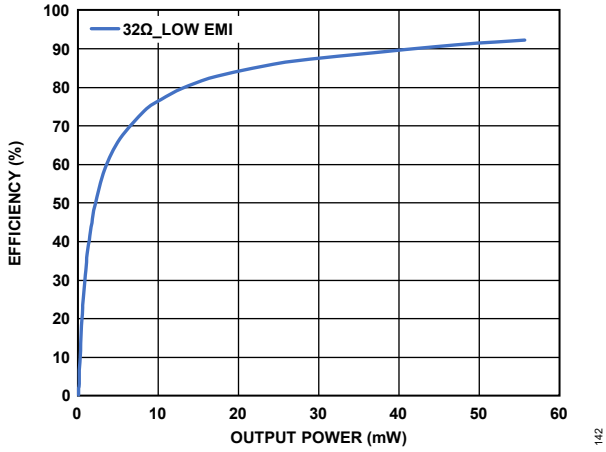


Figure 51. Efficiency, Signal Path = SPTx to HPOUT, 32Ω Load

SYSTEM BLOCK DIAGRAM

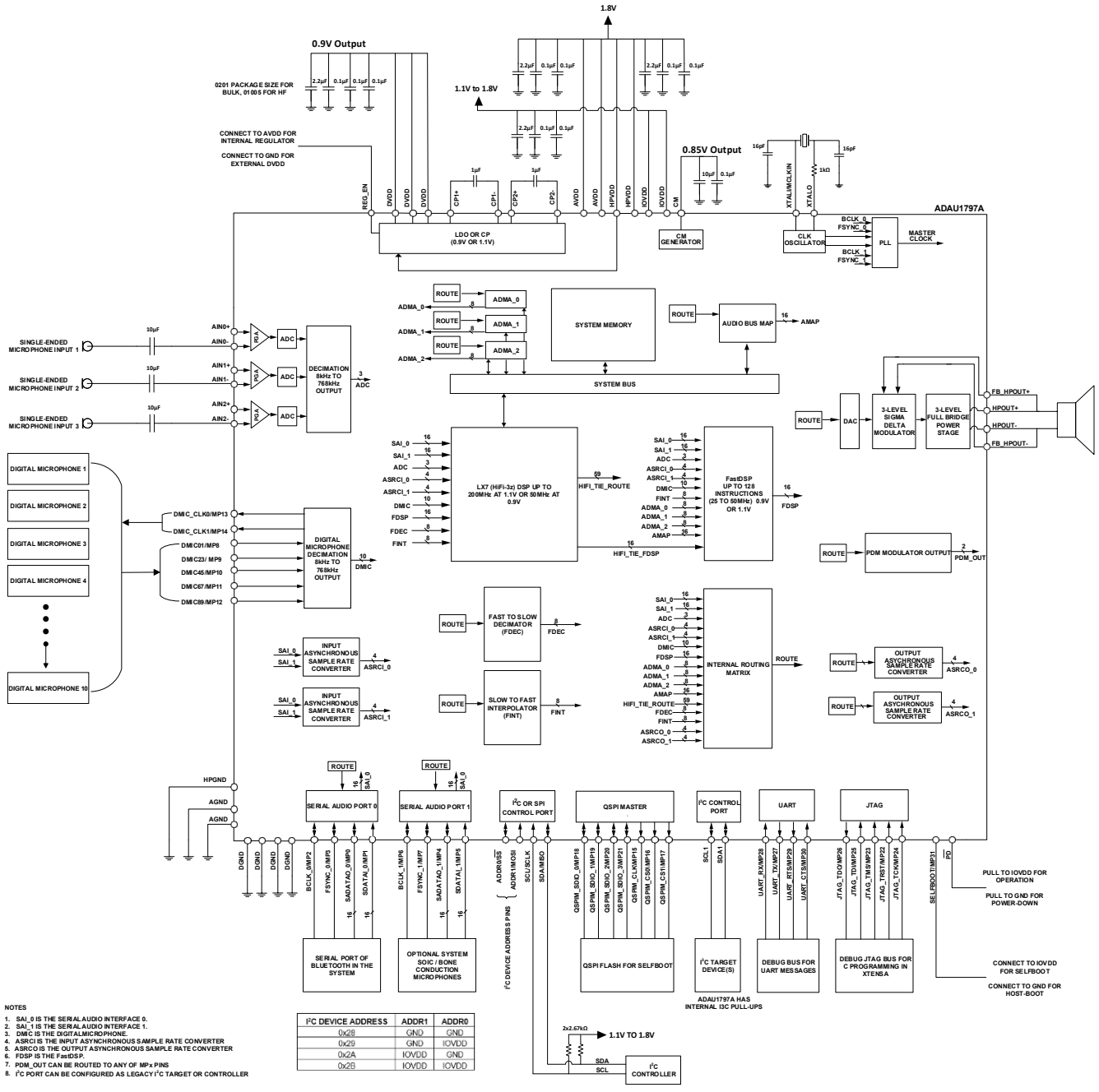


Figure 52. System Block Diagram (Analog Microphones, Self-Boot Mode)

THEORY OF OPERATION

The device is a low power, high-performance audio codec with dual audio processing cores. The device features both a low power HiFi 3z audio DSP core and a low latency optimized FastDSP core. The dual audio DSP cores paired with the low power, high-performance data converters make the device ideal for applications such as noise cancellation, transparency, personal sound amplification, and voice processing.

The device provides three low power, low-noise analog input channels each with a high-performance ADC. The flexible analog inputs accept both line-level and analog microphone input sources. Each analog input can be configured as a single-ended, differential, or pseudo-differential input with or without a programmable gain amplifier (PGA). In addition, the device also supports up to ten digital microphone input channels with two independent digital microphone output clock sources.

The analog output channel includes a high-performance DAC and a low-noise, high-efficiency differential headphone amplifier. The driver is an ultra-low power, pulse density, closed-loop, filter-less, sigma-delta Class-D amplifier that is capable of driving speakers with a 6Ω impedance or higher.

The input ADCs and output DAC are high-performance, 24-bit Σ-Δ converters that operate at a selectable 8kHz to 768kHz sampling rate. Each data converter channel includes a high resolution, digital soft volume control, and an optional high-pass filter with a configurable cutoff frequency.

The device provides two independent serial audio data ports. Each can be configured as either a master or slave interface, and they support I^2S, left justified, right justified, and up to 16 channel TDM compatible data formats. The data port supports either 1.2V or 1.8V logic levels (as set by IOVDD voltage).

The device also provides an I^2C/SPI compatible control port that supports both slave mode and master mode (with a software driver running in the HiFi 3z core) operation. In I^2C mode, the control port can be assigned one of four possible addresses and supports up to fast mode plus timing.

The Tensilica HiFi 3z core is optimized for low power audio processing. This core can either be directly programmed in C/C++ or graphically programmed using the *SigmaStudio®+* software from Analog Devices, Inc. It includes a library of configurable audio processing blocks such as filters, dynamics processors, mixers, and low-level DSP functions for fast, graphical development of custom signal flows. Software running on the core also enables access to additional hardware interface ports and operating modes including the I^3C, QSPI, and UART interface ports, master mode control for the I^2C/SPI port, and debug access through the JTAG interface port.

The FastDSP core has a reduced instruction set optimized for latency-critical applications such as noise cancellation and ambient transparency. The program and parameter random access memory (RAM) can be loaded with a custom audio processing signal flow built using *SigmaStudio+*.

The device also has a self-boot function that can load the program and data/parameter RAMs of both cores along with the register settings for the device on power-up using an external electronically erasable programmable read-only memory (EEPROM) or flash memory over a master quad SPI interface. The external flash memory is fully memory-mapped to the HiFi 3z bus fabric.

The flexible *SigmaStudio+* software connects to the device control port and can both configure the device registers, as well as program and control the cores. The graphical user interface (GUI) provides the flexibility and programmability needed by an experienced DSP programmer. However, the GUI is also designed to be user-friendly to enable even less experienced users with baseline digital or analog audio processing knowledge to design the DSP signal flow and export the flow to a target application. A full description of the device register map and memory maps is available in the companion programming guide.

In *SigmaStudio+*, the user can connect graphical blocks (such as biquad filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the device memory through the control port. The software also allows the user to download the design to an external EEPROM or Flash to prepare for self-boot operation.

The device features an on-board, bypassable fractional PLL that can generate all required internal clocks. The external clock input can either be derived from the master clock input or the bit clock input of either serial audio data port. If the input source clock frequency is within the 900kHz to 2.1MHz range it can be directly accepted by the PLL. Higher source clock frequencies up to 49.152MHz can also be accepted by first dividing the input clock down into this range by using the configurable input pre-scaler divider. For standalone operation, the source clock can be generated using the on-board crystal oscillator.

The device is available in a small, 77-ball, 3.24mm × 4.83mm WLCSP (0.4mm pitch and 0.5mm height) and is specified for operation over the extended -40°C to +85°C temperature range.

Signal Routing Diagram

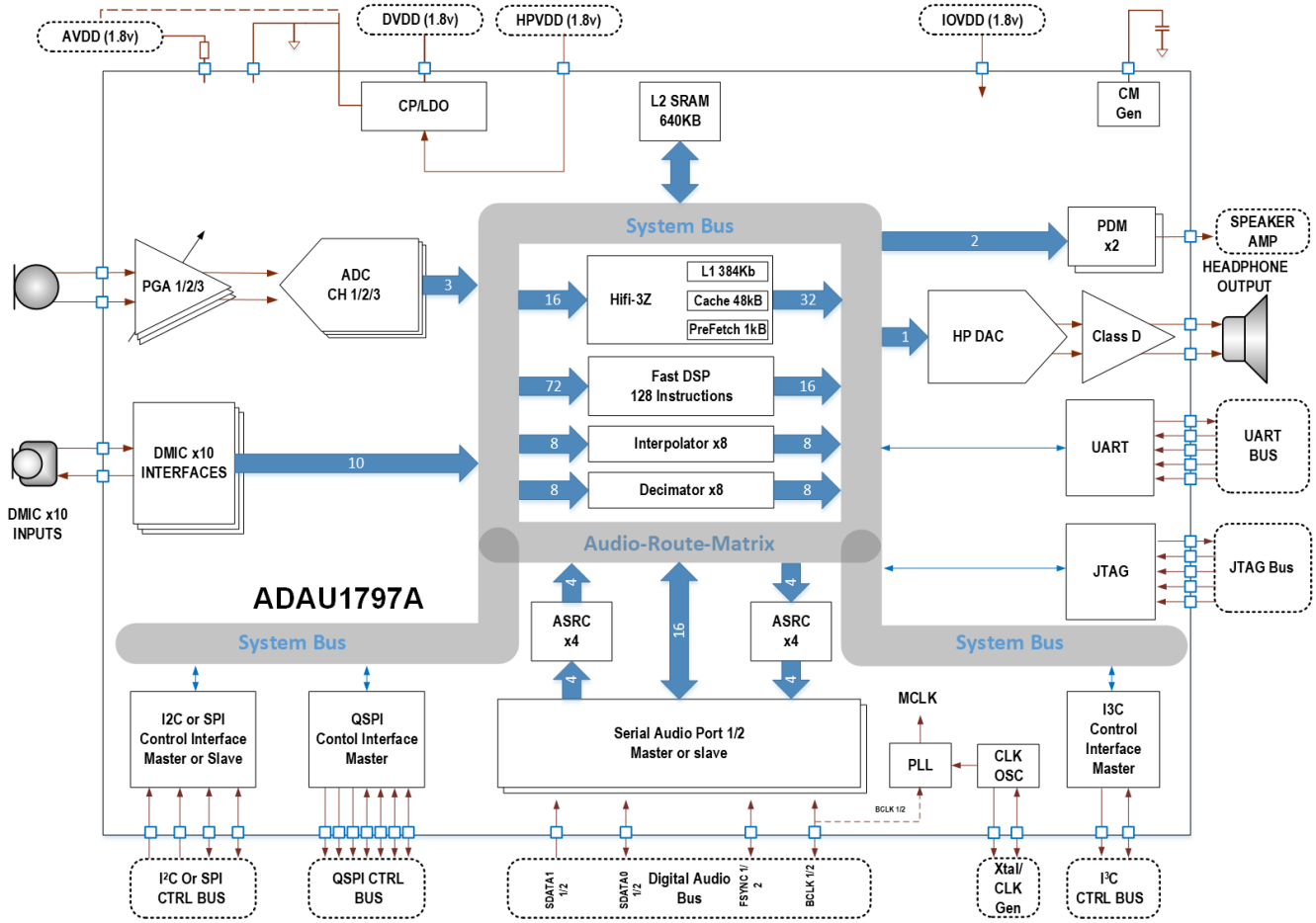


Figure 53. Device Input and Output Signal Routing

Power Supplies and Sequencing Requirements

The device requires four primary power supplies. Three of these supplies must be provided externally to the device. These are the primary analog supply (AVDD), the headphone amplifier and internal linear regulator/charge pump supply (HPVDD), and the digital interface logic level supply (IOVDD). The core digital supply (DVDD) can either be provided externally or generated internally from the HPVDD supply.

The analog supply (AVDD) and headphone/internal regulator supply (HPVDD) support operation from a 1.8V nominal level. The digital interface logic supply (IOVDD) supports operation from either a 1.8V or 1.2V nominal level. The required digital core supply level (DVDD) is dependent on the required core processing load of the implemented use case. In low power/light processing load cases, a 0.9V nominal DVDD supply level is acceptable (HIFI_SPEED = 0), while high performance/heavy processing load cases require a 1.1V nominal DVDD supply level (HIFI_SPEED = 1). This applies both for an internally generated or an externally provided DVDD source.

Power Supply Sequencing

If the DVDD supply is to be generated by the internal linear regulator or charge pump, then the REG_EN input should be externally connected to the HPVDD supply. Otherwise, the REG_EN input must be connected to ground and the DVDD supply must be externally supplied to the device.

Before powering down the device supplies, all signal input and output channels should be muted or powered down. Audible glitches may be recorded or played back if any supply is removed while audio channels are active.

Hardware Full Chip Power-Down States

The device is placed into the hardware full chip power-down (or hardware shutdown) state when the $\overline{PD}$ input pin is asserted low. This is the lowest power device state, and in this state, external supplies can either be present or fully powered down (with proper sequencing). In this state, the internal regulators for DVDD (if used) are also disabled and powered down. The device is fully reset in this state and retains no state memory (all registers and blocks return to their PoR states/configurations). No interface communication with the device is possible in this state.

As with the supply sequencing, before entering the hardware power-down state (asserting the $\overline{PD}$ input low), all signal input and output channels should be muted or already powered down. Otherwise, audible glitches may be recorded or played back before the hardware shutdown sequence is completed.

When the device transitions out of reset and the hardware power-down state (supply sequencing is complete and the $\overline{PD}$ input is asserted high), the device enters the software full chip power-down (software shutdown) state.

Software Full Chip Power-Down State

The software power-down state is the lowest power state where software/driver control is possible, and the control register map retains any programmed settings. In this state, the I^2C/SPI control ports operate as slave interfaces. Most other blocks are powered down except for internal DVDD regulators (if the REG_EN input is high), and both the common mode voltage generator and the crystal oscillator (by default).

In this state, the device power enable bit (POWER_EN) defaults to 0. To transition out of the software power-down state set POWER_EN = 1. Conversely, from a power-up state, setting POWER_EN = 0 transitions the device back into the software power-down state. As with previous power-down scenarios, to avoid audible glitches all signal input and output channels should be muted or powered down before setting POWER_EN = 0.

By default, in the software power-down state the common-mode output voltage (and CM output pin) is active (CM_KEEP_ALIVE = 1). To reduce power consumption, this can be disabled by setting CM_KEEP_ALIVE = 0. However, as a result, the device will have a longer power-up time as this adds a wait time of up to 35ms (maximum) for the

common mode voltage to charge before any analog blocks can be enabled. Conversely, with CM_KEEP_ALIVE = 1, the software power-down current is increased but the power-up time is faster as this wait time can be omitted.

Similarly, the internal digital clocks can be gated to reduce power consumption when idle in the software power-down state by setting XTAL_EN = 0. To idle the device in the lowest possible power configuration for the software power-down state (POWER_EN = 0), set both CM_KEEP_ALIVE = 0 and XTAL_EN bit = 0.

It is important to note the following restrictions when setting CM_KEEP_ALIVE = 0:

- If the pin REG_EN is pulled high, then the CM voltage always is 0.85V, regardless of the CM_KEEP_ALIVE setting.
- In self-boot mode, the CM voltage always is 0.85V, regardless of the CM_KEEP_ALIVE setting. The CM voltage can only be brought to 0V in host-boot mode.
- When setting CM_KEEP_ALIVE = 0, ensure that the PLL is still on and locked (or bypassed with MCLK present). Once CM_KEEP_ALIVE has been cleared, disable the PLL and gate the clocks for the lowest power consumption.
- The CM_KEEP_ALIVE is dependent on POWER_EN = 0 also.

The digital portion of the chip has several power domains. By default, in the software power-down state, only the domain that powers the control ports and their associated registers are powered on. The remainder of the digital domain has its power supplies gated resulting in the loss of the internal states. In addition, to retain core (FDSP/HiFi 3z) state memory in the software power-down state set the KEEP_MEM bit to 1.

Device Power-Up Sequencing

The device transitions out of the software power-down state when POWER_EN is set to 1. The power supplies on the rest of the digital portion of the chip are not enabled until this occurs, so this must be set first during the power-up sequence. After the internal digital power supplies are powered up, the PLL is locked, and other needed sequencing is complete, the POWER_UP_COMPLETE bit sets to 1 and the DSP memories can be programmed or accessed.

Interrupt requests (IRQs) can also be sent when the power-up is completed. If the IRQs are used to indicate power up is complete, then the appropriate IRQs must be unmasked. For the power-up sequence, these are the IRQ1_POWER_UP_COMPLETE and IRQ2_POWER_UP_COMPLETE bits. The associated mask bits that must be cleared (they are set by default) are the IRQ1_POWER_ UP_COMPLETE_MASK and IRQ2_POWER_UP_COMPLETE bits.

The device has highly flexible block-level power controls. Each channel of each block can be powered on or off separately. There is a control bit, MASTER_BLOCK_EN, that by default is 0 and that overrides all block level enables except for PLL_EN, XTAL_EN, HIFI_EN, and FDSP_EN. The PLL, HiFi 3z DSP, and FastDSP can be enabled even when MASTER_ BLOCK_EN = 0. All other blocks are always in power-down in this state, allowing the PLL to be enabled and locked and the DSP memories to be initialized before all other signal path blocks are enabled.

Block-level power controls and other settings can be changed on the fly while the chip is active. However, care must be taken when enabling or disabling blocks other than the DAC and/or headphone mode blocks that are actively routed out to the DAC and/or headphone mode as audible glitches may occur.

To power down the chip, disable or mute any active audio channels, set MASTER_BLOCK_EN low, and then set POWER_EN low. This allows the device to power down all blocks with any required power-down sequencing.

Table 9 shows example power-up sequences for host-boot and self-boot configurations.

Table 9. General Power-Up Sequencing Overview

STEP	DESCRIPTION
HOST-BOOT	
1	Set PD = 1 to exit reset and the hardware power-down state, and to transition the device to the software power-down state. This enables the internal DVDD regulator (if REG_EN is asserted high), the slave I²C/SPI ports, and enables the common mode voltage generator and crystal oscillator.
2	Wait 15ms if the REG_EN input pin was asserted high in step 1.
3	Set POWER_EN = 1 to exit the software power-down state. This un-gates the digital power domains and initiates the power-up sequence. The POWER_UP_COMPLETE bit sets when this is complete. **Note:** XTAL_EN is set to 1 by default in this sequence and must be set this way to complete this step.
4	Set SEL_0V9 = 1 if DVDD = 0.9V. Set SEL_0V9 = 0 if DVDD = 1.1V.
5	Set HIFI_SPEED = 0 if desired HiFi 3z core speed is 49.152MHz. Set HIFI_SPEED = 1 if desired HiFi 3z core speed is 196.608MHz. **Note:** If HIFI_SPEED = 1, DVDD must be 1.1V.
6	Set MASTER_BLOCK_EN = 1 to un-gate blocks within the ADAU1797A. Set CM_STARTUP_OVER = 1 to disable the high-power CM start-up boost. This saves power consumption on the AVDD rail now that the CM is fully powered up.
7	Configure the PLL using CLK_CTRLx registers and set PLL_UPDATE = 1 to update the PLL parameters.
8	Set XTAL_MODE and PLL_EN = 1 to un-gate the clocks and enable the PLL.
9	All register settings, FDSP memory, and HiFi 3z memory are configured within the app pack. Begin writing the app pack to the L2 memory of the ADAU1797A, beginning at register address 0x20000000.
10	Once the entire app pack has been written to L2 memory, set FDSP_EN and PROC_EN = 1. Writing PROC_EN = 1 enables the boot loader, thus loading the app pack. **Note:** If the FDSP is not being used then FDSP_EN can be set to 0.
SELF-BOOT	
1	Set PD = 1 to exit reset and the hardware power-down state, and to transition the device to the software power-down state. This enables the internal DVDD regulator (if REG_EN is high), the slave I²C/SPI ports, and enables the common mode voltage generator and crystal oscillator.
2	Wait 15ms if the REG_EN input pin was pulled high in step 1.
3	In self-boot mode, DVDD must be 1.1V, and MCLK must be 24.576MHz. **Note:** The clock configuration registers are locked in self-boot mode.
4	Once the ADAU1797A has powered up, it reads the external flash through QPI transactions. The external flash contents are stored in L2 memory and boot-loaded to the HiFi 3z core.

Power-Up Sequencing Use Case Example: Host-Boot at 0.9V, 49.152MHz HiFi 3z Speed (Detailed)

To illustrate the power-on sequencing for a real use case configuration, a full example sequence of supply application, device register writes, and required wait times follows. This case assumes an MCLK input of 24.576MHz and that an internally generated 0.9V DVDD level is used. The sequence is executed in host-boot mode.

Note: The data writes in this sequence are endian-swapped, meaning that for each register the last byte (bits[7:0]) is shown first, and the first byte (bits[32:25]) is shown last. The bits are ordered from MSB first to LSB last.

Table 10. Use Case Power-Up Sequencing Example (I^2C, Host-Boot)

STEP	ACTION	DESCRIPTION
1	Power-Up External AVDD/HPVDD/IOVDD	Power up the HPVDD, AVDD, and IOVDD supplies to within their operating ranges.
2	Power-Up DVDD	Verify that the REG_EN input pin is pulled high (HPVDD) and wait 15ms for DVDD LDO regulation to settle.
3	Set Power Enable	Set POWER_EN = 1 by writing 0x01000000 to register address 0xF000003C.
4	Set HiFi 3z Speed	Set HIFI_SPEED = 0 for 49.152MHz by writing 0x00000000 to register address 0xF00001FC.
5	Set DVDD Voltage and Assert MASTER_BLOCK_EN	Set SEL_0V9 = 1, using an internal charge pump to generate DVDD, by writing 0x13000000 to register address 0xF000002C.
6	Disable CM Fast Charge	Set CM_STARTUP_OVER = 1 by writing 0x02000000 to address 0xF000002C.
7	Apply Clocks	Apply the necessary clocks to source the PLL (MCLK or BCLK0/1).
8	Clock Configuration	Configure XTAL_MODE (crystal oscillator used), set the PLL for integer mode and set MCLK as the PLL input source by writing 0x08070000 to address 0xF0000040.
9	Set Clock Ratio	Set PLL_INPUT_PRESCALER = 16 by writing 0x10000000 to address 0xF0000044.
10	Set Clock Ratio	Set PLL_INTEGER_DIVIDER = 128 by writing 0x80000000 to address 0xF0000048. **Note:** These PLL settings configure the PLL output for 196.608MHz.
11	Update PLL Settings	Set PLL_UPDATE = 1 to ensure these changes take effect in the PLL by writing 0x01000000 to address 0xF0000054.
12	Disable Clock Gating and Enable PLL	Set XTAL_EN = 1 and PLL_EN = 1 by writing 0x03000000 to address 0xF0000030. XTAL_EN must = 1 to un-gate the clock tree, even if the crystal oscillator is not used.
13	Verify PLL Lock	Check PLL_LOCK (read 0xF0000408). If PLL_LOCK = 0, wait until PLL_LOCK = 1.
14	Verify Successful Power-Up Complete	Check POWER_UP_COMPLETE = 1 (read 0xF000040C). If POWER_UP_COMPLETE = 0, wait until POWER_UP_COMPLETE = 1. If POWER_UP_COMPLETE = 1 and PLL_LOCK = 1, continue configuring the device.
15	Write App Pack to L2 Memory	Write App Pack to L2 memory starting at address 0x20000000.
16	Enable Boot Loader	Once the entire App Pack has been written to L2 memory, set FDSP_EN and PROC_EN = 1 by writing 0x11000000 to address 0xF0000034. Writing PROC_EN = 1 enables the boot loader, thus loading the App Pack. Note: If the FDSP is not being used then FDSP_EN can be set to 0, and the write would be 0x10000000 to address 0xF0000034.

Internal DVDD Linear Regulator (LDO) and Switched-Cap Regulator

The device features both a fully integrated linear regulator and an internal switched-cap regulator. These can be used to internally generate the required 0.9V or 1.1V nominal DVDD voltage from the HPVDD input (nominal 1.8V).

If the REG_EN input pin is tied to ground when the device enters the software power-down state, the internal regulators are disabled, and an appropriate DVDD voltage must be supplied externally to the DVDD pin.

If the REG_EN pin is instead tied to HPVDD, then when the device enters the software power-down state the internal LDO regulator automatically enables and generates the required DVDD voltage (maximum settling time of 20ms).

Once the device is in the software power-down state (if the internal DVDD regulator is enabled), the integrated switched-cap regulator (charge pump) can be enabled instead of the LDO by setting the CP_EN bit to 1. To utilize this integrated regulator mode, two additional external caps are required and must be populated. The switched-cap regulator provides a more efficient power structure than the LDO for DVDD voltage regulation, however, two additional external caps are required (and must be populated) and line regulation is slightly degraded.

When using internal DVDD regulator mode, the SEL_0V9 bit determines the DVDD voltage output level and by default, the output is set to 1.1V. It can also be configured to 0.9V (SEL_0V9 = 1), however, this should only be selected when the HiFi 3z core is running at 50MHz (HIFI_SPEED = 0).

When CM_KEEP_ALIVE = 1, both the CM output and internal DVDD regulators remain powered up in the software power-down state. To minimize device power-down state power consumption when using the internal regulator, either disable common mode keep alive (CM_KEEP_ALIVE = 0) or place the device into the hardware power-down state.

DVDD Dynamic Voltage Switching

The ADAU1797A supports dynamic voltage switching of the DVDD rail, supporting transitions from DVDD of 1.1V down to 0.9V and also 0.9V up to 1.1V. The HiFi 3z core does not need to be disabled or paused during this transition. However, it is recommended to mute the audio paths before dynamically switching DVDD. This is because the ADAU1797A pauses the memories for a brief amount of time during the voltage transition, resulting in audible transients if the audio paths are not muted. The ADAU1797A pauses the memories so that it can adjust to the new DVDD voltage. Depending on whether DVDD is supplied externally or internally through the LDO/CP, different steps must be taken.

If using the internal LDO/CP, it must be assured that less than 50MIPS are being used by the HiFi before asserting SEL_0V9 = 1. Otherwise, there are no sequencing requirements as the ADAU1797A internally handles the transition from 1.1V down to 0.9V or vice versa.

If supplying DVDD externally, more care must be taken to ensure no memory access occurs while the voltage is being ramped up or down, since the ADAU1797A is not internally managing the transition automatically.

Below are the proposed sequences listed for changing DVDD to 1.1V or 0.9V. The signal path in these examples is Serial Port 0 → ADMA → HiFi 3z → HPOUT.

For this sequence, it is assumed the MAX38647B is supplying the external DVDD. The MAX38647B is an excellent fit for this application due to its high efficiency, NanoPower quiescent consumption, small footprint, and ability to provide different output voltages from the same single pin based on the values of its VSEL pins. In the sequence in Table X, the ADAU1797A has one GPO pin routed to VSEL2 on the MAX38647B. This is the only GPO connection needed between the two devices.

Also, it is assumed that the application is being run within FreeRTOS.

If switching DVDD from 1.1V down to 0.9V:

- Ensure HiFi 3z uses less than 50MIPS
- Set HIFI_SPEED = 0
- Mute DAC
- Put HiFi 3z into WAITI(0)
- [CRITICAL REGION]
  - Set ADMA_EN = 0, AIF_TX_LP_EN = 0, AMAP_EN = 0
  - Set GPO_x = HIGH (Change the VSEL2 pin on MAX38647B to output 0.9V)
  - Set SEL_0V9 = 1
- [CRITICAL REGION]
- Put HiFi 3z into WAITI(0)
- Set ADMA_EN = 1, AIF_TX_LP_EN = 1, AMAP_EN = 1
- Un-mute DAC

By putting the HiFi 3z core into WAITI(0) and then immediately disabling the AMAP, TiE, and ADMAs, we ensure no memory access occurs. Next, the DVDD voltage is switched to 0.9V, but the MAX38647B takes approximately 40µs to 80µs to ramp down its output voltage. Next, SEL_0V9 is asserted. At this juncture, the ADAU1797A adjusts to accommodate 0.9V, but the external DVDD has not yet switched to 0.9V. This is allowable since no memory access is occurring. However, it is important to put these steps into a critical region within the application so that no other function calls disrupt the timing of these steps.

The HiFi 3z is then put into the WAITI(0) state a second time. In this example, it is assumed that the timer task interrupt is a 1mS interval. Hence, by putting a WAITI(0) instruction both before and after the critical region tasks, we ensure at least 1mS of time for the MAX38647B to ramp down its voltage before beginning to attempt any memory access. For bare metal applications, other means of achieving this 1mS buffer are achievable. The important thing to ensure is that no memory access is attempted until the MAX38647B output voltage has ramped down.

An example excerpt of C code is shown in *Figure 54* to show what this may look like in the application:

```
void SWITCH_1V1_to_0V9()
{
    result = adi_pwr_SetHiFiClockSpeed(ADI_PWR_HIFI_SPEED_SLOW);

    //Mute
    *pREG_ADAU1797_MAINMAP_DAC_CTRL_DAC_CTRL2 = 0x00000044;

    //WaitI
    asm("WAITI (0)");

    taskENTER_CRITICAL();

    // ADMA_EN=0, AIF_TX_LP_EN=0, AMAP_EN=0
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_ADMA_PWR = 0x00000000;
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_AMAP_PWR = 0x00000000;
    *pREG_ADAU1797_MAINMAP_TIE_AIF_CTRL_LP_EN = 0x00000000;

    // set GPO
    gpioResult = adi_gpio_SetOutputState(hDevice, GPIO_OUTPUT, ADI_GPIO_OUTPUT_STATE_HI);

    // set SEL0V9 = 1
    *pREG_ADAU1797_MAINMAP_POWER_CTRL_CHIP_PWR = 0x00000013;

    taskEXIT_CRITICAL();

    //WaitI
    asm("WAITI (0)");

    // ADMA_EN=1, AIF_TX_LP_EN=1, AMAP_EN=1
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_ADMA_PWR = 0x00000007;
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_AMAP_PWR = 0x00000001;
    *pREG_ADAU1797_MAINMAP_TIE_AIF_CTRL_LP_EN = 0x00000001;

    //Unmute
    *pREG_ADAU1797_MAINMAP_DAC_CTRL_DAC_CTRL2 = 0x00000004;
}
```

Figure 54. Switch 1.1V to 0.9V Code Example

The steps for switching from 0.9V to 1.1V are similar but in the reverse. This is shown in *Figure 55*.

```
void SWITCH_0V9_to_1V1()
{
    result = adi_pwr_SetHiFiClockSpeed(ADI_PWR_HIFI_SPEED_SLOW);

    //Mute
    *pREG_ADAU1797_MAINMAP_DAC_CTRL_DAC_CTRL2 = 0x00000044;
    asm("WAITI (0)");

    taskENTER_CRITICAL();

    // ADMA_EN=0, AIF_TX_LP_EN=0, AMAP_EN=0
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_ADMA_PWR = 0x00000000;
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_AMAP_PWR = 0x00000000;
    *pREG_ADAU1797_MAINMAP_TIE_AIF_CTRL_LP_EN = 0x00000000;

    // Set GPO
    gpioResult = adi_gpio_SetOutputState(hDevice, GPIO_OUTPUT, ADI_GPIO_OUTPUT_STATE_LO);
    // set SEL0V9 = 0
    *pREG_ADAU1797_MAINMAP_POWER_CTRL_CHIP_PWR = 0x00000003;

    taskEXIT_CRITICAL();

    //WaitI
    asm("WAITI (0)");

    // ADMA_EN=1, AIF_TX_LP_EN=1, AMAP_EN=1
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_ADMA_PWR = 0x00000007;
    *pREG_ADAU1797_MAINMAP_POWER_CTRL2_AMAP_PWR = 0x00000001;
    *pREG_ADAU1797_MAINMAP_TIE_AIF_CTRL_LP_EN = 0x00000001;

    // Set Hifi Speed = 1
    result = adi_pwr_SetHiFiClockSpeed(ADI_PWR_HIFI_SPEED_FAST);

    //Unmute
    *pREG_ADAU1797_MAINMAP_DAC_CTRL_DAC_CTRL2 = 0x00000004;
}
```

Figure 55. Switch 0.9V to 1.1V Code Example

Noise Performance of Internal Regulators vs. External DVDD

If using the internal DVDD regulator (LDO or CP), a performance trade-off may exist relative to using an external DVDD rail. The internal DVDD regulator is powered by the HPVDD rail. If a large amount of current is used by the DVDD rail, the application may be sinking that current in a periodic manner. If this occurs, some low-level ripple will be present on the DVDD rail and hence on the HPVDD rail as well.

The PSRR of the DAC is not infinite, hence a small amount of this ripple may couple to the headphone output as noise. Note that if AVDD is supplied by the same source as HPVDD, then the ADCs on the ADAU1797A may also experience this noise coupling.

While this noise is not large, it can increase as the DVDD current increases or as the periodic frequency of the DVDD current sinks increases. Hence, projects that use large amounts of MIPS may be more likely to see a performance trade-off between the internal DVDD regulator and an externally provided DVDD.

Clock Configuration and Control

The device requires a valid external reference clock source with a frequency between 0.9MHz and 50MHz. Using the PLL_SOURCE bits, the device can be configured to accept this clock from either the crystal/master clock input pin (XTALI/MCLKIN) or from either of the bit clock input pins (BCLK_x).

If the external clock source is a crystal oscillator, the terminals should be connected between the XTALI/MCLKIN and XTALO pins as illustrated in the *System Block Diagram*. The internal crystal amplifier should then be selected and enabled by setting the XTAL_MODE bit to 1 (default). If instead a line-level master clock signal is used, the crystal amplifier can be disabled by setting XTAL_MODE to 0.

The XTAL_EN bit is used to gate all internal clocks (minimizes idle power in the software power-down state). For all cases (bit clock, master clock, or crystal clock input), XTAL_EN must be set high for device power-up to be possible.

PLL Overview

The integrated PLL is enabled with the PLL_EN bit and uses the selected input reference clock source (set with the PLL_SOURCE bits) to generate all required internal reference clocks and any master mode interface output clocks.

The PLL accepts input clock frequencies between 0.9MHz and 2.1MHz, and before reaching the PLL the selected external input clock signal is routed through an integer clock prescaler divider. The divide ratio must be set (with the PLL_INPUT_PRESCALER bits) to divide down the input source clock frequency to within this range (see below).

$$f_{PLL\_INPUT\_CLOCK} = f_{EXTERNAL\_INPUT\_CLOCK}/(PLL\_INPUT\_PRESCALER)$$

The PLL supports both an integer and fractional clock ratio mode (for PLL input to output clock ratio), and this is selected with the PLL_TYPE bit. In either mode, the PLL feedback ratio must be configured such that the PLL output frequency is fixed at 196.608MHz. All specified internal sample rates within the documentation assume this PLL output frequency, which is a 48kHz sample rate x 4096. The clock and PLL structure are illustrated in *Figure 56*.

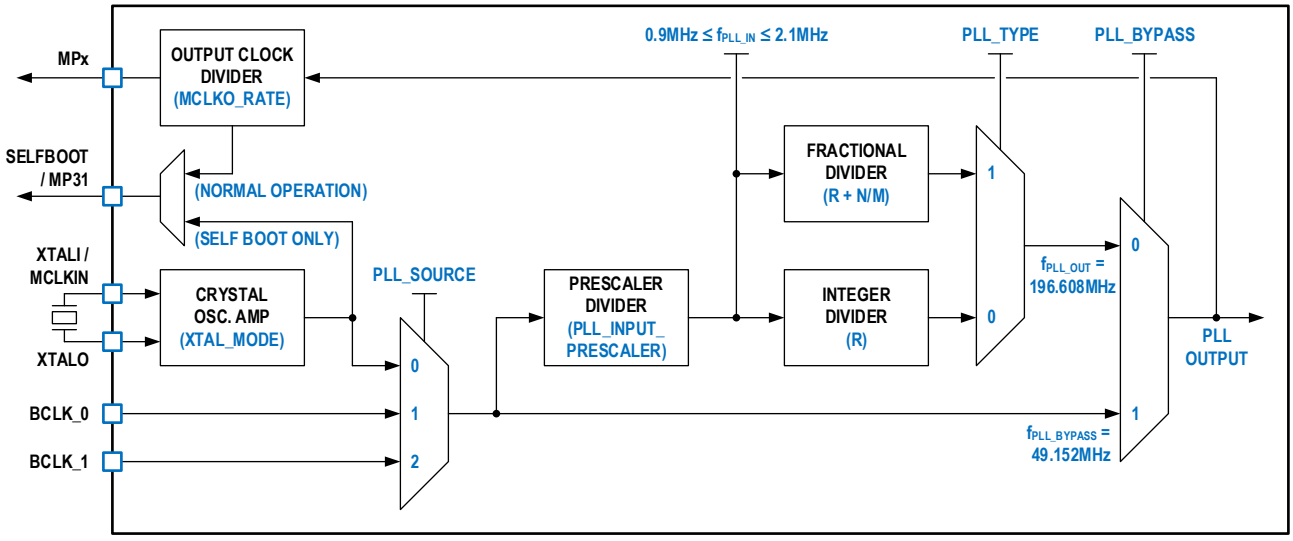


Figure 56. Clock Input and PLL Block Diagram

PLL Integer Clock Ratio Mode

Integer clock ratio mode (PLL_TYPE = 0) can be used when the target PLL output frequency of 196.608MHz is an integer multiple of the PLL input clock frequency (after prescaler divide). The integer feedback clock divider calculation is shown below, and the divider ratio value R is set with the PLL_INTEGER_DIVIDER bits.

$$f_{PLL\_OUTPUT\_CLOCK}/f_{PLL\_INPUT\_CLOCK} = R$$

For example, if the selected external reference clock input frequency is 24.576MHz, and the integer clock prescaler divider ratio is set to 16 (PLL_INPUT_PRESCALER = 16), the PLL input clock frequency will then be:

$$f_{PLL\_INPUT\_CLOCK} = f_{EXTERNAL\_INPUT\_CLOCK}/(PLL\_INPUT\_PRESCALER)$$

$$1.536MHz = 24.576MHz/16$$

The required PLL output frequency is 196.608MHz, so the integer feedback clock ratio R must be 128 (set with the PLL_INTEGER_DIVIDE bits). In integer clock ratio mode, the fractional mode numerator and denominator settings have no effect (M and N as set by the PLL_DENOMINATOR and PLL_NUMERATOR bits respectively)

$$f_{PLL\_OUTPUT\_CLOCK}/f_{PLL\_INPUT\_CLOCK} = R$$

$$196.608MHz/1.536MHz = 128$$

By default, the power-on reset states of the prescaler and integer divider bits are configured for a typical use case with a 24.576MHz input reference clock source to the PLL.

PLL Fractional Clock Ratio Mode

Fractional clock ratio mode (PLL_TYPE = 1) must be used when the target PLL output frequency of 196.608MHz is NOT a simple integer multiple of the PLL input clock frequency (after prescaler divide). Instead, a mixed clock ratio calculation is used (as shown below). The integer ratio portion R is still set with PLL_INTEGER_DIVIDER, and the fractional clock denominator M and numerator N are set with the PLL_DENOMINATOR and PLL_NUMERATOR bits.

$$f_{PLL\_OUTPUT\_CLOCK}/f_{PLL\_INPUT\_CLOCK} = R + N/M$$

For example, if the selected external reference clock input frequency is 13MHz then one possible integer clock prescaler divider ratio is 10 (PLL_INPUT_PRESCALER + 1 = 10) resulting in a PLL input clock frequency of 1.3MHz.

$$196.608MHz/1.3MHz = 151.2369 = 151 + 77/325$$

Taking the ratio of the PLL output clock to the input clock results in a value of ~151.2369. Splitting this into whole numbers and fractional portions results in 151 + 77/325 or R = 151, N = 77, and M = 325. Note that when the PLL is used in fractional mode, it is important that the N/M ratio be kept within the 0.1 ≤ N/M ≤ 0.9 range to ensure correct operation of the PLL. When used in fractional mode, the input to the PLL after the input divider must be ≥1MHz.

PLL Reference Clock Output

If the selected external PLL clock source is from the XTALI/MCLKIN input (PLL_SOURCE = 0x00), the device can also output this clock or a divided-down version of it to any available multipurpose pin. The input clock (XTALI/MCLKIN input) to output clock ratio (on a multipurpose output) is selected with the MCLKO_RATE bits and can be set to no divider (divide by 1) or to any power of 2 integer divider ratio from 2 to 128.

By default, the SELFBOOT/MP31 pin outputs the XTALI/MCLKIN input clock divided by 2. This occurs automatically when the device completes the transition from the hardware power-down state to the software power-down state. If this clock is not needed, to reduce power consumption it can be disabled with the MP31_MODE bits.

PLL Bypass Mode Operation

The device also supports operation with the PLL bypassed (PLL_BYPASS = 1). This is only possible if the selected external clock source (PLL_SOURCE) is at a fixed 49.152MHz frequency.

Power consumption is reduced in PLL bypass mode. All internal blocks operate the same except for the HiFi 3z DSP core. In PLL bypass mode, the HiFi 3z DSP core can only be set to run at the slower 49.152MHz speed setting (HIFI_SPEED = 0), and as a result, the number of instructions it can execute is limited (≤ 50MIPs).

Table 11. PLL Bypass Mode Power Reduction

PLL_BYPASS	PLL OPERATION	RELATIVE POWER CONSUMPTION (mW)
0	Used	+0.968
1	Bypassed	—

If the 49.152MHz external clock is available, then there is no downside to operating in PLL Bypass mode other than the HiFi 3z DSP core processing limitation.

PLL Multichip Clock Phase Synchronization

If multiple devices are operating from the same shared external reference clocks, then the internal audio channels of the devices can be phase synchronized. The synchronization clock source is selected by setting the SYNC_SOURCE bit, and it must be set to select the same clock source on each device (to be synchronized).

If the shared input frame clock (FSYNC_x from either port) is synchronous to the PLL-derived core clock, then the same frame clock input can be selected as the sync source for each device. However, if the shared frame clock is asynchronous to the core clock, then the sync source for each device must instead be set to one of the input asynchronous sample rate converters (ASRCI_x). If no serial audio data ports are used but each device uses the same external clock source (to the PLL), then an internal PLL-derived sync source can be used instead.

PLL Clock Configuration Sequencing

To configure the PLL during initialization or to reconfigure it for a different use case, the following sequence is recommended. To avoid potentially audible glitches, the PLL should not be reconfigured while it is active.

1. Ensure that POWER_EN = 1.
2. Ensure that PLL_EN = 0.
3. Configure (or reconfigure) the PLL control bits.
4. Write 1 to PLL_UPDATE to propagate the PLL settings.
5. Enable (or re-enable) the PLL by setting PLL_EN = 1.

Other blocks can be powered up while the PLL is not enabled or locked. However, if the PLL is enabled and not locked, all other circuitry waits until the PLL is locked to begin the power-up sequences.

All hardware control registers can be accessed at any time during PLL initialization, before PLL is enabled, or during PLL lock. However, to access the HiFi 3z DSP or FDSP memories, the respective core must be enabled (HIFI_EN = 1 or FDSP_EN = 1 respectively), and the PLL (if not bypassed) must be locked.

Input Signal Channels

The device provides three analog input signal channels each with a low power, low noise ADC. In addition, the device also accepts up to ten digital microphone input sources.

Analog Input Channels

The three flexible analog input channels accept both line-level and analog microphone input sources. Each analog input channel individually supports either a single-ended, differential, or pseudo-differential configuration, with or without a programmable gain amplifier (PGA).

When enabled (ADCx_EN), the analog inputs of each channel (AINx- and AINx+) are internally biased to the input common-mode voltage (V_{CM}). For external reference, the common mode voltage is output on the CM pin. The simplified block diagram is shown in *Figure 57*.

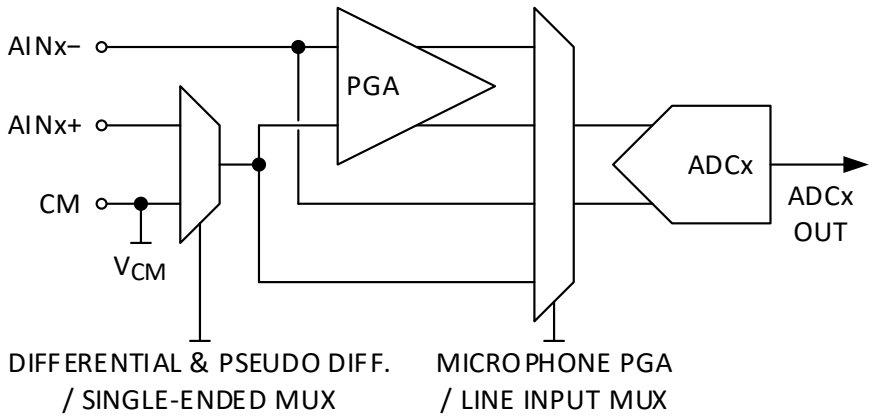


Figure 57. Analog Input Channel Simplified Block Diagram

Analog Input Mode Configuration

The analog input mode (single-ended, differential, or pseudo-differential mode) is selected for each channel using the AFEx_DIFF and AFEx_PDIFF bits. Each of these input modes can be used with the series programmable gain amplifier (PGA) either enabled or disabled (and bypassed) using the PGAx_EN bits. The default setting (after power on or reset) is single-ended mode with PGA disabled.

When a given analog input channel is configured for single-ended (SE) mode, the input signal must be applied to the negative analog input pin (AINx-). As a result, for these configurations, the input signal polarity is inverted and can be corrected by setting the ADCx_INVERT bits.

In differential (DIFF) mode, the input signal can be applied (with correct polarity) to both the positive (AINx+) and negative (AINx-) analog input pins.

In pseudo-differential (PDIFF) mode, the analog input signal can be applied to either the positive (AINx+) or negative (AINx-) input (with the other input AC coupled to the ground reference of the signal source). When using the negative input, the polarity is inverted and can be corrected by setting the ADCx_INVERT bits.

Table 12 shows the settings required for each of the supported analog input channel configurations.

Table 12. Analog Input Channel Configuration Settings

AFEx_PDIFF	AFEx_DIFF	PGAx_EN	CONFIGURATION
0x0	0x0	0x0	Single-Ended (SE) Mode with PGA Disabled (Default)
0x0	0x0	0x1	Single-Ended (SE) Mode with PGA Enabled
0x0	0x1	0x0	Differential (DIFF) Mode with PGA Disabled
0x0	0x1	0x1	Differential (DIFF) Mode with PGA Enabled
0x1	Don't Care	0x0	Pseudo-Differential (PDIFF) Mode with PGA Disabled
0x1	Don't Care	0x1	Pseudo-Differential (PDIFF) Mode with PGA Enabled

Analog Input External Connections

Figure 58 illustrates the typical external connections for a single-ended analog microphone input. The microphone output is AC coupled to the AINx- input pin and the AINx+ pin must be unconnected. For an analog microphone input use case the PGA is typically enabled (PGAx_EN set to 1). For a single-ended line-level input use case replace the AC-coupled microphone output with the line input and disable the PGA.

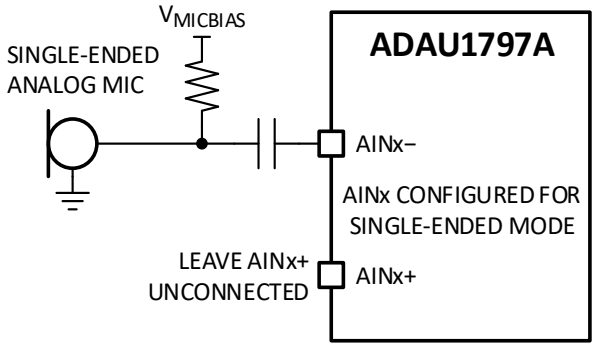


Figure 58. Single-Ended Analog Microphone Input

The device also supports a pseudo-differential mode that provides improved CMRR. *Figure 59* illustrates a polarity inverted use case with a single-ended analog microphone connected to the negative input (AINx-). The unused analog input (AINx+) is AC coupled as close as possible to the ground reference of the single-ended signal source (in this case the analog microphone). For a non-inverted polarity, reverse the positive and negative input connections.

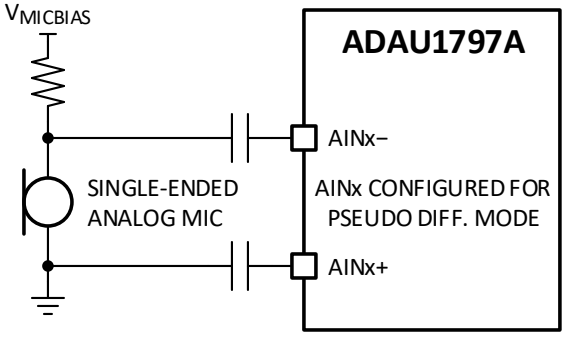


Figure 59. Pseudo-Differential Analog Microphone Input

Figure 60 illustrates a differential analog microphone input use case. The microphone outputs are AC coupled to both the AINx+ and AINx- inputs, and the PGA is typically enabled. For a differential line level input use case, connect the line inputs to the AC coupled input instead, and disable the PGA.

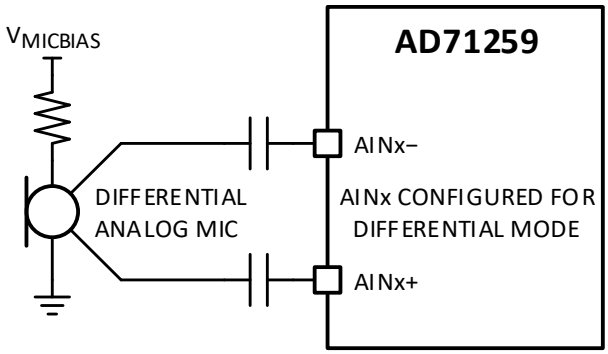


Figure 60. Differential Analog Microphone Input

Analog Input Programmable Gain Amplifier (PGA)

The analog input channels each provide an optional series PGA. When the device is configured for a line-level input, the PGA can be disabled and bypassed (PGAx_EN). When the PGA is disabled, the input impedance is fixed at 21kΩ.

When the device is configured for an analog microphone input with PGA enabled, the gain (for a given analog input channel) is selected with a combination of the PGAx_GAIN and PGAx_SUBGAIN bits. First, the target gain is selected with the PGAx_GAIN bit. The gain is adjustable from a minimum of 0dB (PGAx_GAIN = 0x00) to a maximum of +29.25dB (PGAx_GAIN = 0x27) in 0.75dB steps. Next, set the PGAx_SUBGAIN bits based on the selected analog input mode and the PGA gain level. *Table 13* details the required PGAx_SUBGAIN settings by PGA gain range and input mode.

When using the PGA gain controls, the PGAx_SLEW_DIS bit must always be set high. To avoid audible artifacts the PGA gain level should never be changed while the analog input channel is active. The digital volume control (ADCx_VOL) can be used to implement smooth volume changes while the channel is active. If settings outside of those in *Table 13* are selected, the PGA gain and signal levels may not be as expected, and the audio performance may be degraded.

Table 13. PGAx_SUBGAIN Settings by PGA Gain Range

PGA GAIN RANGE	PGAx_GAIN SETTING	PGAx_SUBGAIN SETTING	
		SE OR PDIFF MODES	DIFF MODE
0dB to +6dB	Don't Care	0b00000	0b00000
+6.75dB to +12dB	0bXXXXX0	0b00000	0b00000
	0bXXXXX1	0b11111	0b00000
+12.75dB to +29.25dB	0bXXXXX0	0b00000	0b00000
	0bXXXXX1	0b11111	0b11111

The PGA can also be configured for coarse attenuation settings (PGAx_MODE). In this mode, the PGA attenuation settings are used instead of the gain settings, and they can be adjusted from 0dB to -9dB in 3dB steps (PGAx_ATTEN).

The internal resistors used for these settings are precisely matched to each other to minimize gain and attenuation errors. However, the exact nominal value of the resistors depends on various conditions in the silicon manufacturing process and can vary by as much as ±20%.

The PGA gain of each analog input channel by default is set individually by the respective PGAx_GAIN bits. To enable synchronous PGA gain changes across all three channels, set the PGA_GAIN_LINK bit to 1. When set, the PGA gain of all three channels matches the channel 0 setting (PGA0_GAIN).

The analog input channel PGA has four power modes: lowest power, low power, normal, and high-performance modes. By default, the PGA operates in normal mode, and the mode is changed with the PGAx_IBIAS bits.

Analog Input Coupling Capacitor Precharge

By default, precharge amplifiers are enabled to quickly charge the large AC coupling capacitors in series with the analog inputs. Precharging these capacitors before enabling the channels can prevent audible signals.

The precharge amplifiers are powered up by default when an analog input ADC channel is enabled (ADCx_EN set to 1) and remain active for the selected precharge time (as set by the ADC_AIN_CHRG_TIME bits). The Precharge time can be disabled or set to one of the available times ranging from 5ms to 400ms. Longer precharge times are needed for larger input coupling capacitors, but this does increase the analog input channel startup times as well.

The internal impedance for the AINx pins is 750Ω during Precharge. However, at startup, the internal impedance is governed by the time constant of the common mode reference voltage (CM pin) because the precharge amplifiers use the CM voltage as a reference.

Analog Input Channel ADCs

Each of the three analog input channels features a high-performance 24-bit, Σ-Δ ADC. Each analog input channel and ADC is enabled with the respective ADCx_EN bit and provides a selectable sample rate, configurable digital filters, and digital volume control.

Analog Input Channel ADC Full-Scale Level

The full-scale analog input (for a 0dBFS output code with 0dB of PGA gain) is nominally $1.08V_{RMS}$ for a differential input. For a single-ended or pseudo-differential input, the full-scale input depends on whether the PGA is enabled. It is $0.64V_{RMS}$ with the PGA disabled and $0.54V_{RMS}$ with it enabled. Input signals that exceed the full-scale level (including PGA gain) cause the channel to clip.

Analog Input Channel ADC Configuration

The output sample rate for the ADC decimation filters can be configured from 8kHz to 768kHz. The sample rate for analog input channels 0 and 1 is linked (ADC01_FS), while the sample rate of channel 2 is individually selected (ADC2_FS). Both high-order (higher delay) and low-order (reduced delay) decimation filters are available. As before the setting for channel 0 and channel 1 is linked (ADC01_DEC_ORDER), while channel 2 is configured separately (ADC2_DEC_ORDER). The output of each channel can be inverted with the ADCx_INVERT bits.

To remove DC offsets, each channel provides a digital high-pass filter (enabled with the ADCx_HPF_EN bits). The HPF cutoff frequency can be configured from 0.25Hz to 241Hz. The setting for channels 0 and 1 is linked (ADC01_HPF_FC), while channel 2 is configured separately (ADC2_HPF_FC).

Compensation filters for the high-frequency roll-off of the ADC decimation filters are provided. These are enabled for channels 0 and 1 with the ADC01_FCOMP bit and for channel 2 with the ADC2_FCOMP bit. Disabling the compensation filters (default) provides the lowest propagation delay, but results in a slight signal attenuation in the passband at higher frequencies.

Analog Input Channel ADC Digital Volume Control

The digital volume of each channel can be set from -71.25dB to +24dB in 0.375dB steps with the ADCx_VOL bits. Each analog input channel can be independently placed into digital mute by setting the corresponding ADCx_MUTE bit high. The channels can also be digitally muted by configuring the digital volume control (ADCx_VOL) to the lowest setting (code 0xFF).

By default, fine-step volume ramping based on zero cross-detection is used for all digital volume changes. Volume change zero cross detection can be disabled with the ADC_VOL_ZC bit, and when disabled each volume step occurs without regard to signal level every 4.5dB/ms. Volume ramping can be bypassed entirely to allow for instantaneous (hard) single-step volume changes by setting the ADC_ HARD_VOL bit.

By default, volume control is independent for each channel. If the ADC_VOL_LINK bit is set, the volume level and any changes for all channels are linked to the channel 0 settings.

When a channel is enabled, it powers up at the volume set by the respective ADCx_VOL bits. When disabled, it powers down immediately without ramping down the volume.

Analog Input Channel ADC Bias and Power Modes

By default, all analog input channel ADCs are configured to operate with a normal bias current in the standard power mode. The ADC bias current can be set to (in order of increasing power consumption and overall performance) extreme power saving, power saving, normal operation, and enhanced performance modes. The overall power mode of all channels is set with the ADC_LP_MODE bit. In low-power mode, a +6dB gain is applied to any channel where the PGA is disabled.

Digital Microphone Input Channels

The device provides two independent digital microphone (DMIC) clock outputs (DMIC_CLK0 and DMIC_CLK1), and five separate digital microphone data input interfaces (DMIC0_1, DMIC2_3, DMIC4_5, DMIC6_7 or DMIC8_9). Each of the DMIC pins shares functionality with a multipurpose pin (MP9 to MP14).

Digital Microphone Input Channel Interface

Each input interface (DMICx_x) can accept two DMIC input channels, allowing for up to ten total digital microphone input channels. Each DMIC data input and signal channel is enabled with the corresponding enable bit (DMICx_EN). The decimation ratio and resulting output sample rate of each digital microphone input channel pair are set by the corresponding DMICxx_FS bit. The output sample rate of each pair can be set from 8kHz to 768kHz.

Each digital microphone data input channel pair (DMICx_x) is mapped to one of the two DMIC clock outputs (DMIC_CLK0 or DMIC_CLK1). The DMIC clock source is mapped independently for each DMIC data input with the respective DMICxx_MAP bit. The DMIC data inputs only support the two DMIC clock outputs and cannot be clocked from another source (such as an external host or audio device).

Each input interface accepts pulse density modulation (PDM) input data. PDM input data is channel interleaved with data for one channel on rising clock edges and the data for the second channel on falling clock edges. The PDM data is mapped directly to the relative pulse code modulation (PCM) data full-scale. For example, data with a 50% PDM density results in a -6dBFS output amplitude (when set to the default DMIC volume setting of 0dB).

By default, the lower channel number of each DMIC input channel pair is clocked on the DMIC clock rising edge while the higher channel is on the falling edge (often denoted as the left channel on the rising edge and the right channel on the falling edge for two microphone systems). The polarity of the active edges for each channel pair can be swapped by setting the corresponding DMICxx_EDGE bit high.

Digital Microphone Input Channel Clocking

Each of the two DMIC clock outputs is independently enabled with the respective DMIC_CLKx_EN bit. The frequency of each clock output is also set individually with the corresponding DMIC_CLKx_RATE bits. The clock output supports a wide range of output frequencies from a maximum of 6.144MHz down to a minimum of 256kHz.

The available DMIC clock frequencies are restricted by the selected output sample rate (set by DMICxx_FS). DMIC clock rates from 256kHz to 4.096MHz (in integer ratios of 2) are only valid with 8/16kHz output sample rates (common voice sample rates). DMIC clock rates from 384kHz to 6.144MHz (also in integer ratios of 2) are only valid with 12/24/48/96/192/384/768kHz output sample rates.

Digital Microphone Input Channel Filters

The DMIC input decimation filter provides both a fourth-order and a fifth-order option. This is selected for each channel pair with the corresponding DMICxx_DEC_ORDER bits. The fourth-order filter provides the lowest propagation delay, while the fifth-order filter improves in-band noise shaping and may be needed to maximize performance with some very high dynamic range digital microphones.

The device provides compensation filters for the high-frequency roll-off of the input decimation filters. These are enabled for each channel pair with the appropriate DMICxx_FCOMP bits. Disabling these filters (default) provides the lowest propagation delay but results in a slight signal attenuation in the passband at higher frequencies.

To remove DC offsets, each DMIC input channel pair also provides a digital high-pass filter (enabled with the corresponding DMICxx_HPF_EN bits). The HPF cutoff frequency can be configured from 0.25Hz to 241Hz. The cutoff frequency setting for each channel pair is selected with the appropriate DMICxx_HPF_FC bits.

The digital microphone input channels and the analog input channel ADCs are completely independent and do not share the same digital decimation filter chains.

Digital Microphone Input Channel Volume Control

The digital volume setting of each digital microphone input channel is independently selected with the corresponding DMICx_VOL bits. The DMIC input channel volume can be set between +24dB and -71.25dB in 0.375dB steps. Each digital microphone input channel can be independently placed into digital mute by setting the corresponding DMICx_MUTE bit high. Alternatively, the channels can also be digitally muted by configuring the digital volume control (DMICx_VOL) to the lowest setting (code 0xFF).

By default, fine-step volume ramping based on zero cross-detection is used for all DMIC channel volume changes. Volume change zero cross-detection can be disabled with the DMIC_VOL_ZC bit. Volume ramping can be bypassed for instantaneous (hard) single-step volume changes by setting the DMIC_ HARD_VOL bit.

By default, volume control is independent for each DMIC input channel. If the DMIC_VOL_LINK bit is set, the volume level and any changes for all channels are linked to the DMIC input channel 0 volume settings.

When a DMIC channel is enabled, it powers up at the volume set by the respective DMICx_VOL bits. When disabled, it powers down immediately without ramping down the volume.

Digital Microphone Input Use Case Example

For a stereo (two DMIC) input use case using a single digital microphone data input interface, the data output of both DMICs should be connected to the same DMIC input pin (DMICx_x). In this case, the same DMIC clock output source (DMIC_CLKx) should be mapped (with DMICxx_MAP) to the selected DMIC input channel pair.

The selected DMIC_CLKx output pin should be connected to the clock input of both DMICs. The clock polarity select pin of one DMIC should be connected for the rising edge and the other for the falling edge. The DMIC physical connection polarity should match the configured clock edge polarity of the DMIC input channel pair (as set with DMICxx_EDGE). *Figure 61* illustrates the typical connections in an example stereo DMIC use case.

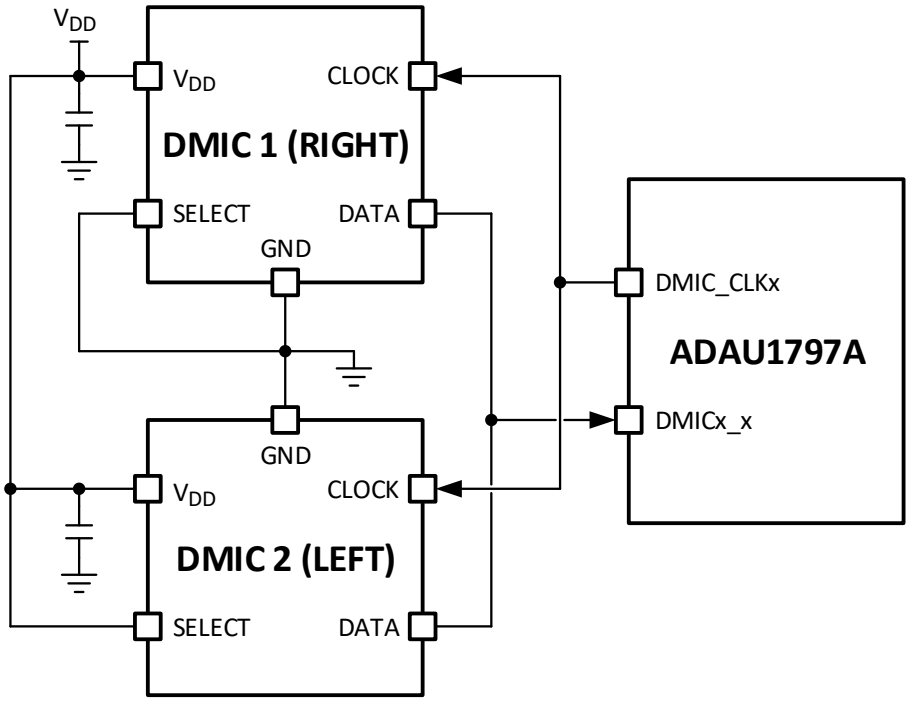


Figure 61. Digital Microphone Stereo Use Case Example

Output Signal Channels

The device provides a single amplifier output channel that includes a high-performance DAC and a low-noise, high-efficiency differential Class-D headphone amplifier.

The device also provides two low latency, high-performance 1-bit PDM output channels suitable for driving an external amplifier or transmitting data to a peripheral device.

Audio data can be routed into any combination of the output signal channels from the outputs of most internal audio subsystem blocks including the serial data ports, serial data input ASRCs, analog input ADC channels, DMIC input interfaces, interpolator filter channels, audio bus map, audio output DMA, FastDSP core, and the HiFi 3z core.

Output Channel DAC

The analog output audio playback channel features a high-performance, low latency, 24-bit resolution Σ-Δ digital-to-analog converter (DAC). The channel is enabled with the PB0_EN bit and provides a selectable input sample rate, configurable digital filters, and digital volume control.

Output Channel DAC Full-Scale Level

The full-scale output (corresponding to a 0dBFS input code with 0dB of digital volume) is nominally 1.15V_{RMS} from the DAC to the differential Class-D amplifier output. Output signals that exceed the full-scale input code (with digital volume applied) cause the channel to clip.

The signal level where the channel digitally clips can be reduced (from 0dBFS) to a selected lower level using the DAC_HF_CLIP bits. This setting reduces the full-scale level in increments of 1/256 (single-bit decrement at 8-bit resolution per setting). By default, it is set for no clipping level reduction relative to full scale. The control allows the clipping level to be set from 255/256 (-0.034dBFS) down to 1/256 (-48.165dBFS).

Output Channel DAC Configuration

The analog output channel DAC can accept audio data from other blocks at a range of input sampling rates from 8kHz to 768kHz. The DAC input data sample rate is selected with the DAC_FS bits, and the output of any audio channel routed to the DAC must be configured to the same sample rate. The input data source is selected with the DAC0_ROUTE bits.

The input signal to the channel can be inverted with the DAC_INVERT bit. Both high-order (higher delay) and low-order (reduced delay) input interpolation filters are provided, and this is selected with the DAC_MORE_FILT bit.

To remove DC offsets a digital high-pass filter (HPF) is available and can be enabled with the DAC0_HPF_EN bit. The cutoff frequency can be configured from 0.25Hz to 241Hz and is selected with the DAC_HPF_FC bits.

The device provides optional compensation filters for the high-frequency roll-off of the analog output channel DAC that is enabled with the DAC_FCOMP bit. Disabling the compensation filters (default) provides the lowest propagation delay, but results in a slight signal attenuation in the passband at higher frequencies.

Output Channel DAC Volume Control
The digital volume can be set from -71.25dB to +24dB in 0.375dB steps with the DAC0_VOL bits. The channel can be placed into digital mute by setting the DAC0_MUTE bit high. The channel can also be muted by setting the digital volume control (DAC0_VOL) to the lowest setting (code 0xFF).

By default, fine-step volume ramping based on zero cross-detection is used for all digital volume changes. Volume change zero cross detection can be disabled with the DAC_VOL_ZC bit, and when disabled each volume step occurs without regard to signal level at 4.5dB/ms. Volume ramping can be bypassed entirely to allow for instantaneous (hard) single-step volume changes by setting the DAC_ HARD_VOL bit.

When the channel is enabled, it powers up at the volume set by the DAC0_VOL bits. When disabled, it powers down while using the fine-step volume ramping if DAC_HARD_VOL = 0. Otherwise, it powers down immediately if DAC_HARD_VOL = 1.

Output Channel DAC Power Modes
Three power mode options trade off varying degrees of performance with power consumption.

The DAC power mode bits (DAC_PWR_MODE) can be set to normal, low-power saving, and high-power saving modes. The low-power modes offer a similar level of performance at reduced power, however, the lowest-power mode increases channel latency by about 1µs.

The DAC can also be placed into a high-performance mode by setting the DAC_PERF_MODE bit high. In this mode, THD+N is improved at high signal amplitudes at the cost of slightly increased power consumption.

The DAC bias current can be adjusted with the DAC_IBIAS bits and can be set to normal operation, power saving, or enhanced performance modes. The lower power settings result in slightly increased distortion.

Output Channel Class-D Amplifier

The device features a Sigma-Delta Pulse Density Modulation differential Class-D amplifier with very low output noise and distortion. The amplifier has very low quiescent power, enabling very high active power efficiency over the full output power range.

The differential headphone amplifier output (HPOUTP and HPOUTN) can drive a minimum load of 6Ω. The common mode stable output does not typically require any output filter to directly drive the speaker load, saving board space and reducing component count. In addition, the modulation scheme reduces the amplitude of spectral components at high frequencies, reducing EMI emissions that can otherwise be radiated by speakers and cable traces.

Class-D Amplifier Operation
The Class-D amplifier is automatically enabled when the analog output channel is enabled with the PB0_EN bit. The amplifier does not provide any direct analog gain or an analog mute control. The overall volume (or gain) of the analog output channel should be set with the digital volume control (DAC0_VOL) and if output mute is needed the digital mute control must be used (DAC0_MUTE).

The differential load between HPOUTP and HPOUTN must exceed the specified minimum load resistance and inductance to ensure that power and performance specifications are met. To optimize the amplifier output power stage performance, the output resistive load bits (HP_RLOAD) should be set to the closest matching value to the attached load resistance.

The amplifier defaults to high-performance mode but can be placed in low-power mode by setting HP_LPM = 1. This reduces the Class-D modulator power consumption at the expense of increased THD+N and output noise.

Class-D Amplifier Pop-and-Click Suppression

The analog output channel and amplifier architecture provides advanced pop-and-click suppression that minimizes any potentially audible transients during channel power-up (activation) and power-down (deactivation). To minimize pop-and-click, the proper sequencing should be followed.

Before the amplifier output power up, the audio clocks should be active and stable, and the input data should either be silent (zero code) or the channel should be muted (DAC0_MUTE). Once the power-up sequence is complete, the channel can be unmuted and playback can begin. If the internal digital volume control is used for soft ramping, then the channel should be unmuted once audio data is present. Alternatively, if the host is ramping up the audio data, then the channel can be unmuted first before sending ramped audio data.

Before power-down, the input data to the channel should be muted (for soft ramp-down) or ramped down by the host to silent input data. The audio clocks must not be disabled until the power-down sequence is completed. Changing any output channel settings (outside of volume and mute) while playback is active may result in audible transients. These changes should only occur when the channel is either muted or powered down (disabled).

Class-D Amplifier EMI Management

The amplifier uses a proprietary common-mode stable output switching, modulation, and spread-spectrum technology to minimize EMI emissions. This results in lower emission levels than other filterless Class-D topologies. The distance from the amplifier outputs to the speaker load impacts the radiated emissions from the board and/or cables. For some applications with longer trace or cable lengths, a small ferrite bead filter may be required for EMC compliance. Typically for trace or cable lengths less than 4" no extra filter components are needed.

For additional EMI emissions reduction, the device provides a Class-D output slew rate control (HP_EDGE) that when set, places the outputs into low EMI mode. This mode significantly reduces the output radiated emissions (particularly above 30MHz) at the expense of reduced output power efficiency.

If an output filter is required (or for extended trace lengths), amplifier output feedback connections (FB_HPOUTP and FB_HPOUTN) should be connected post-filter to correct for any non-linearities of the filtering components. These externalized feedback connections enable the use of smaller ferrite beads, which may have less linearity in the audible spectrum. With these feedback connections, package sizes such as 0201 are now usable for the ferrite beads. If no filter is used, the feedback pins must still be connected either directly to the appropriate headphone output pins (HPOUTP and HPOUTN) or to a point in the trace or wiring that is closer to the speaker load.

Class-D Amplifier Fault Protection

The analog output headphone amplifier includes fault detection, protection, and status reporting for amplifier over current (short circuit) and over-temperature faults. Headphone amplifier output over current protection is enabled by default but can be disabled by setting HP_OCP_EN = 0 (not recommended).

Output over current protection can detect an output short to GND or supply (which reports the status and disables the analog output channel amplifier). However, if HPOUTP and HPOUTN are shorted together, there can be instances where the overcurrent protection is not triggered resulting in significant HPVDD current. If it is necessary to protect against an output short, then system-level protection is recommended.

Both over-current and over-temperature faults are by default set to auto-recovery mode. In auto mode, the headphone amplifier automatically attempts to recover and re-enable after being shut down during a fault event.

To place over-current and over-temperature protection into the manual-recovery mode, set the HP_ARCV_SC and HP_ARCV_OT bits high (respectively). In manual mode, after a fault occurs and is detected (with the status bits and/or interrupts), the amplifier output is disabled and requires driver action to re-enable it. To manually attempt to restart the amplifier, the system software can either toggle the playback enable bit (set PB0_EN to disabled, then back to enabled) or switch the device into auto mode (until recovery occurs, then it can be placed back into manual mode).

PDM Output Channels

The device provides two low latency, high-performance 1-bit PDM output channels suitable for driving an external amplifier or data to a peripheral device. The outputs are enabled with the corresponding PDMx_EN bits.

The two PDM output channels share a single output clock and data interface. PDM channel 0 data is clocked on rising edges, and PDM channel 1 data is clocked on falling edges. The shared PDM clock and data outputs can each be individually routed to one or more multipurpose pins (MP0 to MP31) with the respective MPx_MODE bits.

PDM Output Channel Full-Scale Level

Full-scale input data (corresponding to a 0dBFS input code with 0dB of digital volume) results in full-scale output PDM data. The performance of the PDM modulator is degraded for PDM output amplitudes greater than -7.5dBFS.

PDM Output Channel Configuration

The PDM output channels can accept audio data from other blocks at a range of input sampling rates from 12kHz to 768kHz. The input data sample rate for both channels is selected with the PDM_FS bits, and the internal audio data routed to each channel must be configured to the same sample rate. The input data source for each PDM output channel is selected with the respective PDMx_ROUTE bits.

The PDM output channel modulators can operate at sample rates of 3.072MHz, 6.144MHz, or 12.2888MHz. The PDM data sample rate is always equal to the PDM output clock frequency and is selected with the PDM_RATE bits.

The input signal to the PDM channels can be inverted with the respective PDMx_INVERT bits. Both high-order (higher delay) and low-order (reduced delay) input interpolation filters are provided, and this is selected with the PDM_MORE_FILT bit. To remove DC offsets digital high-pass filters are available for each PDM channel and can be enabled with the respective PDMx_HPF_EN bits. The cutoff frequency can be set from 0.25Hz to 241Hz and is selected with the DAC_HPF_FC bits.

Optional compensation filters for the high-frequency roll-off of the channels are enabled with the PDM_FCOMP bit. Disabling the compensation filters (default) provides the lowest propagation delay but results in a slight signal attenuation in the passband at higher frequencies.

PDM Output Channel Digital Volume Control

The digital volume of each channel can be set individually from -71.25dB to +24dB in 0.375dB steps with the appropriate PDMx_VOL bits. Each channel can be placed into digital mute by setting the respective PDM0_MUTE bit high. They can also be muted by setting the digital volume control (PDMx_VOL) to the lowest setting (code 0xFF).

By default, fine-step volume ramping based on zero cross-detection is used for all digital volume changes. Volume change zero cross detection can be disabled with the PDM_VOL_ZC bit, and when disabled each volume step occurs without regard to signal level at 4.5dB/ms. Volume ramping can be bypassed entirely to allow for instantaneous (hard) single-step volume changes by setting the PDM_ HARD_VOL bit.

By default, volume control is independent for each PDM output channel. If the PDM_VOL_LINK bit is set, the digital volume level and any changes for both channels are linked to the PDM output channel 0 volume settings (PDM0_VOL). When a channel is enabled, it powers up at the volume set by the respective PDMx_VOL bits. When disabled, it powers down immediately without ramping down the volume.

Interpolation and Decimation Filters

In addition to the decimation and interpolation filters that are attached to specific channels, the device provides an additional standalone set of eight decimation filters and eight interpolation filters. These filters can accept output data routed from and provide input data to most internal audio subsystem blocks.

The eight decimation filter channels convert higher sample rate input data (fast) to lower sample rate output data (slow) and can each be enabled individually with the FDECx_EN bits. The input data source is selected individually for each channel and is routed with the corresponding FDECx_ROUTE bits. The input and output sample rate settings for the eight decimation channels are grouped in pairs (channel pairs 0/1, 2/3, 4/5, and 7/8). The input and output sample rate for each pair is set with the respective FDECxx_IN_FS bits (input) and FDECxx_OUT_FS bits (output). The selected input sample rate must be higher than the output sample rate.

The eight interpolation filter channels convert lower sample rate input data (slow) to higher sample rate output data (fast) and are each enabled individually with the FINTx_EN bits. The input data source is selected individually for each channel and is routed with the corresponding FINTx_ROUTE bits. The input and output sample rate settings for the eight interpolation channels are grouped in pairs (channel pairs 0/1, 2/3, 4/5, and 7/8). The input sample rate for each pair is set with the respective FINTxx_IN_FS bits and the output sample rate is set with the respective FINTxx_OUT_FS bits. The selected input sample rate must be higher than the output sample rate.

The interpolation and decimation filter channels support input and output sample rate settings ranging from 8kHz to 768kHz, however, only input-to-output sample rate ratios that do not have a fractional component are supported. For example, a decimation filter with an input sample rate of 16kHz and an output sample rate of 24kHz is not supported since the ratio (24kHz/16kHz) has a fractional component.

Asynchronous Sample Rate Converters

The device provides two full-duplex (input and output) asynchronous sample rate converters (ASRCs) that can each be paired with either of the two serial audio data ports. Each ASRC (ASRC 0 and ASRC 1) provides four digital input and four digital output channels (for a total of eight digital input and eight digital output ASRC channels).

Each ASRC input and output channel is individually enabled. For ASRC 0 the output channels are enabled with the ASRCO0_x_EN bits and the input channels are enabled with the ASRCI1_x_EN bits. For ASRC 1 the output channels are enabled with the ASRCO1_x_EN bits and the input channels are enabled with the ASRCI1_x_EN bits.

ASRC Configuration

The ASRCs convert input and output audio data to or from the sample rate of the paired serial audio data port to or from the selected internal synchronous audio data sample rate. The serial port paired with each of the two ASRCs is selected with the ASRCOx_SAI_SEL and ASRCIx_SOURCE bits for the output and input channels respectively.

When paired with the ASRCs, the serial audio data ports can support external asynchronous input and output audio data at sample rates from 7kHz to 224kHz. All intermediate frequencies and clock ratios are supported. For voice bandwidth external sample rates (typically nominal sample rates from 8kHz to 32kHz), additional low pass filtering can be enabled with the ASRCIx_VFILT (for input channels) and ASRCOx_VFILT (for output channels) bits.

For each ASRC, the sample rate for the input and output channels is individually selected from a discrete set of values ranging from 8kHz to 192khz. The internal sample rate accepted (ASRCOx input rate) by the four output channels is linked and is set for the four output channels with the ASRCOx_IN_FS bits. The sample rate provided (ASRCIx output rate) by the four input channels is also linked and is set with the ASRCIx_OUT_FS bits.

For both ASRCs, the four input channels and four output channels will automatically mute the converted output data to zero code if they have not locked or lose lock. The lock-on state of the input and output channels for each ASRC can be monitored with the corresponding ASRCIx_LOCK (for input channels) and ASRCOx_LOCK (for output channels) read-only status bits. The unlocked-to-locked or locked-to-unlocked transitions for each ASRC can be used as interrupt sources for the two interrupt controllers.

ASRC Signal Routing

Audio data can be routed to each ASRC input channel from any of the input channels of the paired serial audio data port (as set by the ASRCIx_COURSE bits). The source audio data for each ASRC input channel is selected with the respective ASRCIx_x_ROUTE bits.

Similarly, audio data can be routed into the ASRC output channels from the outputs of most internal audio subsystem blocks including the analog input ADC channels, DMIC input channels, decimator filter channels, audio bus map, audio output DMA, Fast DSP core, and the HiFi 3z core. The source audio data for the ASRC output channels is selected with the respective ASRCOx_x_ROUTE bits. The internal audio data routed to each ASRC output channel must be configured to the same sample rate as the ASRC output channel.

ASRC Power Modes

By default, the input and output channels of both ASRCs operate in high-performance mode. Two lower power modes with slightly reduced performance are provided. Generally, if the ASRC input or output data is from or to the ADC or DAC the low-power modes do not degrade the signal below the performance of the converters. For ASRC input channels these modes are enabled with the ASRCIx_LPM (low power) and ASRCIx_LPM_II (lowest power) bits. For output channels, they are enabled with the ASRCOx_LPM (low power) and ASRCOx_LPM_II (lowest power) bits.

Table 14. Input ASRC Power and Performance Options for 44.1kHz to 48kHz Conversion

MODE	THD+N at 1kHz	THD+N at 20kHz	DNR A-WEIGHTED	POWER PER CHANNEL (mW)
Default	-130dB	-120dB	130dB	0.174
ASRCI_LPM = 1	-120dB	-110dB	130dB	0.130
ASRCI_LPM_II = 1	-115dB	-90dB	130dB	0.108

Table 15. Output ASRC Power and Performance Options for 48kHz to 44.1kHz Conversion

MODE	THD+N at 1kHz	THD+N at 20kHz	DNR AW	POWER PER CHANNEL (mW)
Default	-130dB	-120dB	130dB	0.452
ASRCO_LPM = 1	-120dB	-110dB	130dB	0.289
ASRCI_LPM_II = 1	-115dB	-90dB	130dB	0.205

Control and Data Ports

The device provides multiple control and data interface ports including an I²C interface, an I³C interface, an SPI interface, a quad SPI (QSPI) interface, a UART interface, and a JTAG interface. Each interface supports either a master mode, slave mode, or both modes of operation. Some interface and operating mode combinations are compatible with either automatic self-boot or external host control, while other combinations can only be operated by local software running on the HiFi 3z Core. *Table 16* provides an overview of each supported interface port.

Table 16. Supported Control and Data Interface Ports

INTERFACE	PINS	MODES	ACCESS
I²C Interface Port	SDA0, SCL0	Slave Mode	Standalone Host Control
	SDA0, SCL0, SDA1, SCL1	Master Mode	Local Software Control
I³C Interface Port	SDA1, SCL1	Master/Slave Mode	Local Software Control
SPI Interface Port	SCLK, MOSI, MISO, $\overline{SS}$	Slave Mode	Standalone Host Control
		Master Mode	Local Software Control
QSPI Interface Port	QSPIM_* (CLK, CS0/1, SDIO_1/2/3/4)	Master Mode	Self-Boot Mode or Local Software Control
UART Interface Port	UART_* (RX, TX, RTS, CTS)	Tx/Rx Modes	Standalone or Local Software
JTAG Interface Port	JTAG_* (TDI, TDO, TCK, TMS, TRST)	Master Mode	Debug Only (See *HiFi 3z Overview*)

I²C/SPI Control Interface Port

The device provides a 4-wire SPI control interface and a 2-wire I²C control interface that share control port pins and by default operate as slave mode interfaces. Both slave interfaces require an external clock source from the host. The device also supports master mode operation for both control interfaces that require a local software driver running on the HiFi 3z core. A secondary I²C master interface can also be implemented using the I³C interface.

The device's default operation is to use the I²C control interface in slave mode. To activate the SPI control interface in slave mode, the $\overline{SS}$ pin must be pulled low three times (toggling high in between each assertion). When in I²C interface mode, the unused control pins (ADDR0 and ADDR1) determine the I²C device address. *Table 17* shows the shared control port pin functions based on the selected control interface operating mode.

Table 17. Multifunction Pin Operation by Control Interface Mode

CONTROL PORT PIN	I²C SLAVE MODE	SPI SLAVE MODE
SCL/SCLK	SCL (I²C Clock Input)	SCLK (SPI Clock Input)
SDA/MISO	SDA (I²C Bidirectional Data)	MISO (SPI Data Output)
ADDR1/MOSI	ADDR1 (I²C Address Input Bit 1)	MOSI (SPI Data Input)
ADDR0/$\overline{SS}$	ADDR0 (I²C Address Input Bit 0)	$\overline{SS}$ (SPI Inverted Slave Select)

Each slave interface can read and write from the device memories and main control registers. All addressable registers can be accessed either individually in each transaction (in single address mode) or sequentially in a single transaction (in burst mode). The first byte (Byte 0) of a control port write contains the 7-bit device address plus the R/$\overline{W}$ bit. The next four bytes (Byte 1 through Byte 4) are the 32-bit sub-address of the memory or register location. All subsequent bytes (starting with Byte 5) contain data (such as register, program, or parameter data). Control registers and bits marked as reserved in the register map/programming guide always read back as 0.

I²C/SPI Control Interface Burst Mode Communication

Burst mode addressing, in which the sub-addresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single word write unless the transaction is stopped (with a stop condition for I²C, or with $\overline{SS}$ brought high for SPI). The control registers and memory locations vary in width from one byte to five bytes, so the auto-increment feature knows the mapping between sub-addresses and the word length of the destination register or memory location.

If large blocks of data must be downloaded to the DSP cores, the output of the cores can be disabled, new data can be loaded, and the core can then be restarted. This is typically done during the booting sequence at start-up or when loading a new program into memory.

Table 18. I²C/SPI Control Data Word Sizes and Address Ranges

BASE ADDRESS	END ADDRESS	DESCRIPTION
0x0000-0000	0x0001-FFFF	Reserved
0x0002-0000	0x0003-FFFF	HiFi 3z Data RAM 0
0x0004-0000	0x0005-FFFF	HiFi 3z Data RAM 1
0x0006-0000	0x0007-FFFF	HiFi 3z Instruction RAM
0x0008-0000	0x0FFF-FFFF	Reserved
0x1000-0000	0x1009-FFFF	Level 2 Memory
0x100A-0000	0x1FFF-FFFF	Reserved
0x2000-0000	0x2009-FFFF	Level 2 Memory Non-Cached
0x200A-0000	0x3FFF-FFFF	Reserved
0x4000-0000	0x4FFF-FFFF	External QSPI Flash Memory
0x5000-0000	0xEFFF-FFFF	Reserved
0xF000-0000	0xF000-11FC	Main Control Registers
0xF000-11FD	0xF001-FFFF	Reserved
0xF002-0000	0xF002-077F	FastDSP Parameter Memory
0xF002-0780	0xF002-FFFF	Reserved
0xF003-0000	0xF003-01FF	FastDSP State Memory
0xF003-0200	0xF003-FFFF	Reserved
0xF004-0000	0xF004-007F	FastDSP Program Memory
0xF004-0080	0xF004-FFFF	Reserved
0xF005-0000	0xF005-01FF	Audio Bus Mapping
0xF005-0200	0xF00F-FFFF	Reserved
0xF010-0000	0xF01F-FFFF	System Fabric Global Program View
0xF020-0000	0xFFFF-FFFF	Reserved

I²C/SPI Control Interface Memories Access

All memory and control register locations are 32-bits or 4 bytes in width. Each data word occupies a single 32-bit address, and when writing to these memories an entire word (all 4 bytes) must be written for the write to complete and take effect (starting with the lowest address and continuing sequentially). Similarly, a read must begin at the lowest memory address, however, all 4 bytes of a data word need not be read before ending the transaction.

The mapping of bytes over the control interface is where the most significant byte of a memory location is written or read first, and the least significant byte is written or read last. The memories can be read or written in burst mode or single-byte mode if the write and read requirements are met.

I²C Slave Control Interface Operation

The device features an I²C-compatible, 2-wire serial interface. The interface comprises a bidirectional serial data line (SDA) and an input serial clock line (SCL) that facilitate communication between the slave device and the upstream I²C host (also referred to as the I²C master). The I²C interface supports FM+ clock rates up to 1MHz, but for most bus capacitances the SDA_MISO_DRIVE bit must be set to 1 to support these operating speeds.

The ADDR0 and ADDR1 pins set the LSBs of the device's I²C interface address. Therefore, each device can be set to one of four unique addresses, allowing multiple ICs to exist on the same I²C bus without address contention. The 7-bit I²C addresses are shown in *Table 19*.

Table 19. Device I²C Interface Address Selection

ADDR1 (MOSI)	ADDR0 ($\overline{SS}$)	SLAVE ADDRESS
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B

Each slave device is recognized by a unique 7-bit device address. The I²C address format is shown in *Table 20*. The LSB of the first byte is sent from the I²C master and sets either a read or write operation, where logic level 1 corresponds to a read operation, and logic level 0 corresponds to a write operation. A stop condition always terminates an I²C data transfer (transaction).

Table 20. Device I²C Interface Address Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	0	1	0	ADDR1	ADDR0	R/$\overline{W}$ Bit

Both the SDA and SCL pins must have external pullup resistors (2kΩ typical) on the lines/traces connected to the pins. The pull-up voltage on these signal lines cannot be higher than V_{IOVDD}.

I²C Slave Interface Addressing

Initially, each device on the I²C bus is in an idle state and monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. A start condition indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first.

The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte indicates that the master writes information to the peripheral, whereas a Logic 1 indicates that the master reads information from the peripheral (after writing the subaddress and repeating the start address). A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the device immediately jumps to the idle condition. During a given SCL high period, the user can only issue one-start condition, one-stop condition, or a single-stop condition followed by a single-start condition. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL.

If an invalid sub-address is issued by the user, the device issues an acknowledge, but no data write occurs and a read is responded to with zero data. If the highest sub-address location is reached while in write mode, the data for the invalid byte is not loaded to any sub-address register.

I²C Slave Interface Read and Write Operations

Figure 62 shows the format of a single-word (4-byte) write operation. The device address is sent first (with the write bit set), and then the 32-bit sub-address is sent next (1 byte at a time). Finally, the data word is written (1 byte at a time). All sub-address locations point to the start of a data word and all 4 bytes must be written sequentially for the write to take effect. Ending the transaction before all 4 bytes are written results in no new values being stored.

Figure 63 shows the format of a burst mode write sequence. In this case, the host may require multiple word writes to multiple sub-addresses. The device automatically increments its sub-address after each data word is written (4 bytes) until a stop condition is sent. The device decodes the sub-address and sets the appropriate auto-increment.

The format of a single word (4 bytes) read operation is shown in *Figure 64*. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation because the sub-address still must be written to set up the internal address pointer. After the device acknowledges the receipt of the sub-address, the master must issue a repeated start command, followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). This causes the SDA to set as an output, and the device begins sending the requested read data back to the master. The master now must respond to every ninth pulse with an acknowledge.

Figure 65 shows the format of a burst mode read sequence. In this case, the device also auto-increments its sub-address after each read until the host sends a no-acknowledge condition (ending the burst read) followed by a stop condition. The device always decodes the sub-address and sets the auto-increment appropriately.

The data bytes written over the I²C interface use little-endian format (lowest significant byte first followed by most significant bytes). Data word width is 32 bits wide, so while writing the data into the register little endean format must be used. The 32-bit data is divided into 4 bytes. While writing the data into the register, the lowest significant byte must be written first followed by the remaining 3 bytes with the most significant byte as the last or fourth byte.

Figure 62, *Figure 63*, *Figure 64*, and *Figure 65* use the following abbreviations:

- S is the start bit.
- Sr is the repeated start bit.
- P is the stop bit.
- A is acknowledge (ACK)
- $\overline{A}$ is not acknowledge (NACK)

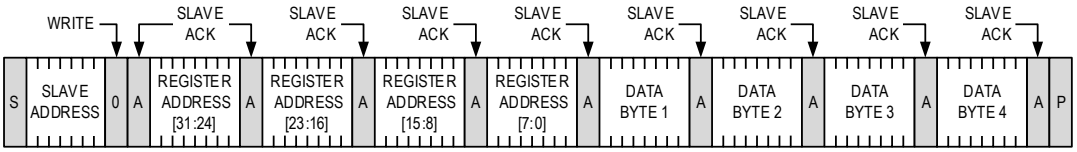


Figure 62. Single-Word I²C Write Format

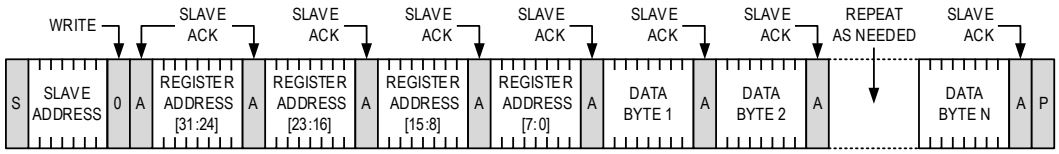


Figure 63. Burst Mode I²C Write Format

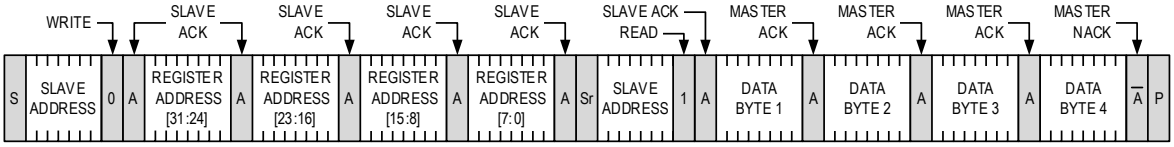


Figure 64. Single-Word I²C Read Format

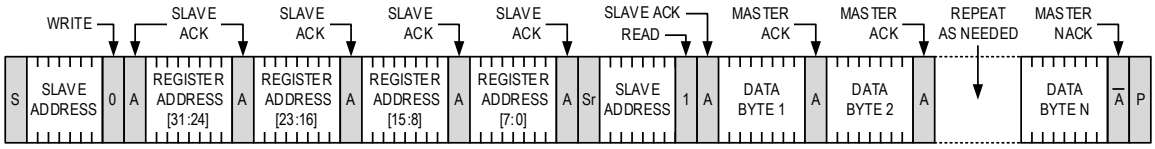


Figure 65. Burst Mode I²C Read Format

SPI Slave Control Interface Operation

By default, the device operates in I²C slave control interface mode. To place the device in SPI slave control interface mode, the $\overline{SS}$ pin must be pulled low three times by issuing three SPI writes (which are in turn ignored by the device). The SPI slave interface is then active, and the device is ready to respond to the next SPI transaction (fourth).

The SPI slave control port is a 4-wire interface consisting of the $\overline{SS}$ SCLK, MOSI, and MISO signals. The $\overline{SS}$ signal must go low at the beginning of a transaction and high at the end of a transaction. The MOSI signal carries the serial input data, and the MISO signal is the serial output data, and all data is sent to MSB first. The SCLK signal latches MOSI input data on a rising clock edge. Likewise, MISO output data is changed on the falling SCLK edge and must be clocked into the receiving device (such as a microcontroller) on the rising SCLK edge. The MISO output remains tri-stated until a read operation is requested, allowing other SPI-compatible peripherals to share the same MISO readback bus.

Once the device is placed into SPI slave interface control mode, it can only be placed back into I²C slave interface control mode by pulling the $\overline{PD}$ pin low (hardware power down) or by powering down the supplies.

SPI Slave Interface Transaction Format

All SPI transactions have the same basic structure, and this format is described in *Table 21*. All device sub-addresses are 32 bits in length (4 bytes) and each data word is also 32 bits wide (4 bytes). As a result, each SPI transaction is at least 10 bytes in length. A timing diagram for SPI transactions is also illustrated in *Figure 5*.

The first byte of an SPI slave interface transaction is always sent on the MOSI line (from master to slave device) and indicates (with the R/$\overline{W}$ bit) whether the transaction is a read or a write. The LSB of this first byte is the R/$\overline{W}$ bit, with a logic level 1 setting a read transaction and a logic level 0 setting a write transaction.

The next 5 bytes (sent on the MOSI line) contain the 32-bit device sub-address location (for the target memory location or control register) followed by an unused dummy byte containing zero code data. The dummy byte effectively extends the sub-address to 40 bits, with the actual sub-address being placed in the 32 MSBs.

For a single read or single write transaction, the next 4 bytes contain the data bits (from MSB to LSB). The device also supports burst mode read and writes, in which case the transaction can be extended by n bytes of data (where n should be a multiple of 4 to read or write n / 4 complete data words). In a burst mode transaction, the device auto-increments the sub-address appropriately. For write transactions, data bytes are received on the MOSI line, while for a read transaction data bytes are transmitted on the MISO line (which is tristated before and after data transmission). The transaction (single or burst mode) is ended when the master pulls the $\overline{SS}$ line high.

For burst mode read and writes, the dummy byte is only needed during the first read or write operation. Subsequent reads or writes occur in increments of four bytes. If host-booting an app pack to the L2 memory over the SPI port, no dummy bytes are needed.

Table 21. Generic SPI Interface Transaction Format

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
0000000x (x is the R/$\overline{W}$ Bit)	Target Device Sub-Address				Dummy	First Read or Write Data Word (4 Bytes)			
	Bits[31:24]	Bits[23:16]	Bits[15:8]	Bits[7:0]	00000000	Bits[31:24]	Bits[23:16]	Bits[15:8]	Bits[7:0]

The format for a single-write SPI operation is illustrated in *Figure 66* and the format for a single-read SPI operation is shown in *Figure 67*. For simplicity, the $\overline{SS}$ and SCLK lines are not shown but each tick/step on the MOSI or MISO lines represents a single SCLK period. For labels, these diagrams use the following abbreviations:

- SSL is the transaction start where the master pulls the $\overline{SS}$ line low
- SSH is the transaction end where the master pulls the $\overline{SS}$ line low
- X is a don't care condition for the MOSI data input line
- HIGH-Z indicates where the MISO output line is tristated

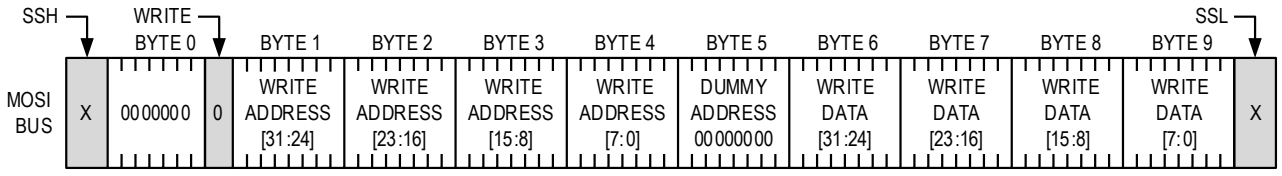


Figure 66. SPI Write Format (Single-Write Mode)

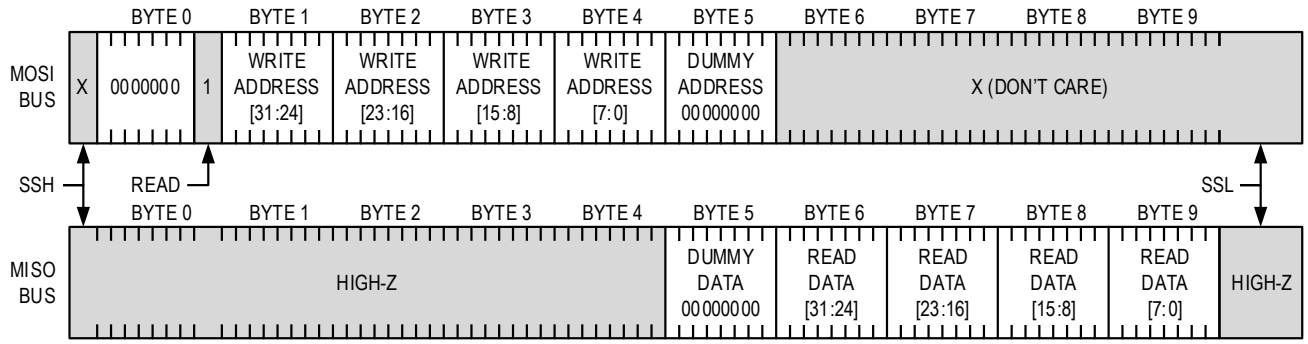


Figure 67. SPI Read Format (Single-Read Mode)

I²C/SPI Master Control Interface Operation

The device can also be configured to support I²C or SPI master control interface modes. This operating mode can only be controlled and configured by a software driver running on the HiFi 3z core. These master mode use cases operate through the same pins as the I²C and SPI slave control interfaces and are mutually exclusive if enabled (the shared pins restrict the device to either an I²C or an SPI interface configured to either master or slave mode).

For the I²C and SPI master control interface modes, the read and write data formats for both single and burst data transfers must be configured to match the address length and word length of the target slave device.

I³C Interface Port

The device also supports an I³C interface port (master or slave mode on SDA1 and SCL1) that can only be controlled and configured by a software driver running on the HiFi 3z core. The I³C interface complies with the MIPI I³C v1.1 specification (refer to this documentation for additional details).

The control interface can also be configured to be backward compatible with I²C interfaces, allowing it to support legacy slave devices. All data rates are supported except for the I³C HDR ternary options.

Table 22. Supported I²C/I³C Modes

MODE	SCL FREQ	SDA RATE
I²C Interface Standard Mode	96kHz	96kHz
I²C Fast Mode	384kHz	384kHz
I²C Fast-Mode Plus	768kHz	768kHz
I³C SDR	6.144MHz	6.144MHz
I³C HDR-DDR	3.072MHz	6.144MHz

I³C Features

As an I³C bus master, the device supports all required and optional features of the MIPI Alliance Specification for I³C except for HDR-TSL and HDR-TSP modes. The device can be programmed to function as either the I³C bus main master or secondary master.

The device can be configured to implement the full set of required and optional I³C slave features or just the subset of features required by the application. In the minimum configuration, the device supports the minimum set of slave features required by the MIPI Alliance Specification for I³C:

- I³C Standard Data Rate (SDR) mode data transfers.
- The minimum set of I³C Common Command Codes (CCCs) that must be supported for basic I³C SDR mode operation.

Through hardware configuration parameters, additional slave mode features are supported including:

- Support for an I²C-style static address so that the device can connect to an I²C bus.
- I³C HDR-DDR mode.
- Generation of I³C In-Band Interrupts (IBIs), with or without data payload.
- Hot-Join.
- Master request (secondary master).
- Support for I³C Timing Control Asynchronous Mode 0.
- Support for I³C Timing Control Synchronous Mode.
- Support for CCCs related to I³C activity states and events.
- Support for CCCs related to maximum read/write data length and maximum data speed.
- Generating interrupts to the application for a programmable set of conditions.
- Inclusion of an additional memory-mapped register that can be used for any application-specific purpose.

When support for either IBI, Hot-Join requests or master requests is included, the device also provides the following slave mode features:

- I³C read message timeout—The device abandons an I³C read message (by releasing SDA) if SCL does not change for 100 µs or more.
- S0/S1 error timeout—After detecting an SO or S1 error, if the device detects that the I³C bus is free for 60 s or more, the device stops waiting for the HDR Exit Pattern and returns to normal operation, waiting for the next START.

The following system features are optional and, when implemented, can be used for both master and slave mode operation:

- FIFOs on the transmit/receive data paths.

Note: Interrupt support is optional for slave mode and included by default for master mode.

I³C Master Mode Operations

When operating in I³C bus master mode, the device implements the functions required for an I³C master device, as defined by the MIPI Alliance Specification for I³C, including:

- Generating the SCL clock signal, with application-specified frequencies and duty cycles for I³C push-pull, open-drain, and I²C mode operation.
- Performing dynamic address assignment (DAA) on the I³C bus under application control.
- Responding to IBIs, Hot-Join requests, and master requests issued by I3C bus slaves.
- Generating read/write messages on the I³C bus.
- Control of SDA input/output, including I³C open-drain, push-pull, and high-keeper requirements.

The device interacts with host system software for configuration, control, read/write data, and status through the registers described in the I³C Master Slave Registers section.

Master Mode Initialization

To use the device in master mode the registers MCONFIG, MDATACTRL, and IBIRULES need to be written primarily.

- The MCONFIG register should be written to specify the SCL frequency and duty cycle along with the SCL-to-SDA skew and to enable the device for master mode, either as the main master or as a secondary bus master.
- The MDATACTRL register can be written to configure the device to use the internal FIFOs and configure the transmit/receive FIFO trigger levels. The IBIRULES register can be written to optimize response to incoming IBIs.

SCL Generation

When operating in master mode, the device is responsible for generating the bus clock, SCL. Through the MCONFIG register, you can configure the SCL frequency and duty cycle for each of the following bus conditions:

- I^3C push-pull operation (SDA is driven with push-pull drive).
- I^3C open-drain operation (SDA is driven low for logic 0 and is Hi-Z with pull-up for logic 1).
- I^2C mode.

Assigning Dynamic Addresses

The I^3C main bus master is responsible for assigning dynamic addresses at I^3C bus initialization. In addition, the current I^3C bus master may need to assign dynamic addresses to additional slaves that join the I^3C bus after I^3C bus initialization.

To assign a dynamic address to a bus slave with a known I^2C-style static address, the application can issue a SETDASA CCC through the device.

To perform Dynamic Address Assignment (DAA) through the device:

- Enable the interrupts MCTRLDONE, COMPLETE, RXPEND, IBIWON, and ERRWARN.
- Write to MCTRL.REQUETS = 4, MCTRL > IBIRESP = the response if an IBI occurs during DAA.
- When an RXPEND interrupt occurs, begin reading data (Provisional ID from slave).
- When an MCTRLDONE interrupt occurs, check the MSTATUS register.

I^3C Address Arbitration Optimization

To use I^3C address arbitration optimization:

1. Only assign I^3C bus slaves dynamic addresses 0x3F or lower.
2. Set MSB0, bit [30] of IBIRULES register to enable I^3C address arbitration optimization.

Generating Messages with MCTRL or Message Mode

The application can use either message mode or the MCTRL register to generate I^2C or I^3C mode read/write messages.

Message mode provides a means to generate messages with fewer processor interactions and can be used with processor control. The process differs for SDR and HDR-DDR mode messages. If an IBI occurs during the message, the I3C_MS uses MCTRL.IBIRESP to determine how to respond to the IBI. Message data can be written/read by the processor using the TXNOTFULL/RXPEND interrupts (if enabled).

Working with Interrupts

The application can be informed by interrupt when any of the MSTATUS register bits [19:8] becomes set. Each interrupt source can be individually enabled or disabled. When the MSTATUS bit for the enabled interrupt source is set, the device irq output goes active (high) and remains high until the interrupt source is cleared.
Figure 68 shows the interrupt generation flow.

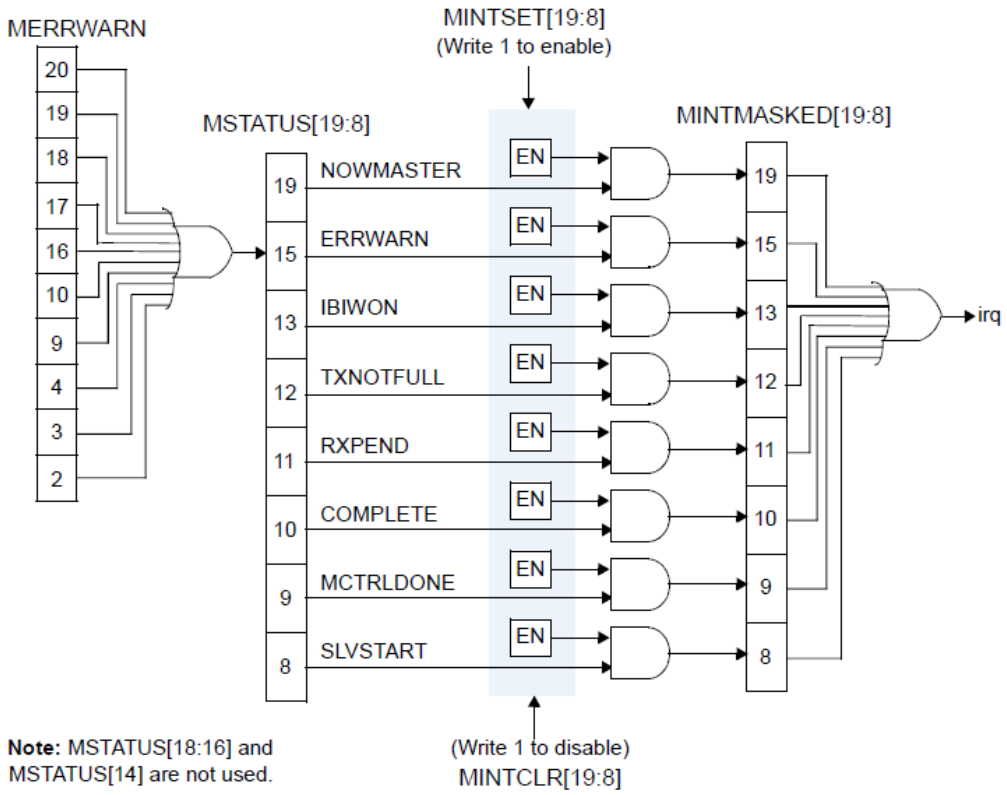


Figure 68. Interrupt Generation

The TXNOTFULL and RXPEND interrupts (MSTATUS bits [12:11]) also activate the wakeup output when the respective interrupt source is active and enabled as seen in *Figure 69*.

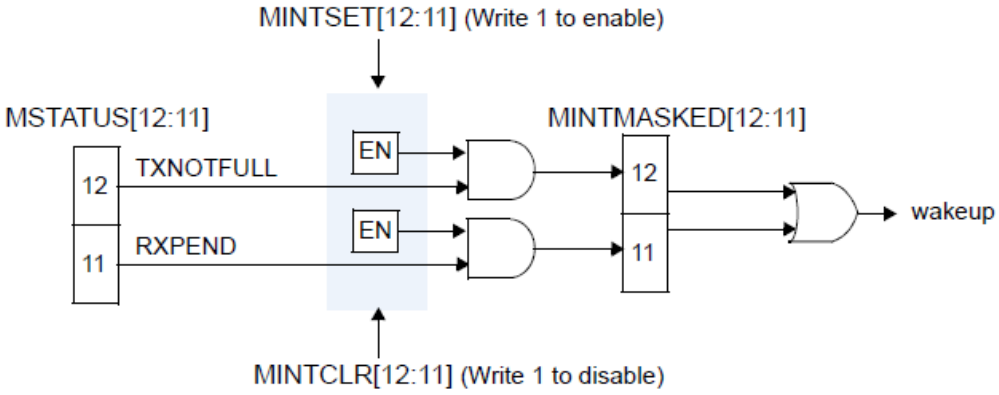


Figure 69. Wakeup Generation

Generating CCCs

The device automatically generates the following CCCs when the respective conditions occur:

- ENTDAA when the application requests DAA mode by setting bits [2:0] (REQUEST) of the MCTRL register to 4 (ProcessDAA).
- ENTHDR0 when the application generates a message in HDR-DDR mode using either the MCTRL register or the MWMSG_DDR (message mode) register.

Any other CCC sent to any or all slaves must be generated by the application using either MCTRL or message mode, as I^3C write/read messages. For example, to send broadcast CCC ENEC, use either MCTRL or message mode to generate a write message with the following controls and data:

- Address = 0x7E
- Direction = Write
- First data byte = 0x00 (ENEC)
- Second data byte = ENEC data byte (for example, 0x02 to enable bus master requests)
- End condition = STOP or repeated START

To send direct CCC SETDASA to a specific slave, use either MCTRL or message mode to generate write messages with the following controls and data:

- Message
    a. Address = 0x7E
    b. Direction = Write
    c. Data byte = 0x87 (SETDASA)
    d. End condition = Repeated START

Handling IBIs

An I^3C slave device can generate an IBI in either of two ways:

- When the I^3C bus master issues a START, the I^3C bus slave emits its own dynamic address on SDA and wins address arbitration. The MSTATUS register bit [13] (IBIWON) is then set (and interrupt generated if enabled), MSTATUS register bits [30:24] (IBIADDR) contains the address of the slave that generated the IBI (or 0x02 if the IBI is a Hot-Join request), and MSTATUS register bits [7:6] (IBITYPE) indicates the IBI type (IBI, Hot-Join request, or master request). For an IBI, the device responds according to the value in the MCTRL register bits [7:6] (IBIRESP). For a Hot-Join request or master request, the application must decide whether to ACK or NACK the request.
- From the Bus Available state, the I^3C bus slave pulls SDA low to initiate a START. The application can use either of the following methods to respond to the slave-initiated START:
    1. If the MCTRL register bits [2:0] (REQUEST) = 7 (AutoIBI), the device MS automatically emits address 0x7E when the slave initiates the START condition. When the slave wins address arbitration, the MSTATUS register bit [13] (IBIWON) is set, the MSTATUS register bits [30:24] (IBIADDR) contains the address of the slave that generated the IBI, and the MSTATUS register bits [7:6] (IBITYPE) indicates the IBI type.
    2. MCTRL register bits [2:0] (REQUEST) is set to another value (for example, 0), the application can use the SLVSTART interrupt as notification that an I^3C slave has initiated START. The application then uses MCTRL to emit a START with address 0x7E. When the slave wins address arbitration, the MSTATUS register bit [13] (IBIWON) is set, the MSTATUS register bits [30:24] (IBIADDR) contains the address of the slave that generated the IBI, and the MSTATUS register bits [7:6] (IBITYPE) indicates the IBI type.

For an IBI, the device responds according to the value in MCTRL bits [7:6] (IBIRESP). For a Hot-Join request or master request, the application must decide whether to ACK or NACK the request. The device sets MSTATUS register bit [10] (COMPLETE) (and generates an interrupt if enabled) when the IBI is complete.

Bit 2 of each I3C bus slave's BCR value indicates whether the slave provides a mandatory byte when generating an IBI. The application uses this information to write to the IBIRULES register the dynamic address of up to five I3C bus slaves that either do or do not provide an IBI. When MCTRL register bits [7:6] (IBIRESP) = 00, the device uses the IBIRULES register to determine whether the I3C bus slave that is currently generating an IBI also provides a mandatory byte with the IBI.

I3C Slave Mode Operations

When operating in I3C bus slave mode, the device implements the functions required for an I3C slave device, as defined by the MIPI Alliance Specification for I3C, including I3C protocol-related functions such as:

- Dynamic address assignment.
- Recognition of its assigned dynamic address and the I3C broadcast address.
- Responding to CCCs issued by the I3C bus master.
- Extracting write data from I3C/I2C write frames and providing the data to the application.
- Responding to I3C ENTHDRn mode commands and recognizing the I3C HDR Exit Pattern.
- Control of SDA input/output, including I3C open-drain and push-pull requirements.

In the minimum configuration, the device supports only I3C SDR mode and only the minimum subset of CCCs that are required for an I3C slave device. The bus must be controlled by an I3C bus master but may have legacy I2C devices also connected to the bus. If the device is configured with an I2C-style static address, then it may also function on an I2C bus controlled by an I2C bus master.

I3C Bus Configuration

The I3C bus main master is responsible for configuring the I3C bus at initial power-up. Configuring the I3C bus involves assigning an I3C dynamic address to each attached slave. Once the device has been enabled in slave mode, dynamic address assignment occurs without any intervention from the host application. The device automatically responds to any SETDASA or ENTDAA CCC issued by the I3C bus master. When the device has a valid dynamic address, the DYNADDR register bit [0] (DAVALID) is set, and the dynamic address is available in DYNADDR register bits [7:0] (DADDR).

Hot Join Request

An I3C slave device can join an already configured I3C bus by generating a Hot-Join request. A Hot-Join request can be used in either of the following conditions:

- The I3C slave device is physically connected to the I3C bus but is powered on after the I3C bus has been configured.
- The I3C slave device is physically connected to the I3C bus after the I3C bus has been configured. For example, a board is inserted into a system that is already powered on and configured.

Reading Data

When there is data available to be read in the device receive (from-bus) buffer, the STATUS register bit [11] (RXPEND) is set, and the current data byte or half-word can be read from the RDATAB or RDATAH register. The source of the data is the current I3C or I2C bus master.

When STATUS register bit [11] (RXPEND) = 1, the application should read the current data byte from RDATAB. If a half-word of data is available, the application can read the current half-word from RDATAH. The DATACTRL register bit [28:24] (RXCOUNT) value indicates the number of bytes of data available for reading. The STATUS register bit [11] (RXPEND) automatically self-clears when there is no more data to be read.

Writing Data

When there is space available in the transmit (to-bus) buffer, the STATUS register bit [12] (TXNOTFULL) is set, and the application can write the next byte of transmit data to either of the following registers:

- If the byte being written is the last byte to be returned in response to a read from the I3C bus master, write the byte to the WDATABE register, or the WDATAB register with the WDATAB bit [16] or bit [8] or both (END) bits are also set.
- If the byte being written is any byte other than the last byte to be returned in response to a read from the I3C bus master, write the byte to the WDATAB register with the WDATAB register bit [16] or bit [8] or both (END) bits are not set.

If there are two bytes of space available in the transmit buffer, the application can write the next two bytes of transmit data to WDATAH or WDATAHE. The DATACTRL register bits [20:16] (TXCOUNT) value indicates the number of bytes of data currently in the transmit buffer. The STATUS register bit [12] (TXNOTFULL) automatically self-clears when there is no more space available in the transmit buffer.

CCC Handling

Depending on the device hardware configuration, the device either handles a specific CCC automatically or passes the CCC to the application through the receive (from-bus) buffer. For example, regardless of the device hardware configuration, the device automatically handles CCCs related to I3C dynamic address assignment. Handling of other CCCs such as ENEC/DISEC depends on how the device is configured.

When the device receives a CCC that it does not handle automatically, it passes the CCC to the application and sets the STATUS register bit [14] (CCC). This applies to both broadcast CCCs and direct CCCs that match the device's dynamic address. STATUS bit [14] (CCC)is set in the same cycle as STATUS register bit [11] (RXPEND) and the first byte of the received data is the CCC command.

For direct GET CCCs that the device does not handle automatically, the device passes the command code to the application and sends the associated GET data from the transmit buffer. If there is no data available in the transmit buffer, the device NACKs the slave address and the master can retry the CCC.

Generating an IBI

If the configuration parameter IBI_IMPL is set to either 1 or 2, the device supports the generation of I3C In-Band Interrupts (IBIs). The IBI includes the slave's dynamic address and, if IBI_IMPL = 2, one or more bytes of payload data. As an example of using an IBI, a sensor I3C slave device can send an IBI to the I3C master when there is new or changed sensor data available.

To support the generation of IBIs, the device must have the following hardware configuration:

- IBI_IMPL = 1 or 2 (IBIs are supported).
- A clock applied to the clk_slow input for 1- s Bus Available time measurement.
- The CLOCK_SLOW_BITS, CLOCK_SLOW_MATCH, and WITH_BAMATCH parameters must be configured to measure the 1- s Bus Available time required for I3C event generation.

Switching to Bus Master Role

The I3C bus current master can transfer bus mastership to a master-capable slave by issuing a GETACCMST CCC, either independently or in response to a slave that issues a master request. For the device to receive a GETACCMST CCC and respond by switching to master mode, the following conditions must be met:

- The device must be operating in slave mode (CONFIG register bit [0] (SLVENA) = 1) and have a valid dynamic address assigned.
- The MCONFIG register bits [1:0] (MSTENA) must be set to 10.

In addition, the NOWMASTER interrupt should be enabled in the MINTSET register so that an interrupt is generated when the device switches to master mode.

Requesting Bus Mastership

If configuration parameter WITH_MASTER_REQUEST = 1 the device supports generation of I³C bus master requests. The device can issue a bus master request when it is operating in slave mode and the register bits [1:0] (MSTENA) value is 10.

To support the generation of master requests, the device must have the following hardware configuration:

- WITH_MASTER_REQUEST = 1
- A clock applied to the clk_slow input for 1- s Bus Available time measurement.
- The CLOCK_SLOW_BITS, CLOCK_SLOW_MATCH, and WITH_BAMATCH parameters must be configured to measure the 1- s Bus Available time required for I³C event generation.

The I³C bus master can disable/enable master requests using DISEC and ENEC CCCs. If configuration parameter WITH_BASIC_CCC = 1, the device automatically handles DISEC and ENEC CCCs, and the STATUS register bit [25] (MRDIS) indicates whether master requests are currently disabled. If STATUS register bit [25] (MRDIS) = 1, master requests are disabled, and the device does not generate a master request.

HDR-DDR Mode

When configuration parameter WITH_DDR = 1, the device supports HDR-DDR mode and HDR-DDR mode can be enabled by setting the CONFIG register bit [4] (DDROK) to 1.

When the device receives an HDR-DDR Command Word that matches its dynamic address, it stores the R/W bit and 7-bit command code in either the HDRCMD register or the receive buffer, depending on the hardware configuration parameter WITH_HDRCMD and the value of CONFIG register bit [10] (HDRCMD). When writing the HDR-DDR command code to the receive buffer, the device also sets the STATUS register bit [10] (RXPEND). The STATUS register bit [16] (DDRMATCH) is also set, indicating that an HDR-DDR command was received, and the command code is available. If the command is a write, subsequent bytes contain the write data. The application can read the data from the receive buffer.

I³C Timing Control

The MIPI Alliance Specification for I³C defines several Timing Control modes through which communication between an I³C master and slave can be synchronized and data sampled can be timestamped. The device can be configured to support the following Timing Control modes:

- Asynchronous Mode 0
- Synchronous Mode

Asynchronous Mode 0

In Asynchronous mode 0, the I³C slave timestamps data so that the master knows when the data was sampled even if there is a delay in delivering the sampled data to the master.

To configure the device for Timing Control Asynchronous mode 0, supply a Timing Control clock source on the clk_slow_tc pin and set the following hardware configuration parameters to the appropriate values:

- WITH_ASYNC0 = 1 (Asynchronous mode 0 supported).
- IBI_IMPL = 2 (IBIs are supported and include a payload byte).
- The CLOCK_SLOW_BITS, CLOCK_SLOW_MATCH, and WITH_BAMATCH parameters must be configured to measure the 1- s Bus Available time required for I³C IBI event generation.
- FREQ_AS_REG - Set to either 1 or 0 to include or exclude the TCCLOCK register.
- TIME_FREQ_ACC [15:8] = clk_slow_tc frequency in 0.5-MHz units:
    1. If FREQ_AS_REG = 1, TIME_FREQ_ACC [15:8] is used as the default value of TCCLOCK[FREQ].
    2. If FREQ_AS_REG = 0, TIME_FREQ_ACC [15:8] is used as the value of Frequency Byte returned in response to a GETXTIME CCC.
- TIME_FREQ_ACC [7:0] = Maximum variation of the clk_slow_tc frequency in 0.1% units:
    1. If FREQ_AS_REG = 1, TIME_FREQ_ACC [7:0] is used as the default value of TCCLOCK[ACCURACY].
    2. If FREQ_AS_REG = 0, TIME_FREQ_ACC [7:0] is used as the value of Inaccuracy Byte returned in response to a GETXTIME CCC.

Synchronous Mode

In Synchronous mode, the I³C master emits periodic time synchronization events to synchronize the clocks and sampling times of the I³C slaves. Support for Synchronous mode requires that Asynchronous mode 0 is also supported. To configure the device to support Timing Control Synchronous mode:

- Configure the device to support Asynchronous mode 0.
- Set parameter WITH_SYNC to 1 (Synchronous mode supported).

Quad SPI (QSPI) Master Control Interface Port

The device contains a QSPI master control interface port capable of single, dual, or quad data line communication. This port is also used to configure the device from an external memory when in self-boot mode.

The QSPI port can either operate in legacy mode where access and control of the port are through a software driver running on the HiFi 3z core or in memory-mapped mode where the access is automated and external memory can be directly accessed by the host. The host interface contains support for pre-fetch and catching.

QSPI Self-Boot Mode Configuration

During initial power-up, the device can either be directly configured by the system host through the I^2C or SPI slave interfaces (referred to as host-boot mode) or it can automatically load the configuration from an EEPROM or Flash through the QSPI master interface (called self-boot mode). The boot mode is selected based on the state of the SELFBOOT input pin, and this is checked internally when the device comes out of reset (exits the hardware full chip power-down state when the supplies are powered up and the $\overline{PD}$ pin is asserted high). If the SELFBOOT input pin is asserted to logic-low state then the host-boot mode is selected, while a logic-high state selects self-boot mode.

To place the device into a self-boot mode during the initial power-up, the SELFBOOT pin must be asserted to a logic high level either concurrently with or before both the $\overline{PD}$ input pin being asserted high and all supplies being powered up. Likewise, for host-boot mode, the SELFBOOT pin should instead be asserted to a logic-low level. If the use case does not require the SELFBOOT pin to be reconfigured to a multipurpose pin function (MP31 function), the pin can be tied to either IOVDD (for self-boot mode) or DGND (for host-boot mode) through a resistor (typically 100kΩ).

Once the device powers up into self-boot mode an external master clock (MCLK) source must be present to proceed. The default clock settings are configured to accept a master clock frequency of 24.576MHz. If a master clock signal of the correct frequency is not provided, the self-boot operation cannot start (or continue).

Once the self-boot operation begins loading the settings, DVDD must remain stable and within its normal operating range (whether it is internally generated or externally provided). The $\overline{PD}$ input pin must also remain stable and asserted high and the external master clock signal cannot be removed during the self-boot operation.

QSPI Self-Boot Mode Operation

The device's self-boot mode is compatible with an EEPROM or Flash memory that supports a QSPI interface with a 12MHz clock frequency and has a 3-byte address. The ADAU1797A is only compatible with certain external flash devices. For the list of requirements and compatible devices see the *External Flash Considerations* section.

During self-boot, if an app pack boot image error is detected and no valid image is found, the self-boot is stopped. The HiFi 3z is then released and ready for operation (see the *Boot Loader* section).

Universal Asynchronous Receiver/Transmitter (UART) Data Interface Port

The UART data interface port is a full-duplex peripheral compatible with PC-style industry-standard UART interfaces. The UART interface converts data between serial and parallel formats. The serial communication follows an asynchronous protocol that supports various word lengths, stop bits, and parity generation options. The UART interface includes interrupt-handling hardware, and interrupts can be generated from multiple events.

In addition to a basic UART operation mode, UART4 supports the half-duplex IrDA® (Infrared Data Association) SIR (9.6/115.2 Kbps rate) protocol and full-duplex Multi-Drop Bus (MDB/ICP v2.0) protocol. The UART interface operating mode is selectable.

Partial modem status and control functionality are supported by the UART module to allow for hardware flow control. The UARTs are DMA-capable peripherals.

The UART interface supports:

- 5 to 8 Data bits
- Programmable extra stop bit and programmable extra half stop bit.
- Even, odd, and sticky parity bit options
- 8-Stage receive FIFO with programmable threshold interrupt
- Flexible transmit and receive interrupt timings
- Three interrupt outputs for reception, transmission, and status
- Programmable automatic RTS/CTS hardware flow control
- False start bit detection

The UART interface has dedicated DMA channels with support for separate transmitter and receiver DMA master channels. They can be used in either DMA or programmed non-DMA modes of operation. The non-DMA mode requires software management of the data flow using either interrupts or polling. The DMA method requires minimal software intervention as the DMA engine itself moves the data. The UART interface has separate transmit and receive DMA channels, though they may be mixed with other peripherals at the system level. The external peripheral timers can be used to provide a hardware-assisted auto-baud detection mechanism for use with the UART.

FastDSP Core

The device features a proprietary FastDSP core optimized for low-latency audio processing use cases such as active noise cancellation and ambient transparency. The FastDSP is designed to be intuitively configured with the *SigmaStudio+* software. The core is controlled with a 27-bit program word and supports a maximum of 128 instructions per frame. The configured clock speed, DVDD voltage level, and frame rate source limit the number of instructions that can be run in each frame (*Table 23*).

Each FastDSP core instruction is configured independently, and the supported functions include biquad filters, limiters, expanders, multipliers, bitwise operations, clippers, volume controls, and weighted mixing. The Fast DSP instructions can accept input source data channels (external to the core) from the ADC inputs, DMIC inputs, Interpolators, ADMA, AMAP, HiFi 3z TIE, serial audio data ports, and ASRC inputs.

The FastDSP core provides sixteen output data channels. While the FastDSP core can maintain up to 24dBFS of headroom internally, it clips symmetrically to 0dBFS at each output channel. The FastDSP provides output clip detectors on each output channel that can be read as status bits or used as an IRQ source. By default, there is no gain adjustment between any instruction or block.

FastDSP Power and Run Control

Setting the FDSP_EN high enables the FastDSP and allows access to the core memories. All program, parameter, and data memories for the FastDSP can be read or written from any control interface or the HiFi 3z DSP when POWER_EN = 1, FDSP_EN = 1, and the PLL is locked (if in use). The FastDSP starts processing data when it is both enabled (FDSP_EN = 1) and set to run (FDSP_RUN = 1).

FastDSP Clock Speed and Frame Rate

The FastDSP core clock speed supports operation at either 24.576MHz or 49.152MHz, and this is selected with the FDSP_SPEED control bit. The 24.576MHz clock speed setting can be supported with a nominal DVDD supply voltage level of either 0.9V or 1.1V, however, the 49.152MHz setting only operates with a DVDD supply level of 1.1V. The maximum number of FastDSP instructions per frame based on the selected configuration is shown in *Table 23*.

Table 23. Maximum FastDSP Instructions per Frame

FastDSP CLOCK SPEED (MHz)	DVDD LEVEL (V)	FastDSP SOURCE FRAME RATE		
		≤ 192kHz	384kHz	768kHz
24.576	0.9 or 1.1	128 Instructions	64 Instructions	32 Instructions
49.152	1.1 Only	128 Instructions	128 Instructions	64 Instructions

The source frame rate of the FastDSP is selected with the FDSP_RATE_SOURCE bits, and this determines when the program counter starts counting each frame at 0. The frame rate must be set equal to the audio data sample rate of the fastest input source to any instruction. Supported frame rate sources include ADC channels, DMIC channels, serial audio data ports, input ASRC channels, and interpolator channels. If the fixed source setting is selected, the FastDSP frame rate can be set independently of any source. In this case, the frame rate is set relative to the clock speed using the FDSP_RATE_DIV bits.

FastDSP Input Sources

Any instruction can use any of the following as an input source: any digital microphone or ADC input channel, any serial port input channel, any ASRCI input channel, any interpolation filter channel, any HiFi 3z output channel, any audio output DMA channel, or any other FastDSP instruction output (routed through a data or accumulator register).

FastDSP Data Channels and Memory

The FastDSP core internal data channels are 28-bits (5.23 format), and provide sufficient headroom for up to 24dBFS of signal swing before clipping occurs. All input sources to and output channels from the FastDSP are limited to 24 bits (1.23 format). The FastDSP provides 16 output channels each of which is truncated to 24 bits. If any output channel data exceeds full scale, it clips symmetrically to 0dBFS. The FastDSP provides output clip detectors on each channel that can be read as status bits or used as an IRQ source.

FastDSP Supported Instructions

The function of each instruction is individually configured, and a complete list of supported instructions is provided in the *SigmaStudio+* software. The available instructions include the following:

- Single precision (27-bit fractional precision) biquad/second-order filters
- Double precision (54-bit fractional precision) biquad/second-order filters
- Lower precision (19-bit fractional precision) biquad/second-order filters
- Limiter with/without external detector loop or side chain input
- Expander with/without external detector loop or side chain input
- Ramped volume slider
- Mute function
- Sample-based time delay function
- Two input multiply function
- Linear gain function
- Two to four input weighted mixer
- Two to four input addition
- Symmetrical clipper
- Absolute value function
- Two input min and max value functions
- Bit shift function
- Bitwise and, or, xor, and invert functions
- Memory read or write
- Input to output equivalence function
- T connection for signal routing in *SigmaStudio+*

FastDSP Conditional Execution

Each instruction can be set to either always execute, or to only execute conditionally based on a specific flag result or upon certain state conditions. When an instruction does not execute (based on a condition), it can be set to either do nothing or pass its input to its output. Each instruction can generate flags for conditional execution that are based on the output of that instruction. Instruction output flag set conditions include the following:

- Output equals zero
- Output is not equal to zero
- Output is greater than zero
- Output is less than zero
- Output is greater than or equal to zero
- Output is less than or equal to zero
- Accumulator overflow

Each instruction can also conditionally execute based on the current value of certain state conditions. Instruction conditional execution states include the following:

The logic state of any multipurpose pin (MP0 to MP31) when used as a GPIO input (for a given MPxx input when configured with the corresponding MPxx_MODE bits set to 0x01). In addition, the state of any multipurpose pin configured as a GPIO output (MPxx_MODE bits set to 0x02) can be set in with the GPIOxx_OUT bits.

The state of the FastDSP generic conditional execution register bits (FDSP_REG_COND0 to FDSP_REG_COND7). Each of these bits is read/write, and to control FastDSP execution they can be configured with the control interfaces (I^2C or SPI) or directly by the HiFi 3z DSP.

The Modulo N counter equals zero. The Modulo N counter increments once for every FastDSP frame. The counter is reset to 0 after the number of frames completed is equal to the setting of the FDSP_MOD_N bit. Conditional instructions can then execute every N frame (as set by the FDSP_MOD_N bit), and this results in these instructions running at a lower rate than the configured FastDSP core frame rate.

FastDSP Filter Precision

FastDSP core instructions can be configured as biquad filters and second-order filters with a selectable level of fractional precision. These filters can be either single precision (27-bit), double precision (54-bit), or lower precision (19-bit), where using reduced fractional precision results in lower power consumption. However, care must be taken to ensure that filters have enough precision to maintain stability and create the desired filter response.

FastDSP Parameters

Each FastDSP instruction (up to a maximum of 128 instructions) has 5 associated parameters (for a maximum total of 640 parameters in a single bank). Each parameter is stored in memory as a 32-bit number, and the format of a parameter depends upon the associated instruction. Parameters contain instruction configuration information such as filter coefficients, limiter threshold and ballistic settings, and volume control settings. For example, the 5 parameters for a biquad filter instruction contain the biquad filter coefficients (B0, B1, B2, A1, A2) in a 5.27 format.

Reference the *SigmaStudio+* software for the full list of supported instructions and the associated configuration settings and parameters for each. When instantiating FastDSP instructions with the *SigmaStudio+* software, the assembler automatically maps the instruction configuration settings to the associated parameters in memory. Individual sets of 5 parameters in the parameter memory space are sequentially assigned to instructions in the order in which they are instantiated in the FastDSP code.

FastDSP Parameter Bank Switching

The FastDSP provides three separate banks of parameters designated as parameter bank A, bank B, and bank C. Each FastDSP parameter bank supports a maximum total of 128 instructions (each of which has 5 parameters for a total of 640 parameters per bank). The three banks each support the same single set of instructions but allow for instruction parameters such as filter coefficients, settings, and variables to easily be switched between for different use cases and processing scenarios.

At any given time, the FastDSP actively uses only one of the three-parameter banks. The FastDSP can be switched between Bank A, Bank B, and Bank C on the fly while the core is running. The active parameter bank for the FastDSP is selected with the FDSP_BANK_SEL bits. Instruction parameters in the inactive banks can be updated at any time, however, audible glitches may occur if parameters in the active bank are directly updated while the core is running. Parameters in the active bank can only be safely updated with a FastDSP safeload.

The bank change transition method is determined by the FDSP_RAMP_MODE bit setting. When the active parameter bank is changed (with the FDSP_BANK_SEL bits), the parameter values used for instruction processing can either be instantly changed at the start of the next frame or they can be ramped via linear interpolation between the previously selected bank and the new selected bank.

When the linear ramp mode is selected, the rate at which the ramp between the two banks occurs is selectable via the FDSP_RAMP_RATE bits. Only the parameters associated with the three biquad filter instructions are ramped. All other parameters associated with other instructions change at the beginning of the frame where the bank switch occurs and ramping begins, and parameters in banks that are actively ramping do not change during a bank switch.

The FDSP_ZERO_STATE bit can be set to clear the state of the FASTDSP memory during a bank switch. During a bank switch, this prevents the new filter settings (of the new bank) from using old data (from the previous bank) that can be recirculating in the filters and may prevent potential filter instability or audible glitches.

It is possible to stop the linear ramp of biquad filter parameters between the values in the previous and the values in the current target bank. The 6-bit FDSP_LAMBDA setting selects the point along the linear interpolation curve between the two banks at which the bank switch ramp pauses (with 0 being the beginning and 63 being the end of the ramp). To complete a bank switch without pausing set a value of 63 (default), and to pause midway set a value of 31.

The lambda value can be updated actively with the control interfaces, however once a ramped bank switch is in progress it can only be increased. The progress of the current active ramp (from 0 to 63) can be read at any time with the FDSP_CURRENT_LAMBDA bits. When this value reaches 63, the bank switch is complete, and all current parameters in use match those of the target bank. Parameters in the two banks being ramped between cannot be modified while a ramped bank switch is occurring.

An interrupt for either interrupt controller can be triggered via the IRQx_PRAMP interrupt source bits. This triggers on the first frame when a ramped bank switch is active and FDSP_CURRENT_LAMBDA equals FDSP_LAMBDA.

FastDSP Parameter Bank Copying

The instruction parameters of any given bank (source) can be copied to any other bank (target) with a single-bit write command. There are six FDSP_COPY_xy bits (where x is the source bank and y is the target bank), one for each of the six possible bank copy operations. Writing a 1 to one of these bits initiates a bank copy. Once initiated, the bank copy operation waits until the start of the next FastDSP frame and then copies the parameter content of the source bank to the destination bank while the instructions are executed. The bank copy completes at the start of the subsequent frame and takes at most two frames to complete from the initiation. Copying to the active bank (copy target) is not permitted and results in no action being taken.

FastDSP Parameter Memory Access

If the FastDSP core is enabled but not running, then reads from any parameter memory bank through the I^2C interface, SPI interface, or HiFi 3z DSP are unrestricted. However, when the core is enabled and running, only reads from the inactive parameter banks are unrestricted. While the FastDSP core is running, if multiple sources try to read the same memory location on the same cycle, the HiFi 3z DSP has priority over the I^2C and SPI interfaces, and the read attempt from the I^2C interface or the SPI interface returns all 0s. Direct reads from the memory of the active bank by any source (I^2C interface, SPI interface, HiFi 3z DSP, or mREAD instructions) are not allowed and return 0s.

Similarly, writes to all parameter banks are possible when the FastDSP core is enabled but not running, and are still permitted to inactive banks while the FastDSP is running. While the core is running, if multiple sources try to write to the same location on the same cycle, the HiFi 3z DSP has priority and the other writes do not occur.

Table 24. Memory Addressing for FastDSP Core

MEMORY	MEMORY SIZE	WORD SIZE	BASE ADDRESS (Hex)
Bank A Parameter 0	128	32	0xF0020000
Bank A Parameter 1	128	32	0xF0020080
Bank A Parameter 2	128	32	0xF0020100
Bank A Parameter 3	128	32	0xF0020180
Bank A Parameter 4	128	32	0xF0020200
Bank B Parameter 0	128	32	0xF0020280
Bank B Parameter 1	128	32	0xF0020300
Bank B Parameter 2	128	32	0xF0020380
Bank B Parameter 3	128	32	0xF0020400
Bank B Parameter 4	128	32	0xF0020480
Bank C Parameter 0	128	32	0xF0020500
Bank C Parameter 1	128	32	0xF0020580
Bank C Parameter 2	128	32	0xF0020600
Bank C Parameter 3	128	32	0xF0020680
Bank C Parameter 4	128	32	0xF0020700
State 0 (A1 High)	128	32	0xF0030000
State 1 (A2 High)	128	32	0xF0030080
State 2 (A1 Low)	128	32	0xF0030100
State 3 (A2 Low)	128	32	0xF0030180
Program	128	32	0xF0040000

FastDSP Parameter Safeload

The parameter safe load mechanism allows the parameter memory for a single instruction in the active bank to be updated while the FastDSP is running. First, Set the target instruction number with the FDSP_SL_ADDR bits (numbered in order of instantiation). Then set the new parameter values with the FDSP_SL_Px bits where x is numbered from 0 through 4 for the 5 parameters associated with the selected instruction number. Finally, write a 1 to the FDSP_SL_UPDATE bit to initiate the safeload. All parameters for the selected instruction are updated at the same time at the beginning of the next frame.

Utilize the *SigmaStudio+* software interface and FastDSP program export to identify the correct instruction number and parameter values for a given desired use case. For example, an export can be performed for instruction with the normal settings and updated settings to identify both sets of parameter values needed for a direct parameter safeload operation. Parameter safeload should be treated as an extra FastDSP instruction, and to enable using it at least one instruction must be unused (out of the maximum support instructions for a given use case, see *Table 23*).

There is a second FastDSP safeload interface that is mapped to the data memory space of the HiFi 3z DSP, which allows the HiFi 3z DSP to have word-addressable access.

HiFi 3z DSP Core

Overview

The HiFi 3z core features a 32-bit, audio DSP engine optimized for audio and voice processing and other demanding DSP functions. The HiFi 3z core combines two 32-bit × 32-bit fixed point MACs or four 24-bit × 24-bit fixed point MACs or four 32-bit × 16-bit fixed point MACs or up to eight 16-bit × 16-bit fixed point MACs, a single 32-bit IEEE floating-point multiplier, and support for dual 64-bit load/store per cycle. The processor provides on-chip debug support with control of the software state of the processor through an IEEE 1149.1 test access port, also known as JTAG. The device is software-compatible with a comprehensive ecosystem of HiFi architecture-optimized audio and voice codecs and audio enhancement software packages.

Programming

On power-up, the device must be configured with a clocking scheme and then loaded with register settings. After the codec signal path is set up, the DSP core can be programmed. The device can be programmed using the *SigmaStudio+* graphic tool provided by Analog Devices or in C++. No knowledge of writing line-level DSP code is required for graphical programming. More information about *SigmaStudio+* is available at *www.analog.com/SigmaStudio+*.

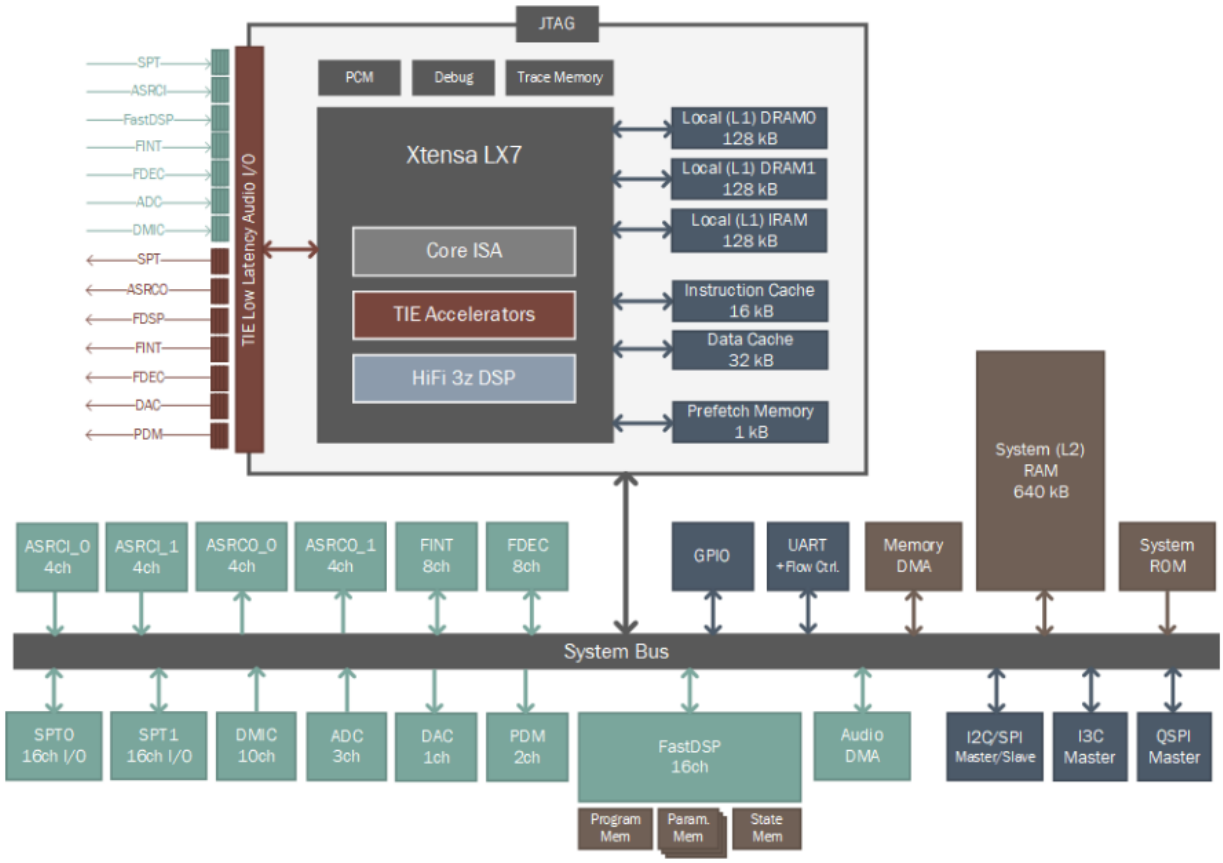


Figure 70. LX7/HiFi 3z IO, Bus, and Memory Structure

Clock Speed Control

By default, HIFI_SPEED is set to 1, the HiFi 3z DSP receives a 196.608MHz clock, and a DVDD nominally of 1.1V is applied. In this scenario, HIFI_SPEED = 1 and SEL_0V9 = 0.

If DVDD = 0.9V, the HiFi 3z DSP core receives a 49.152MHz clock, and HIFI_SPEED must = 0. At DVDD = 0.9V, SEL_0V9 must = 1.

When HIFI_SPEED = 1, the HiFi 3z core can run four times as many instructions. If the extra processing power is not needed, then operating with HIFI_SPEED = 0 reduces overall power consumption.

HIFI_SPEED can be changed during operation, but if this is done, then the PLL must always be operating with a 196.608MHz output. PLL_BYPASS cannot be selected if HIFI_SPEED is changed while the part is operating.

Interrupts

The HiFi core has several internal core interrupts.

- Three timer interrupts
- Bus write error
- Profiling interrupt
- 5 Software interrupts (1 at each priority level)
- Non-Maskable Interrupt (NMI)

In addition to the core interrupts, there are three additional external interrupt types comprising a total of 20 external interrupts.

Nine system interrupts aggregate interrupts from various system events and peripherals. The system interrupt controller can individually mask each interrupt source to every system interrupt. System interrupts can interrupt the core and/or also signal an interrupt on an MP pin. MP interrupt controls are described in the *Multipurpose Pins as Interrupt Outputs* section. The interrupt sources for system interrupts include.

- QSPI port and its Rx and Tx DDEs
- UART Rx and Tx DDEs
- Audio DMA engine, which has separate internal interrupt sources.
- FastDSP memory read and write access errors
- Memory copy read and write DMA/DDEs
- Watchdog counter
- Power-up complete signal (only useful for pin interrupts)
- PLL locking and unlocking
- Headphone amplifier protections and faults
- AVDD undervoltage detection
- ASRCs locking and unlocking
- ADC, DAC, and FastDSP output clipping detection
- Generic HiFi interrupts that the core can set through registers to aggregate interrupts from the core and other sources to an MP pin interrupt.

Which interrupt source triggered each system interrupt can be determined by the IRQx_STATUS registers in the READ_ONLY register map. All sources of each interrupt are cleared via a write of 1 to the IRQx_CLEAR bits. The interrupt status bits are sticky, such that if an interrupt source becomes true, the status reads 1 until a clear occurs, even if that interrupt source is no longer true.

Pin interrupts can either be edge or level-sensitive, there are three of each type. Each pin interrupt can map any single pin to its source. The routing of the pins to the interrupt source is set via the HIFI_EDGE_IRQx_SRC and HIFI_LEVEL_IRQx_SRC registers. Each of these interrupt pin sources can also be inverted if desired.

Audio interrupts are generated by the various audio source peripherals when a new sample is ready. Each audio interrupt can map to any single audio source via its HIFI_AUD_IRQx_SRC setting. Additionally, these can be set to block mode by setting HIFI_AUD_IRQx_TYPE to 1 to interrupt after several samples determined by HIFI_AUD_IRQx_CNTR are received. If HIFI_AUD_IRQx_TYPE is set to 0 and counter is selected as the source then an interrupt occurs every number of 24.576MHz (40.69ns) clock cycles determined by the HIFI_AUD_IRQx_CNTR, effectively acting as a timer interrupt.

Initiating RESET in a HiFi 3z Application

There are multiple ways to reset the ADAU1797A, including by pulling the PD/RST pin to GND, or by asserting the SOFT_FULL_RESET (Bit[0] of Register Address 0xF0000400).

It is important to note that SOFT_FULL_RESET is not accessible from the HiFi 3z core. It is only accessible from the I^2C/SPI port. Hence, SOFT_FULL_RESET must be written through the I^2C/SPI port.

One example where this should be considered is regarding the Watchdog Timer Interrupt. If a Watchdog Timer Interrupt occurs, the ADAU1797A must likely be reset quickly to prevent indeterminate operation. The first option is to route the Watchdog Interrupt Timer to a GPO pin on the ADAU1797A. This would allow the ADAU1797A to alert a host processor of the interrupt, and allow the host to drive the PD/RST pin low through one of its GPIO pins. Otherwise, SOFT_FULL_RESET must be written over the I^2C/SPI port.

Audio DMA

The three audio DMA blocks support moving up to 8 channels of audio into and out of the processor memory space. The audio data is stored and retrieved as interleaved data.

The DMA block supports a read and a write circular buffer pointer. The circular buffer pointer consists of an index-, start-, and end-address. The index address always points to the start of the current sample. The start- and end-address are the beginning and end of the circular buffer. For non-circular buffer mode, the end address is set to 0 [default]. All addresses are byte addresses.

Each DMA supports up to 8 channels. The channels are configured independently, such that we have up to 8 input channels and up to 8 output channels. The channel enable configuration is a simple 7-bit value. Which audio peripheral source channels are routed into the Audio DMA are selectable through routing registers. Outputs from the Audio DMA to Audio sink peripherals are selected through the peripherals routing controls.

The actual number of channels copied in, and out, is configured in a channel count register. This register defines the stride the DMA uses when moving through its circular buffer. The channel count is limited to a power of 2 numbers, such that 1, 2, 4, or 8 channels can be selected.

The format of the data can be configured as 32-bit, 24-bit, 24-bit packed, 16-bit packed, floating, and raw formats. This format is configured independently in the input and output direction.

The DMA initiates when an Fs pulse is seen from the selected audio source. The DMA copies data from the audio source towards the DSP first and issues a done when this task is completed, followed by copying data from the DSP memory towards the audio peripherals.

Because of this behavior using the DMA introduces an extra sample of latency compared to the time domain path.

Direct Audio IO

All peripheral audio sources have custom TIE instructions to directly import audio data from these sources to the Hi-Fi core. These TIE instructions allow for the lowest latency audio input to the core. Alternatively, all audio sources can also be read over the system bus.

All peripheral audio sinks have customer TIE instructions to directly output audio data to these. The sinks need to select “HiFi TIE output” in their routing controls as their input to enable this. These TIE instructions allow for the lowest latency audio input to the core. Alternatively, all audio sources can also be written over the system bus. The sources need to select “System Bus” in their routing controls as their input to enable this.

BUS Audio IO

All audio peripherals are also memory-mapped to the Hi-Fi core. Audio source data can be read over the bus and audio sinks can be written to. The sinks need to select “System Bus” in their routing controls as their input to enable this.

Debug

A JTAG interface port is included for ease of development and debugging.

FastDSP Memory Access and Safeload

The HiFi 3z DSP can directly read and write to all FastDSP memories when the FastDSP is not running. While the FastDSP core is running the HiFi 3z DSP can read and write to all non-active parameter memory banks. There are five memory locations available that the HiFi 3z DSP can use to update the current bank parameters of a single instruction of the FastDSP. *Table 25* lists the HiFi 3z DSP assembler names for the functions used for safeload.

Table 25. HiFi 3z DSP Safeload to the FastDSP Current Bank

NAME	FUNCTION
FDSP_SL_ADDR	FastDSP Safeload instruction number
FDSP_SL_P0	FastDSP Safeload Parameter B0
FDSP_SL_P1	FastDSP Safeload Parameter B1
FDSP_SL_P2	FastDSP Safeload Parameter B2
FDSP_SL_P3	FastDSP Safeload Parameter A1
FDSP_SL_P4	FastDSP Safeload Parameter A2

The functionality of this is the same as the functionality of the FastDSP safeload through the control port (see the *FastDSP Parameter Safeload* section). The parameters are also written to the FastDSP as soon as the frame executes, without needing to write a trigger bit.

Audio Data Handling

The device has two subsystems for processing audio data—a low-latency audio subsystem and a processor subsystem. The device relies on the efficient movement of audio samples within and between these subsystems to enable processing and building applications. The Low-Latency Subsystem is centered on the FDSP and an audio fabric that sends individual samples between blocks with minimal latency. The processor subsystem supports applications run on the HiFi 3z processor where blocks of samples are located in system memories and/or where individual samples can be inserted or pulled directly from the audio fabric.

Low-Latency Audio Subsystem

Within the audio subsystem, the functional blocks that act as sources broadcast their audio samples. The functional blocks that are syncs are selected from the available sources and match the source's frame rate. This system facilitates the construction of chains of blocks moving data between inputs, through the FDSP for filtering and mixing, and to output interfaces, potentially utilizing sample rate converters between major blocks. From the audio subsystem perspective, the connections to the processor subsystem function the same as any other source or sync by providing or consuming individual samples at their selected frame rate.

Processor Subsystem

The applications running on the HiFi 3z access audio data from either block of samples storied in memories, memory-mapped sample FIFOs, or specialty processor instructions that read and write sample registers directly attached to the audio subsystem routing matrix. Processing of the data is triggered by interrupts from the audio subsystem based on when data is available or needed. The choice of access method is driven by application needs for sample granularity and latency requirements.

Data Movement Between Subsystems

- With the Audio DMA's ability to source and sync up to 8 channels on 3 separate engines and access system memories, blocks of data can be stored in memories with limited supervision of the processor. These blocks can comprise interleaved or contiguous blocks connected to a single engine. The engines are independent, so they can vary the sample rate, data organization, and block sizes. This is an ideal choice for applications that process data in blocks. It reduces processor overhead, particularly in the number of interrupts required to send a receive data.
- The Direct IO (TIE) gives the most granular access to audio samples by utilizing processor instructions to give direct access to sample registers within the Audio subsystem. At any point, the processor can set a source register or read the most recent sample generated by any other source. Sample rate synchronization is handled by configuring interrupts to trigger based on an audio component's sample rate or a multiple of the sample rate. The Direct IO is targeted to applications that require the lowest latency and those that require working on individual samples. Using the direct IO for high sample rates or multiple sample rates incurs a larger interrupt latency penalty and therefore must be balanced with the ease of use and sample access latency.
- The Audio Bus Map is indented as a middle ground between the other two access methods. A set of 16 input and output FIFOs act as sources and syncs in the audio subsystem. The Audio Bus Map will collect or transmit multiple samples and multiple samples can be pushed or popped within a single sample period. By having the FIFOs mapped to system memory, the method of writing and reading is simple. The application can either use interrupts generated by the audio bus map FIFO status or use the sample interrupts. The Audio Bus Map should be considered by applications that are interested in small numbers of samples from a given source with some latency tolerance or potentially an application interested in multi-rate processing where the latency of the lower rate is strict and the higher rate can be stored in the FIFO.

Example—Simple ANC with Bluetooth Playback

In this example system, the inputs to the audio subsystem are feedforward and feedback microphones generating 192khz samples and 44.1kHz serial audio data from a Bluetooth SoC (BT). The serial audio data is then sent to the ASRC which up-samples and synchronously outputs a 192kHz stream. These three sources are then used by the FDSP to generate anti-noise and mix in the BT. The output of the FDSP is then routed to the DAC.

At this point, an additional path can utilize the existing sample streams for applications running on the processor subsystem. In this case, there could be two independent threads running on the processor that need access to data from the audio subsystem.

The first thread would conduct scene detection by taking individual samples from the FF mic and comparing the BT audio to what is seen at the FB mic. Utilizing a HIFI_INT_CTRL0 to select the ADC and HIFI_INT_CTRL3 to select every nth sample to generate processor interrupts, the corresponding thread could read the current ADC value, converted to floating point format, via the DirectIO instruction in the HiFi core.

The second thread would select the output of the ASRC and FDSP, using them as inputs to an FDEC pair down-sampling both to 48kHz. The output of the FDEC is then used as the source for the ADMA that stores the set of samples in System memory in a 1.31 format. The ADMA then generates interrupts based on the programmed block size.

Distributed DMA Engines (DDE)

The device uses several distributed DMA engines to automate copying between memories and between the UART, QSPI, and I^{3}C interfaces and memory.

The processor uses Direct Memory Access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processor can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity. The DMA controllers are dispersed throughout the infrastructure, as Distributed DMA Engines (DDE) and connected to the AXI Fabric.

The DDEs can perform transfers between a memory and a peripheral or between one memory and another memory. Two DDEs are used for Memory to Memory DMA (MemDMA). One channel is the source channel, and the second is the destination channel.

The CONFIG register is used to set up DMA parameters and operation modes. Writing CONFIG while DMA is already running causes a DMA error, except for when the EN bit is being written to 0.

Additional documentation on the DDEs can be found in the respective DDE register description section.

Serial Audio Data Interface Ports

The device provides two independently configurable serial audio data interface ports. For each of the two ports (denoted as x), input channels (SDATAI_x) and output channels (SDATAO_x) are enabled with the SPTx_IN_EN and SPTx_OUT_EN bits respectively. A given port is disabled when both input and output channels are disabled. Data is transmitted and received in twos complement (MSB first) format.

The ports each have independent bit clock (BCLK_x) and frame sync clock (FSYNC_x) pins, and each supports operation in both master mode (interface generates bit and frame clock) and slave mode (interface requires an external bit clock and frame clock). The serial audio data interface ports also support common data formats such as I^2S, left-justified, right-justified, and TDM (with up to 16 channels of data). For all support data formats, individual slots (or channels) can be configured to be 16-bit, 24-bit, or 32-bit wide.

Serial Audio Data Interface Format Configuration and Data Routing

The data format for a given serial audio data interface is selected with the SPTx_SAI_MODE bit. When this is set low the serial audio data interface operates in a two-channel (two-slot or stereo) mode. In two-channel modes, both edges of the frame clock determine where data is placed. The left audio data channel is typically mapped to channel or slot 0, and the right audio data channel is typically mapped to channel or slot 1.

The data format in two-channel modes is selected with the SPTx_DATA_FORMAT bits, and can be set to left justified mode (no delay from frame sync clock edges), I^2S mode (1-bit clock of delay from frame sync clock edges), or right justified mode (8-/12-/16-bit clocks of delay from frame sync clock edges). The length of each channel is determined by the external input (slave mode) or configured output (master mode) bit clock to frame sync clock ratio.

When the SPTx_SAI_MODE bit is set high the serial audio data interface operates in TDM mode. In TDM mode the device supports up to 16 data channels (or data slots). In TDM mode, each data channel or data slot can be 16-bit, 24-bit, or 32-bit wide (number of bit clock periods), and this is configured with the SPTx_SLOT_WIDTH bits. The frame sync clock active edge determines where the frame starts (with either no delay or a 1-bit clock of delay based on the SPTx_DATA_FORMAT setting). The data in each channel (or slot) is accepted (data input) or placed (data output) sequentially from slot 0 up to a maximum of slot 15 based on the channel (or slot) width.

Table 26. Serial Audio Data Interface Port Supported Data Format Settings

DATA FORMAT	FRAME SYNC CLOCK (SPTx_SAI_MODE)	CHANNEL/SLOT WIDTH (SPTx_SLOT_WIDTH)[1]	DATA DELAY FROM FRAME START (SPTx_DATA_FORMAT)
I^2S Mode	0x0 (50% Duty cycle)	(Don't Care)	0x0 (1-bit clock period of delay)
Left-Justified Mode	0x0 (50% Duty cycle)	(Don't Care)	0x1 (No data delay)
Right-Justified Mode	0x0 (50% Duty cycle)	(Don't Care)	0x2 (8-bit clock periods of delay)
	0x0 (50% Duty cycle)	(Don't Care)	0x3 (12-bit clock periods of delay)
	0x0 (50% Duty cycle)	(Don't Care)	0x4 (16-bit clock periods of delay)
TDM Mode	0x1 (Single Bit Pulse)	16-/24-/32-Bits (0x0/0x1/0x2)	0x1/0x0 (No Delay or 1-bit clock period of delay)

For output data, the device always provides 24-bit data. If the channel/slot width is set to 16-bits, the output data is truncated. If instead it is set to 32-bits, the 24-bit data is padded out with 8 trailing bits (either zero-padded or high-z). For input data (except for right-justified mode) the port accepts bits sequentially up to a limit of 24. Extra trailing padding bits in an input channel do not cause an error, but extra bits beyond this are ignored (truncated off). The serial port can operate with an arbitrary number of bit clock periods in each frame.

The source data for each output channel is selected with the SPTx_OUT_ROUTEn bits (for Serial port x and output channel n). Valid output data sources include the ASRC output channels, the ADC channels, the digital microphone channels, the decimator channels, the FastDSP output channels, the HiFi 3z TIE output channel, the audio output DMA channels, and the bus map outputs. To designate an audio data output channel as unused or disabled (allowing it to be driven by another device sharing the bus), the SPTx_OUT_ROUTEn bits must be set to 0x7F.

To allow multiple ICs to drive a shared serial audio data output bus, unused serial audio data interface channels (or slots) and any trailing padding bits (with SPTx_SLOT_WIDTH set for 32-bit channels) can be configured to be tri-stated (high-Z). This is configured by setting the SPTx_TRI_STATE bit (disabled by default).

Figure 71, *Figure 72*, and *Figure 73* illustrate two channel use cases (I²S, left-justified, and right-justified modes).

Figure 74 illustrates a use case where the interface is in TDM mode with timing for 8 channels (or slots).

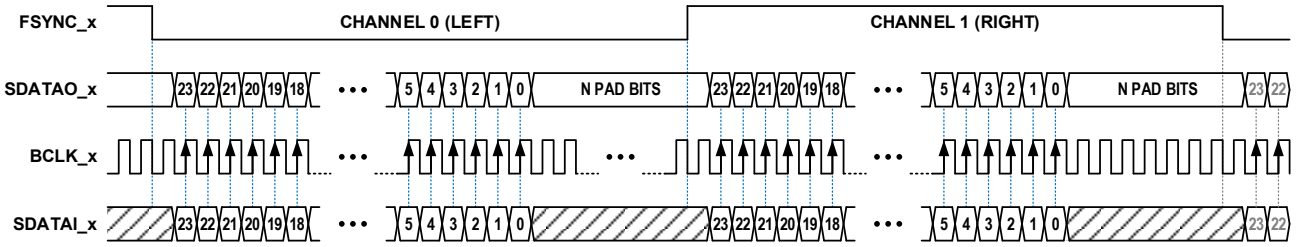


Figure 71. I²S Mode (1-Bit Clock of Delay, 24-Bit Slot Width, Any Number of Pad Bits Allowed)

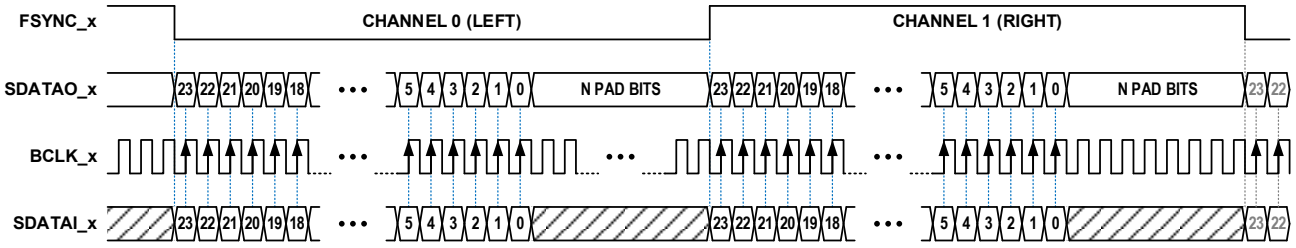


Figure 72. Left-Justified Mode (No Delay, 24-Bit Slot Width, Any Number of Pad Bits Allowed)

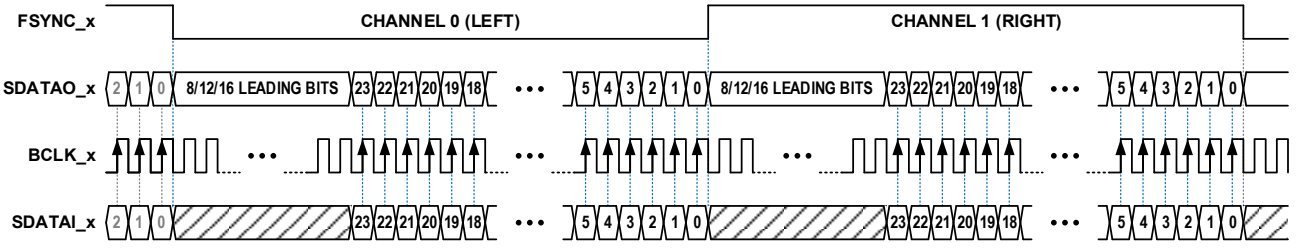


Figure 73. Right-Justified Mode (8-/12-/24-Bit Clocks of Delay, 24-Bit Slot Width)

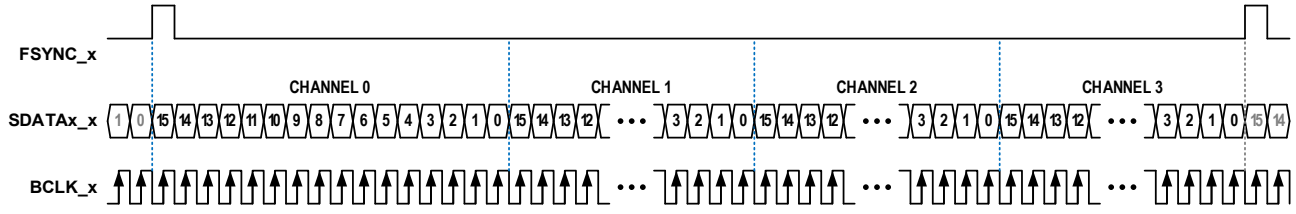


Figure 74. TDM Mode with 4 Audio Data Channels (No Delay, 16-Bit Slot Width, No Padding)

Serial Audio Data Interface Port Clock Configuration

For each of the two serial audio data interfaces, the corresponding FSYNC_x and BCLK_x pins are used to clock both the serial audio data input (SDATAI_x) and output (SDATAO_x) pins. Each port can be configured to operate either in master mode or slave mode.

In master mode, the output bit clock frequency is selected with the SPTx_BCLK_SRC bits, and the frame sync clock frequency is selected with the SPTx_LRCLK_SRC.

To instead place the device in slave mode, both the bit clock frequency setting (SPTx_BCLK_SRC) and the frame sync clock frequency (SPTx_LRCLK_SRC) should be set to the external source setting (0x0 default setting for both). In this mode, an external device or system host must provide both the bit clock and frame sync clock to the configured serial audio data interface. In slave mode, the clocks do not need to be synchronous with the external crystal or master clock input, but the external bit clock and frame sync clock must be synchronous with each other. The input bit clock from either port can also be used as the input clock reference source to the PLL to generate the internal device clocks (instead of a crystal or master clock input).

The active edge polarity of both the bit clock and frame sync clock can be inverted with the SPTx_BCLK_POL and SPTx_LRCLK_POL bits respectively. For example, while serial data and the frame sync clock are by default sampled on the rising edge of the bit clock, setting SPTx_BCLK_POL = 1 inverts this to the falling edge of the bit clock.

When configured for a high bit clock frequency (12.288MHz or higher) in slave mode (clock is an output), it is recommended to increase the drive strength settings for the high-speed output signal pins (in particular the bit clock output and the data output). The high drive strength effectively speeds up the transition times of the waveforms, thereby improving the signal integrity of the clock and data lines. The timing for serial audio data port outputs also changes based on the IOVDD voltage. While the ports can work for inputting a signal on SDATAI_x for any IOVDD and bit clock rate, the drive strength on SDATAO_x at 1.1V excludes operating at higher bit clock rates.

Multipurpose Pin Configuration

The device has 32 multipurpose pins (numbered from MP0 to MP31), each of which is by default configured to its normal function. By using the corresponding MPx_MODE bits, each multipurpose pin can also be set to one of a variety of additional functions including a general-purpose input or output, a master or crystal clock output, a PDM data or clock output, or a system interrupt output.

Care must be taken when using SELFBOOT/MP31 as a multipurpose pin. The state of this pin at power-up (later of either $\overline{PD}$ pin going high or power being applied with $\overline{PD}$ pin already high) determines whether the device self-boots, which must still be followed even if the pin is later reprogrammed to another multipurpose function.

When an MPx pin is set as a general-purpose input, the pin input state can be read by any control interface through the corresponding GPIOx_IN bit. A general-purpose input can also be used by the HiFi 3z core as an external interrupt source by using the level and edge interrupts. In addition, a general-purpose input pin can be used by the FastDSP to conditionally execute instructions or trigger the compressor.

When an MPx pin is set as a general-purpose output, the pin output state can be set by any control interface through the corresponding GPIOx_OUT bit.

Any MPx pin can be configured as either a direct crystal output or as a master clock output. When configured as a master clock output, the frequency of the output is divided down by an integer ratio from the internally generated master clock. The master clock divider ratio is selected with the MCLKO_RATE bits. By default, on initial device power-up, the SELFBOOT/MP31 pin is configured to automatically output the divided down master clock, however, multiple pins can be assigned to this same function if required by the use case.

Any MPx pin can be used to output the PDM clock or data signal for the PDM output interface. In this case, the multipurpose pin can be used to route the PDM data and clock to an external amplifier or upstream host device.

Finally, any MPx pin can be configured to output the interrupt status from any of the nine system interrupt sources (IRQ1 through IRQ9). This is described in more detail in the *Multipurpose Pins as Interrupt Outputs* section.

When using the MPx pins as a high-speed output (such as a master clock, crystal clock, PDM clock, or PDM data line), care must be taken to minimize external capacitive loading on the multipurpose pin otherwise there could be a significant increase in IOVDD current.

Table 27. Multipurpose Pin Functions

MPx PIN FUNCTION[1]	DIRECTION
General-Purpose Input (GPI) to GPIOx_IN Bits, HiFi 3z Interrupts, or FastDSP Triggers	In
General-Purpose Output (GPO) from GPIOx_OUT Bits	Out
Integer Divided Master Clock (MCLK) Output as set by the MCLKO_RATE Bits	Out
PDM Clock Output (PDM_CLK)	Out
PDM Data Output (PDM_DAT)	Out
System IRQx Output (Where x is IRQ1 through IRQ9)	Out

[1] These functions are selected instead of the pins default function with the MPx_MODE bits.

Multipurpose Pins as Interrupt Outputs

Each multipurpose pin can be used to output one of the nine system interrupt bus channels (from IRQ1 to IRQ9), and each of these channels can have a different combination of unmasked individual interrupt sources. The output of each system interrupt bus channel can be individually inverted in polarity with the corresponding IRQx_INVERT bit. Refer to the device main register map programming guide for a full list of the individual interrupt sources.

Each interrupt source has its individual status bit (IRQ_x) and a clear bit (IRQ_x_CLR). The status of each interrupt source is read with the corresponding IRQ status bit (IRQ_x). Once an interrupt status bit is set (IRQ_x) it latches and will remain set (even if that interrupt source is no longer asserted/true) until cleared by setting with the corresponding interrupt clear bit (IRQ_x_CLR).

Each interrupt source has nine mask bits (IRQn_x_MASK) where n is the system interrupt channel (from IRQ1 to IRQ9) and where x is the individual interrupt source. Each system interrupt channel (IRQn) then represents one combined interrupt signal (comprised of all IRQn unmasked individual interrupt sources) that can be assigned to a multipurpose pin. These system interrupt channels are shared by the cores as interrupt options.

Multipurpose Pin Level Control Options

Each digital pin that has both a default function and multipurpose functions has a corresponding control register (x_CTRL where x describes the default function, for example, BCLK0_CTRL for the BCLK_0/MP2 pin). The bits within these registers are used to set pin-level parameters such as weak pull-up/down, slew rate, and drive strength. The pin control settings affect the operation in both default function mode and when used in multipurpose pin modes.

When a multipurpose pin is used as an output, the drive strength can be set to 2mA, 4mA, 8mA, or 12mA with the corresponding x_DRIVE bits. In addition, when used as an output the slew rate can be set to either fast mode or slow mode with the corresponding x_SLEW bit.

If a weak pull-up or pull-down is required for a multipurpose pin (when used as either an input or output), this function is selected with the corresponding x_PULL_SEL bit. The selected pull-up or pull-down function can then be toggled (enabled or disabled) with the corresponding x_PULL_EN bit.

Boot Loader

The device employs a boot loader for loading an application pack into the system memory. This boot loader is used both in self-boot mode and host-boot mode.

To access the HiFi 3z memory, FDSP memory, or main map registers, the boot loader needs to be enabled. This is true even if an application pack is not present in the system memory.

Boot Loader in Host-Boot Mode

In host-boot mode (SELFBOOT pin = GND), an application pack can be written externally through I^2C or SPI into the L2 memory. Once the memory is configured, the PROC_EN bit must be asserted. This enables the boot loader, which then in turn enables the HiFi 3z core.

If the application pack is not successfully loaded or the L2 memory is left blank, then the PROC_EN bit must still be asserted to enable the boot loader. Once the boot loader has been enabled, access to the memories and main control registers is open.

When operating in host-boot mode, make sure to perform the following steps before writing to the L2 memory:

- Assert DVDD_EN
- Set all clock configuration registers
- Update and enable the PLL
- Assert MASTER_BLOCK_EN

Once these steps are completed, write the app pack to the L2 memory and then assert PROC_EN. If nothing is written to the L2 memory, PROC_EN still needs to be asserted to gain access to memories and main control registers.

Boot Loader in Self-Boot Mode

In self-boot mode (SELFBOOT pin = V_{IOVDD}), an application pack can be loaded through an external QSPI Flash.

If the self-boot is unsuccessful or the external flash is empty, the boot loader is enabled during the attempted self-boot. As a result, access to the memories and main control registers is open.

In self-boot mode, the internal DVDD defaults to a value of 1.1V. The boot loader needs 1.1V to attempt the boot and enable the HiFi 3z core. Once the boot loader has finished the attempted boot, then DVDD can be switched to 0.9V. Likewise, if using an external DVDD in self-boot mode, the DVDD voltage provided must be 1.1V.

In self-boot mode, the default clock configuration values assume an MCLK frequency of 24.576MHz. Hence the MCLK must be 24.576MHz during the attempted boot.

Boot Timing

The total self-boot time depends on the size of the application pack. *Figure 75* shows the sequence of events during a boot, and *Table 28* lists the formulas to calculate the total boot time for self-booting or host-booting an app pack. Note, for both *Figure 75* and *Table 28*, it is assumed that the boot occurs right after power-up and that REG_EN is high. Hence, a 15mS ramp time is needed for DVDD to fully ramp up after power-up, and that is reflected in the timing formulas.

In self-boot mode, the ADAU1797A uses QPI Mode to read from the QSPI flash. In host-boot mode, it is assumed that the SPI bulk transactions are used by the host to write to L2 memory.

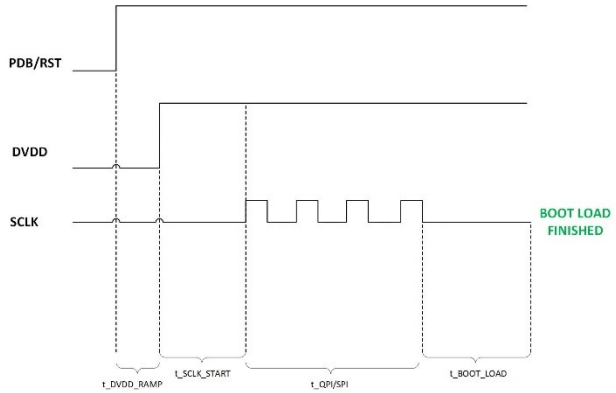


Figure 75. Boot Timing Diagram

Table 28. Boot Timing Formulas

BOOT MODE	t_DVDD_RAMP (mS)	t_SCLK_START (mS)	t_QPI/SPI (mS)	t_BOOT_LOAD (mS)
Host Boot	15	12	(8000000/SPI_SCLK) * (number of kB)	0.06* (number of kB)
Self Boot	15	12	0.59* (number of kB)	0.06* (number of kB)

As an example, we can see the timing for host-boot vs. self-boot mode for an app pack that is 300kB. For host-boot mode, we assume a SPI_SCLK of 5MHz:

Table 29. Boot Timing Example #1

BOOT MODE	TOTAL BOOT TIME (mS)
Host Boot	525
Self Boot	222

As a second example, we can see the timing for host-boot vs. self-boot mode for an app pack that is 300kB. For host-boot mode, we assume a SPI_SCLK of 10MHz:

Table 30. Boot Timing Example #2

BOOT MODE	TOTAL BOOT TIME (mS)
Host Boot	285
Self Boot	222

External Flash Considerations

The ADAU1797 is compatible and verified with only one external QSPI flash device, the MX25U3232F. The ADAU1797A has an updated self-boot relative to the ADAU1797. This updated self-boot allows for compatibility with a wider range of external QSPI flash devices. *Table 31* lists the compatible QSPI flash devices that have been tested and verified with the ADAU1797 and ADAU1797A.

Table 31. Supported QSPI Devices

EXTERNAL QSPI FLASH DEVICE	ADAU1797	ADAU1797A
MX25U3232FBHI02 (Macronix)	Supported	Supported
W25Q32JWBYIQ (Winbond)	NOT Supported	Supported
AT25QL321-UUE-T (Renesas)	NOT Supported	Supported

Note that all three of these devices either automatically assert the Quad Enable (QE) bit when the “Enter QPI Mode” command is sent, or are factory pre-programmed with their QE bit already asserted. Any device used must follow this requirement, as the QE bit is not asserted by the ADAU1797A during self-boot.

Also note that all the ordering numbers listed above are for 32Mb versions of the part, in a WLCSP package. Versions of these same parts that come in other packages, or that support 128Mb would also likely work so long as they adhere to the QE bit requirement. However, only the three specific ordering numbers listed above have been tested with the ADAU1797 and ADAU1797A.

APPLICATIONS INFORMATION

Power Supply Decoupling Capacitors

Bypass each analog and digital power supply pin to its nearest appropriate ground pin with a single 0.1µF capacitor. The connections to each side of the capacitor must be as short as possible, and the trace must be routed on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or slightly closer to the power pin if the equidistant placement is not possible. Thermal connections to the ground planes must be made on the far side of the capacitor.

Each supply signal on the board must also be bypassed with a single bulk capacitor (2.2µF).

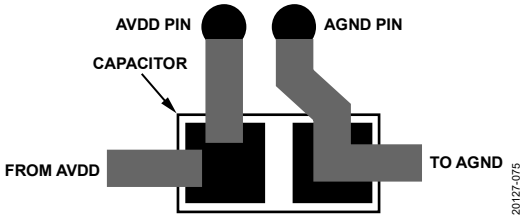


Figure 76. Recommended Power Supply Bypass Capacitor Layout

Layout

The HPVDD supply is for the headphone amplifiers. If the headphone amplifiers are enabled, the PCB trace to this pin must be wider than the traces to other pins to increase the current carrying capacity. A wider trace must also be used for the headphone output lines.

Grounding

Use a single ground plane in the application layout. Place the components in the analog signal path away from the digital signals.

REGISTER MAP

REGISTER SUMMARY: ADAU1797A

Table 32. MAINMAP Register Summary

Address	Name	Description	Reset	Access
0xF0000000	VENDOR_ID	ADI Vendor ID	0x00000041	R
0xF0000004	DEVICE_ID	Device ID	0x00001797	R
0xF0000008	REVISION	Revision Code	0x00000004	R
0xF000000C	ADC_DAC_HP_PWR	ADC, DAC, Headphone Power Controls	0x00000000	R/W
0xF0000010	DMIC_PWR	Digital Microphone Power Controls	0x00000000	R/W
0xF0000014	DMIC_PWR2	Digital Microphone Power Controls 2	0x00000000	R/W
0xF0000018	ASRC_PWR	ASRC0 Power Controls	0x00000000	R/W
0xF0000020	FINT_PWR	Interpolator Power Controls	0x00000000	R/W
0xF0000024	FDEC_PWR	Decimator Power Controls	0x00000000	R/W
0xF0000028	SAI_CLK_PWR	Serial Port, PDM Output, and Digital Mic Clock Power Controls	0x00000000	R/W
0xF000002C	CHIP_PWR	Chip Power Control	0x00000000	R/W
0xF0000030	PLL_MB_PGA_PWR	PLL and PGA Power Controls	0x00000002	R/W
0xF0000034	DSP_PWR	DSP Power Controls	0x00000000	R/W
0xF0000038	KEEPS	State Retention Controls	0x00000010	R/W
0xF000003C	DVDD_CTRL	Digital Power Supply Control	0x00000000	R/W
0xF0000040	CLK_CTRL0	Clock Control	0x00000708	R/W
0xF0000044	CLK_CTRL1	PLL Input Divider	0x00000010	R/W
0xF0000048	CLK_CTRL2	PLL Feedback Integer Divider	0x00000080	R/W
0xF000004C	CLK_CTRL3	PLL Fractional Numerator Value	0x00000000	R/W
0xF0000050	CLK_CTRL4	PLL Fractional Denominator (LSBs)	0x00000000	R/W
0xF0000054	CLK_CTRL5	PLL Update	0x00000000	R/W
0xF0000058	ADC_CTRL1	ADC Sample Rate Control	0x00000404	R/W
0xF000005C	ADC_CTRL2	ADC/Analog Input Mode Selection	0x00000000	R/W
0xF0000060	ADC_CTRL3	ADC IBias Controls	0x00000000	R/W
0xF0000064	ADC_CTRL4	ADC HPF Control 1	0x000000D0	R/W
0xF0000068	ADC_CTRL5	ADC HPF Control 2	0x000000D0	R/W
0xF000006C	ADC_CTRL6	ADC Mute and Compensation Control	0x00000040	R/W
0xF0000070	ADC_CTRL7	Analog Input Pre-Charge Time	0x00000006	R/W
0xF0000074	ADC_MUTES	ADC Channel Mutes	0x00000000	R/W
0xF0000078	ADC0_VOL	ADC Channel 0 Volume Control	0x00000040	R/W
0xF000007C	ADC1_VOL	ADC Channel 1 Volume Control	0x00000040	R/W
0xF0000080	ADC2_VOL	ADC Channel 2 Volume Control	0x00000040	R/W
0xF0000084	PGA0_CTRL1	PGA Channel 0 Gain Control MSBs, Mute, Boost, and Slew	0x00000000	R/W
0xF0000088	PGA0_CTRL2	PGA Channel 0 Gain Control LSBs	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF000008C	PGA1_CTRL1	PGA Channel 1 Gain Control MSBs, Mute, Boost, and Slew	0x00000000	R/W
0xF0000090	PGA1_CTRL2	PGA Channel 1 Gain Control LSBs	0x00000000	R/W
0xF0000094	PGA2_CTRL1	PGA Channel 2 Gain Control MSBs, Mute, Boost, and Slew	0x00000000	R/W
0xF0000098	PGA2_CTRL2	PGA Channel 2 Gain Control LSBs	0x00000000	R/W
0xF000009C	PGA_CTRL	PGA Slew Rate and Gain Link	0x00000000	R/W
0xF00000A0	DMIC_CTRL1	DMIC Clock Rate Control	0x00000033	R/W
0xF00000A4	DMIC_CTRL2	Digital Microphone Channel 0 and Channel 1 Control	0x00000004	R/W
0xF00000A8	DMIC_CTRL3	Digital Microphone Channel 2 and Channel 3 Control	0x00000004	R/W
0xF00000AC	DMIC_CTRL4	Digital Microphone Channel 4 and Channel 5 Control	0x00000004	R/W
0xF00000B0	DMIC_CTRL5	Digital Microphone Channel 6 and Channel 7 Control	0x00000004	R/W
0xF00000B4	DMIC_CTRL6	Digital Microphone Channel 8 and Channel 9 Control	0x00000004	R/W
0xF00000B8	DMIC_CTRL7	Digital Microphone Channels 0-3 Highpass Filter Control	0x000000DD	R/W
0xF00000BC	DMIC_CTRL8	Digital Microphone Channels 4-7 Highpass Filter Control	0x000000DD	R/W
0xF00000C0	DMIC_CTRL9	Digital Microphone Channels 8-9 Highpass Filter Control	0x0000000D	R/W
0xF00000C4	DMIC_CTRL10	DMIC Volume Options	0x00000004	R/W
0xF00000C8	DMIC_MUTES	Digital Microphone Channel Mute Controls	0x00000000	R/W
0xF00000CC	DMIC_VOL0	Digital Microphone Channel 0 Volume Control	0x00000040	R/W
0xF00000D0	DMIC_VOL1	Digital Microphone Channel 1 Volume Control	0x00000040	R/W
0xF00000D4	DMIC_VOL2	Digital Microphone Channel 2 Volume Control	0x00000040	R/W
0xF00000D8	DMIC_VOL3	Digital Microphone Channel 3 Volume Control	0x00000040	R/W
0xF00000DC	DMIC_VOL4	Digital Microphone Channel 4 Volume Control	0x00000040	R/W
0xF00000E0	DMIC_VOL5	Digital Microphone Channel 5 Volume Control	0x00000040	R/W
0xF00000E4	DMIC_VOL6	Digital Microphone Channel 6 Volume Control	0x00000040	R/W
0xF00000E8	DMIC_VOL7	Digital Microphone Channel 7 Volume Control	0x00000040	R/W
0xF00000EC	DMIC_VOL8	Digital Microphone Channel 8 Volume Control	0x00000040	R/W

Address	Name	Description	Reset	Access
0xF00000F0	DMIC_VOL9	Digital Microphone Channel 9 Volume Control	0x00000040	R/W
0xF00000F4	DAC_CTRL1	DAC Sample Rate, Filtering, and Power Controls	0x00000044	R/W
0xF00000F8	DAC_CTRL2	DAC Volume Link, HPF, and Mute Controls	0x00000044	R/W
0xF00000FC	DAC_CTRL3	DAC Channel 0 Highpass Filter Cutoff Control	0x0000000D	R/W
0xF0000100	DAC_VOL0	DAC Channel 0 Volume	0x00000040	R/W
0xF0000104	DAC_HF_CLIP	DAC Clipping Control	0x000000FF	R/W
0xF0000108	DAC_ROUTE0	DAC Channel 0 Routing	0x00000000	R/W
0xF000010C	HP_CTRL1	Headphone Control	0x00000024	R/W
0xF0000110	HP_CTRL2	Headphone Protections	0x00000000	R/W
0xF0000118	FDEC_CTRL1	Fast to Slow Decimator Sample Rates Channel 0 and Channel 1	0x00000047	R/W
0xF000011C	FDEC_CTRL2	Fast to Slow Decimator Sample Rates Channel 2 and Channel 3	0x00000047	R/W
0xF0000120	FDEC_CTRL3	Fast to Slow Decimator Sample Rates Channel 4 and Channel 5	0x00000047	R/W
0xF0000124	FDEC_CTRL4	Fast to Slow Decimator Sample Rates Channel 6 and Channel 7	0x00000047	R/W
0xF0000128	FDEC_ROUTE0	Fast to Slow Decimator Channel 0 Input Routing	0x00000000	R/W
0xF000012C	FDEC_ROUTE1	Fast to Slow Decimator Channel 1 Input Routing	0x00000000	R/W
0xF0000130	FDEC_ROUTE2	Fast to Slow Decimator Channel 2 Input Routing	0x00000000	R/W
0xF0000134	FDEC_ROUTE3	Fast to Slow Decimator Channel 3 Input Routing	0x00000000	R/W
0xF0000138	FDEC_ROUTE4	Fast to Slow Decimator Channel 4 Input Routing	0x00000000	R/W
0xF000013C	FDEC_ROUTE5	Fast to Slow Decimator Channel 5 Input Routing	0x00000000	R/W
0xF0000140	FDEC_ROUTE6	Fast to Slow Decimator Channel 6 Input Routing	0x00000000	R/W
0xF0000144	FDEC_ROUTE7	Fast to Slow Decimator Channel 7 Input Routing	0x00000000	R/W
0xF0000148	FINT_CTRL1	Slow to Fast Interpolator Sample Rates Channel 0/Channel 1	0x00000054	R/W
0xF000014C	FINT_CTRL2	Slow to Fast Interpolator Sample Rates Channel 2/Channel 3	0x00000054	R/W
0xF0000150	FINT_CTRL3	Slow to Fast Interpolator Sample Rates Channel 4/Channel 5	0x00000054	R/W
0xF0000154	FINT_CTRL4	Slow to Fast Interpolator Sample Rates Channel 6/Channel 7	0x00000054	R/W

Address	Name	Description	Reset	Access
0xF0000158	FINT_ROUTE0	Slow to Fast Interpolator Channel 0 Input Routing	0x00000000	R/W
0xF000015C	FINT_ROUTE1	Slow to Fast Interpolator Channel 1 Input Routing	0x00000000	R/W
0xF0000160	FINT_ROUTE2	Slow to Fast Interpolator Channel 2 Input Routing	0x00000000	R/W
0xF0000164	FINT_ROUTE3	Slow to Fast Interpolator Channel 3 Input Routing	0x00000000	R/W
0xF0000168	FINT_ROUTE4	Slow to Fast Interpolator Channel 4 Input Routing	0x00000000	R/W
0xF000016C	FINT_ROUTE5	Slow to Fast Interpolator Channel 5 Input Routing	0x00000000	R/W
0xF0000170	FINT_ROUTE6	Slow to Fast Interpolator Channel 6 Input Routing	0x00000000	R/W
0xF0000174	FINT_ROUTE7	Slow to Fast Interpolator Channel 7 Input Routing	0x00000000	R/W
0xF0000178	ASRCI0_CTRL	Input ASRC0 Control, Source, and Rate Selection	0x00000004	R/W
0xF000017C	ASRCI0_ROUTE01	Input ASRC0 Channel 0 and 1 Input Routing	0x00000000	R/W
0xF0000180	ASRCI0_ROUTE23	Input ASRC0 Channel 2 and 3 Input Routing	0x00000000	R/W
0xF0000184	ASRCO0_CTRL	Output ASRC0 Control	0x00000004	R/W
0xF0000188	ASRCO0_ROUTE0	Output ASRC0 Channel 0 Input Routing	0x00000000	R/W
0xF000018C	ASRCO0_ROUTE1	Output ASRC0 Channel 1 Input Routing	0x00000000	R/W
0xF0000190	ASRCO0_ROUTE2	Output ASRC0 Channel 2 Input Routing	0x00000000	R/W
0xF0000194	ASRCO0_ROUTE3	Output ASRC0 Channel 3 Input Routing	0x00000000	R/W
0xF0000198	ASRCI1_CTRL	Input ASRC1 Control, Source, and Rate Selection	0x00000004	R/W
0xF000019C	ASRCI1_ROUTE01	Input ASRC1 Channel 0 and 1 Input Routing	0x00000000	R/W
0xF00001A0	ASRCI1_ROUTE23	Input ASRC1 Channel 2 and 3 Input Routing	0x00000000	R/W
0xF00001A4	ASRCO1_CTRL	Output ASRC1 Control	0x00000004	R/W
0xF00001A8	ASRCO1_ROUTE0	Output ASRC1 Channel 0 Input Routing	0x00000000	R/W
0xF00001AC	ASRCO1_ROUTE1	Output ASRC1 Channel 1 Input Routing	0x00000000	R/W
0xF00001B0	ASRCO1_ROUTE2	Output ASRC1 Channel 2 Input Routing	0x00000000	R/W
0xF00001B4	ASRCO1_ROUTE3	Output ASRC1 Channel 3 Input Routing	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF00001B8	FDSP_RUN	FastDSP Run	0x00000000	R/W
0xF00001BC	FDSP_SPEED	FastDSP Core Clock Speed Control	0x00000001	R/W
0xF00001C0	FDSP_CTRL1	FastDSP Current Bank and Bank Ramping Controls	0x00000070	R/W
0xF00001C4	FDSP_CTRL2	FastDSP Bank Ramping Stop Point	0x0000003F	R/W
0xF00001C8	FDSP_CTRL3	FastDSP Bank Copying	0x00000000	W
0xF00001CC	FDSP_CTRL4	FastDSP Frame Rate Source	0x00000000	R/W
0xF00001D0	FDSP_CTRL5	FastDSP Fixed Rate Division	0x0000007F	R/W
0xF00001D4	FDSP_CTRL6	FastDSP Modulo N Counter for Lower Rate Conditional Execution	0x00000000	R/W
0xF00001D8	FDSP_CTRL7	FastDSP Generic Conditional Execution Registers	0x00000000	R/W
0xF00001DC	FDSP_SL_ADDR	Fast DSP Safeload Address	0x00000000	R/W
0xF00001E0	FDSP_SL_P0	FastDSP Safeload Parameter 0 Value	0x00000000	R/W
0xF00001E4	FDSP_SL_P1	FastDSP Safeload Parameter 1 Value	0x00000000	R/W
0xF00001E8	FDSP_SL_P2	FastDSP Safeload Parameter 2 Value	0x00000000	R/W
0xF00001EC	FDSP_SL_P3	FastDSP Safeload Parameter 3 Value	0x00000000	R/W
0xF00001F0	FDSP_SL_P4	FastDSP Safeload Parameter 4 Value	0x00000000	R/W
0xF00001F4	FDSP_SL_UPDATE	FastDSP Safeload Update	0x00000000	W
0xF00001F8	HIFI_CTRL1	HiFi Run	0x00000000	R/W
0xF00001FC	HIFI_CTRL2	HiFi Speed	0x00000001	R/W
0xF0000200	HIFI_INT_CTRL0	HiFi Audio Interrupts Source Selection 1	0x00000000	R/W
0xF0000204	HIFI_INT_CTRL1	HiFi Audio Interrupts Source Selection 2	0x00000000	R/W
0xF0000208	HIFI_INT_CTRL2	HiFi Audio Interrupts Source Selection 3	0x00000000	R/W
0xF0000210	HIFI_INT_CTRL3	HiFi Audio Interrupt Counters 1	0x00000000	R/W
0xF0000218	HIFI_INT_CTRL4	HiFi Audio Interrupt Counters 2	0x00000000	R/W
0xF0000220	HIFI_INT_CTRL5	HiFi Audio Interrupt Counters 3	0x00000000	R/W
0xF0000228	HIFI_INT_CTRL6	HiFi Audio Interrupt Counters 4	0x00000000	R/W
0xF0000230	HIFI_INT_CTRL7	HiFi Audio Interrupt Counters 5	0x00000000	R/W
0xF0000234	HIFI_INT_CTRL8	HiFi MP GPI Edge Sensitive Interrupts Source Selection 1	0x00000000	R/W
0xF0000238	HIFI_INT_CTRL9	HiFi MP GPI Edge Sensitive Interrupts Source Selection 2	0x00000000	R/W
0xF000023C	HIFI_INT_CTRL10	HiFi MP GPI Edge Sensitive Interrupts Source Selection 3	0x00000000	R/W
0xF0000248	HIFI_INT_CTRL11	HiFi MP GPI Level Sensitive Interrupts Source Selection 1	0x00000000	R/W
0xF000024C	HIFI_INT_CTRL12	HiFi MP GPI Level Sensitive Interrupts Source Selection 2	0x00000000	R/W
0xF0000250	HIFI_INT_CTRL13	HiFi MP GPI Level Sensitive Interrupts Source Selection 3	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF0000254	HIFI_INT_CTRL14	HiFi Generic System Interrupt Sources for Pin Signaling	0x00000000	R/W
0xF0000258	MP_CTRL1	Multipurpose Pins 0/1/2/3 Mode Select	0x00000000	R/W
0xF000025C	MP_CTRL2	Multipurpose Pins 4/5/6/7 Mode Select	0x00000000	R/W
0xF0000260	MP_CTRL3	Multipurpose Pins 8/9/10/11 Mode Select	0x00000000	R/W
0xF0000264	MP_CTRL4	Multipurpose Pins 12/13/14/15 Mode Select	0x00000000	R/W
0xF0000268	MP_CTRL5	Multipurpose Pins 16/1718/19 Mode Select	0x00000000	R/W
0xF000026C	MP_CTRL6	Multipurpose Pin 20/21/22/23 Mode Select	0x00000000	R/W
0xF0000270	MP_CTRL7	Multipurpose Pin 24/25/26/27 Mode Select	0x00000000	R/W
0xF0000274	MP_CTRL8	Multipurpose Pin 28/29/30/31 Mode Select	0x14000000	R/W
0xF0000298	MP_CTRL9	General-Purpose Input Debounce Control and Master Clock Output Rate Selection	0x00000010	R/W
0xF000029C	MP_CTRL10	General-Purpose Outputs Control	0x00000000	R/W
0xF00002A0	FSYNC0_CTRL	FSYNC_0 Pin Controls	0x00000005	R/W
0xF00002A4	BCLK0_CTRL	BCLK_0 Pin Controls	0x00000005	R/W
0xF00002A8	SDATAO0_CTRL	SDATAO_0 Pin Control	0x00000005	R/W
0xF00002AC	SDATAI0_CTRL	SDATAI_0 Pin Controls	0x00000005	R/W
0xF00002B0	FSYNC1_CTRL	FSYNC_1 Pin Controls	0x00000005	R/W
0xF00002B4	BCLK1_CTRL	BCLK_1 Pin Controls	0x00000005	R/W
0xF00002B8	SDATAO1_CTRL	SDATAO_1 Pin Controls	0x00000005	R/W
0xF00002BC	SDATAI1_CTRL	SDATAI_1 Pin Controls	0x00000005	R/W
0xF00002C0	DMIC_CLK0_CTRL	DMIC_CLK0 Pin Controls	0x00000005	R/W
0xF00002C4	DMIC_CLK1_CTRL	DMIC_CLK1 Pin Controls	0x00000005	R/W
0xF00002C8	DMIC01_CTRL	DMIC01 Pin Controls	0x00000005	R/W
0xF00002CC	DMIC23_CTRL	DMIC23 Pin Controls	0x00000005	R/W
0xF00002D0	DMIC45_CTRL	DMIC45 Pin Controls	0x00000005	R/W
0xF00002D4	DMIC67_CTRL	DMIC67 Pin Controls	0x00000005	R/W
0xF00002D8	DMIC89_CTRL	DMIC89 Pin Controls	0x00000005	R/W
0xF00002DC	QSPIM_CLK_CTRL	QSPIM_CLK Pin Controls	0x00000005	R/W
0xF00002E0	QSPIM_CS0_CTRL	QSPIM_CS0 Pin Controls	0x00000005	R/W
0xF00002E4	QSPIM_CS1_CTRL	QSPIM_CS1 Pin Controls	0x00000005	R/W
0xF00002E8	QSPIM_SDIO0_CTRL	QSPIM_SDIO0 Pin Controls	0x00000005	R/W
0xF00002EC	QSPIM_SDIO1_CTRL	QSPIM_SDIO1 Pin Controls	0x00000005	R/W
0xF00002F0	QSPIM_SDIO2_CTRL	QSPIM_SDIO2 Pin Controls	0x00000005	R/W
0xF00002F4	QSPIM_SDIO3_CTRL	QSPIM_SDIO3 Pin Controls	0x00000005	R/W
0xF00002F8	JTAG_TRST_CTRL	JTAG_TRST Pin Controls	0x00000005	R/W

Address	Name	Description	Reset	Access
0xF00002FC	JTAG_TMS_CTRL	JTAG_TMS Pin Controls	0x00000005	R/W
0xF0000300	JTAG_TCK_CTRL	JTAG_TCK Pin Controls	0x00000005	R/W
0xF0000304	JTAG_TDI_CTRL	JTAG_TDI Pin Controls	0x00000005	R/W
0xF0000308	JTAG_TDO_CTRL	JTAG_TDO Pin Controls	0x00000005	R/W
0xF000030C	UART_TX_CTRL	UART_TX Pin Controls	0x00000005	R/W
0xF0000310	UART_RX_CTRL	UART_RX Pin Controls	0x00000005	R/W
0xF0000314	UART_RTS_CTRL	UART_RTS Pin Controls	0x00000005	R/W
0xF0000318	UART_CTS_CTRL	UART_CTS Pin Controls	0x00000005	R/W
0xF000031C	SELFBOOT_CTRL	SELFBOOT Pin Controls	0x00000001	R/W
0xF0000320	I2C_SPI_CTRL	SDA/MISO Pin Controls	0x00000000	R/W
0xF0000324	I3C_CTRL	SDA/MISO Pin Controls	0x00000003	R/W
0xF0000328	ADDR0_CTRL	SELFBOOT Pin Controls	0x00000005	R/W
0xF000032C	ADDR1_CTRL	SELFBOOT Pin Controls	0x00000005	R/W
0xF0000334	IRQ_INVERT	System IRQ MP Pin Output Signaling	0x00000000	R/W
0xF0000338 to 0xF0000398 by 12	IRQn_MASK1	System IRQ[n] Masking	0xFFFFFFFF	R/W
0xF000033C to 0xF000039C by 12	IRQn_MASK2	System IRQ[n] Masking	0xFFFF3F2F	R/W
0xF0000340 to 0xF00003A0 by 12	IRQn_MASK3	System IRQ[n] Masking	0x9FF3113F	R/W
0xF00003A4	IRQ_CLR1	System IRQ Clear 1	0x00000000	R/W
0xF00003A8	IRQ_CLR2	System IRQ Clear 2	0x00000000	R/W
0xF00003AC	IRQ_CLR3	System IRQ Clear 3	0x00000000	R/W
0xF0000400	RESETS	Chip Resets	0x00000000	W
0xF0000404	FDSP_STATUS	FastDSP Current Lambda	0x0000003F	R/W
0xF0000408	STATUS1	Chip Status 1	0x00000000	R
0xF000040C	DVDD_STATUS	Digital Power Supply Status	0x00000000	R
0xF0000414	GPI1	General-Purpose Input Read 0 to Input Read 31	0x00000000	R
0xF0000424	IRQ_STATUS1	System IRQ Status 1	0x00000000	R
0xF0000428	IRQ_STATUS2	System IRQ Status 2	0x00000000	R
0xF000042C	IRQ_STATUS3	System IRQ Status 3	0x00000000	R
0xF0000500	SPT0_CTRL1	Serial Port 0 Control 1	0x00000000	R/W
0xF0000504	SPT0_CTRL2	Serial Port 0 Control 2	0x00000000	R/W
0xF0000508	SPT0_ROUTE0	Serial Port 0 Output Routing Slot 0 (Left)	0x00000010	R/W
0xF000050C	SPT0_ROUTE1	Serial Port 0 Output Routing Slot 1 (Right)	0x00000011	R/W
0xF0000510	SPT0_ROUTE2	Serial Port 0 Output Routing Slot 2	0x00000012	R/W
0xF0000514	SPT0_ROUTE3	Serial Port 0 Output Routing Slot 3	0x00000013	R/W
0xF0000518	SPT0_ROUTE4	Serial Port 0 Output Routing Slot 4	0x00000014	R/W

Address	Name	Description	Reset	Access
0xF000051C	SPT0_ROUTE5	Serial Port 0 Output Routing Slot 5	0x00000015	R/W
0xF0000520	SPT0_ROUTE6	Serial Port 0 Output Routing Slot 6	0x00000016	R/W
0xF0000524	SPT0_ROUTE7	Serial Port 0 Output Routing Slot 7	0x00000017	R/W
0xF0000528	SPT0_ROUTE8	Serial Port 0 Output Routing Slot 8	0x00000018	R/W
0xF000052C	SPT0_ROUTE9	Serial Port 0 Output Routing Slot 9	0x00000019	R/W
0xF0000530	SPT0_ROUTE10	Serial Port 0 Output Routing Slot 10	0x0000001A	R/W
0xF0000534	SPT0_ROUTE11	Serial Port 0 Output Routing Slot 11	0x0000001B	R/W
0xF0000538	SPT0_ROUTE12	Serial Port 0 Output Routing Slot 12	0x0000001C	R/W
0xF000053C	SPT0_ROUTE13	Serial Port 0 Output Routing Slot 13	0x0000001D	R/W
0xF0000540	SPT0_ROUTE14	Serial Port 0 Output Routing Slot 14	0x0000001E	R/W
0xF0000544	SPT0_ROUTE15	Serial Port 0 Output Routing Slot 15	0x0000001F	R/W
0xF0000548	SPT1_CTRL1	Serial Port 1 Control 1	0x00000000	R/W
0xF000054C	SPT1_CTRL2	Serial Port 1 Control 2	0x00000000	R/W
0xF0000550	SPT1_ROUTE0	Serial Port 1 Output Routing Slot 0 (Left)	0x00000010	R/W
0xF0000554	SPT1_ROUTE1	Serial Port 1 Output Routing Slot 1 (Right)	0x00000010	R/W
0xF0000558	SPT1_ROUTE2	Serial Port 1 Output Routing Slot 2	0x00000010	R/W
0xF000055C	SPT1_ROUTE3	Serial Port 1 Output Routing Slot 3	0x00000010	R/W
0xF0000560	SPT1_ROUTE4	Serial Port 1 Output Routing Slot 4	0x00000010	R/W
0xF0000564	SPT1_ROUTE5	Serial Port 1 Output Routing Slot 5	0x00000010	R/W
0xF0000568	SPT1_ROUTE6	Serial Port 1 Output Routing Slot 6	0x00000010	R/W
0xF000056C	SPT1_ROUTE7	Serial Port 1 Output Routing Slot 7	0x00000010	R/W
0xF0000570	SPT1_ROUTE8	Serial Port 1 Output Routing Slot 8	0x00000010	R/W
0xF0000574	SPT1_ROUTE9	Serial Port 1 Output Routing Slot 9	0x00000010	R/W
0xF0000578	SPT1_ROUTE10	Serial Port 1 Output Routing Slot 10	0x00000010	R/W
0xF000057C	SPT1_ROUTE11	Serial Port 1 Output Routing Slot 11	0x00000010	R/W
0xF0000580	SPT1_ROUTE12	Serial Port 1 Output Routing Slot 12	0x00000010	R/W
0xF0000584	SPT1_ROUTE13	Serial Port 1 Output Routing Slot 13	0x00000010	R/W
0xF0000588	SPT1_ROUTE14	Serial Port 1 Output Routing Slot 14	0x00000010	R/W
0xF000058C	SPT1_ROUTE15	Serial Port 1 Output Routing Slot 15	0x00000010	R/W
0xF0000590	PDM_CTRL1	PDM Sample Rate and Filtering Control	0x00000004	R/W
0xF0000594	PDM_CTRL2	PDM Muting, Highpass, and Volume Options	0x000000C4	R/W
0xF0000598	PDM_CTRL3	PDM Highpass Filter Cutoff Control	0x0000000D	R/W
0xF000059C	PDM_VOL0	PDM Output Channel 0 Volume	0x00000040	R/W
0xF00005A0	PDM_VOL1	PDM Output Channel 1 Volume	0x00000040	R/W
0xF00005A4	PDM_ROUTE0	PDM Output Channel 0 Routing	0x00000000	R/W
0xF00005A8	PDM_ROUTE1	PDM Output Channel 1 Routing	0x00000000	R/W
0xF0000600 to 0xF0000608 by 4	ADMA_IN_CONFIGn	Audio DMA Input Format Select	0x00000000	R/W
0xF0000610 to 0xF0000618 by 4	ADMA_OUT_CONFIGn	Audio DMA Output Format Select	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF0000620 to 0xF0000628 by 4	ADMA_FS_SELECTn	Audio DMA Audio FS Select	0x00000000	R/W
0xF0000640 to 0xF0000648 by 4	ADMA_IN_MASKn	Audio DMA Input Mask Channel Enable/Mask	0x00000000	R/W
0xF0000650 to 0xF0000658 by 4	ADMA_IN_CBEGINn	Audio Input DMA Circular Buffer Begin Address	0x00000000	R/W
0xF0000660 to 0xF0000668 by 4	ADMA_IN_CENDn	Audio Input DMA Circular Buffer End Address	0x00000000	R/W
0xF0000670 to 0xF0000678 by 4	ADMA_IN_CHAN_STRIDEn	Audio Input DMA Channel Stride	0x00000000	R/W
0xF0000680 to 0xF0000688 by 4	ADMA_IN_FRAME_STRIDEn	Audio Input DMA Frame Stride	0x00000000	R/W
0xF0000690 to 0xF0000698 by 4	ADMA_IN_BLOCK_SIZEn	Audio Input DMA Block Size	0x00000000	R/W
0xF00006A0 to 0xF00006A8 by 4	ADMA_IN_CURR_BLOCK_ADDRn	Audio Input DMA Current Block Address	0x00000000	R
0xF00006B0 to 0xF00006B8 by 4	ADMA_IN_PREV_BLOCK_ADDRn	Audio Input DMA Previous Block Address	0x00000000	R
0xF00006C0 to 0xF00006C8 by 4	ADMA_IN_SINGLE_BLOCK_ADDRn	Audio Input DMA Single Mode Block Address	0x00000000	R/W
0xF00006D0 to 0xF00006D8 by 4	ADMA_IN_WRITE_ADDRn	Audio Input DMA Block Address	0x00000000	R
0xF00006E0 to 0xF00006E8 by 4	ADMA_OUT_CBEGINn	Audio Output DMA Circular Buffer Begin Address	0x00000000	R/W
0xF00006F0 to 0xF00006F8 by 4	ADMA_OUT_CENDn	Audio Output DMA Circular Buffer End Address	0x00000000	R/W
0xF0000700 to 0xF0000708 by 4	ADMA_OUT_CHAN_STRIDEn	Audio Output DMA Channel Stride	0x00000000	R/W
0xF0000710 to 0xF0000718 by 4	ADMA_OUT_FRAME_STRIDEn	Audio Output DMA Frame Stride	0x00000000	R/W
0xF0000720 to 0xF0000728 by 4	ADMA_OUT_BLOCK_SIZEn	Audio Output DMA Block Size	0x00000000	R/W
0xF0000730 to 0xF0000738 by 4	ADMA_OUT_READ_ADDRn	Audio Output DMA Block Address	0x00000000	R
0xF0000740 to 0xF0000748 by 4	ADMA_OUT_CURR_BLOCK_ADDRn	Audio Output DMA Current Block Address	0x00000000	R
0xF0000750 to 0xF0000758 by 4	ADMA_OUT_SINGLE_BLOCK_ADDRn	Audio Output DMA Single Mode Block Address	0x00000000	R/W
0xF0000760 to 0xF0000768 by 4	ADMA_OUT_PREV_BLOCK_ADDRn	Audio Output DMA Previous Block Address	0x00000000	R
0xF0000770 to 0xF0000778 by 4	ADMA_OUT_MASKn	Audio DMA Output Mask	0x00000000	R/W
0xF0000790 to 0xF0000798 by 4	ADMA_IN_CONTROLn	Audio DMA Input Control	0x00000000	R/W
0xF00007A0 to 0xF00007A8 by 4	ADMA_OUT_CONTROLn	Audio DMA Output Control	0x00000000	R/W
0xF00007B0	ADMA_INTERRUPT_CONTROL	Audio DMA Interrupt Control	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF00007C0	ADMA_INTERRUPT_STATUS	Audio DMA Interrupt Status	0x00000000	R/W
0xF00007D0	ADMA_DONE_STATUS	Audio DMA Done Status	0x00000000	R/W
0xF0000800 to 0xF0000808 by 4	ADMA_IN_ROUTE0n	Audio Input DMA Channels 0 to 3 Routing	0x00000000	R/W
0xF0000810 to 0xF0000818 by 4	ADMA_IN_ROUTE1n	Audio Input DMA Channels 4 to 7 Routing	0x00000000	R/W
0xF000081C	ADMA_WR_ERR_CODE	Audio DMA Write Error Code (AXI Write Transaction Address).	0x00000000	R
0xF0000820	ADMA_RD_ERR_CODE	Audio DMA Read Error Code (AXI Read Transaction Address)	0x00000000	R
0xF0000824	ADMA_NAN_ERR_CODE	Audio DMA NAN Error Code (Fraction Nan Value)	0x00000000	R
0xF0000828	ADMA_ERR_ACK	Audio DMA Error Acknowledge	0x00000000	R/W
0xF0000C68	HOST_INFO	Host Information Register	0x00100000	R/W
0xF0000D00	AMAP_FIFO_RESET_REG	FIFO_RESET_N	0xFFFFFFFF	R/W
0xF0000D04	AMAP_CHANNEL_SEL_REG	Channel_select	0x00000000	R/W
0xF0000D08 to 0xF0000D44 by 4	AMAP_FLAG_THRESHOLD_REGn	AMAP_Flag_Threshold	0x00006262	R/W
0xF0000D48 to 0xF0000D84 by 4	AMAP_CONFIG_REGn	CONFIG_REG	0x00000303	R/W
0xF0000D88 to 0xF0000DC4 by 4	AMAP_FLAG_REGn	FLAG Register	0x00000303	R/W
0xF0000E08 to 0xF0000E44 by 4	AMAP_ROUTE_REGn	Route Register	0x00000900	R/W
0xF0000E48	AMAP_ERROR_STATUS_REG	Error Status Register	0x00000000	R/W
0xF0000E4C	AMAP_INTERRUPT_MASK_REG	Interrupt Mask Register	0x00000000	R/W
0xF0000E50	AMAP_INTERRUPT_STATUS_REG	Interrupt Status Register	0x00000000	R/W
0xF0000F00	ADMA_PWR	ADMA power controls for ADMA0, 1, and 2	0x00000000	R/W
0xF0000F04	AMAP_PWR	AMAP clock enable	0x00000000	R/W
0xF0000F50	FS_SELECT_REG1	Sample Rate Select Register1 for Audio Interface from Xtensa	0x00090909	R/W
0xF0000F54	FS_SELECT_REG2	Sample Rate Select Register2 for Audio Interface from Xtensa	0x00000909	R/W
0xF0000F58	FS_SELECT_REG3	Sample Rate Select Register3 for Audio Interface from Xtensa	0x09090909	R/W
0xF0000F5C	FS_SELECT_REG4	Sample Rate Select Register4 for Audio Interface from Xtensa	0x09090909	R/W
0xF0000F60	FS_SELECT_REG5	Sample Rate Select Register5 for Audio Interface from Xtensa	0x09090909	R/W
0xF0000F64	FS_SELECT_REG6	Sample Rate Select Register6 for Audio Interface from Xtensa	0x09090909	R/W
0xF0000F68	FS_SELECT_REG7	Sample Rate Select Register7 for Audio Interface from Xtensa	0x00090909	R/W
0xF00011FC	WATCHDOG	Watchdog Maximum Count and Prescale	0x00000000	R/W

Table 33. SPI MASTER (SPI) Register Summary

Address	Name	Description	Reset	Access
0xF0010004	CTL	Control Register	0x00000040	R/W
0xF0010008	RXCTL	Receive Control Register	0x00000000	R/W
0xF001000C	TXCTL	Transmit Control Register	0x00000000	R/W
0xF0010010	CLK	Clock Rate Register	0x00000003	R/W
0xF0010014	DLY	Delay Register	0x00000301	R/W
0xF0010018	SLVSEL	Slave Select Register	0x0000FE00	R/W
0xF001001C	RWC	Received Word Count Register	0x00000000	R/W
0xF0010020	RWCR	Received Word Count Reload Register	0x00000000	R/W
0xF0010024	TWC	Transmitted Word Count Register	0x00000000	R/W
0xF0010028	TWCR	Transmitted Word Count Reload Register	0x00000000	R/W
0xF0010030	IMSK	Interrupt Mask Register	0x00000000	R
0xF0010034	IMSK_CLR	Interrupt Mask Clear Register	0x00000000	R/W
0xF0010038	IMSK_SET	Interrupt Mask Set Register	0x00000000	R/W
0xF0010040	STAT	Status Register	0x00440001	R/W
0xF0010044	ILAT	Masked Interrupt Condition Register	0x00000000	R
0xF0010048	ILAT_CLR	Masked Interrupt Clear Register	0x00000000	R/W
0xF0010050	RFIFO	Receive FIFO Data Register	0x00000000	R
0xF0010058	TFIFO	Transmit FIFO Data Register	0x00000000	W
0xF0010060	MMRDH	Memory Mapped Read Header	0x00000000	R/W
0xF0010064	MMTOP	SPI Memory Top Address	0x00000000	R/W

Table 34. MEMCOPY DDE0 (DDE) Register Summary

Address	Name	Description	Reset	Access
0xF0011000	DSCPTR_NXT	Pointer to Next Initial Descriptor	0x00000000	R/W
0xF0011004	ADDRSTART	Start Address of Current Buffer	0x00000000	R/W
0xF0011008	CFG	Configuration Register	0x00000000	R/W
0xF001100C	XCNT	Inner Loop Count Start Value	0x00000000	R/W
0xF0011010	XMOD	Inner Loop Address Increment	0x00000000	R/W
0xF0011014	YCNT	Outer Loop Count Start Value (2D only)	0x00000000	R/W
0xF0011018	YMOD	Outer Loop Address Increment (2D only)	0x00000000	R/W
0xF0011024	DSCPTR_CUR	Current Descriptor Pointer	0x00000000	R/W
0xF0011028	DSCPTR_PRV	Previous Initial Descriptor Pointer	0x00000000	R
0xF001102C	ADDR_CUR	Current Address	0x00000000	R/W
0xF0011030	STAT	Status Register	0x00006000	R/W
0xF0011034	XCNT_CUR	Current Count(1D) or intra-row XCNT (2D)	0x00000000	R
0xF0011038	YCNT_CUR	Current Row Count (2D only)	0x00000000	R
0xF0011040	BWLCNT	Bandwidth Limit Count	0x00000000	R/W
0xF0011044	BWLCNT_CUR	Bandwidth Limit Count Current	0x00000000	R
0xF0011048	BWMCNT	Bandwidth Monitor Count	0x00000000	R/W
0xF001104C	BWMCNT_CUR	Bandwidth Moni00tor Count Current	0x00000000	R

Table 35. MEM COPYDDE1 (DDE) Register Summary

Address	Name	Description	Reset	Access
0xF0011080	DSCPTR_NXT	Pointer to Next Initial Descriptor	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF0011084	ADDRSTART	Start Address of Current Buffer	0x00000000	R/W
0xF0011088	CFG	Configuration Register	0x00000000	R/W
0xF001108C	XCNT	Inner Loop Count Start Value	0x00000000	R/W
0xF0011090	XMOD	Inner Loop Address Increment	0x00000000	R/W
0xF0011094	YCNT	Outer Loop Count Start Value (2D only)	0x00000000	R/W
0xF0011098	YMOD	Outer Loop Address Increment (2D only)	0x00000000	R/W
0xF00110A4	DSCPTR_CUR	Current Descriptor Pointer	0x00000000	R/W
0xF00110A8	DSCPTR_PRV	Previous Initial Descriptor Pointer	0x00000000	R
0xF00110AC	ADDR_CUR	Current Address	0x00000000	R/W
0xF00110B0	STAT	Status Register	0x00006000	R/W
0xF00110B4	XCNT_CUR	Current Count(1D) or intra-row XCNT (2D)	0x00000000	R
0xF00110B8	YCNT_CUR	Current Row Count (2D only)	0x00000000	R
0xF00110C0	BWLCNT	Bandwidth Limit Count	0x00000000	R/W
0xF00110C4	BWLCNT_CUR	Bandwidth Limit Count Current	0x00000000	R
0xF00110C8	BWMCNT	Bandwidth Monitor Count	0x00000000	R/W
0xF00110CC	BWMCNT_CUR	Bandwidth Monitor Count Current	0x00000000	R

Table 36. UART (UART) Register Summary

Address	Name	Description	Reset	Access
0xF0012004	CTL	Control Register	0x00000000	R/W
0xF0012008	STAT	Status Register	0x000000A0	R/W
0xF0012010	CLK	Clock Rate Register	0x0000FFFF	R/W
0xF0012014	IMSK	Interrupt Mask Register	0x00000000	R/W
0xF0012018	IMSK_SET	Interrupt Mask Set Register	0x00000000	R/W
0xF001201C	IMSK_CLR	Interrupt Mask Clear Register	0x00000000	R/W
0xF0012020	RBR	Receive Buffer Register	0x00000000	R
0xF0012024	THR	Transmit Hold Register	0x00000000	R/W
0xF0012028	TAIP	Transmit Address/Insert Pulse Register	0x00000000	R/W
0xF001202C	TSR	Transmit Shift Register	0x000007FF	R
0xF0012030	RSR	Receive Shift Register	0x00000000	R
0xF0012034	TXCNT	Transmit Counter Register	0x00000000	R
0xF0012038	RXCNT	Receive Counter Register	0x00000000	R

Table 37. UART DDE0 (DDE) Register Summary

Address	Name	Description	Reset	Access
0xF0012100	DSCPTR_NXT	Pointer to Next Initial Descriptor	0x00000000	R/W
0xF0012104	ADDRSTART	Start Address of Current Buffer	0x00000000	R/W
0xF0012108	CFG	Configuration Register	0x00000000	R/W
0xF001210C	XCNT	Inner Loop Count Start Value	0x00000000	R/W
0xF0012110	XMOD	Inner Loop Address Increment	0x00000000	R/W
0xF0012114	YCNT	Outer Loop Count Start Value (2D only)	0x00000000	R/W
0xF0012118	YMOD	Outer Loop Address Increment (2D only)	0x00000000	R/W
0xF0012124	DSCPTR_CUR	Current Descriptor Pointer	0x00000000	R/W
0xF0012128	DSCPTR_PRV	Previous Initial Descriptor Pointer	0x00000000	R
0xF001212C	ADDR_CUR	Current Address	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF0012130	STAT	Status Register	0x00006000	R/W
0xF0012134	XCNT_CUR	Current Count(1D) or intra-row XCNT (2D)	0x00000000	R
0xF0012138	YCNT_CUR	Current Row Count (2D only)	0x00000000	R
0xF0012140	BWLCNT	Bandwidth Limit Count	0x00000000	R/W
0xF0012144	BWLCNT_CUR	Bandwidth Limit Count Current	0x00000000	R
0xF0012148	BWMCNT	Bandwidth Monitor Count	0x00000000	R/W
0xF001214C	BWMCNT_CUR	Bandwidth Monitor Count Current	0x00000000	R

Table 38. UART DDE1 (DDE) Register Summary

Address	Name	Description	Reset	Access
0xF0012180	DSCPTR_NXT	Pointer to Next Initial Descriptor	0x00000000	R/W
0xF0012184	ADDRSTART	Start Address of Current Buffer	0x00000000	R/W
0xF0012188	CFG	Configuration Register	0x00000000	R/W
0xF001218C	XCNT	Inner Loop Count Start Value	0x00000000	R/W
0xF0012190	XMOD	Inner Loop Address Increment	0x00000000	R/W
0xF0012194	YCNT	Outer Loop Count Start Value (2D only)	0x00000000	R/W
0xF0012198	YMOD	Outer Loop Address Increment (2D only)	0x00000000	R/W
0xF00121A4	DSCPTR_CUR	Current Descriptor Pointer	0x00000000	R/W
0xF00121A8	DSCPTR_PRV	Previous Initial Descriptor Pointer	0x00000000	R
0xF00121AC	ADDR_CUR	Current Address	0x00000000	R/W
0xF00121B0	STAT	Status Register	0x00006000	R/W
0xF00121B4	XCNT_CUR	Current Count(1D) or intra-row XCNT (2D)	0x00000000	R
0xF00121B8	YCNT_CUR	Current Row Count (2D only)	0x00000000	R
0xF00121C0	BWLCNT	Bandwidth Limit Count	0x00000000	R/W
0xF00121C4	BWLCNT_CUR	Bandwidth Limit Count Current	0x00000000	R
0xF00121C8	BWMCNT	Bandwidth Monitor Count	0x00000000	R/W
0xF00121CC	BWMCNT_CUR	Bandwidth Monitor Count Current	0x00000000	R

Table 39. I3C MASTER SLAVE Register Summary

Address	Name	Description	Reset	Access
0xF0013000	MCONFIG	Master Configuration Register	0x00000000	R/W
0xF0013004	CONFIG	Configuration Register	0x00320000	R/W
0xF0013008	STATUS	Status Register	0x00010000	R/W
0xF001300C	CTRL	I3C Control Register	0x00000000	R/W
0xF0013010	INTSET	Interrupt Enable Set Register	0x00000000	R/W
0xF0013014	INTCLR	Interrupt Enable Clear Register	0x00000000	R/W
0xF0013018	INTMASKED	Interrupt Masked Register	0x00000000	R
0xF001301C	ERRWARN	Error and Warning Register	0x00000000	R/W
0xF001302C	DATACTRL	Data Control Register	0x80000030	R/W
0xF0013030	WDATAB	Write Byte Data Register	0x00000000	R/W
0xF0013034	WDATABE	Write Byte Data as End Register	0x00000000	R/W
0xF0013038	WDATAH	Write Half-Word Data Register	0x00000000	R/W
0xF001303C	WDATAHE	Write Half-Word Data as End Register	0x00000000	R/W

Address	Name	Description	Reset	Access
0xF0013040	RDATAB	Read Byte Data Register	0x00000000	R
0xF0013048	RDATAH	Read Half-Word Data Register	0x00000000	R
0xF0013054	WDATAB1	Byte-Only Write Byte Data Register	0x00000000	R/W
0xF0013060	CAPABILITIES	Capabilities Register	0x7C1FFE78	R
0xF0013064	DYNADDR	Dynamic Address Register	0x00000000	R
0xF0013068	MAXLIMITS	Maximum Limits Register	0x0FFF0FFF	R/W
0xF001306C	PARTNO	Part Number Register	0x00000000	R/W
0xF0013070	IDEXT	ID Extension Register	0x00000000	R/W
0xF0013074	VENDORID	Vendor ID Register	0x00000177	R/W
0xF0013084	MCTRL	Master Control Register	0x00000000	R/W
0xF0013088	MSTATUS	Master Status Register	0x00001000	R/W
0xF001308C	IBIRULES	IBI Registry and Rules Register	0x00000000	R/W
0xF0013090	MINTSET	Master Interrupt Enable Set Register	0x00000000	R/W
0xF0013094	MINTCLR	Master Interrupt Enable Clear Register	0x00000000	R/W
0xF0013098	MINTMASKED	Master Interrupt Masked Register	0x00000000	R
0xF001309C	MERRWARN	Master Error and Warning Register	0x00000000	R/W
0xF00130AC	MDATACTRL	Master Data Control Register	0x80000030	R/W
0xF00130B0	MWDATAB	Master Write Byte Data Register	0x00000000	R/W
0xF00130B4	MWDATABE	Master Write Byte Data as End Register	0x00000000	R/W
0xF00130B8	MWDATAH	Master Write Half-Word Data Register	0x00000000	R/W
0xF00130BC	MWDATAHE	Master Write Half-Word Data as End Register	0x00000000	R/W
0xF00130C0	MRDATAB	Master Read Byte Data Register	0x00000000	R
0xF00130C8	MRDATAH	Master Read Half-Word Data Register	0x00000000	R
0xF00130CC	MWDATAB1	Master Byte-Only Write Byte Data Register	0x00000000	R/W
0xF00130D0	MWMSG_SDR	Start or Continue SDR Message Register	0x00000000	R/W
0xF00130D4	MRMSG_SDR	Read SDR Message Data Register	0x00000000	R
0xF00130D8	MWMSG_DDR	Start or Continue DDR Message Register	0x00000000	R/W
0xF00130DC	MRMSG_DDR	Read DDR Message Data Register	0x00000000	R
0xF00130E4	MDYNADDR	Master Dynamic Address Register	0x00000000	R/W
0xF0013108	HDRCMD	HDR Command Register	0x00000000	R
0xF0013140	IBIEXT1	Extended IBI Data Register 1	0x00000070	R/W
0xF0013144	IBIEXT2	Extended IBI Data Register 2	0x00000000	R/W
0xF0013FFC	ID	Block ID Register	0x000003F5	R

Table 40. L2 MEMORY CONTROLLER (L2CTL) Register Summary

Address	Name	Description	Reset	Access
0xF0015000	L2_STAT	Status Register	0x00000000	R/W
0xF0015004	L2_INIT	Initialization Register	0x00000000	R/W
0xF0015008	L2_ISTAT	Initialization Status Register	0x00000000	R
0xF001500C	L2_ERRADDR0	Parity Error Address 0 Register	0x10000000	R
0xF0015010	L2_ERRADDR1	Parity Error Address 1 Register	0x10020000	R
0xF0015014	L2_ERRADDR2	Parity Error Address 2 Register	0x10040000	R

Address	Name	Description	Reset	Access
0xF0015018	L2_ERRADDR3	Parity Error Address 3 Register	0x10060000	R
0xF001501C	L2_ERRADDR4	Parity Error Address 4 Register	0x10080000	R
0xF0015020	L2_ET0	Error Type 0 Register	0x00000000	R
0xF0015024	L2_EADDR0	L2 EADDR0	0x00000000	R

REGISTER DETAILS: ADAU1797A

ADI VENDOR ID REGISTER

Address: 0xF0000000, Reset: 0x00000041, Name: VENDOR_ID

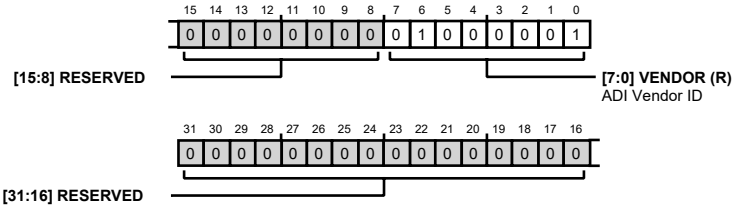


Table 41. Bit Descriptions for VENDOR_ID

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	VENDOR	ADI Vendor ID	0x41	R

DEVICE ID REGISTER

Address: 0xF0000004, Reset: 0x00001797, Name: DEVICE_ID

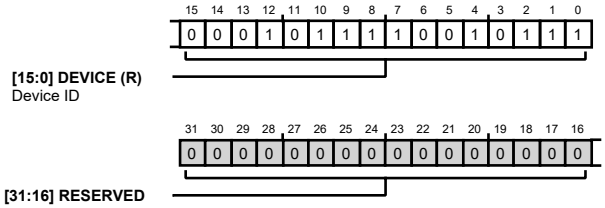


Table 42. Bit Descriptions for DEVICE_ID

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	DEVICE	Device ID	0x1797	R

REVISION CODE REGISTER

Address: 0xF0000008, Reset: 0x00000000, Name: REVISION

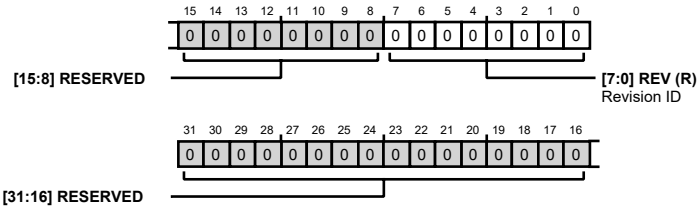


Table 43. Bit Descriptions for REVISION

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	REV	Revision ID	0x4	R

ADC, DAC, HEADPHONE POWER CONTROLS REGISTER

Address: 0xF000000C, Reset: 0x00000000, Name: ADC_DAC_HP_PWR

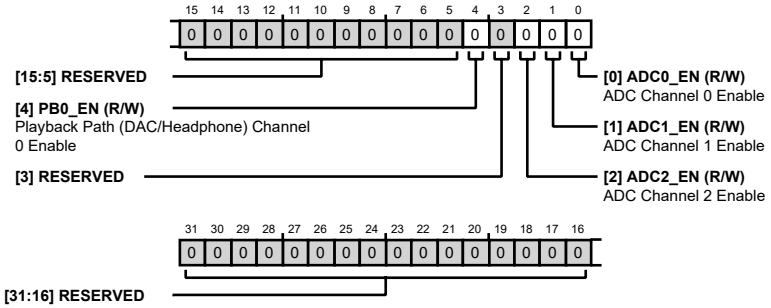


Table 44. Bit Descriptions for ADC_DAC_HP_PWR

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	PB0_EN	Playback Path (DAC/Headphone) Channel 0 Enable 0: DAC and Headphone/Line Output Channel 0 Powered Off 1: DAC and Headphone/Line Output Channel 0 Powered On	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	ADC2_EN	ADC Channel 2 Enable 0: ADC Channel 2 Powered Off 1: ADC Channel 2 Powered On	0x0	R/W
1	ADC1_EN	ADC Channel 1 Enable. 0: ADC Channel 1 Powered Off 1: ADC Channel 1 Powered On	0x0	R/W
0	ADC0_EN	ADC Channel 0 Enable 0: ADC Channel 0 Powered Off 1: ADC Channel 0 Powered On	0x0	R/W

DIGITAL MICROPHONE POWER CONTROLS REGISTER

Address: 0xF0000010, Reset: 0x00000000, Name: DMIC_PWR

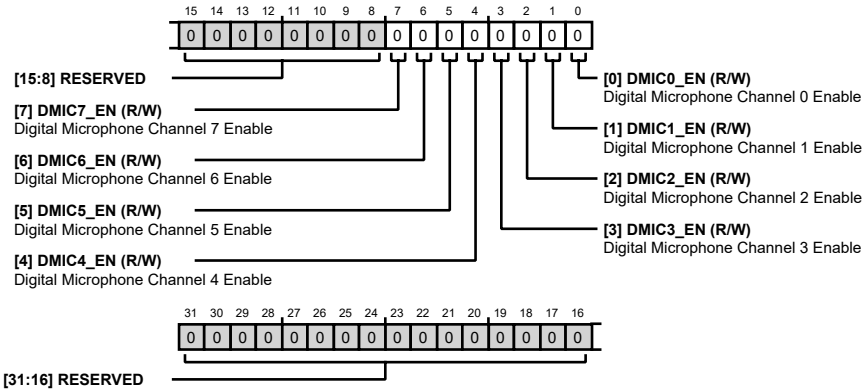


Table 45. Bit Descriptions for DMIC_PWR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	DMIC7_EN	Digital Microphone Channel 7 Enable 0: Digital Microphone Channel 7 Powered Off 1: Digital Microphone Channel 7 Powered On	0x0	R/W
6	DMIC6_EN	Digital Microphone Channel 6 Enable 0: Digital Microphone Channel 6 Powered Off 1: Digital Microphone Channel 6 Powered On	0x0	R/W
5	DMIC5_EN	Digital Microphone Channel 5 Enable 0: Digital Microphone Channel 5 Powered Off 1: Digital Microphone Channel 5 Powered On	0x0	R/W
4	DMIC4_EN	Digital Microphone Channel 4 Enable 0: Digital Microphone Channel 4 Powered Off 1: Digital Microphone Channel 4 Powered On	0x0	R/W
3	DMIC3_EN	Digital Microphone Channel 3 Enable 0: Digital Microphone Channel 3 Powered Off 1: Digital Microphone Channel 3 Powered On	0x0	R/W
2	DMIC2_EN	Digital Microphone Channel 2 Enable 0: Digital Microphone Channel 2 Powered Off 1: Digital Microphone Channel 2 Powered On	0x0	R/W
1	DMIC1_EN	Digital Microphone Channel 1 Enable 0: Digital Microphone Channel 1 Powered Off 1: Digital Microphone Channel 1 Powered On	0x0	R/W
0	DMIC0_EN	Digital Microphone Channel 0 Enable 0: Digital Microphone Channel 0 Powered Off 1: Digital Microphone Channel 0 Powered On	0x0	R/W

DIGITAL MICROPHONE POWER CONTROLS 2 REGISTER

Address: 0xF0000014, Reset: 0x00000000, Name: DMIC_PWR2

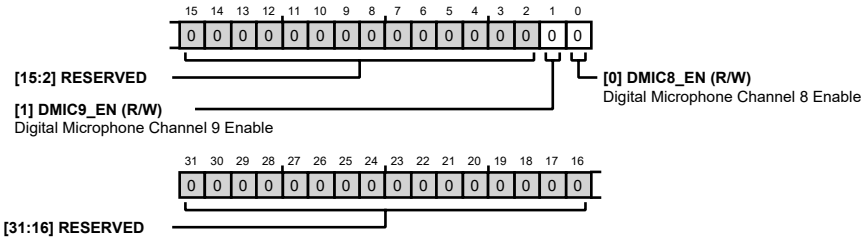


Table 46. Bit Descriptions for DMIC_PWR2

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved	0x0	R
1	DMIC9_EN	Digital Microphone Channel 9 Enable 0: Digital Microphone Channel 9 Powered Off 1: Digital Microphone Channel 9 Powered On	0x0	R/W
0	DMIC8_EN	Digital Microphone Channel 8 Enable 0: Digital Microphone Channel 8 Powered Off 1: Digital Microphone Channel 8 Powered On	0x0	R/W

ASRC0 POWER CONTROLS REGISTER

Address: 0xF0000018, Reset: 0x00000000, Name: ASRC_PWR

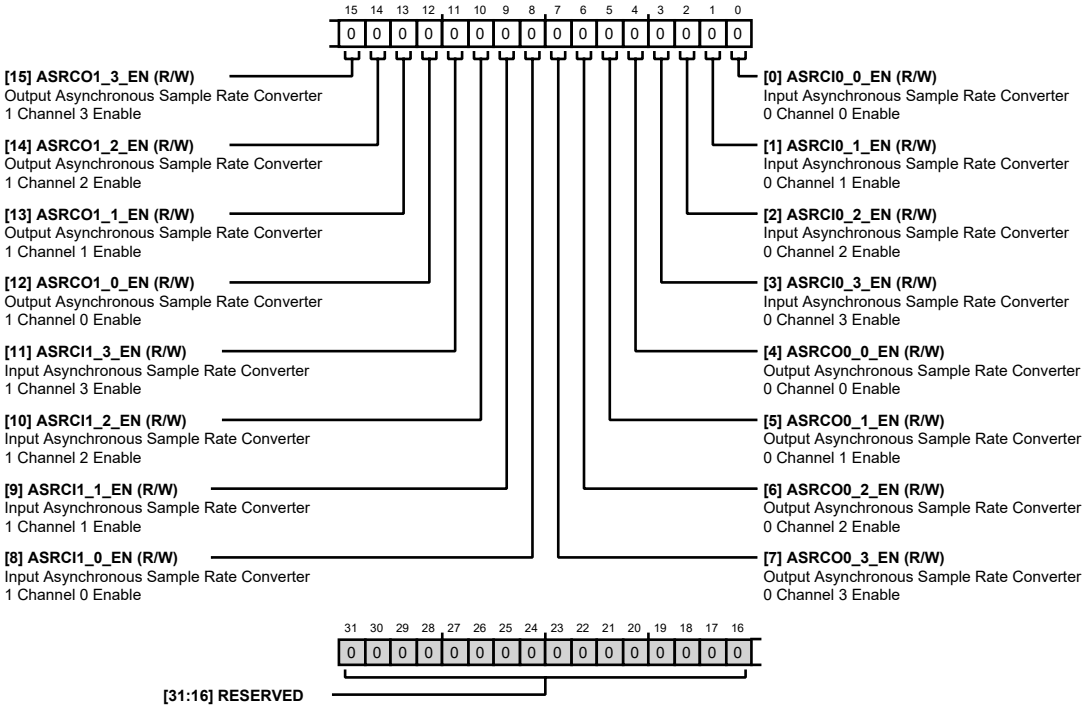


Table 47. Bit Descriptions for ASRC_PWR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
15	ASRCO1_3_EN	Output Asynchronous Sample Rate Converter 1 Channel 3 Enable 0: Output Asynchronous Sample Rate Converter Channel 3 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 3 Powered On	0x0	R/W
14	ASRCO1_2_EN	Output Asynchronous Sample Rate Converter 1 Channel 2 Enable 0: Output Asynchronous Sample Rate Converter Channel 2 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 2 Powered On	0x0	R/W
13	ASRCO1_1_EN	Output Asynchronous Sample Rate Converter 1 Channel 1 Enable 0: Output Asynchronous Sample Rate Converter Channel 1 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 1 Powered On	0x0	R/W
12	ASRCO1_0_EN	Output Asynchronous Sample Rate Converter 1 Channel 0 Enable 0: Output Asynchronous Sample Rate Converter Channel 0 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 0 Powered On	0x0	R/W
11	ASRCI1_3_EN	Input Asynchronous Sample Rate Converter 1 Channel 3 Enable 0: Input Asynchronous Sample Rate Converter Channel 3 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 3 Powered On	0x0	R/W
10	ASRCI1_2_EN	Input Asynchronous Sample Rate Converter 1 Channel 2 Enable 0: Input Asynchronous Sample Rate Converter Channel 2 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 2 Powered On	0x0	R/W
9	ASRCI1_1_EN	Input Asynchronous Sample Rate Converter 1 Channel 1 Enable 0: Input Asynchronous Sample Rate Converter Channel 1 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 1 Powered On	0x0	R/W
8	ASRCI1_0_EN	Input Asynchronous Sample Rate Converter 1 Channel 0 Enable 0: Input Asynchronous Sample Rate Converter Channel 0 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 0 Powered On	0x0	R/W
7	ASRCO0_3_EN	Output Asynchronous Sample Rate Converter 0 Channel 3 Enable 0: Output Asynchronous Sample Rate Converter Channel 3 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 3 Powered On	0x0	R/W
6	ASRCO0_2_EN	Output Asynchronous Sample Rate Converter 0 Channel 2 Enable 0: Output Asynchronous Sample Rate Converter Channel 2 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 2 Powered On	0x0	R/W
5	ASRCO0_1_EN	Output Asynchronous Sample Rate Converter 0 Channel 1 Enable 0: Output Asynchronous Sample Rate Converter Channel 1 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 1 Powered On	0x0	R/W
4	ASRCO0_0_EN	Output Asynchronous Sample Rate Converter 0 Channel 0 Enable 0: Output Asynchronous Sample Rate Converter Channel 0 Powered Off 1: Output Asynchronous Sample Rate Converter Channel 0 Powered On	0x0	R/W
3	ASRCI0_3_EN	Input Asynchronous Sample Rate Converter 0 Channel 3 Enable 0: Input Asynchronous Sample Rate Converter Channel 3 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 3 Powered On	0x0	R/W
2	ASRCI0_2_EN	Input Asynchronous Sample Rate Converter 0 Channel 2 Enable 0: Input Asynchronous Sample Rate Converter Channel 2 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 2 Powered On	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	ASRCI0_1_EN	Input Asynchronous Sample Rate Converter 0 Channel 1 Enable 0: Input Asynchronous Sample Rate Converter Channel 1 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 1 Powered On	0x0	R/W
0	ASRCI0_0_EN	Input Asynchronous Sample Rate Converter 0 Channel 0 Enable 0: Input Asynchronous Sample Rate Converter Channel 0 Powered Off 1: Input Asynchronous Sample Rate Converter Channel 0 Powered On	0x0	R/W

INTERPOLATOR POWER CONTROLS REGISTER

Address: 0xF0000020, Reset: 0x00000000, Name: FINT_PWR

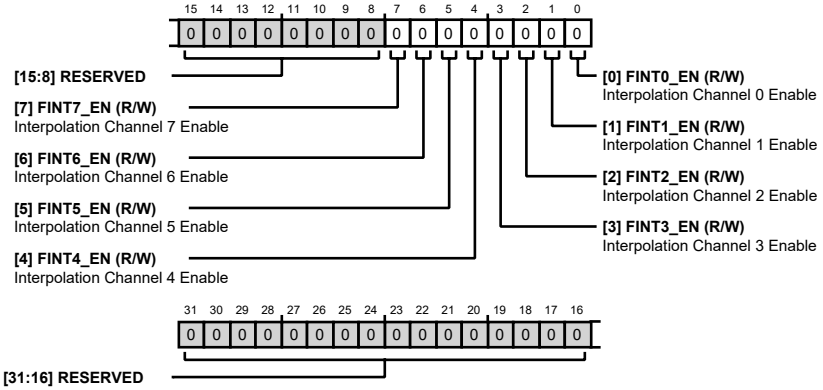


Table 48. Bit Descriptions for FINT_PWR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved.	0x0	R
7	FINT7_EN	Interpolation Channel 7 Enable 0: Interpolation Channel 7 Powered Off 1: Interpolation Channel 7 Powered On	0x0	R/W
6	FINT6_EN	Interpolation Channel 6 Enable 0: Interpolation Channel 6 Powered Off 1: Interpolation Channel 6 Powered On	0x0	R/W
5	FINT5_EN	Interpolation Channel 5 Enable 0: Interpolation Channel 5 Powered Off 1: Interpolation Channel 5 Powered On	0x0	R/W
4	FINT4_EN	Interpolation Channel 4 Enable 0: Interpolation Channel 4 Powered Off 1: Interpolation Channel 4 Powered On	0x0	R/W
3	FINT3_EN	Interpolation Channel 3 Enable 0: Interpolation Channel 3 Powered Off 1: Interpolation Channel 3 Powered On	0x0	R/W
2	FINT2_EN	Interpolation Channel 2 Enable 0: Interpolation Channel 2 Powered Off 1: Interpolation Channel 2 Powered On	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	FINT1_EN	Interpolation Channel 1 Enable 0: Interpolation Channel 1 Powered Off 1: Interpolation Channel 1 Powered On	0x0	R/W
0	FINT0_EN	Interpolation Channel 0 Enable 0: Interpolation Channel 0 Powered Off 1: Interpolation Channel 0 Powered On	0x0	R/W

DECIMATOR POWER CONTROLS REGISTER

Address: 0xF0000024, Reset: 0x00000000, Name: FDEC_PWR

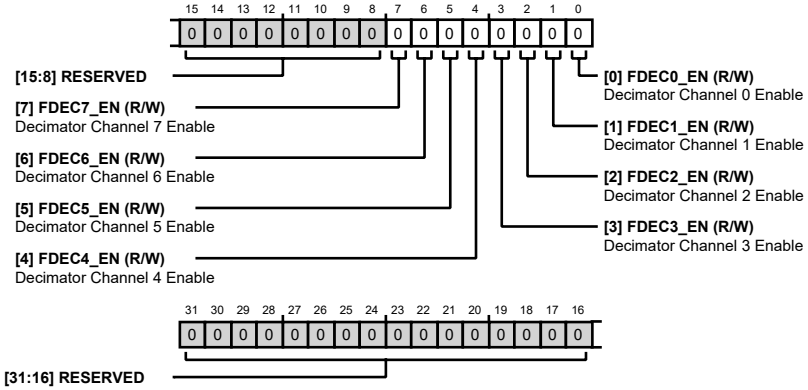


Table 49. Bit Descriptions for FDEC_PWR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	FDEC7_EN	Decimator Channel 7 Enable 0: Decimator Channel 7 Powered Off 1: Decimator Channel 7 Powered On	0x0	R/W
6	FDEC6_EN	Decimator Channel 6 Enable 0: Decimator Channel 6 Powered Off 1: Decimator Channel 6 Powered On	0x0	R/W
5	FDEC5_EN	Decimator Channel 5 Enable 0: Decimator Channel 5 Powered Off 1: Decimator Channel 5 Powered On	0x0	R/W
4	FDEC4_EN	Decimator Channel 4 Enable 0: Decimator Channel 4 Powered Off 1: Decimator Channel 4 Powered On	0x0	R/W
3	FDEC3_EN	Decimator Channel 3 Enable 0: Decimator Channel 3 Powered Off 1: Decimator Channel 3 Powered On	0x0	R/W
2	FDEC2_EN	Decimator Channel 2 Enable 0: Decimator Channel 2 Powered Off 1: Decimator Channel 2 Powered On	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	FDEC1_EN	Decimator Channel 1 Enable 0: Decimator Channel 1 Powered Off 1: Decimator Channel 1 Powered On	0x0	R/W
0	FDEC0_EN	Decimator Channel 0 Enable 0: Decimator Channel 0 Powered Off 1: Decimator Channel 0 Powered On	0x0	R/W

SERIAL PORT, PDM OUTPUT, AND DIGITAL MIC CLOCK POWER CONTROLS REGISTER

Address: 0xF0000028, Reset: 0x00000000, Name: SAI_CLK_PWR

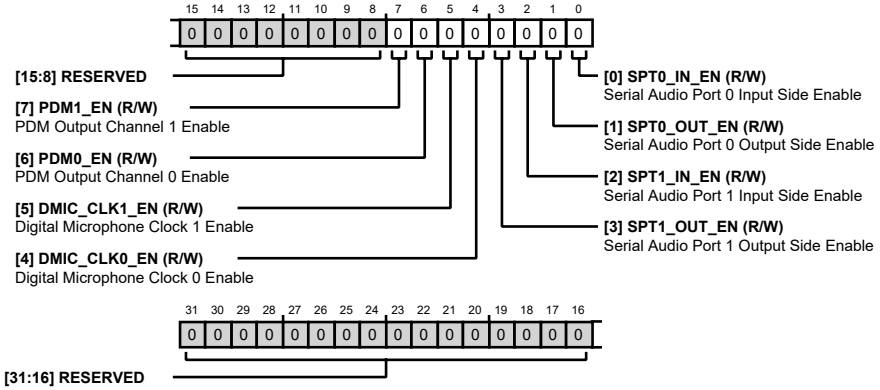


Table 50. Bit Descriptions for SAI_CLK_PWR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	PDM1_EN	PDM Output Channel 1 Enable 0: PDM Output Channel 1 Powered Off 1: PDM Output Channel 1 Powered On	0x0	R/W
6	PDM0_EN	PDM Output Channel 0 Enable 0: PDM Output Channel 0 Powered Off 1: PDM Output Channel 0 Powered On	0x0	R/W
5	DMIC_CLK1_EN	Digital Microphone Clock 1 Enable 0: Digital Microphone Clock 1 Powered Off 1: Digital Microphone Clock 1 Powered On	0x0	R/W
4	DMIC_CLK0_EN	Digital Microphone Clock 0 Enable 0: Digital Microphone Clock 0 Powered Off 1: Digital Microphone Clock 0 Powered On	0x0	R/W
3	SPT1_OUT_EN	Serial Audio Port 1 Output Side Enable 0: Serial Audio Port 1 Output Side Powered Off 1: Serial Audio Port 1 Output Side Powered On	0x0	R/W
2	SPT1_IN_EN	Serial Audio Port 1 Input Side Enable 0: Serial Audio Port 1 Input Side Powered Off 1: Serial Audio Port 1 Input Side Powered On	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	SPT0_OUT_EN	Serial Audio Port 0 Output Side Enable 0: Serial Audio Port 0 Output Side Powered Off 1: Serial Audio Port 0 Output Side Powered On	0x0	R/W
0	SPT0_IN_EN	Serial Audio Port 0 Input Side Enable 0: Serial Audio Port 0 Input Side Powered Off 1: Serial Audio Port 0 Input Side Powered On	0x0	R/W

CHIP POWER CONTROL REGISTER

Address: 0xF000002C, Reset: 0x00000000, Name: CHIP_PWR

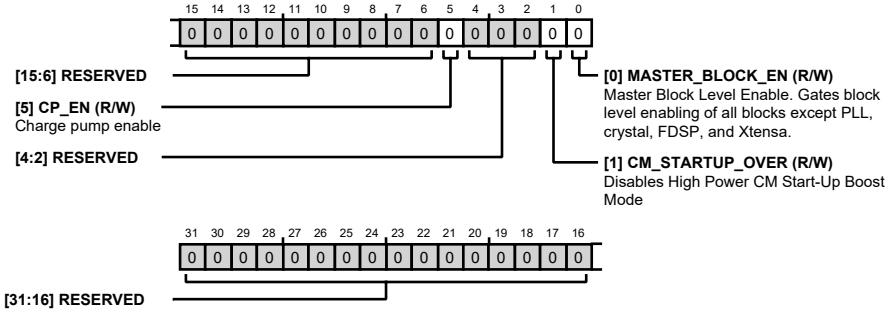


Table 51. Bit Descriptions for CHIP_PWR

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
5	CP_EN	Charge pump enable 1: Charge pump enabled 0: Charge pump disabled	0x0	R/W
4	SEL_0V9	Operating voltage. 1: 0.9V operating voltage. 0: 1.1V operating voltage.	0x0	R/W
[3:2]	RESERVED	Reserved	0x0	R/W
1	CM_STARTUP_OVER	Disables High Power CM Start-Up Boost Mode 0: CM pin fast charge is enabled. 1: CM pin fast charge is disabled.	0x0	R/W
0	MASTER_BLOCK_EN	Master Block Level Enable. Gates block level enabling all blocks except PLL, crystal, FDSP, and Xtensa. 0: All blocks are disabled. 1: All blocks that have their respective block enable set are enabled.	0x0	R/W

PLL AND PGA POWER CONTROLS REGISTER

Address: 0xF0000030, Reset: 0x00000002, Name: PLL_MB_PGA_PWR

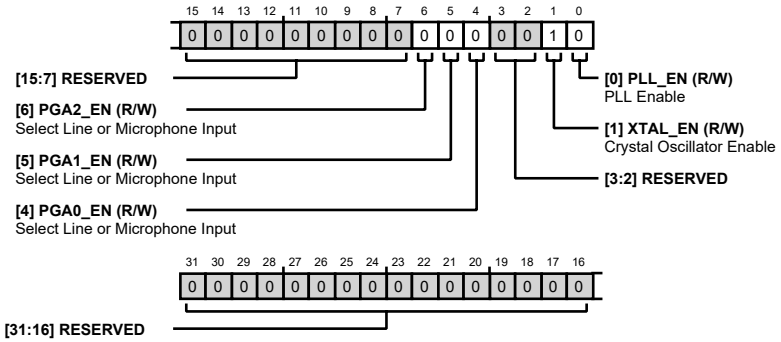


Table 52. Bit Descriptions for PLL_MB_PGA_PWR

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	PGA2_EN	Select Line or Microphone Input. Note that the PGA inverts the signal going through it. 0: AIN2 is used as a single-ended line input. PGA powered down. 1: AIN2 is used as a single-ended microphone input. PGA powered up with slewing.	0x0	R/W
5	PGA1_EN	Select Line or Microphone Input. Note that the PGA inverts the signal going through it. 0: AIN1 is used as a single-ended line input. PGA powered down. 1: AIN1 is used as a single-ended microphone input. PGA powered up with slewing.	0x0	R/W
4	PGA0_EN	Select Line or Microphone Input. Note that the PGA inverts the signal going through it. 0: AIN0 is used as a single-ended line input. PGA powered down. 1: AIN0 is used as a single-ended microphone input. PGA powered up with slewing.	0x0	R/W
[3:2]	RESERVED	Reserved	0x0	R
1	XTAL_EN	Crystal Oscillator Enable 0: Crystal Oscillator Powered Off 1: Crystal Oscillator Powered On	0x1	R/W
0	PLL_EN	PLL Enable 0: PLL Powered Off 1: PLL Powered On	0x0	R/W

DSP POWER CONTROLS REGISTER

Address: 0xF0000034, Reset: 0x00000000, Name: DSP_PWR

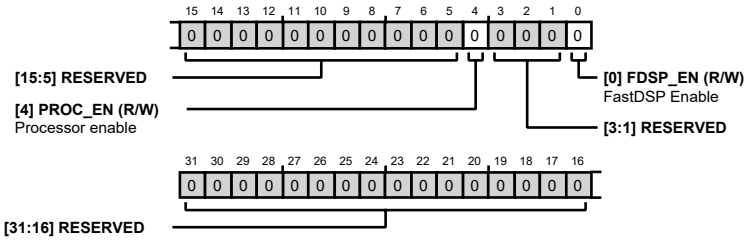


Table 53. Bit Descriptions for DSP_PWR

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	PROC_EN	Processor Enable 0: TE and Xtensa clocks are disabled. 1: TE and Xtensa clocks are enabled.	0x0	R/W
[3:1]	RESERVED	Reserved	0x0	R
0	FDSP_EN	FastDSP Enable 0: FastDSP Powered Off 1: FastDSP Powered On	0x0	R/W

STATE RETENTION CONTROLS REGISTER

Address: 0xF0000038, Reset: 0x00000010, Name: KEEPS

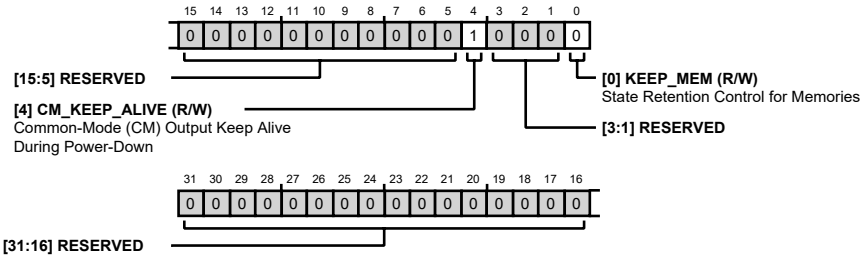


Table 54. Bit Descriptions for KEEPS

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	CM_KEEP_ALIVE	Common-Mode (CM) Output Keep Alive During Power-Down 0: CM output turns off when POWER_EN = 0, which allows lower shutdown power but longer start-up timing. 1: CM output stays on when POWER_EN = 0, which allows faster start-up timing but greater shutdown power.	0x1	R/W
[3:1]	RESERVED	Reserved	0x0	R
0	KEEP_MEM	State Retention Control for Memories 1: Retains memory contents. 0: Does not retain memory contents.	0x0	R/W

DIGITAL POWER SUPPLY CONTROL REGISTER

Address: 0xF000003C, Reset: 0x00000000, Name: DVDD_CTRL

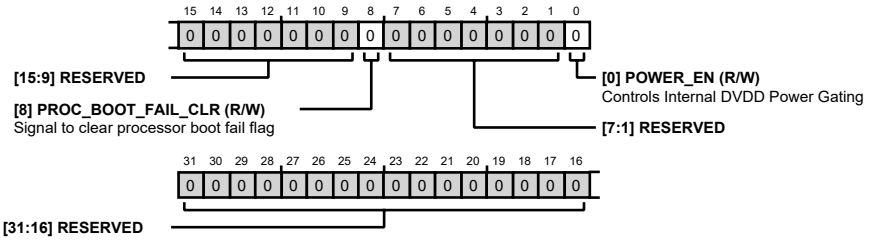


Table 55. Bit Descriptions for DVDD_CTRL

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	PROC_BOOT_FAIL_CLR	Signal to clear processor boot fail flag.	0x0	R/W
[7:1]	RESERVED	Reserved	0x0	R
0	POWER_EN	Controls Internal DVDD Power Gating 0: Disables Internal DVDD Supply 1: Enables Internal DVDD Supply. Allows block enabling of PLL and FDSP.	0x0	R/W

CLOCK CONTROL REGISTER

Address: 0xF0000040, Reset: 0x00000708, Name: CLK_CTRL0

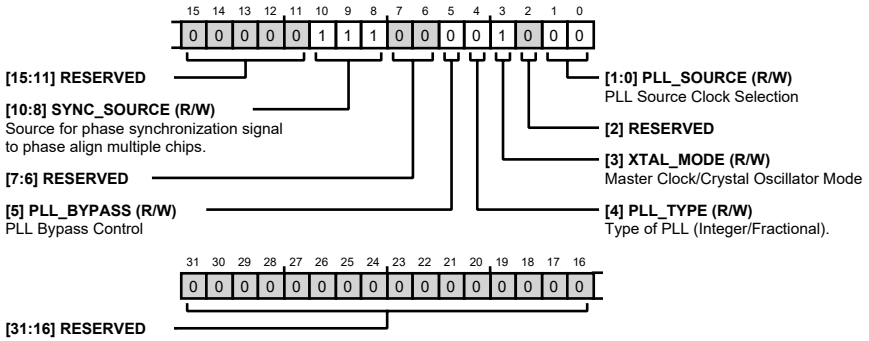


Table 56. Bit Descriptions for CLK_CTRL0

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved	0x0	R
[10:8]	SYNC_SOURCE	Source for phase synchronization signal to phase align multiple chips. 000: LRCLK_0 signal used for phase synchronization. 001: LRCLK_1 signal used for phase synchronization. 010: Input ASRC0 used for a phase synchronization signal. Used when LRCLK signal is async to core clock. 011: Input ASRC1 used for a phase synchronization signal. Used when LRCLK signal is async to core clock. 111: Phase synchronization signal internally generated.	0x7	R/W
[7:6]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
5	PLL_BYPASS	PLL Bypass Control 0: PLL output is the source of the main chip clock. 1: PLL is bypassed. Main chip clock sourced directly from PLL_SOURCE. MCLK must be 49.152 MHz in this case.	0x0	R/W
4	PLL_TYPE	Type of PLL (Integer/Fractional) 0: Integer PLL 1: Fractional PLL	0x0	R/W
3	XTAL_MODE	Master Clock/Crystal Oscillator Mode 0: Logic level master clock input used. 1: Crystal oscillator used.	0x1	R/W
2	RESERVED	Reserved	0x0	R
[1:0]	PLL_SOURCE	PLL Source Clock Selection 00: MCLKIN pin or crystal is the PLL source. 01: BCLK_0 pin is the PLL source. 10: BCLK_1 pin is the PLL source.	0x0	R/W

PLL INPUT DIVIDER REGISTER

Address: 0xF0000044, Reset: 0x00000010, Name: CLK_CTRL1

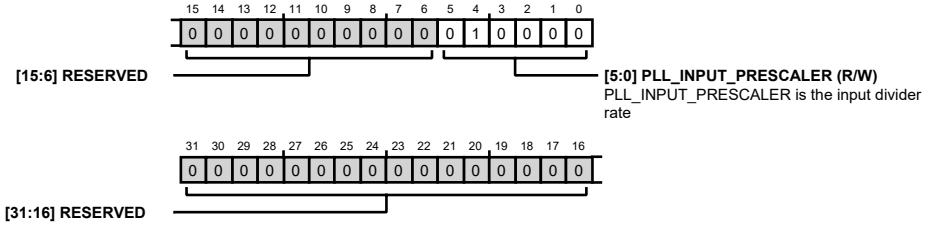


Table 57. Bit Descriptions for CLK_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
[5:0]	PLL_INPUT_PRESCALER	PLL_INPUT_PRESCALER is the input divider rate.	0x10	R/W

PLL FEEDBACK INTEGER DIVIDER REGISTER

Address: 0xF0000048, Reset: 0x00000080, Name: CLK_CTRL2

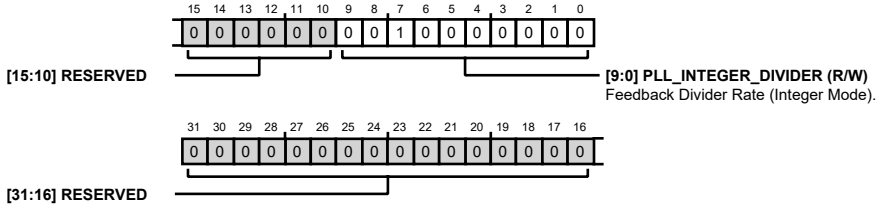


Table 58. Bit Descriptions for CLK_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
[9:0]	PLL_INTEGER_DIVIDER	Feedback Divider Rate (Integer Mode)	0x80	R/W

PLL FRACTIONAL NUMERATOR VALUE REGISTER

Address: 0xF000004C, Reset: 0x00000000, Name: CLK_CTRL3

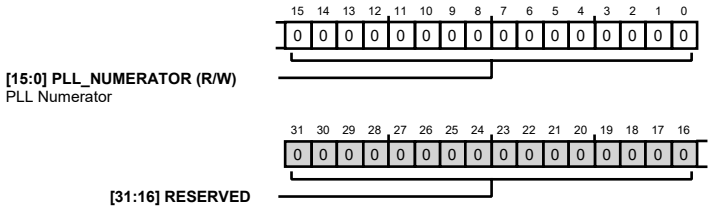


Table 59. Bit Descriptions for CLK_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	PLL_NUMERATOR	PLL Numerator	0x0	R/W

PLL FRACTIONAL DENOMINATOR (LSBS) REGISTER

Address: 0xF0000050, Reset: 0x00000000, Name: CLK_CTRL4

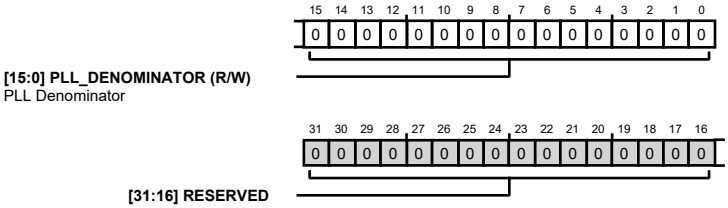


Table 60. Bit Descriptions for CLK_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	PLL_DENOMINATOR	PLL Denominator	0x0	R/W

PLL UPDATE REGISTER

Address: 0xF0000054, Reset: 0x00000000, Name: CLK_CTRL5

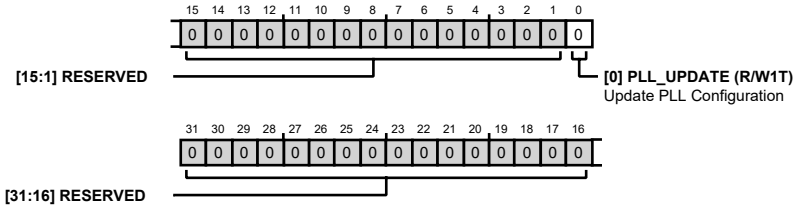


Table 61. Bit Descriptions for CLK_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	PLL_UPDATE	Update PLL Configuration 0: Write of 0 does nothing. 1: Write of 1 updates all PLL configuration settings.	0x0	R/W1T

ADC SAMPLE RATE CONTROL REGISTER

Address: 0xF0000058, Reset: 0x00000404, Name: ADC_CTRL1

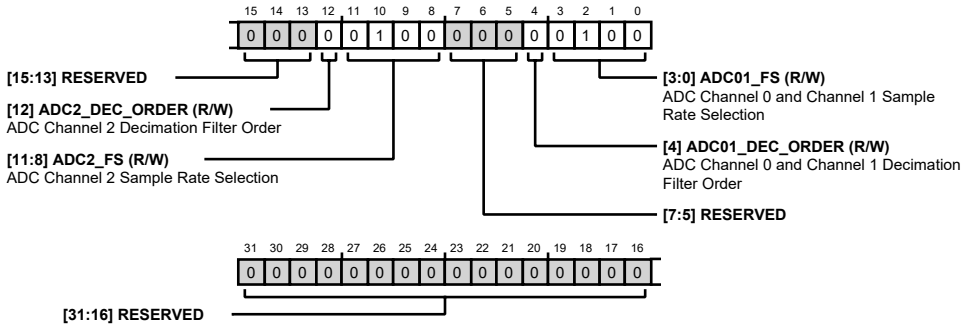


Table 62. Bit Descriptions for ADC_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved	0x0	R
12	ADC2_DEC_ORDER	ADC Channel 2 Decimation Filter Order 0: Lower Order Decimation Filter: Lower Delay 1: Higher Order Decimation Filter: Higher Delay	0x0	R/W
[11:8]	ADC2_FS	ADC Channel 2 Sample Rate Selection 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W
[7:5]	RESERVED	Reserved	0x0	R
4	ADC01_DEC_ORDER	ADC Channel 0 and Channel 1 Decimation Filter Order 0: Lower Order Decimation Filter: Lower Delay 1: Higher Order Decimation Filter: Higher Delay	0x0	R/W
[3:0]	ADC01_FS	ADC Channel 0 and Channel 1 Sample Rate Selection 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

ADC/ANALOG INPUT MODE SELECTION REGISTER

Address: 0xF000005C, Reset: 0x00000000, Name: ADC_CTRL2

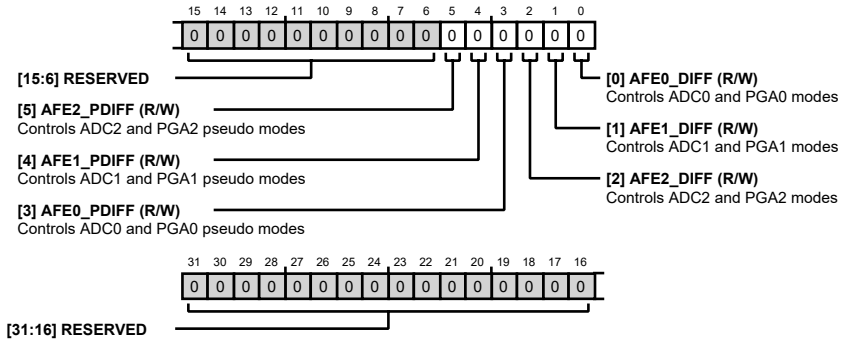


Table 63. Bit Descriptions for ADC_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
5	AFE2_PDIFF	Controls ADC2 and PGA2 modes. 0: Single-Ended or Differential Mode 1: Psuedo-Differential Mode	0x0	R/W
4	AFE1_PDIFF	Controls ADC1 and PGA1 modes. 0: Single-Ended or Differential Mode 1: Psuedo-Differential Mode	0x0	R/W
3	AFE0_PDIFF	Controls ADC0 and PGA0 modes. 0: Single-Ended or Differential Mode 1: Psuedo-Differential Mode	0x0	R/W
2	AFE2_DIFF	Controls ADC2 and PGA2 Modes. 0: ADC/Analog Input Single-Ended Mode 1: ADC/Analog Input Differential Mode	0x0	R/W
1	AFE1_DIFF	Controls ADC1 and PGA1 Modes 0: ADC/Analog Input Single-Ended Mode 1: ADC/Analog Input Differential Mode	0x0	R/W
0	AFE0_DIFF	Controls ADC0 and PGA0 Modes 0: ADC/Analog Input Single-Ended Mode 1: ADC/Analog Input Differential Mode	0x0	R/W

ADC IBIAS CONTROLS REGISTER

Address: 0xF0000060, Reset: 0x00000000, Name: ADC_CTRL3

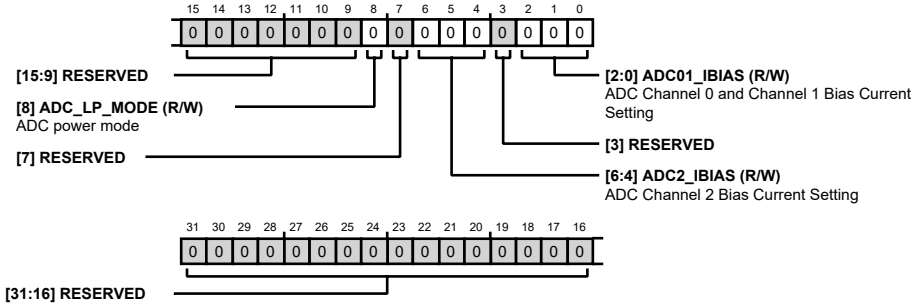


Table 64. Bit Descriptions for ADC_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	ADC_LP_MODE	ADC Power Mode 0: Standard power mode. 1: Configure all ADC channels into low-power mode with a 6dB gain boost. If PGA is enabled on any channel, the 6dB gain boost is not applicable on that channel.	0x0	R/W
7	RESERVED	Reserved	0x0	R
[6:4]	ADC2_IBIAS	ADC Channel 2 Bias Current Setting. Higher bias currents result in higher performance. 000: Normal Operation (Default). 001: Extreme Power Saving. 010: Power Saving. 011: Enhanced Performance.	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	ADC01_IBIAS	ADC Channel 0 and Channel 1 Bias Current Setting. Higher bias currents result in higher performance. 000: Normal Operation (Default). 001: Extreme Power Saving. 010: Power Saving. 011: Enhanced Performance.	0x0	R/W

ADC HPF CONTROL 1 REGISTER

Address: 0xF0000064, Reset: 0x000000D0, Name: ADC_CTRL4

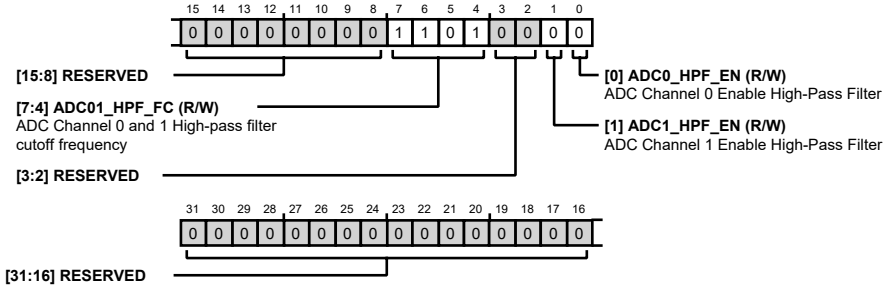


Table 65. Bit Descriptions for ADC_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ADC01_HPF_FC	ADC Channel 0 and 1 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz	0xD	R/W

Bits	Bit Name	Description	Reset	Access
		1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz		
[3:2]	RESERVED	Reserved	0x0	R
1	ADC1_HPF_EN	ADC Channel 1 Enable Highpass Filter 0: ADC Highpass Filter Off 1: ADC Highpass Filter On	0x0	R/W
0	ADC0_HPF_EN	ADC Channel 0 Enable Highpass Filter 0: ADC Highpass Filter Off 1: ADC Highpass Filter On	0x0	R/W

ADC HPF CONTROL 2 REGISTER

Address: 0xF0000068, Reset: 0x000000D0, Name: ADC_CTRL5

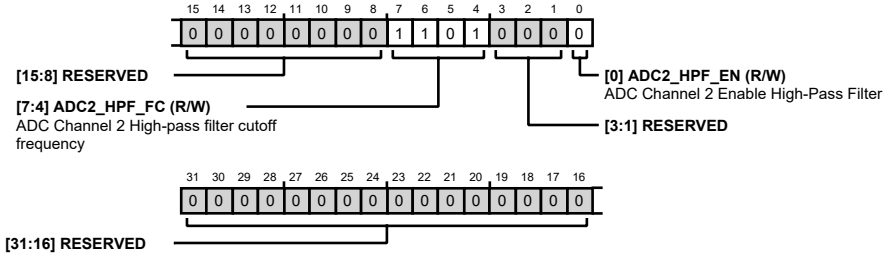


Table 66. Bit Descriptions for ADC_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ADC2_HPF_FC	ADC Channel 2 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz	0xD	R/W

Bits	Bit Name	Description	Reset	Access
		1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz		
[3:1]	RESERVED	Reserved	0x0	R
0	ADC2_HPF_EN	ADC Channel 2 Enable Highpass Filter 0: ADC Highpass Filter Off 1: ADC Highpass Filter On	0x0	R/W

ADC MUTE AND COMPENSATION CONTROL REGISTER

Address: 0xF000006C, Reset: 0x00000040, Name: ADC_CTRL6

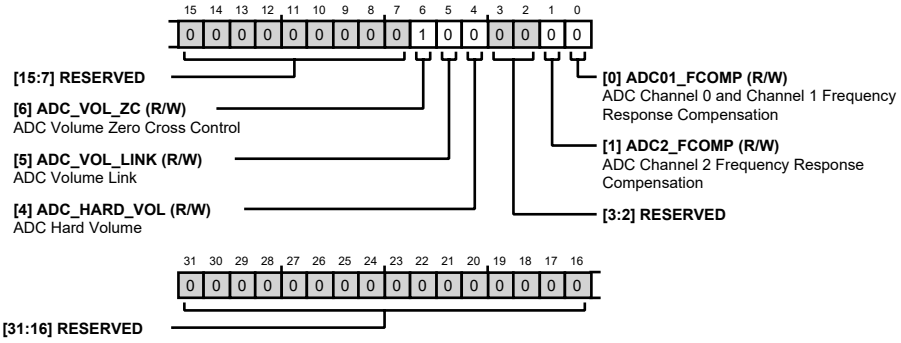


Table 67. Bit Descriptions for ADC_CTRL6

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	ADC_VOL_ZC	ADC Volume Zero Cross-Control 0: Volume change occurs at any time. 1: Volume change only occurs at zero crossing.	0x1	R/W
5	ADC_VOL_LINK	ADC Volume Link 0: Each ADC channel uses its respective volume value. 1: All ADC channels use Channel 0 volume value.	0x0	R/W
4	ADC_HARD_VOL	ADC Hard Volume 0: Soft Volume Ramping 1: Hard/Immediate Volume Change	0x0	R/W
[3:2]	RESERVED	Reserved	0x0	R
1	ADC2_FCOMP	ADC Channel 2 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W
0	ADC01_FCOMP	ADC Channel 0 and Channel 1 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W

ANALOG INPUT PRE-CHARGE TIME REGISTER

Address: 0xF0000070, Reset: 0x00000006, Name: ADC_CTRL7

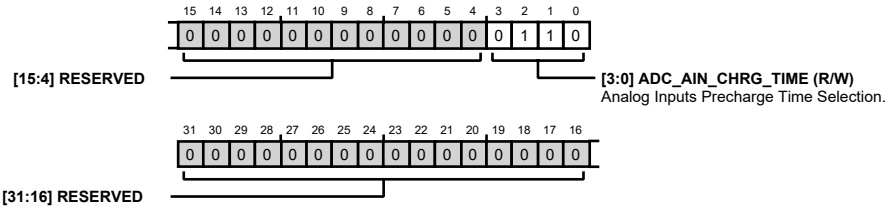


Table 68. Bit Descriptions for ADC_CTRL7

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved	0x0	R
[3:0]	ADC_AIN_CHRG_TIME	Analog Inputs Precharge Time Selection. Controls the amount of time the precharge circuit is used to charge up the coupling capacitors. The time used depends on the value of the capacitor used and the required start-up time of the ADC. 0x0: No Precharge 0x1: 5ms Precharge 0x2: 10ms Precharge 0x3: 20ms Precharge 0x4: 30ms Precharge 0x5: 40ms Precharge 0x6: 50ms Precharge 0x7: 60ms Precharge 0x8: 80ms Precharge 0x9: 100ms Precharge 0xA: 125ms Precharge 0xB: 150ms Precharge 0xC: 200ms Precharge 0xD: 250ms Precharge 0xE: 300ms Precharge 0xF: 400ms Precharge	0x6	R/W

ADC CHANNEL MUTES REGISTER

Address: 0xF0000074, Reset: 0x00000000, Name: ADC_MUTES

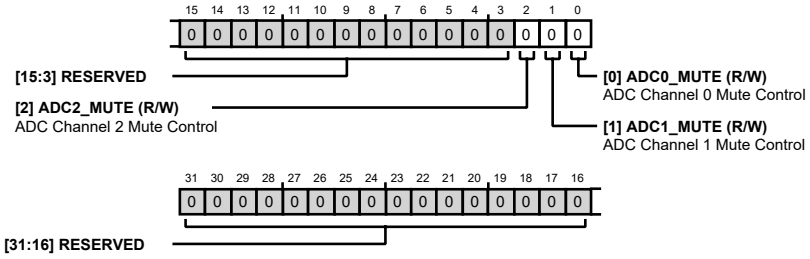


Table 69. Bit Descriptions for ADC_MUTES

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved	0x0	R
2	ADC2_MUTE	ADC Channel 2 Mute Control 0: ADC Unmuted 1: ADC Muted	0x0	R/W
1	ADC1_MUTE	ADC Channel 1 Mute Control 0: ADC Unmuted 1: ADC Muted	0x0	R/W
0	ADC0_MUTE	ADC Channel 0 Mute Control 0: ADC Unmuted 1: ADC Muted	0x0	R/W

ADC CHANNEL 0 VOLUME CONTROL REGISTER

Address: 0xF0000078, Reset: 0x00000040, Name: ADC0_VOL

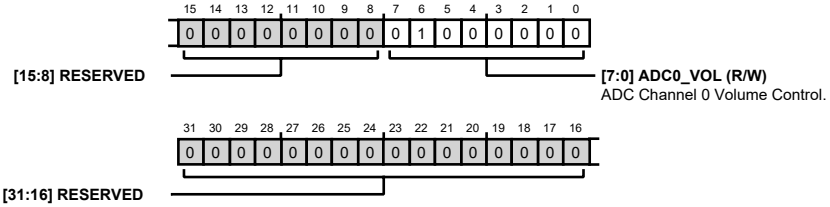


Table 70. Bit Descriptions for ADC0_VOL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	ADC0_VOL	ADC Channel 0 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

ADC CHANNEL 1 VOLUME CONTROL REGISTER

Address: 0xF000007C, Reset: 0x00000040, Name: ADC1_VOL

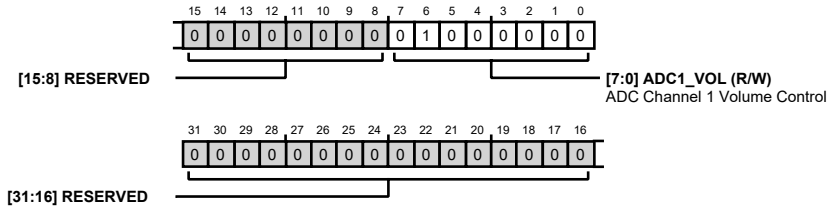


Table 71. Bit Descriptions for ADC1_VOL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	ADC1_VOL	ADC Channel 1 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

ADC CHANNEL 2 VOLUME CONTROL REGISTER

Address: 0xF0000080, Reset: 0x00000040, Name: ADC2_VOL

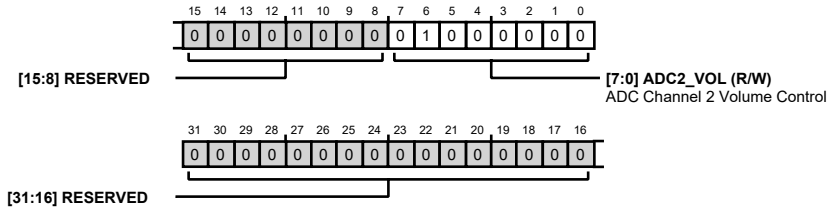


Table 72. Bit Descriptions for ADC2_VOL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	ADC2_VOL	ADC Channel 2 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ...	0x40	R/W

Bits	Bit Name	Description	Reset	Access
		00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute		

PGA CHANNEL 0 GAIN CONTROL MSBs, MUTE, BOOST, SLEW REGISTER

Address: 0xF0000084, Reset: 0x00000000, Name: PGA0_CTRL1

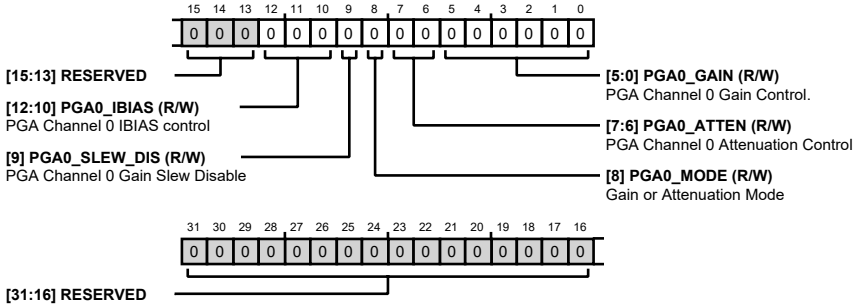


Table 73. Bit Descriptions for PGA0_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved	0x0	R
[12:10]	PGA0_IBIAS	PGA Channel 0 IBIAS control. 000: Normal. 001: Lowest power. 010: Low power. 011: High performance. 100-111: RESERVED	0x0	R/W
9	PGA0_SLEW_DIS	PGA Channel 0 Gain Slew Disable 0: PGA slew enabled. 1: PGA slew disabled.	0x0	R/W
8	PGA0_MODE	Gain or Attenuation Mode. Note that the PGA inverts the signal going through it. 0: Use gain register. 1: Use attenuation register.	0x0	R/W
[7:6]	PGA0_ATTEN	PGA Channel 0 Attenuation Control 00: 0dB 01: -3dB 10: -6dB 11: -9dB	0x0	R/W
[5:0]	PGA0_GAIN	PGA Channel 0 Gain Control. 29.25dB is the maximum gain. 000000: 0dB 000001: 0.75dB 000010: 1.5dB	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		... 001000: 6dB ... 100000: 24dB 100111: 29.25dB		

PGA CHANNEL 0 GAIN CONTROL LSBs REGISTER

Address: 0xF0000088, Reset: 0x00000000, Name: PGA0_CTRL2

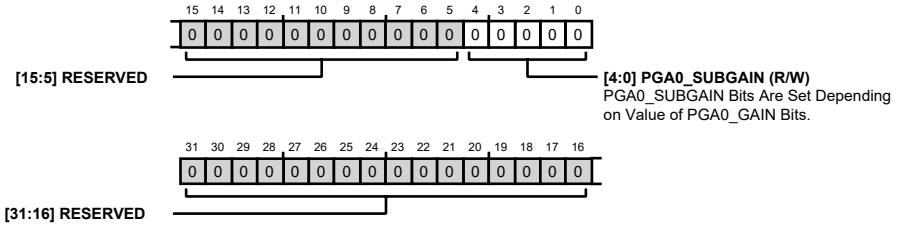


Table 74. Bit Descriptions for PGA0_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
[4:0]	PGA0_SUBGAIN	PGA0_SUBGAIN bits are set depending on the value of PGA0_GAIN bits.	0x0	R/W

PGA CHANNEL 1 GAIN CONTROL MSBs, MUTE, BOOST, SLEW REGISTER

Address: 0xF000008C, Reset: 0x00000000, Name: PGA1_CTRL1

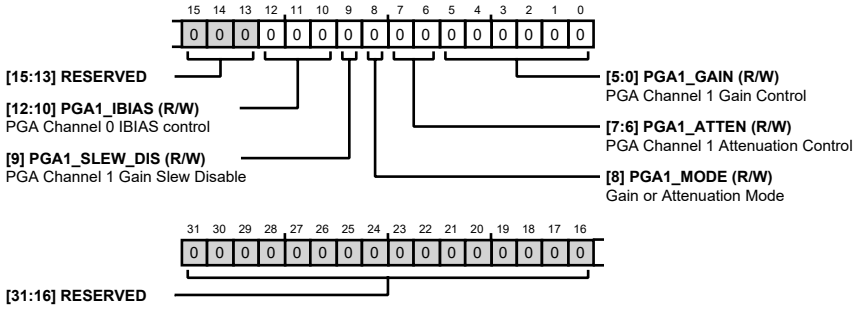


Table 75. Bit Descriptions for PGA1_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved	0x0	R
[12:10]	PGA1_IBIAS	PGA Channel 1 IBIAS Control 000: Normal. 001: Lowest power. 010: Low power. 011: High performance. 100-111: RESERVED	0x0	R/W
9	PGA1_SLEW_DIS	PGA Channel 1 Gain Slew Disable 0: PGA slew enabled. 1: PGA slew disabled.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
8	PGA1_MODE	Gain or Attenuation Mode. Note that the PGA inverts the signal going through it. 0: Use gain register. 1: Use attenuation register.	0x0	R/W
[7:6]	PGA1_ATTEN	PGA Channel 1 Attenuation Control 00: 0dB 01: -3dB 10: -6dB 11: -9dB	0x0	R/W
[5:0]	PGA1_GAIN	PGA Channel 1 Gain Control. 29.25dB is the maximum gain. 000000: 0dB 000001: 0.75dB 000010: 1.5dB ... 001000: 6dB ... 100000: 24dB 100111: 29.25dB	0x0	R/W

PGA CHANNEL 1 GAIN CONTROL LSBs REGISTER

Address: 0xF0000090, Reset: 0x00000000, Name: PGA1_CTRL2

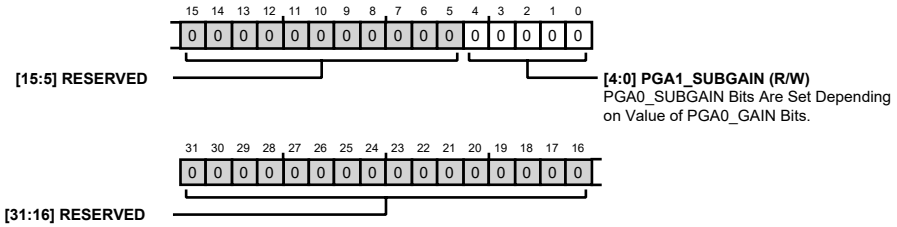


Table 76. Bit Descriptions for PGA1_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
[4:0]	PGA1_SUBGAIN	PGA0_SUBGAIN bits are set depending on the value of PGA0_GAIN bits.	0x0	R/W

PGA CHANNEL 2 GAIN CONTROL MSBs, MUTE, BOOST, SLEW REGISTER

Address: 0xF0000094, Reset: 0x00000000, Name: PGA2_CTRL1

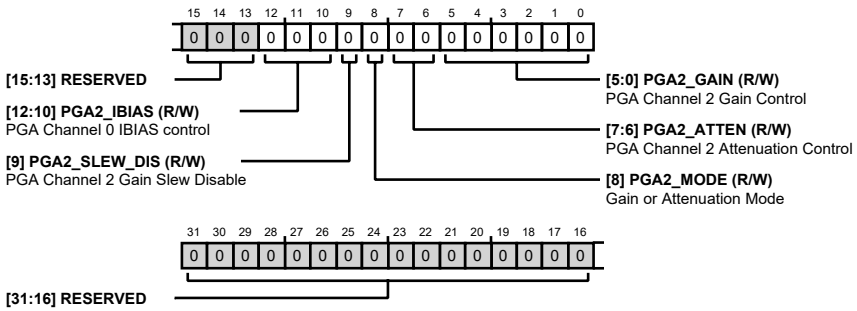


Table 77. Bit Descriptions for PGA2_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved	0x0	R
[12:10]	PGA2_IBIAS	PGA Channel 2 IBIAS control. 000: Normal. 001: Lowest power. 010: Low power. 011: High performance. 100-111: RESERVED	0x0	R/W
9	PGA2_SLEW_DIS	PGA Channel 2 Gain Slew Disable 0: PGA slew enabled. 1: PGA slew disabled.	0x0	R/W
8	PGA2_MODE	Gain or Attenuation Mode. Note that the PGA inverts the signal going through it. 0: Use gain register. 1: Use attenuation register.	0x0	R/W
[7:6]	PGA2_ATTEN	PGA Channel 2 Attenuation Control. 00: 0dB 01: -3dB 10: -6dB 11: -9dB	0x0	R/W
[5:0]	PGA2_GAIN	PGA Channel 2 Gain Control. 29.25dB is the maximum gain. 000000: 0dB 000001: 0.75dB 000010: 1.5dB ... 001000: 6dB ... 100000: 24dB 100111: 29.25dB	0x0	R/W

PGA CHANNEL 2 GAIN CONTROL LSB'S REGISTER

Address: 0xF0000098, Reset: 0x00000000, Name: PGA2_CTRL2

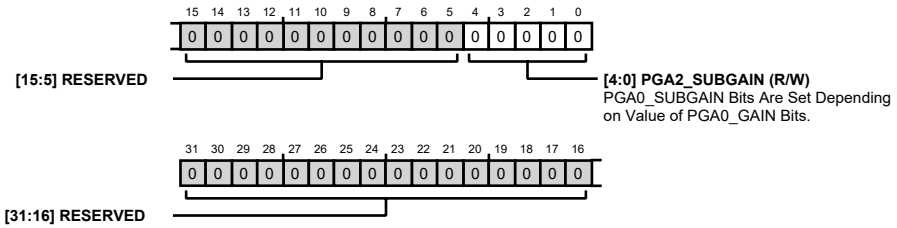


Table 78. Bit Descriptions for PGA2_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
[4:0]	PGA2_SUBGAIN	PGA0_SUBGAIN bits are set depending on the value of PGA0_GAIN bits.	0x0	R/W

PGA SLEW RATE AND GAIN LINK REGISTER

Address: 0xF000009C, Reset: 0x00000000, Name: PGA_CTRL

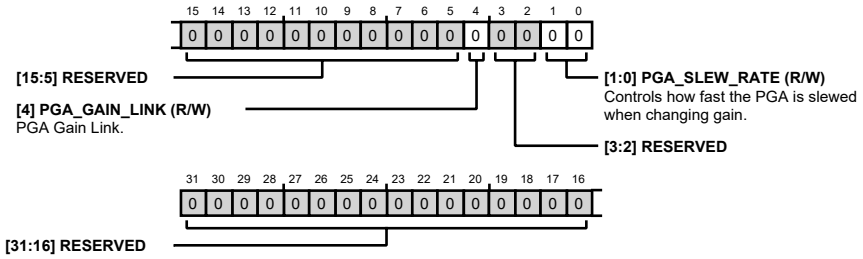


Table 79. Bit Descriptions for PGA_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	PGA_GAIN_LINK	PGA Gain Link 0: Each PGA channel uses its respective gain value. 1: All PGA channels use Channel 0 gain value.	0x0	R/W
[3:2]	RESERVED	Reserved	0x0	R
[1:0]	PGA_SLEW_RATE	Controls how fast the PGA is slewed when changing gain. 00: 2.2dB/ms 01: 1.1dB/ms 10: 0.5dB/ms	0x0	R/W

DMIC CLOCK RATE CONTROL REGISTER

Address: 0xF00000A0, Reset: 0x00000033, Name: DMIC_CTRL1

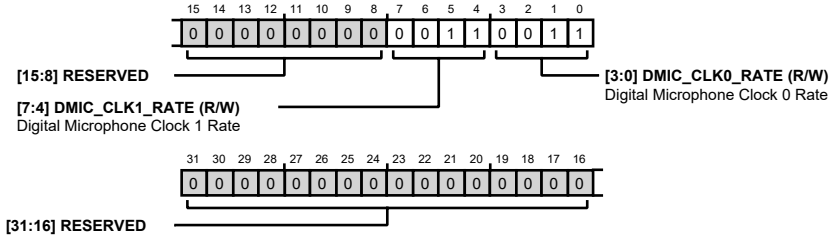


Table 80. Bit Descriptions for DMIC_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	DMIC_CLK1_RATE	Digital Microphone Clock 1 Rate 0000: 384kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0001: 768kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0010: 1536kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0011: 3072kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0100: 6144kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0101: 256kHz Clock Rate (8/16kHz FS only) 0110: 512kHz Clock Rate (8/16kHz FS only) 0111: 1024kHz Clock Rate (8/16kHz FS only) 1000: 2048kHz Clock Rate (8/16kHz FS only) 1001: 4096kHz Clock Rate (8/16kHz FS only)	0x3	R/W

Bits	Bit Name	Description	Reset	Access
[3:0]	DMIC_CLK0_RATE	Digital Microphone Clock 0 Rate 0000: 384kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0001: 768kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0010: 1536kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0011: 3072kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0100: 6144kHz Clock Rate (12/24/48/96/192/384/768kHz FS only) 0101: 256kHz Clock Rate (8/16kHz FS only) 0110: 512kHz Clock Rate (8/16kHz FS only) 0111: 1024kHz Clock Rate (8/16kHz FS only) 1000: 2048kHz Clock Rate (8/16kHz FS only) 1001: 4096kHz Clock Rate (8/16kHz FS only)	0x3	R/W

DIGITAL MICROPHONE CHANNEL 0 AND CHANNEL 1 CONTROL REGISTER

Address: 0xF00000A4, Reset: 0x00000004, Name: DMIC_CTRL2

Rate, order, mapping, and edge control.

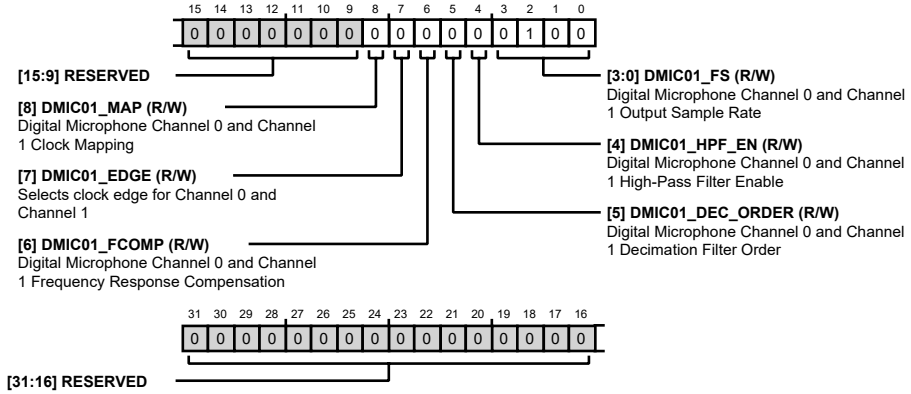


Table 81. Bit Descriptions for DMIC_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DMIC01_MAP	Digital Microphone Channel 0 and Channel 1 Clock Mapping 0: Digital microphone channels use DMIC_CLK0. 1: Digital microphone channels use DMIC_CLK1.	0x0	R/W
7	DMIC01_EDGE	Selects the clock edge for Channel 0 and Channel 1 0: 0 is the rising edge, and 1 is the falling edge. 1: 1 is the rising edge, and 0 is the falling edge.	0x0	R/W
6	DMIC01_FCOMP	Digital Microphone Channel 0 and Channel 1 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W
5	DMIC01_DEC_ORDER	Digital Microphone Channel 0 and Channel 1 Decimation Filter Order 0: Fourth-Order Decimation Filter 1: Fifth-Order Decimation Filter	0x0	R/W

Bits	Bit Name	Description	Reset	Access
4	DMIC01_HPF_EN	Digital Microphone Channel 0 and Channel 1 Highpass Filter Enable 0: Highpass Filter Off 1: Highpass Filter On	0x0	R/W
[3:0]	DMIC01_FS	Digital Microphone Channel 0 and Channel 1 Output Sample Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DIGITAL MICROPHONE CHANNEL 2 AND CHANNEL 3 CONTROL REGISTER

Address: 0xF00000A8, Reset: 0x00000004, Name: DMIC_CTRL3

Rate, order, mapping, and edge control.

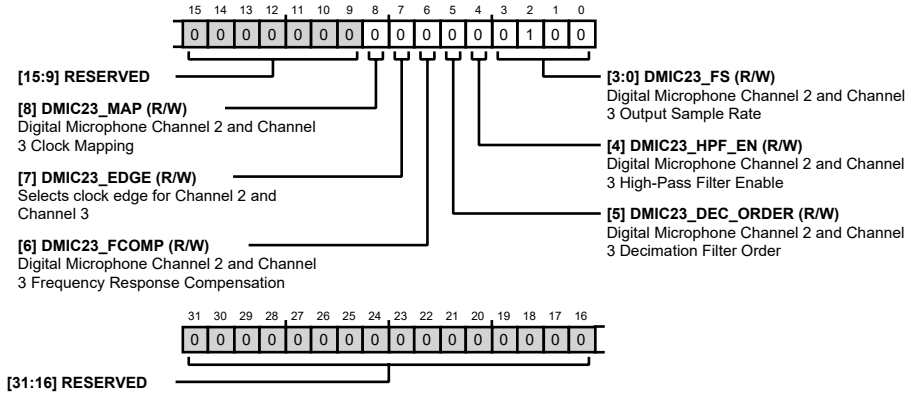


Table 82. Bit Descriptions for DMIC_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DMIC23_MAP	Digital Microphone Channel 2 and Channel 3 Clock Mapping 0: Digital microphone channels use DMIC_CLK0. 1: Digital microphone channels use DMIC_CLK1.	0x0	R/W
7	DMIC23_EDGE	Selects the clock edge for Channel 2 and Channel 3 0: 0 is the rising edge, and 1 is the falling edge. 1: 1 is the rising edge, and 0 is the falling edge.	0x0	R/W
6	DMIC23_FCOMP	Digital Microphone Channel 2 and Channel 3 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W

Bits	Bit Name	Description	Reset	Access
5	DMIC23_DEC_ORDER	Digital Microphone Channel 2 and Channel 3 Decimation Filter Order 0: Fourth-Order Decimation Filter 1: Fifth-Order Decimation Filter	0x0	R/W
4	DMIC23_HPF_EN	Digital Microphone Channel 2 and Channel 3 High-Pass Filter Enable 0: Highpass Filter Off 1: Highpass Filter On	0x0	R/W
[3:0]	DMIC23_FS	Digital Microphone Channel 2 and Channel 3 Output Sample Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DIGITAL MICROPHONE CHANNEL 4 AND CHANNEL 5 CONTROL REGISTER

Address: 0xF00000AC, Reset: 0x00000004, Name: DMIC_CTRL4

Rate, order, mapping, and edge control.

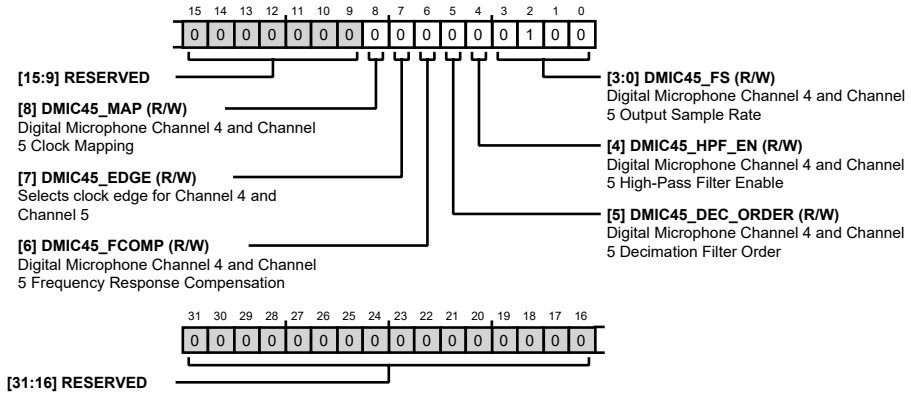


Table 83. Bit Descriptions for DMIC_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DMIC45_MAP	Digital Microphone Channel 4 and Channel 5 Clock Mapping 0: Digital microphone channels use DMIC_CLK0. 1: Digital microphone channels use DMIC_CLK1.	0x0	R/W
7	DMIC45_EDGE	Selects the clock edge for Channel 4 and Channel 5 0: 0 is the rising edge, and 1 is the falling edge. 1: 1 is the rising edge, and 0 is the falling edge.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
6	DMIC45_FCOMP	Digital Microphone Channel 4 and Channel 5 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W
5	DMIC45_DEC_ORDER	Digital Microphone Channel 4 and Channel 5 Decimation Filter Order 0: Fourth-Order Decimation Filter 1: Fifth-Order Decimation Filter	0x0	R/W
4	DMIC45_HPF_EN	Digital Microphone Channel 4 and Channel 5 High-Pass Filter Enable 0: High-Pass Filter Off 1: High-Pass Filter On	0x0	R/W
[3:0]	DMIC45_FS	Digital Microphone Channel 4 and Channel 5 Output Sample Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DIGITAL MICROPHONE CHANNEL 6 AND CHANNEL 7 CONTROL REGISTER

Address: 0xF00000B0, Reset: 0x00000004, Name: DMIC_CTRL5

Rate, order, mapping, and edge control.

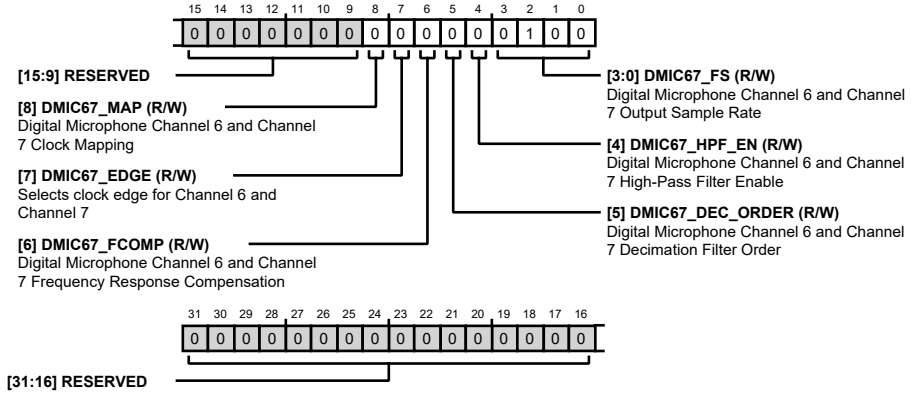


Table 84. Bit Descriptions for DMIC_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DMIC67_MAP	Digital Microphone Channel 6 and Channel 7 Clock Mapping 0: Digital microphone channels use DMIC_CLK0. 1: Digital microphone channels use DMIC_CLK1.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	DMIC67_EDGE	Selects the clock edge for Channel 6 and Channel 7 0: 0 is the rising edge, and 1 is the falling edge. 1: 1 is the rising edge, and 0 is the falling edge.	0x0	R/W
6	DMIC67_FCOMP	Digital Microphone Channel 6 and Channel 7 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W
5	DMIC67_DEC_ORDER	Digital Microphone Channel 6 and Channel 7 Decimation Filter Order 0: Fourth-Order Decimation Filter 1: Fifth-Order Decimation Filter	0x0	R/W
4	DMIC67_HPF_EN	Digital Microphone Channel 6 and Channel 7 Highpass Filter Enable 0: Highpass Filter Off 1: Highpass Filter On	0x0	R/W
[3:0]	DMIC67_FS	Digital Microphone Channel 6 and Channel 7 Output Sample Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DIGITAL MICROPHONE CHANNEL 8 AND CHANNEL 9 CONTROL REGISTER

Address: 0xF00000B4, Reset: 0x00000004, Name: DMIC_CTRL6

Rate, order, mapping, and edge control.

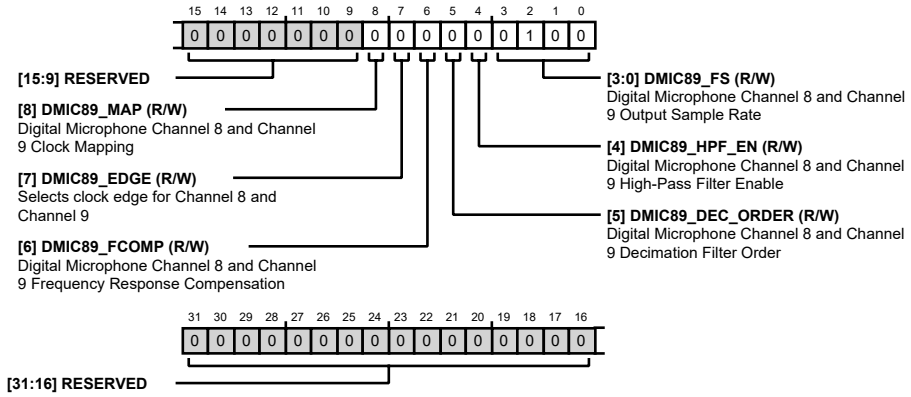


Table 85. Bit Descriptions for DMIC_CTRL6

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DMIC89_MAP	Digital Microphone Channel 8 and Channel 9 Clock Mapping 0: Digital microphone channels use DMIC_CLK0. 1: Digital microphone channels use DMIC_CLK1.	0x0	R/W
7	DMIC89_EDGE	Selects the clock edge for Channel 8 and Channel 9 0: 0 is the rising edge, and 1 is the falling edge. 1: 1 is the rising edge, and 0 is the falling edge.	0x0	R/W
6	DMIC89_FCOMP	Digital Microphone Channel 8 and Channel 9 Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated (higher delay).	0x0	R/W
5	DMIC89_DEC_ORDER	Digital Microphone Channel 8 and Channel 9 Decimation Filter Order 0: Fourth-Order Decimation Filter 1: Fifth-Order Decimation Filter	0x0	R/W
4	DMIC89_HPF_EN	Digital Microphone Channel 8 and Channel 9 Highpass Filter Enable 0: Highpass Filter Off 1: Highpass Filter On	0x0	R/W
[3:0]	DMIC89_FS	Digital Microphone Channel 8 and Channel 9 Output Sample Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DIGITAL MICROPHONE CHANNELS 0-3 HIGH-PASS FILTER CONTROL REGISTER

Address: 0xF00000B8, Reset: 0x000000DD, Name: DMIC_CTRL7

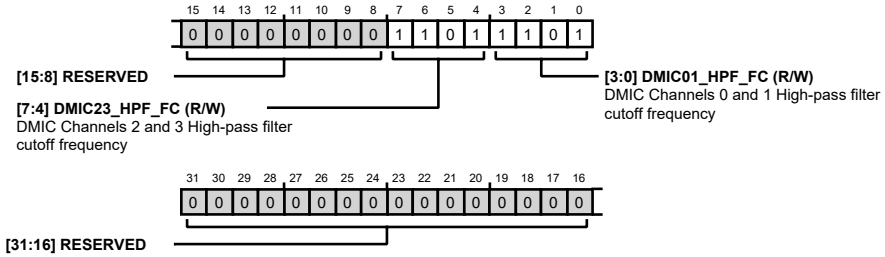


Table 86. Bit Descriptions for DMIC_CTRL7

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	DMIC23_HPF_FC	DMIC Channels 2 and 3 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz	0xD	R/W
[3:0]	DMIC01_HPF_FC	DMIC Channels 0 and 1 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz	0xD	R/W

DIGITAL MICROPHONE CHANNELS 4-7 HIGHPASS FILTER CONTROL REGISTER

Address: 0xF00000BC, Reset: 0x000000DD, Name: DMIC_CTRL8

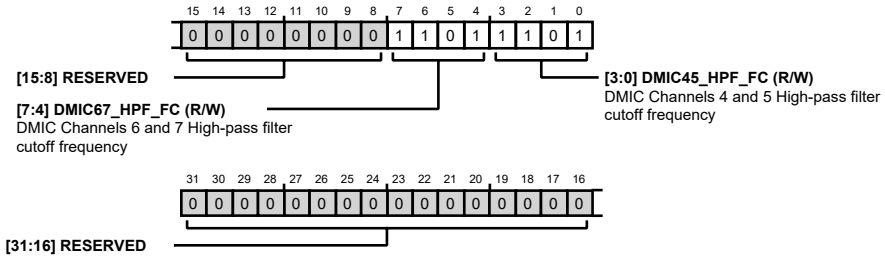


Table 87. Bit Descriptions for DMIC_CTRL8

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	DMIC67_HPF_FC	DMIC Channels 6 and 7 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz	0xD	R/W
[3:0]	DMIC45_HPF_FC	DMIC Channels 4 and 5 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz	0xD	R/W

Bits	Bit Name	Description	Reset	Access
		1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz		

DIGITAL MICROPHONE CHANNELS 8-9 HIGHPASS FILTER CONTROL REGISTER

Address: 0xF00000C0, Reset: 0x0000000D, Name: DMIC_CTRL9

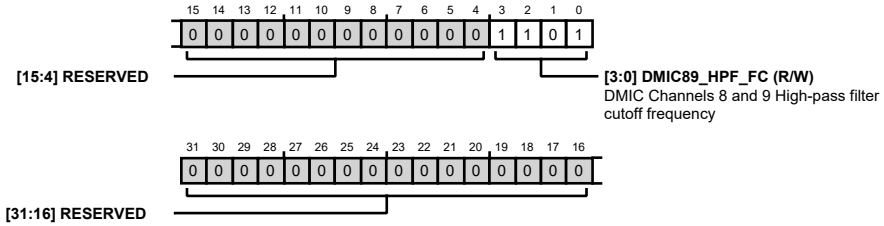


Table 88. Bit Descriptions for DMIC_CTRL9

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved	0x0	R
[3:0]	DMIC89_HPF_FC	DMIC Channels 8 and 9 Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz	0xD	R/W

DMIC VOLUME OPTIONS REGISTER

Address: 0xF00000C4, Reset: 0x00000004, Name: DMIC_CTRL10

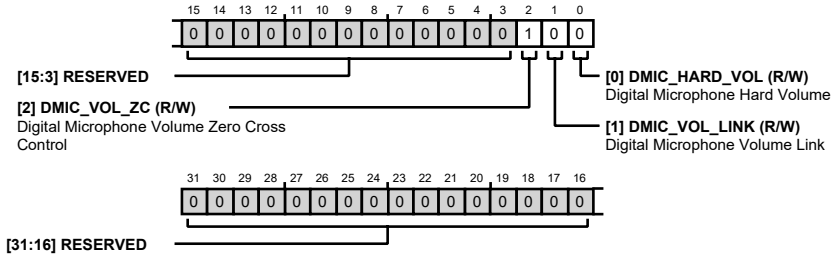


Table 89. Bit Descriptions for DMIC_CTRL10

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved	0x0	R
2	DMIC_VOL_ZC	Digital Microphone Volume Zero Cross Control 0: Volume change occurs at any time. 1: Volume change only occurs at zero crossing.	0x1	R/W
1	DMIC_VOL_LINK	Digital Microphone Volume Link 0: Each digital microphone channel uses its respective volume value. 1: All digital microphone channels use Channel 0 volume value.	0x0	R/W
0	DMIC_HARD_VOL	Digital Microphone Hard Volume 0: Soft Volume Ramping 1: Hard/Immediate Volume Change	0x0	R/W

DIGITAL MICROPHONE CHANNEL MUTE CONTROLS REGISTER

Address: 0xF00000C8, Reset: 0x00000000, Name: DMIC_MUTES

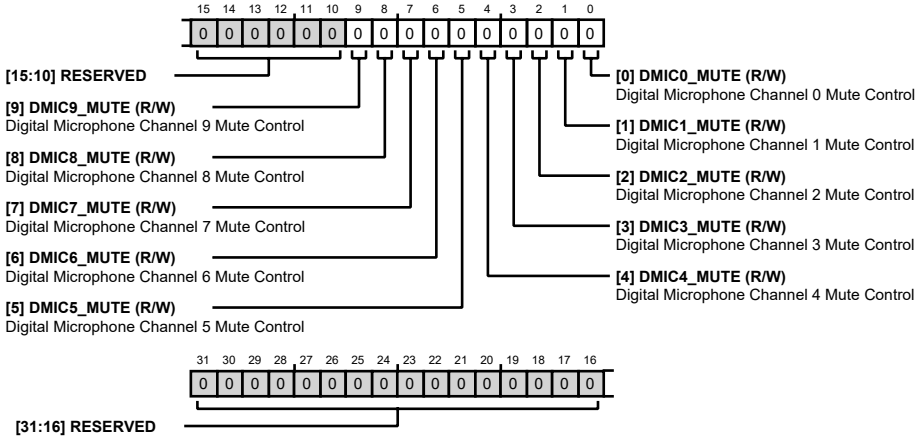


Table 90. Bit Descriptions for DMIC_MUTES

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	DMIC9_MUTE	Digital Microphone Channel 9 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
8	DMIC8_MUTE	Digital Microphone Channel 8 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
7	DMIC7_MUTE	Digital Microphone Channel 7 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
6	DMIC6_MUTE	Digital Microphone Channel 6 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W

Bits	Bit Name	Description	Reset	Access
5	DMIC5_MUTE	Digital Microphone Channel 5 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
4	DMIC4_MUTE	Digital Microphone Channel 4 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
3	DMIC3_MUTE	Digital Microphone Channel 3 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
2	DMIC2_MUTE	Digital Microphone Channel 2 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
1	DMIC1_MUTE	Digital Microphone Channel 1 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W
0	DMIC0_MUTE	Digital Microphone Channel 0 Mute Control 0: Digital Microphone Unmuted 1: Digital Microphone Muted	0x0	R/W

DIGITAL MICROPHONE CHANNEL 0 VOLUME CONTROL REGISTER

Address: 0xF00000CC, Reset: 0x00000040, Name: DMIC_VOL0

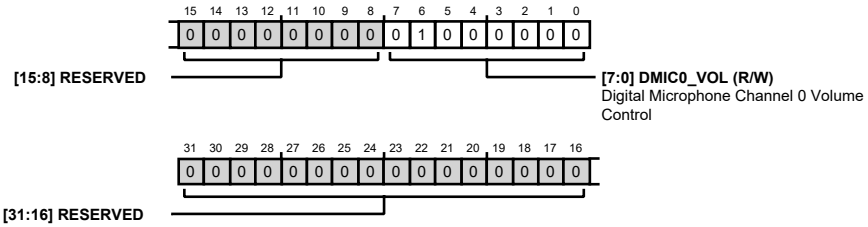


Table 91. Bit Descriptions for DMIC_VOL0

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC0_VOL	Digital Microphone Channel 0 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB … 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB …	0x40	R/W

Bits	Bit Name	Description	Reset	Access
		11111101: -70.875dB 11111110: -71.25dB 11111111: Mute		

DIGITAL MICROPHONE CHANNEL 1 VOLUME CONTROL REGISTER

Address: 0xF00000D0, Reset: 0x00000040, Name: DMIC_VOL1

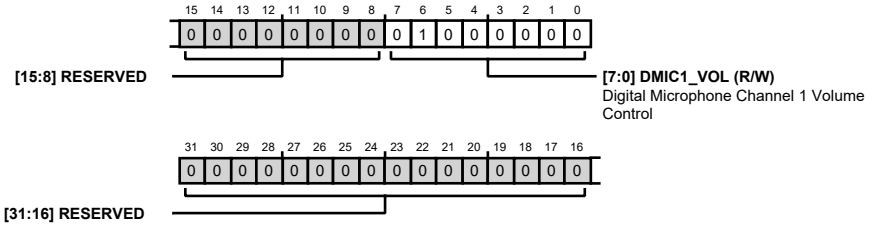


Table 92. Bit Descriptions for DMIC_VOL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC1_VOL	Digital Microphone Channel 1 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 2 VOLUME CONTROL REGISTER

Address: 0xF00000D4, Reset: 0x00000040, Name: DMIC_VOL2

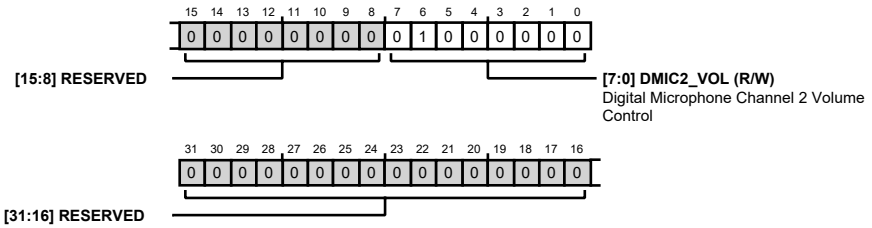


Table 93. Bit Descriptions for DMIC_VOL2

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC2_VOL	Digital Microphone Channel 2 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 3 VOLUME CONTROL REGISTER

Address: 0xF00000D8, Reset: 0x00000040, Name: DMIC_VOL3

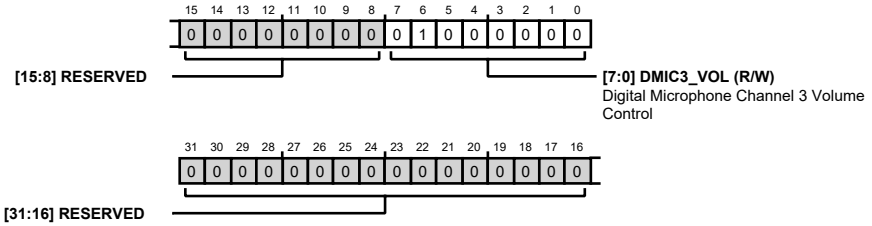


Table 94. Bit Descriptions for DMIC_VOL3

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC3_VOL	Digital Microphone Channel 3 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 4 VOLUME CONTROL REGISTER

Address: 0xF00000DC, Reset: 0x00000040, Name: DMIC_VOL4

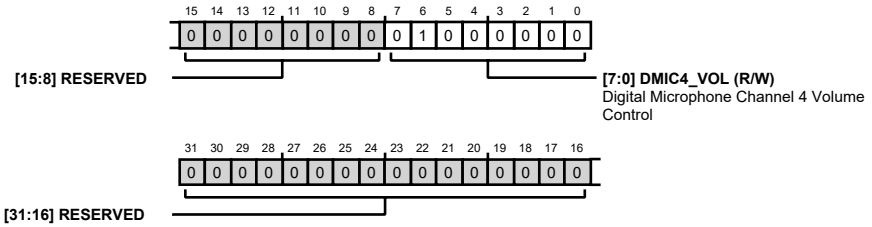


Table 95. Bit Descriptions for DMIC_VOL4

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC4_VOL	Digital Microphone Channel 4 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 5 VOLUME CONTROL REGISTER

Address: 0xF00000E0, Reset: 0x00000040, Name: DMIC_VOL5

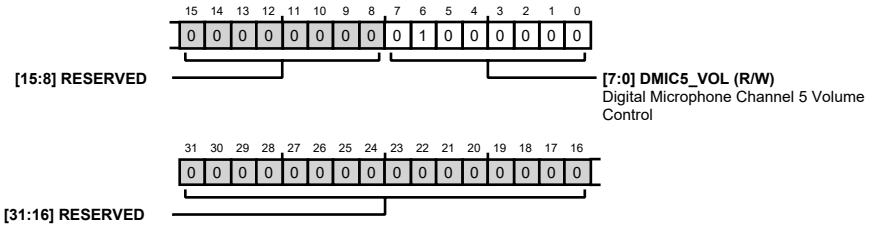


Table 96. Bit Descriptions for DMIC_VOL5

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC5_VOL	Digital Microphone Channel 5 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB	0x40	R/W

Bits	Bit Name	Description	Reset	Access
		... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute		

DIGITAL MICROPHONE CHANNEL 6 VOLUME CONTROL REGISTER

Address: 0xF00000E4, Reset: 0x00000040, Name: DMIC_VOL6

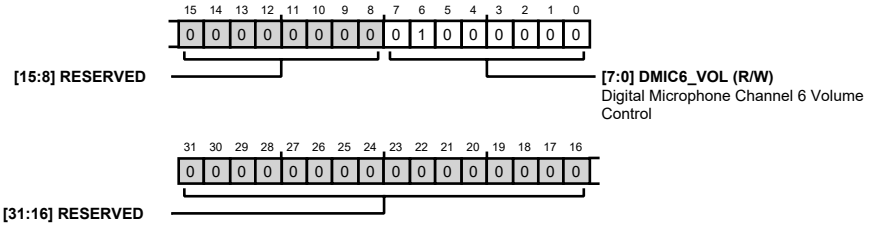


Table 97. Bit Descriptions for DMIC_VOL6

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC6_VOL	Digital Microphone Channel 6 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 7 VOLUME CONTROL REGISTER

Address: 0xF00000E8, Reset: 0x00000040, Name: DMIC_VOL7

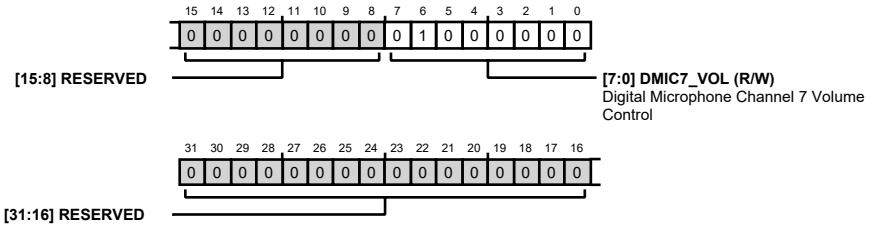


Table 98. Bit Descriptions for DMIC_VOL7

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC7_VOL	Digital Microphone Channel 7 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DIGITAL MICROPHONE CHANNEL 8 VOLUME CONTROL REGISTER

Address: 0xF00000EC, Reset: 0x00000040, Name: DMIC_VOL8

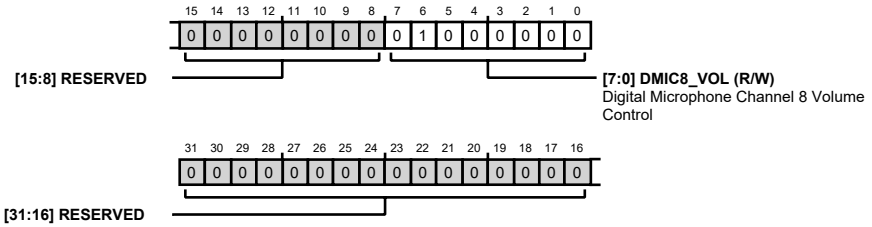


Table 99. Bit Descriptions for DMIC_VOL8

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC8_VOL	Digital Microphone Channel 8 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB	0x40	R/W

Bits	Bit Name	Description	Reset	Access
		... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute		

DIGITAL MICROPHONE CHANNEL 9 VOLUME CONTROL REGISTER

Address: 0xF00000F0, Reset: 0x00000040, Name: DMIC_VOL9

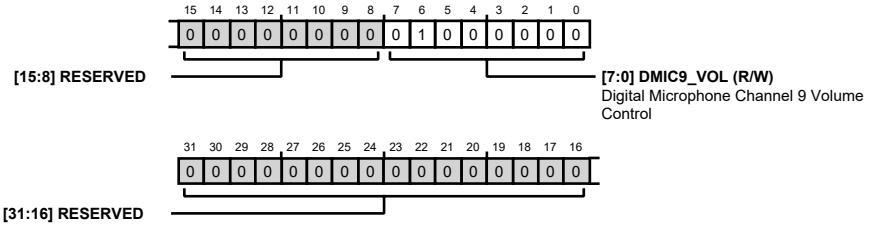


Table 100. Bit Descriptions for DMIC_VOL9

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DMIC9_VOL	Digital Microphone Channel 9 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

DAC SAMPLE RATE, FILTERING, AND POWER CONTROLS REGISTER

Address: 0xF00000F4, Reset: 0x00000044, Name: DAC_CTRL1

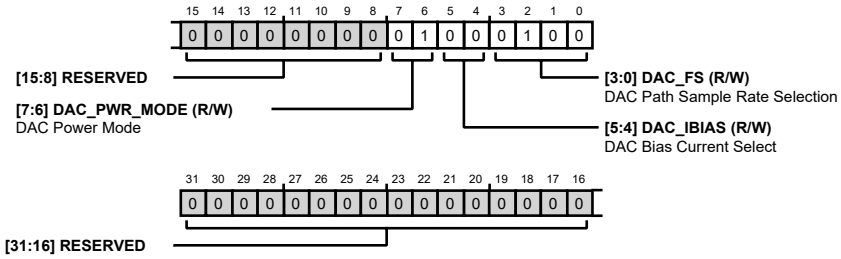


Table 101. Bit Descriptions for DAC_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:6]	DAC_PWR_MODE	DAC Power Mode 00: No power savings. 01: Low power savings mode. 10: High power savings mode (1µs additional latency).	0x1	R/W
[5:4]	DAC_IBIAS	DAC Bias Current Select. Higher bias currents result in higher performance. 00: Normal Operation (Default) 01: Power Saving 10: Enhanced Performance 11: Reserved	0x0	R/W
[3:0]	DAC_FS	DAC Path Sample Rate Selection 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

DAC VOLUME LINK, HPF, AND MUTE CONTROLS REGISTER

Address: 0xF00000F8, Reset: 0x00000044, Name: DAC_CTRL2

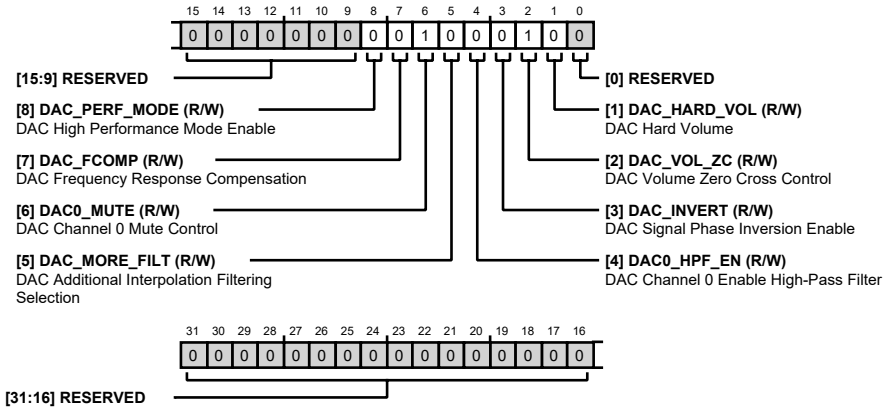


Table 102. Bit Descriptions for DAC_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	DAC_PERF_MODE	DAC High-Performance Mode Enable 0: Normal Operation 1: DAC High-Performance Mode Enabled	0x0	R/W
7	DAC_FCOMP	DAC Frequency Response Compensation 0: High-frequency response is not compensated (lower delay). 1: High-frequency response is compensated for sample rates of 192kHz or lower when DAC_MORE_FILT = 1 (higher delay).	0x0	R/W
6	DAC0_MUTE	DAC Channel 0 Mute Control 0: DAC Unmuted 1: DAC Muted	0x1	R/W
5	DAC_MORE_FILT	DAC Additional Interpolation Filtering Selection 0: Less Interpolation Filtering: Lower Delay 1: More Interpolation Filtering: Higher Delay	0x0	R/W
4	DAC0_HPF_EN	DAC Channel 0 Enable High-Pass Filter 0: DAC Highpass Filter Off 1: DAC Highpass Filter On	0x0	R/W
3	DAC_INVERT	DAC Signal Phase Inversion Enable 0: No phase inversion in DAC. 1: DAC will invert the signal phase 180 degrees.	0x0	R/W
2	DAC_VOL_ZC	DAC Volume Zero Cross Control 0: Volume change occurs at any time. 1: Volume change only occurs at zero crossing.	0x1	R/W
1	DAC_HARD_VOL	DAC Hard Volume 0: Soft Volume Ramping 1: Hard/Immediate Volume Change	0x0	R/W
0	RESERVED	Reserved	0x0	R

DAC CHANNEL 0 HIGHPASS FILTER CUTOFF CONTROL REGISTER

Address: 0xF00000FC, Reset: 0x0000000D, Name: DAC_CTRL3

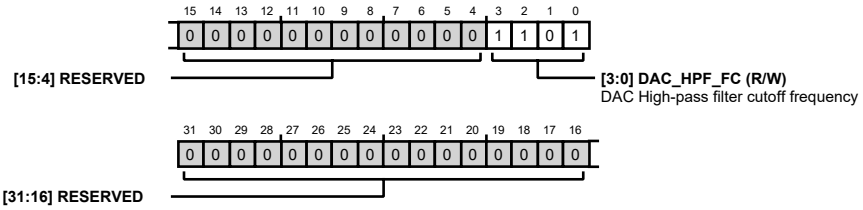


Table 103. Bit Descriptions for DAC_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved	0x0	R
[3:0]	DAC_HPF_FC	DAC Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz 1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz	0xD	R/W

DAC CHANNEL 0 VOLUME REGISTER

Address: 0xF0000100, Reset: 0x00000040, Name: DAC_VOL0

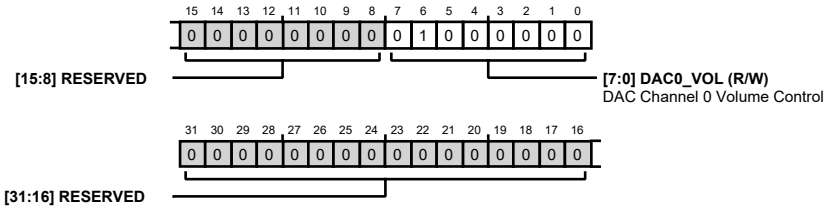


Table 104. Bit Descriptions for DAC_VOL0

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DAC0_VOL	DAC Channel 0 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB	0x40	R/W

Bits	Bit Name	Description	Reset	Access
		00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute		

DAC CLIPPING CONTROL REGISTER

Address: 0xF0000104, Reset: 0x000000FF, Name: DAC_HF_CLIP

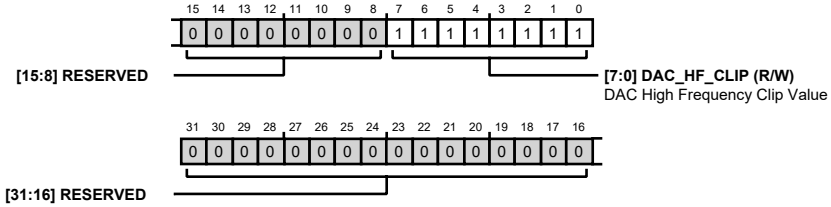


Table 105. Bit Descriptions for DAC_HF_CLIP

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	DAC_HF_CLIP	DAC High-Frequency Clip Value 11111111: No Clipping 11111110: Clip to 255/256 11111101: Clip to 254/256 11111100: ... 00000000: Clip to 1/256	0xFF	R/W

DAC CHANNEL 0 ROUTING REGISTER

Address: 0xF0000108, Reset: 0x00000000, Name: DAC_ROUTE0

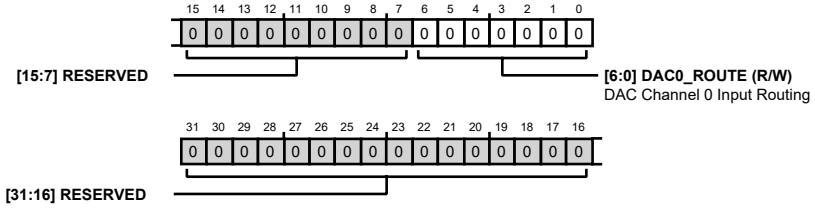


Table 106. Bit Descriptions for DAC_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	DAC0_ROUTE	DAC Channel 0 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9. 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: HiFi Core TIE Output 0111100: Digital Microphone Channel 0 0111101: Digital Microphone Channel 1 0111110: Digital Microphone Channel 2 0111111: Digital Microphone Channel 3 1000000: Digital Microphone Channel 4 1000001: Digital Microphone Channel 5 1000010: Digital Microphone Channel 6 1000011: Digital Microphone Channel 7 1000100: Digital Microphone Channel 8 1000101: Digital Microphone Channel 9 1000110: Audio Output DMA 0 Channel 0 1000111: Audio Output DMA 0 Channel 1 1001000: Audio Output DMA 0 Channel 2 1001001: Audio Output DMA 0 Channel 3 1001010: Audio Output DMA 0 Channel 4 1001011: Audio Output DMA 0 Channel 5 1001100: Audio Output DMA 0 Channel 6 1001101: Audio Output DMA 0 Channel 7 1001110: Audio Output DMA 1 Channel 0 1001111: Audio Output DMA 1 Channel 1 1010000: Audio Output DMA 1 Channel 2 1010001: Audio Output DMA 1 Channel 3 1010010: Audio Output DMA 1 Channel 4 1010011: Audio Output DMA 1 Channel 5 1010100: Audio Output DMA 1 Channel 6		

Bits	Bit Name	Description	Reset	Access
		1010101: Audio Output DMA 1 Channel 7 1010110: Audio Output DMA 2 Channel 0 1010111: Audio Output DMA 2 Channel 1 1011000: Audio Output DMA 2 Channel 2 1011001: Audio Output DMA 2 Channel 3 1011010: Audio Output DMA 2 Channel 4 1011011: Audio Output DMA 2 Channel 5 1011100: Audio Output DMA 2 Channel 6 1011101: Audio Output DMA 2 Channel 7 1011110: Slow to Fast Interpolator Channel 0 1011111: Slow to Fast Interpolator Channel 1 1100000: Slow to Fast Interpolator Channel 2 1100001: Slow to Fast Interpolator Channel 3 1100010: Slow to Fast Interpolator Channel 4 1100011: Slow to Fast Interpolator Channel 5 1100100: Slow to Fast Interpolator Channel 6 1100101: Slow to Fast Interpolator Channel 7 1100110: Audio Bus Map out 0 1100111: Audio Bus Map out 1 1101000: Audio Bus Map out 2 1101001: Audio Bus Map out 3 1101010: Audio Bus Map out 4 1101011: Audio Bus Map out 5 1101100: Audio Bus Map out 6 1101101: Audio Bus Map out 7 1101110: Audio Bus Map out 8 1101111: Audio Bus Map out 9 1110000: Audio Bus Map out 10 1110001: Audio Bus Map out 11 1110010: Audio Bus Map out 12 1110011: Audio Bus Map out 13 1110100: Audio Bus Map out 14 1110101: Audio Bus Map out 15		

HEADPHONE CONTROL REGISTER

Address: 0xF000010C, Reset: 0x00000024, Name: HP_CTRL1

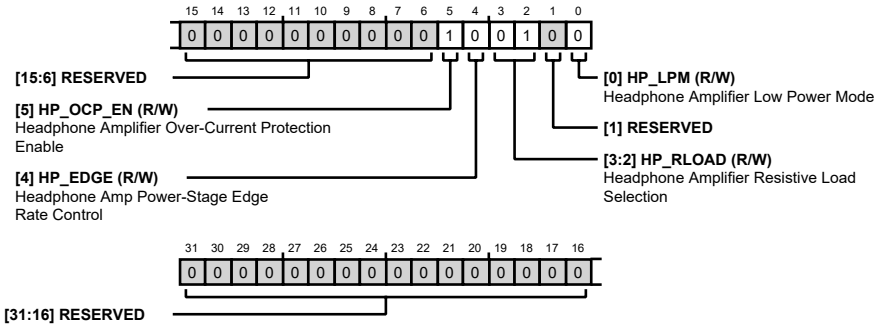


Table 107. Bit Descriptions for HP_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved.	0x0	R
5	HP_OCP_EN	Headphone Amplifier Over-Current Protection Enable 0: Over-Current Protection Disabled 1: Over-Current Protection Enabled	0x1	R/W
4	HP_EDGE	Headphone Amp Power-Stage Edge Rate Control. This controls the edge speed of the power stage. The low EMI operation mode reduces the edge speed, lowering EMI and power efficiency. 0: Normal Operation 1: Low EMI Mode Operation	0x0	R/W
[3:2]	HP_RLOAD	Headphone Amplifier Resistive Load Selection 00: 8Ω Headphone Amplifier Resistive Load 01: 16Ω Headphone Amplifier Resistive Load 10: 24Ω Headphone Amplifier Resistive Load 11: 32Ω or Higher Headphone Amplifier Resistive Load	0x1	R/W
1	RESERVED	Reserved	0x0	R
0	HP_LPM	Headphone Amplifier Low-Power Mode 0: Headphone amp high-performance mode. 1: Headphone amp low-power mode.	0x0	R/W

HEADPHONE PROTECTIONS REGISTER

Address: 0xF0000110, Reset: 0x00000000, Name: HP_CTRL2

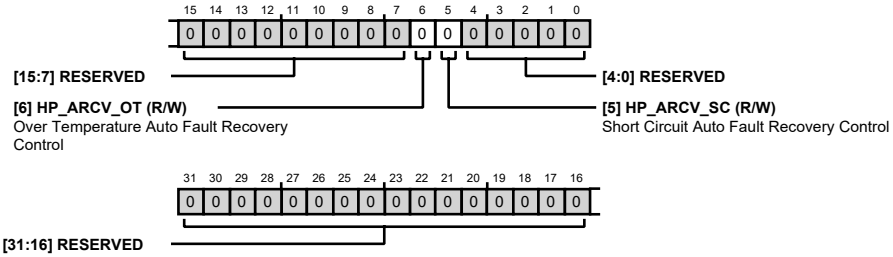


Table 108. Bit Descriptions for HP_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HP_ARCV_OT	Over-Temperature Auto Fault Recovery Control 0: Auto Fault Recovery for Over-Temperature Fault 1: Manual Fault Recovery for Over-Temperature Fault	0x0	R/W
5	HP_ARCV_SC	Short-Circuit Auto Fault Recovery Control 0: Auto Fault Recovery for Over-Current Fault 1: Manual Fault Recovery for Over-Current Fault	0x0	R/W
[4:0]	RESERVED	Reserved	0x0	R

FAST TO SLOW DECIMATOR SAMPLE RATES CHANNEL 0 AND CHANNEL 1 REGISTER

Address: 0xF0000118, Reset: 0x00000047, Name: FDEC_CTRL1

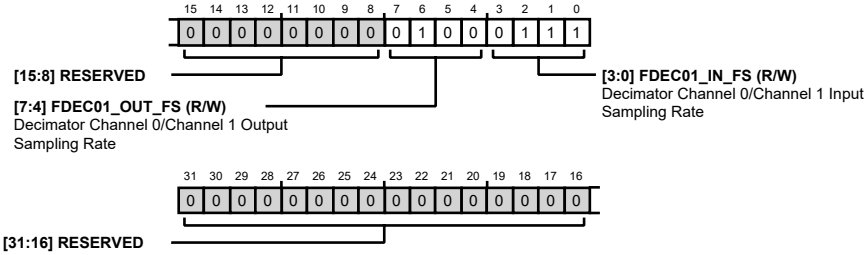


Table 109. Bit Descriptions for FDEC_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	FDEC01_OUT_FS	Decimator Channel 0/Channel 1 Output Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W
[3:0]	FDEC01_IN_FS	Decimator Channel 0/Channel 1 Input Sampling Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x7	R/W

FAST TO SLOW DECIMATOR SAMPLE RATES CHANNEL 2 AND CHANNEL 3 REGISTER

Address: 0xF000011C, Reset: 0x00000047, Name: FDEC_CTRL2

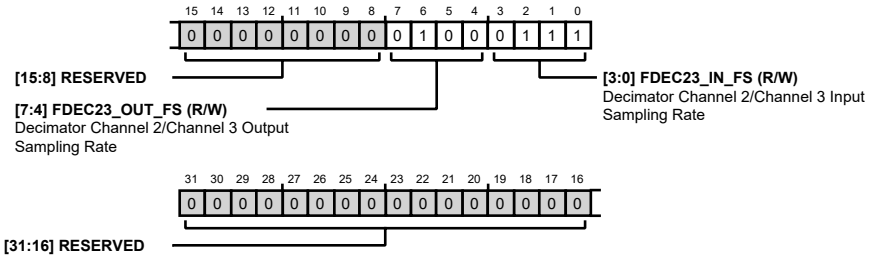


Table 110. Bit Descriptions for FDEC_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	FDEC23_OUT_FS	Decimator Channel 2/Channel 3 Output Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W
[3:0]	FDEC23_IN_FS	Decimator Channel 2/Channel 3 Input Sampling Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x7	R/W

FAST TO SLOW DECIMATOR SAMPLE RATES CHANNEL 4 AND CHANNEL 5 REGISTER

Address: 0xF0000120, Reset: 0x00000047, Name: FDEC_CTRL3

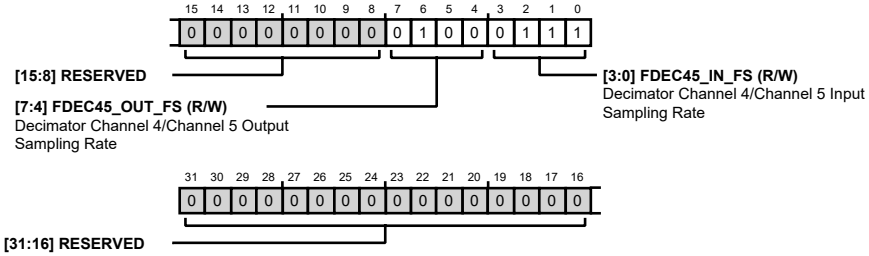


Table 111. Bit Descriptions for FDEC_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	FDEC45_OUT_FS	Decimator Channel 4/Channel 5 Output Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W
[3:0]	FDEC45_IN_FS	Decimator Channel 4/Channel 5 Input Sampling Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x7	R/W

FAST TO SLOW DECIMATOR SAMPLE RATES CHANNEL 6 AND CHANNEL 7 REGISTER

Address: 0xF0000124, Reset: 0x00000047, Name: FDEC_CTRL4

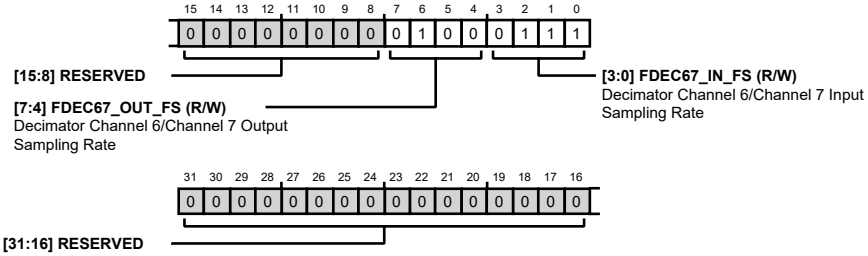


Table 112. Bit Descriptions for FDEC_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	FDEC67_OUT_FS	Decimator Channel 6/Channel 7 Output Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W

Bits	Bit Name	Description	Reset	Access
[3:0]	FDEC67_IN_FS	Decimator Channel 6/Channel 7 Input Sampling Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x7	R/W

FAST TO SLOW DECIMATOR CHANNEL 0 INPUT ROUTING REGISTER

Address: 0xF0000128, Reset: 0x00000000, Name: FDEC_ROUTE0

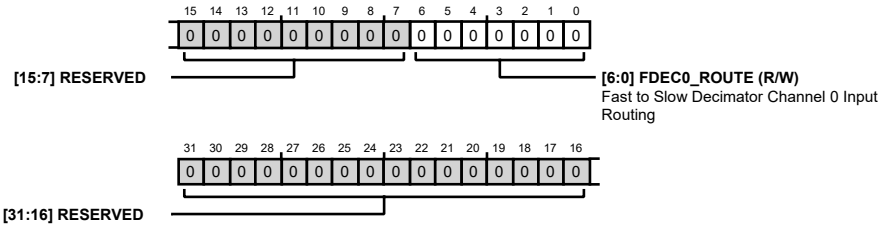


Table 113. Bit Descriptions for FDEC_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC0_ROUTE	Fast to Slow Decimator Channel 0 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11		

Bits	Bit Name	Description	Reset	Access
		1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 1 INPUT ROUTING REGISTER

Address: 0xF000012C, Reset: 0x00000000, Name: FDEC_ROUTE1

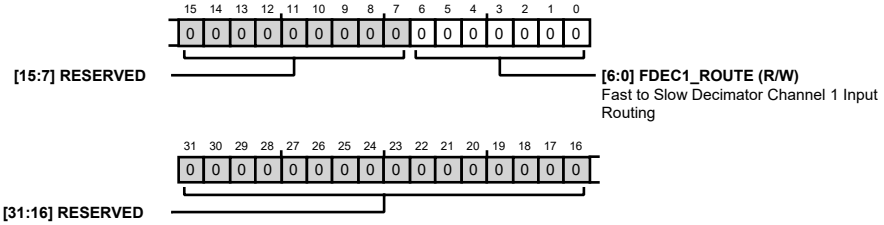


Table 114. Bit Descriptions for FDEC_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC1_ROUTE	Fast to Slow Decimator Channel 1 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4		

Bits	Bit Name	Description	Reset	Access
		1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 2 INPUT ROUTING REGISTER

Address: 0xF0000130, Reset: 0x00000000, Name: FDEC_ROUTE2

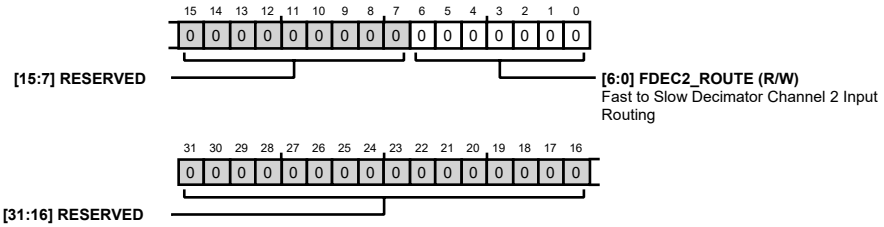


Table 115. Bit Descriptions for FDEC_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC2_ROUTE	Fast to Slow Decimator Channel 2 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5		

Bits	Bit Name	Description	Reset	Access
		1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 3 INPUT ROUTING REGISTER

Address: 0xF0000134, Reset: 0x00000000, Name: FDEC_ROUTE3

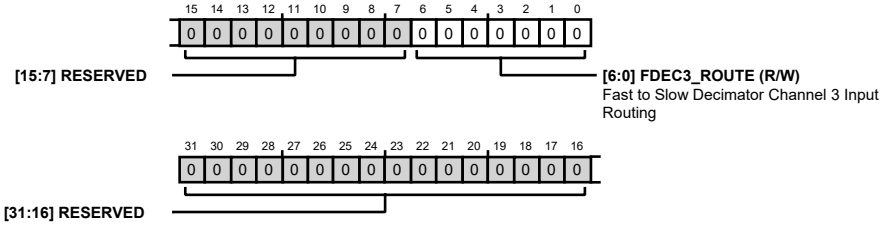


Table 116. Bit Descriptions for FDEC_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC3_ROUTE	Fast to Slow Decimator Channel 3 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6		

Bits	Bit Name	Description	Reset	Access
		1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 4 INPUT ROUTING REGISTER

Address: 0xF0000138, Reset: 0x00000000, Name: FDEC_ROUTE4

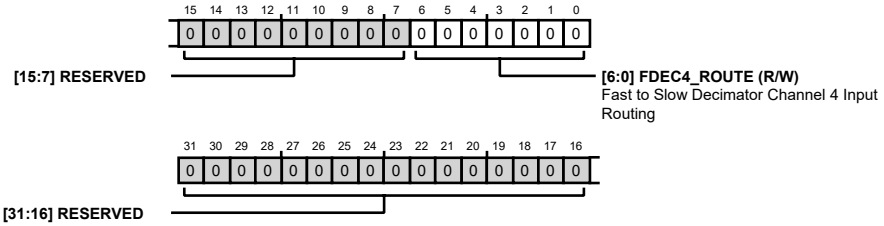


Table 117. Bit Descriptions for FDEC_ROUTE4

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC4_ROUTE	Fast to Slow Decimator Channel 4 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10		

Bits	Bit Name	Description	Reset	Access
		0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6		

Bits	Bit Name	Description	Reset	Access
		1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 5 INPUT ROUTING REGISTER

Address: 0xF000013C, Reset: 0x00000000, Name: FDEC_ROUTE5

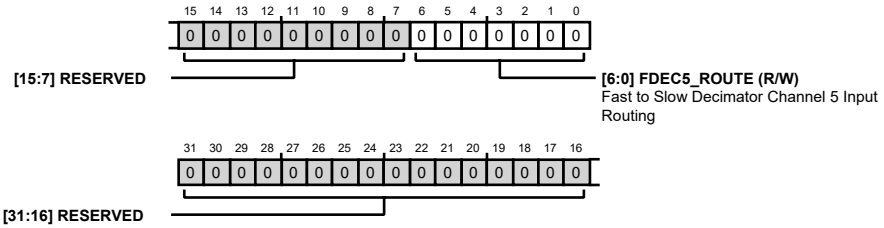


Table 118. Bit Descriptions for FDEC_ROUTE5

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC5_ROUTE	Fast to Slow Decimator Channel 5 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2		

Bits	Bit Name	Description	Reset	Access
		0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 6 INPUT ROUTING REGISTER

Address: 0xF0000140, Reset: 0x00000000, Name: FDEC_ROUTE6

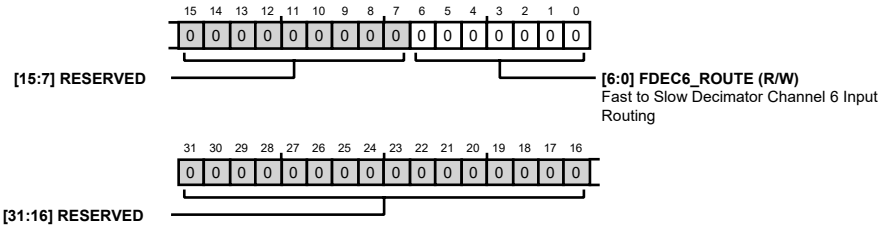


Table 119. Bit Descriptions for FDEC_ROUTE6

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC6_ROUTE	Fast to Slow Decimator Channel 6 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10		

Bits	Bit Name	Description	Reset	Access
		1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0 1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12		

Bits	Bit Name	Description	Reset	Access
		1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

FAST TO SLOW DECIMATOR CHANNEL 7 INPUT ROUTING REGISTER

Address: 0xF0000144, Reset: 0x00000000, Name: FDEC_ROUTE7

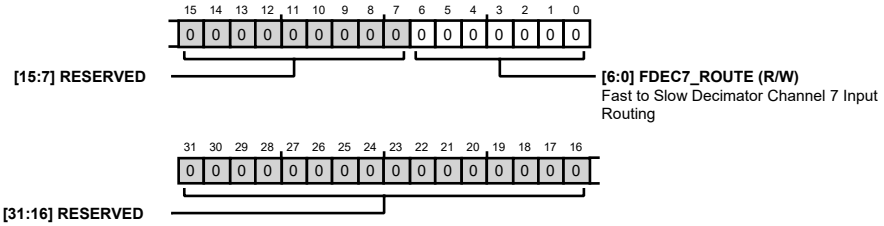


Table 120. Bit Descriptions for FDEC_ROUTE7

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDEC7_ROUTE	Fast to Slow Decimator Channel 7 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Input ASRC 0 Channel 0 0010001: Input ASRC 0 Channel 1 0010010: Input ASRC 0 Channel 2 0010011: Input ASRC 0 Channel 3 0010100: Input ASRC 1 Channel 0 0010101: Input ASRC 1 Channel 1 0010110: Input ASRC 1 Channel 2 0010111: Input ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: HiFi Core TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Serial Port 0 Channel 0 0100111: Serial Port 0 Channel 1 0101000: Serial Port 0 Channel 2 0101001: Serial Port 0 Channel 3 0101010: Serial Port 0 Channel 4 0101011: Serial Port 0 Channel 5 0101100: Serial Port 0 Channel 6 0101101: Serial Port 0 Channel 7 0101110: Serial Port 0 Channel 8 0101111: Serial Port 0 Channel 9 0110000: Serial Port 0 Channel 10 0110001: Serial Port 0 Channel 11 0110010: Serial Port 0 Channel 12 0110011: Serial Port 0 Channel 13 0110100: Serial Port 0 Channel 14 0110101: Serial Port 0 Channel 15 0110110: Serial Port 1 Channel 0 0110111: Serial Port 1 Channel 1 0111000: Serial Port 1 Channel 2 0111001: Serial Port 1 Channel 3 0111010: Serial Port 1 Channel 4 0111011: Serial Port 1 Channel 5 0111100: Serial Port 1 Channel 6 0111101: Serial Port 1 Channel 7 0111110: Serial Port 1 Channel 8 0111111: Serial Port 1 Channel 9 1000000: Serial Port 1 Channel 10 1000001: Serial Port 1 Channel 11 1000010: Serial Port 1 Channel 12 1000011: Serial Port 1 Channel 13 1000100: Serial Port 1 Channel 14 1000101: Serial Port 1 Channel 15 1000110: Audio DMA 0 Channel 0		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio DMA 0 Channel 1 1001000: Audio DMA 0 Channel 2 1001001: Audio DMA 0 Channel 3 1001010: Audio DMA 0 Channel 4 1001011: Audio DMA 0 Channel 5 1001100: Audio DMA 0 Channel 6 1001101: Audio DMA 0 Channel 7 1001110: Audio DMA 1 Channel 0 1001111: Audio DMA 1 Channel 1 1010000: Audio DMA 1 Channel 2 1010001: Audio DMA 1 Channel 3 1010010: Audio DMA 1 Channel 4 1010011: Audio DMA 1 Channel 5 1010100: Audio DMA 1 Channel 6 1010101: Audio DMA 1 Channel 7 1010110: Audio DMA 2 Channel 0 1010111: Audio DMA 2 Channel 1 1011000: Audio DMA 2 Channel 2 1011001: Audio DMA 2 Channel 3 1011010: Audio DMA 2 Channel 4 1011011: Audio DMA 2 Channel 5 1011100: Audio DMA 2 Channel 6 1011101: Audio DMA 2 Channel 7 1011110: Audio Bus Map Out 0 1011111: Audio Bus Map Out 1 1100000: Audio Bus Map Out 2 1100001: Audio Bus Map Out 3 1100010: Audio Bus Map Out 4 1100011: Audio Bus Map Out 5 1100100: Audio Bus Map Out 6 1100101: Audio Bus Map Out 7 1100110: Audio Bus Map Out 8 1100111: Audio Bus Map Out 9 1101000: Audio Bus Map Out 10 1101001: Audio Bus Map Out 11 1101010: Audio Bus Map Out 12 1101011: Audio Bus Map Out 13 1101100: Audio Bus Map Out 14 1101101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR SAMPLE RATES CHANNEL 0/CHANNEL 1 REGISTER

Address: 0xF0000148, Reset: 0x00000054, Name: FINT_CTRL1

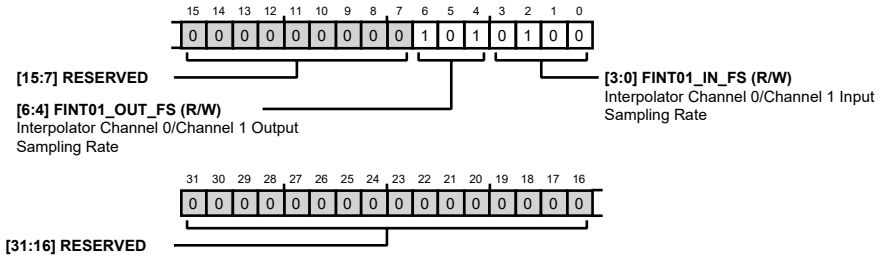


Table 121. Bit Descriptions for FINT_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:4]	FINT01_OUT_FS	Interpolator Channel 0/Channel 1 Output Sampling Rate 001: 24kHz Sample Rate 000: 16kHz Sample Rate 010: 48kHz Sample Rate 011: 96kHz Sample Rate 100: 192kHz Sample Rate 101: 384kHz Sample Rate 110: 768kHz Sample Rate	0x5	R/W
[3:0]	FINT01_IN_FS	Interpolator Channel 0/Channel 1 Input Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W

SLOW TO FAST INTERPOLATOR SAMPLE RATES CHANNEL 2/CHANNEL 3 REGISTER

Address: 0xF000014C, Reset: 0x00000054, Name: FINT_CTRL2

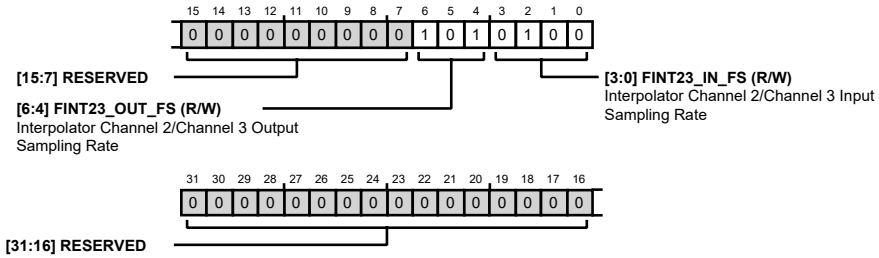


Table 122. Bit Descriptions for FINT_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:4]	FINT23_OUT_FS	Interpolator Channel 2/Channel 3 Output Sampling Rate 001: 24kHz Sample Rate 010: 48kHz Sample Rate 011: 96kHz Sample Rate 100: 192kHz Sample Rate 101: 384kHz Sample Rate 110: 768kHz Sample Rate 000: 16kHz Sample Rate	0x5	R/W
[3:0]	FINT23_IN_FS	Interpolator Channel 2/Channel 3 Input Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W

SLOW TO FAST INTERPOLATOR SAMPLE RATES CHANNEL 4/CHANNEL 5 REGISTER

Address: 0xF0000150, Reset: 0x00000054, Name: FINT_CTRL3

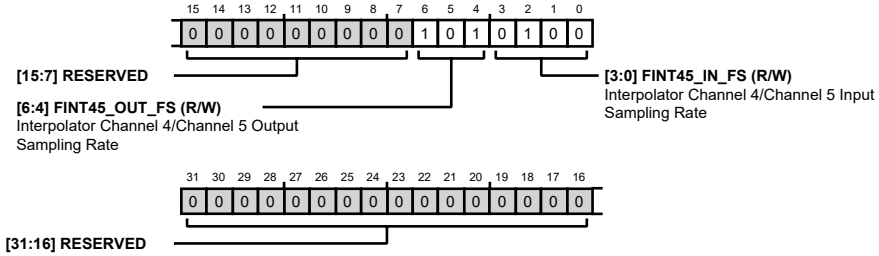


Table 123. Bit Descriptions for FINT_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:4]	FINT45_OUT_FS	Interpolator Channel 4/Channel 5 Output Sampling Rate 001: 24kHz Sample Rate 010: 48kHz Sample Rate 011: 96kHz Sample Rate 100: 192kHz Sample Rate 101: 384kHz Sample Rate 110: 768kHz Sample Rate 000: 16kHz Sample Rate	0x5	R/W

Bits	Bit Name	Description	Reset	Access
[3:0]	FINT45_IN_FS	Interpolator Channel 4/Channel 5 Input Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W

SLOW TO FAST INTERPOLATOR SAMPLE RATES CHANNEL 6/CHANNEL 7 REGISTER

Address: 0xF0000154, Reset: 0x00000054, Name: FINT_CTRL4

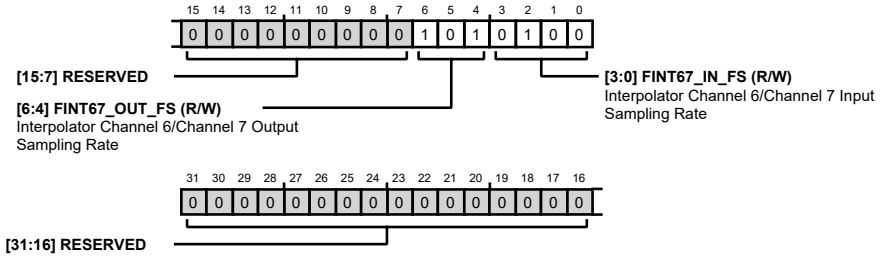


Table 124. Bit Descriptions for FINT_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:4]	FINT67_OUT_FS	Interpolator Channel 6/Channel 7 Output Sampling Rate 001: 24kHz Sample Rate 010: 48kHz Sample Rate 011: 96kHz Sample Rate 100: 192kHz Sample Rate 101: 384kHz Sample Rate 110: 768kHz Sample Rate 000: 16kHz Sample Rate	0x5	R/W
[3:0]	FINT67_IN_FS	Interpolator Channel 6/Channel 7 Input Sampling Rate 0000: 8kHz Sample Rate 0001: 12kHz Sample Rate 0010: 16kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate	0x4	R/W

SLOW TO FAST INTERPOLATOR CHANNEL 0 INPUT ROUTING REGISTER

Address: 0xF0000158, Reset: 0x00000000, Name: FINT_ROUTE0

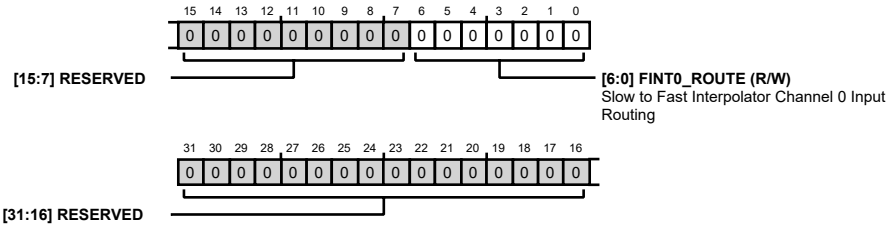


Table 125. Bit Descriptions for FINT_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT0_ROUTE	Slow to Fast Interpolator Channel 0 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1 0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5		

Bits	Bit Name	Description	Reset	Access
		1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 1 INPUT ROUTING REGISTER

Address: 0xF000015C, Reset: 0x00000000, Name: FINT_ROUTE1

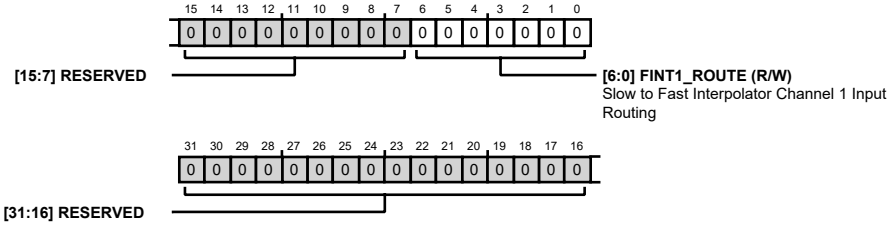


Table 126. Bit Descriptions for FINT_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT1_ROUTE	Slow to Fast Interpolator Channel 1 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5 1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 2 INPUT ROUTING REGISTER

Address: 0xF0000160, Reset: 0x00000000, Name: FINT_ROUTE2

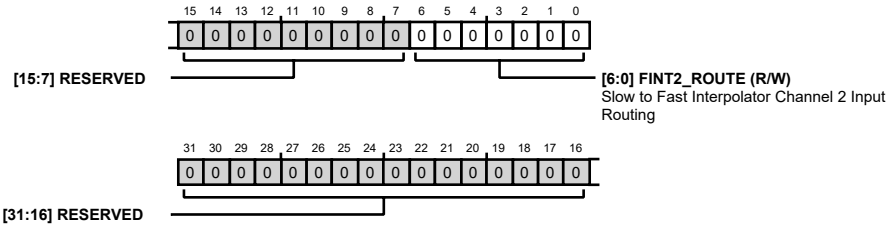


Table 127. Bit Descriptions for FINT_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT2_ROUTE	Slow to Fast Interpolator Channel 2 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1 0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5		

Bits	Bit Name	Description	Reset	Access
		1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 3 INPUT ROUTING REGISTER

Address: 0xF0000164, Reset: 0x00000000, Name: FINT_ROUTE3

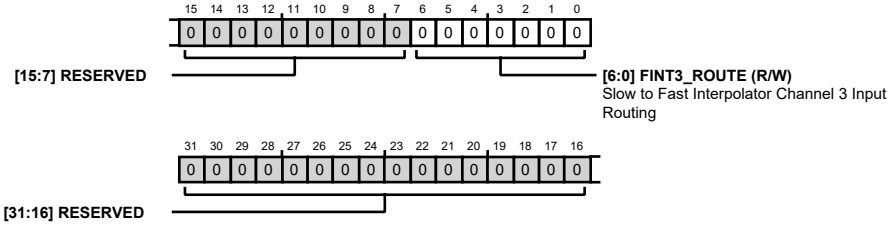


Table 128. Bit Descriptions for FINT_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved.	0x0	R
[6:0]	FINT3_ROUTE	Slow to Fast Interpolator Channel 3 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5 1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 4 INPUT ROUTING REGISTER

Address: 0xF0000168, Reset: 0x00000000, Name: FINT_ROUTE4

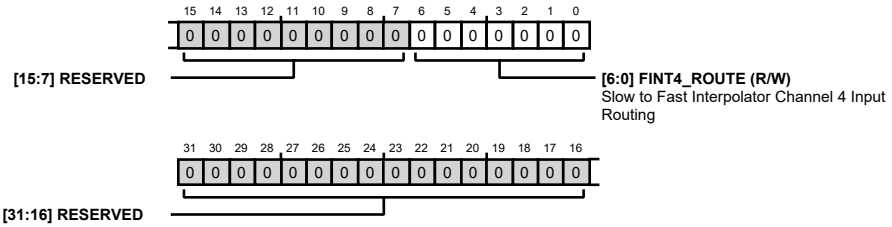


Table 129. Bit Descriptions for FINT_ROUTE4

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT4_ROUTE	Slow to Fast Interpolator Channel 4 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1 0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5		

Bits	Bit Name	Description	Reset	Access
		1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 5 INPUT ROUTING REGISTER

Address: 0xF000016C, Reset: 0x00000000, Name: FINT_ROUTE5

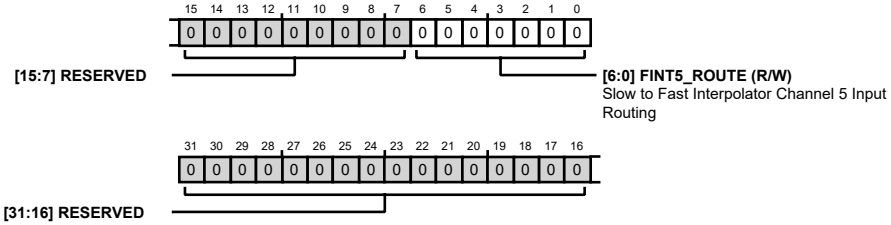


Table 130. Bit Descriptions for FINT_ROUTE5

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT5_ROUTE	Slow to Fast Interpolator Channel 5 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2. 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5 1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 6 INPUT ROUTING REGISTER

Address: 0xF0000170, Reset: 0x00000000, Name: FINT_ROUTE6

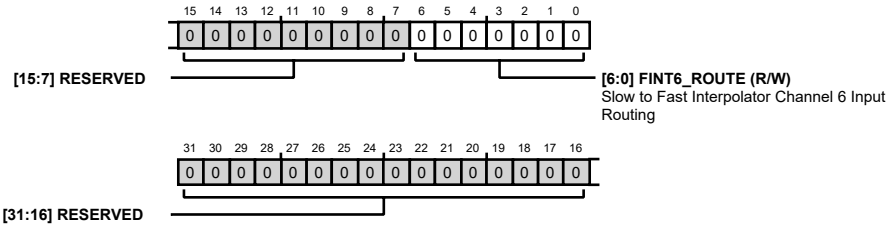


Table 131. Bit Descriptions for FINT_ROUTE6

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT6_ROUTE	Slow to Fast Interpolator Channel 6 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1 0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3 1001010: Audio DMA1 Channel 4 1001011: Audio DMA1 Channel 5		

Bits	Bit Name	Description	Reset	Access
		1001100: Audio DMA1 Channel 6 1001101: Audio DMA1 Channel 7 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

SLOW TO FAST INTERPOLATOR CHANNEL 7 INPUT ROUTING REGISTER

Address: 0xF0000174, Reset: 0x00000000, Name: FINT_ROUTE7

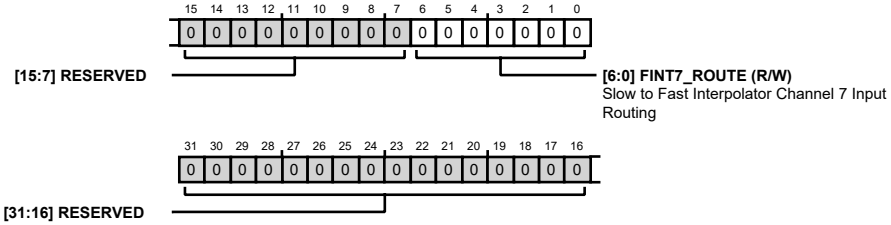


Table 132. Bit Descriptions for FINT_ROUTE7

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FINT7_ROUTE	Slow to Fast Interpolator Channel 7 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: Input ASRC 0 Channel 0 0100001: Input ASRC 0 Channel 1 0100010: Input ASRC 0 Channel 2 0100011: Input ASRC 0 Channel 3 0100100: Input ASRC 1 Channel 0 0100101: Input ASRC 1 Channel 1 0100110: Input ASRC 1 Channel 2 0100111: Input ASRC 1 Channel 3 0101000: ADC Channel 0 0101001: ADC Channel 1 0101010: ADC Channel 2 0101011: HiFi Core TIE Output 0101100: Digital Microphone Channel 0 0101101: Digital Microphone Channel 1 0101110: Digital Microphone Channel 2 0101111: Digital Microphone Channel 3 0110000: Digital Microphone Channel 4 0110001: Digital Microphone Channel 5 0110010: Digital Microphone Channel 6 0110011: Digital Microphone Channel 7 0110100: Digital Microphone Channel 8 0110101: Digital Microphone Channel 9 0110110: Audio DMA0 Channel 0 0110111: Audio DMA0 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111000: Audio DMA0 Channel 2 0111001: Audio DMA0 Channel 3 0111010: Audio DMA0 Channel 4 0111011: Audio DMA0 Channel 5 0111100: Audio DMA0 Channel 6 0111101: Audio DMA0 Channel 7 0111110: Audio DMA1 Channel 0 0111111: Audio DMA1 Channel 1 1000000: Audio DMA1 Channel 2 1000001: Audio DMA1 Channel 3 1000010: Audio DMA1 Channel 4 1000011: Audio DMA1 Channel 5 1000100: Audio DMA1 Channel 6 1000101: Audio DMA1 Channel 7 1000110: Audio DMA1 Channel 0 1000111: Audio DMA1 Channel 1 1001000: Audio DMA1 Channel 2 1001001: Audio DMA1 Channel 3. 1001010: Audio DMA1 Channel 4. 1001011: Audio DMA1 Channel 5. 1001100: Audio DMA1 Channel 6. 1001101: Audio DMA1 Channel 7. 1001110: Audio Bus Map Out 0 1001111: Audio Bus Map Out 1 1010000: Audio Bus Map Out 2 1010001: Audio Bus Map Out 3 1010010: Audio Bus Map Out 4 1010011: Audio Bus Map Out 5 1010100: Audio Bus Map Out 6 1010101: Audio Bus Map Out 7 1010110: Audio Bus Map Out 8 1010111: Audio Bus Map Out 9 1011000: Audio Bus Map Out 10 1011001: Audio Bus Map Out 11 1011010: Audio Bus Map Out 12 1011011: Audio Bus Map Out 13 1011100: Audio Bus Map Out 14 1011101: Audio Bus Map Out 15		

INPUT ASRC0 CONTROL, SOURCE AND RATE SELECTION REGISTER

Address: 0xF0000178, Reset: 0x00000004, Name: ASRCI0_CTRL

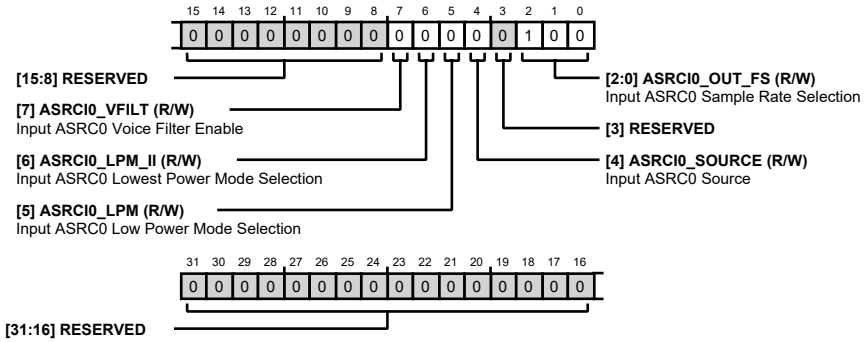


Table 133. Bit Descriptions for ASRCI0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	ASRCI0_VFILT	Input ASRC0 Voice Filter Enable 0: Voice Filter Off 1: Voice Filter On	0x0	R/W
6	ASRCI0_LPM_II	Input ASRC0 Lowest Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
5	ASRCI0_LPM	Input ASRC0 Low Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
4	ASRCI0_SOURCE	Input ASRC0 Source 0: Serial Audio Port 0 Source for Input ASRC 1: Serial Audio Port 1 Source for Input ASRC	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	ASRCI0_OUT_FS	Input ASRC0 Sample Rate Selection 000: 8kHz Sample Rate 001: 12kHz Sample Rate 010: 16kHz Sample Rate 011: 24kHz Sample Rate 100: 48kHz Sample Rate 101: 96kHz Sample Rate 110: 192kHz Sample Rate	0x4	R/W

INPUT ASRC0 CHANNEL 0 AND 1 INPUT ROUTING REGISTER

Address: 0xF000017C, Reset: 0x00000000, Name: ASRCI0_ROUTE01

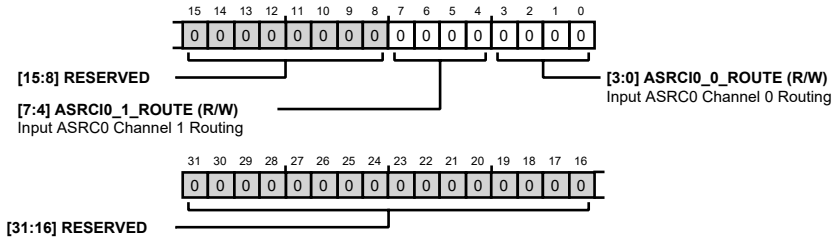


Table 134. Bit Descriptions for ASRCI0_ROUTE01

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ASRCI0_1_ROUTE	Input ASRC0 Channel 1 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8 1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12 1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15	0x0	R/W
[3:0]	ASRCI0_0_ROUTE	Input ASRC0 Channel 0 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8 1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15		

INPUT ASRC0 CHANNEL 2 AND 3 INPUT ROUTING REGISTER

Address: 0xF0000180, Reset: 0x00000000, Name: ASRCI0_ROUTE23

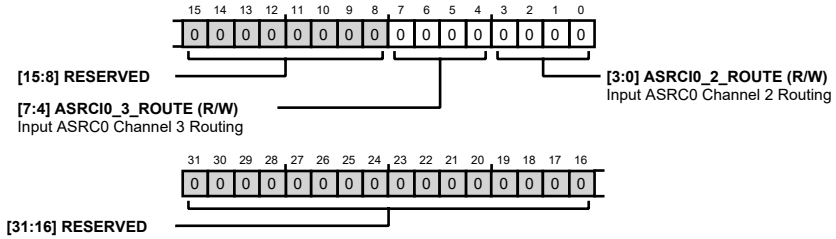


Table 135. Bit Descriptions for ASRCI0_ROUTE23

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ASRCI0_3_ROUTE	Input ASRC0 Channel 3 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8 1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12 1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15	0x0	R/W
[3:0]	ASRCI0_2_ROUTE	Input ASRC0 Channel 2 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12 1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15		

OUTPUT ASRC0 CONTROL REGISTER

Address: 0xF0000184, Reset: 0x00000004, Name: ASRCO0_CTRL

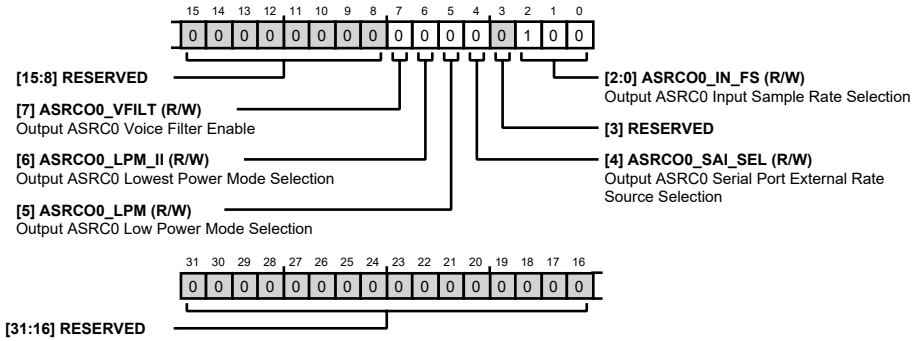


Table 136. Bit Descriptions for ASRCO0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	ASRCO0_VFILT	Output ASRC0 Voice Filter Enable 0: Voice Filter Off 1: Voice Filter On	0x0	R/W
6	ASRCO0_LPM_II	Output ASRC0 Lowest-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
5	ASRCO0_LPM	Output ASRC0 Low-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
4	ASRCO0_SAI_SEL	Output ASRC0 Serial Port External Rate Source Selection 0: Use Serial Port 0 as Rate Source 1: Use Serial Port 1 as Rate Source	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	ASRCO0_IN_FS	Output ASRC0 Input Sample Rate Selection 000: 8kHz Sample Rate 001: 12kHz Sample Rate 010: 16kHz Sample Rate 011: 24kHz Sample Rate	0x4	R/W

Bits	Bit Name	Description	Reset	Access
		100: 48kHz Sample Rate 101: 96kHz Sample Rate 110: 192kHz Sample Rate		

OUTPUT ASRC0 CHANNEL 0 INPUT ROUTING REGISTER

Address: 0xF0000188, Reset: 0x00000000, Name: ASRCO0_ROUTE0

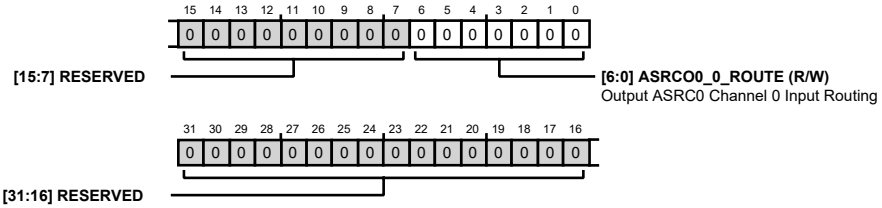


Table 137. Bit Descriptions for ASRCO0_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO0_0_ROUTE	Output ASRC0 Channel 0 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC0 CHANNEL 1 INPUT ROUTING REGISTER

Address: 0xF000018C, Reset: 0x00000000, Name: ASRCO0_ROUTE1

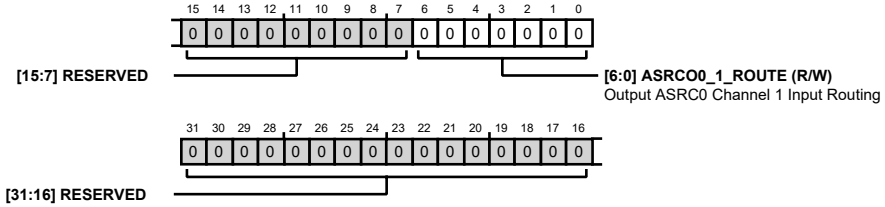


Table 138. Bit Descriptions for ASRCO0_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO0_1_ROUTE	Output ASRC0 Channel 1 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4		

Bits	Bit Name	Description	Reset	Access
		1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC0 CHANNEL 2 INPUT ROUTING REGISTER

Address: 0xF0000190, Reset: 0x00000000, Name: ASRCO0_ROUTE2

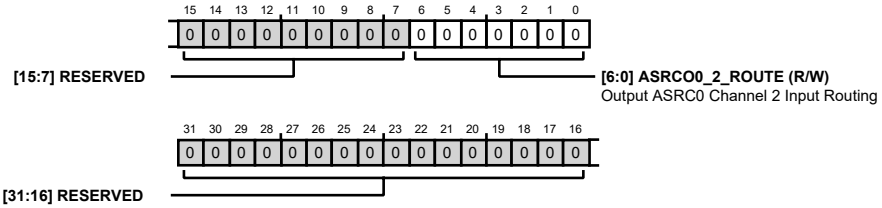


Table 139. Bit Descriptions for ASRCO0_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO0_2_ROUTE	Output ASRC0 Channel 2 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0		

Bits	Bit Name	Description	Reset	Access
		0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC0 CHANNEL 3 INPUT ROUTING REGISTER

Address: 0xF0000194, Reset: 0x00000000, Name: ASRCO0_ROUTE3

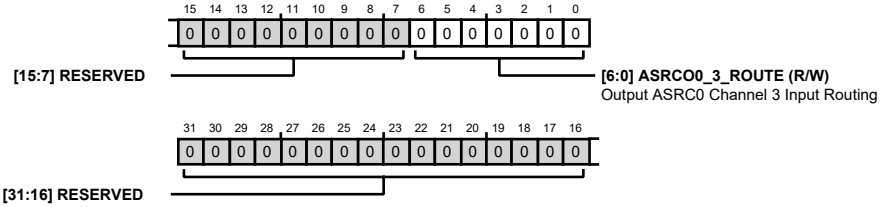


Table 140. Bit Descriptions for ASRCO0_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO0_3_ROUTE	Output ASRC0 Channel 3 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4		

Bits	Bit Name	Description	Reset	Access
		0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

INPUT ASRC1 CONTROL, SOURCE AND RATE SELECTION REGISTER

Address: 0xF0000198, Reset: 0x00000004, Name: ASRCI1_CTRL

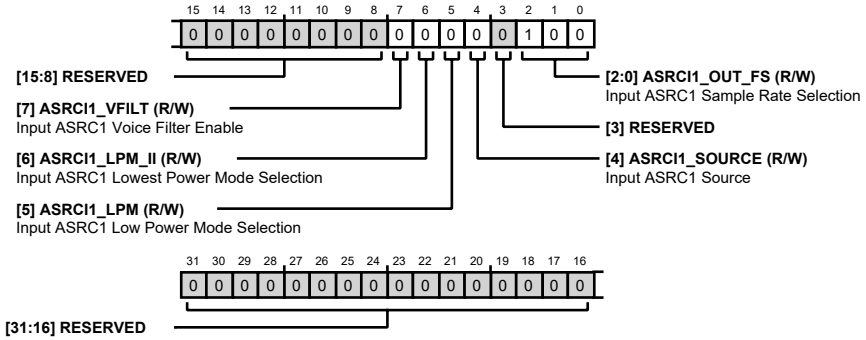


Table 141. Bit Descriptions for ASRCI1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	ASRCI1_VFILT	Input ASRC1 Voice Filter Enable 0: Voice Filter Off 1: Voice Filter On	0x0	R/W
6	ASRCI1_LPM_II	Input ASRC1 Lowest-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W

Bits	Bit Name	Description	Reset	Access
5	ASRCI1_LPM	Input ASRC1 Low-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
4	ASRCI1_SOURCE	Input ASRC1 Source 0: Serial Audio Port 0 Source for Input ASRC 1: Serial Audio Port 1 Source for Input ASRC	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	ASRCI1_OUT_FS	Input ASRC1 Sample Rate Selection 000: 8kHz Sample Rate 001: 12kHz Sample Rate 010: 16kHz Sample Rate 011: 24kHz Sample Rate 100: 48kHz Sample Rate 101: 96kHz Sample Rate 110: 192kHz Sample Rate	0x4	R/W

INPUT ASRC1 CHANNEL 0 AND 1 INPUT ROUTING REGISTER

Address: 0xF000019C, Reset: 0x00000000, Name: ASRCI1_ROUTE01

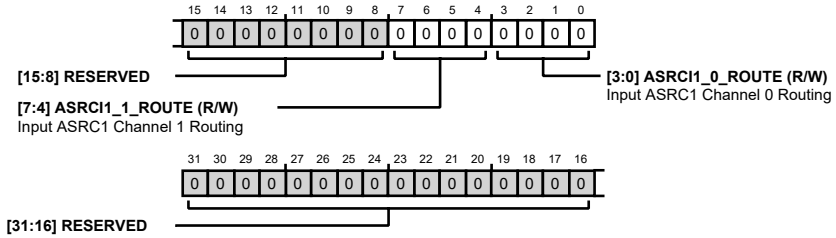


Table 142. Bit Descriptions for ASRCI1_ROUTE01

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ASRCI1_1_ROUTE	Input ASRC1 Channel 1 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8 1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		1101: Serial Port Channel 13		
		1110: Serial Port Channel 14		
		1111: Serial Port Channel 15		
[3:0]	ASRCI1_0_ROUTE	Input ASRC1 Channel 0 Routing	0x0	R/W
		0000: Serial Port Channel 0		
		0001: Serial Port Channel 1		
		0010: Serial Port Channel 2		
		0011: Serial Port Channel 3		
		0100: Serial Port Channel 4		
		0101: Serial Port Channel 5		
		0110: Serial Port Channel 6		
		0111: Serial Port Channel 7		
		1000: Serial Port Channel 8		
		1001: Serial Port Channel 9		
		1010: Serial Port Channel 10		
		1011: Serial Port Channel 11		
		1100: Serial Port Channel 12		
		1101: Serial Port Channel 13		
		1110: Serial Port Channel 14		
		1111: Serial Port Channel 15		

INPUT ASRC1 CHANNEL 2 AND 3 INPUT ROUTING REGISTER

Address: 0xF00001A0, Reset: 0x00000000, Name: ASRCI1_ROUTE23

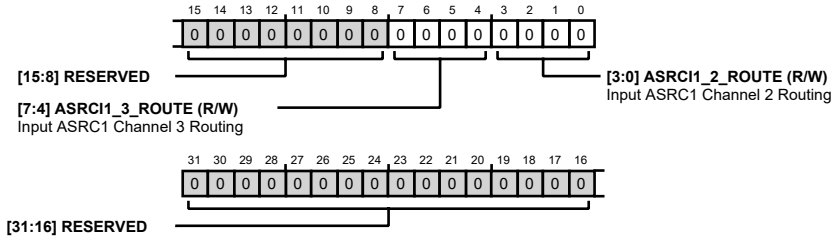


Table 143. Bit Descriptions for ASRCI1_ROUTE23

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	ASRCI1_3_ROUTE	Input ASRC1 Channel 3 Routing	0x0	R/W
		0000: Serial Port Channel 0		
		0001: Serial Port Channel 1		
		0010: Serial Port Channel 2		
		0011: Serial Port Channel 3		
		0100: Serial Port Channel 4		
		0101: Serial Port Channel 5		
		0110: Serial Port Channel 6		
		0111: Serial Port Channel 7		
		1000: Serial Port Channel 8		

Bits	Bit Name	Description	Reset	Access
		1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12 1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15		
[3:0]	ASRCI1_2_ROUTE	Input ASRC1 Channel 2 Routing 0000: Serial Port Channel 0 0001: Serial Port Channel 1 0010: Serial Port Channel 2 0011: Serial Port Channel 3 0100: Serial Port Channel 4 0101: Serial Port Channel 5 0110: Serial Port Channel 6 0111: Serial Port Channel 7 1000: Serial Port Channel 8 1001: Serial Port Channel 9 1010: Serial Port Channel 10 1011: Serial Port Channel 11 1100: Serial Port Channel 12 1101: Serial Port Channel 13 1110: Serial Port Channel 14 1111: Serial Port Channel 15	0x0	R/W

OUTPUT ASRC1 CONTROL REGISTER

Address: 0xF00001A4, Reset: 0x00000004, Name: ASRCO1_CTRL

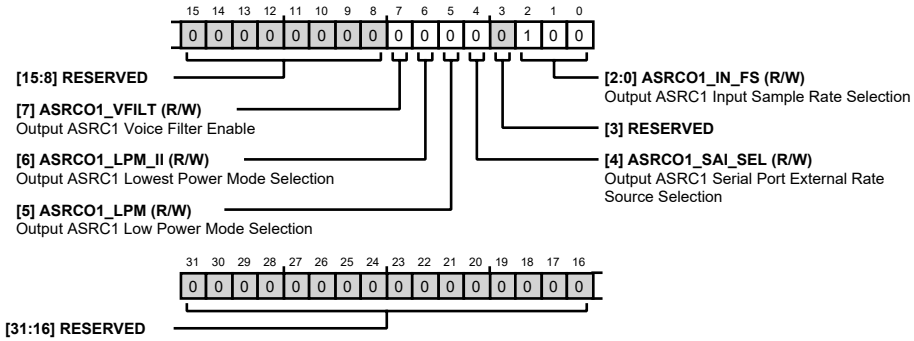


Table 144. Bit Descriptions for ASRCO1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	ASRCO1_VFILT	Output ASRC1 Voice Filter Enable 0: Voice Filter Off 1: Voice Filter On	0x0	R/W

Bits	Bit Name	Description	Reset	Access
6	ASRCO1_LPM_II	Output ASRC1 Lowest-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
5	ASRCO1_LPM	Output ASRC1 Low-Power Mode Selection 0: High-Performance Mode 1: Low-Power Mode	0x0	R/W
4	ASRCO1_SAI_SEL	Output ASRC1 Serial Port External Rate Source Selection 0: Use Serial Port 0 as Rate Source 1: Use Serial Port 1 as Rate Source	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	ASRCO1_IN_FS	Output ASRC1 Input Sample Rate Selection 000: 8kHz Sample Rate 001: 12kHz Sample Rate 010: 16kHz Sample Rate 011: 24kHz Sample Rate 100: 48kHz Sample Rate 101: 96kHz Sample Rate 110: 192kHz Sample Rate	0x4	R/W

OUTPUT ASRC1 CHANNEL 0 INPUT ROUTING REGISTER

Address: 0xF00001A8, Reset: 0x00000000, Name: ASRCO1_ROUTE0

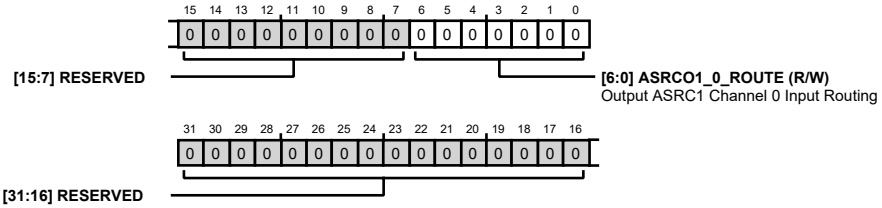


Table 145. Bit Descriptions for ASRCO1_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO1_0_ROUTE	Output ASRC1 Channel 0 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC1 CHANNEL 1 INPUT ROUTING REGISTER

Address: 0xF00001AC, Reset: 0x00000000, Name: ASRCO1_ROUTE1

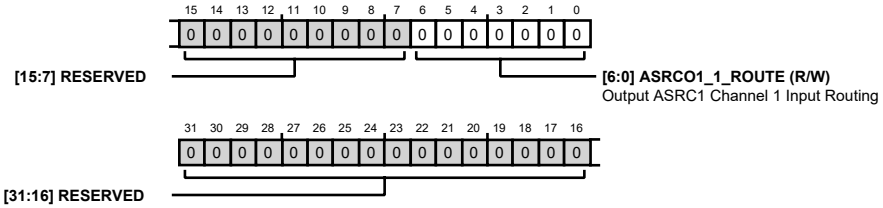


Table 146. Bit Descriptions for ASRCO1_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO1_1_ROUTE	Output ASRC1 Channel 1 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5		

Bits	Bit Name	Description	Reset	Access
		0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC1 CHANNEL 2 INPUT ROUTING REGISTER

Address: 0xF00001B0, Reset: 0x00000000, Name: ASRCO1_ROUTE2

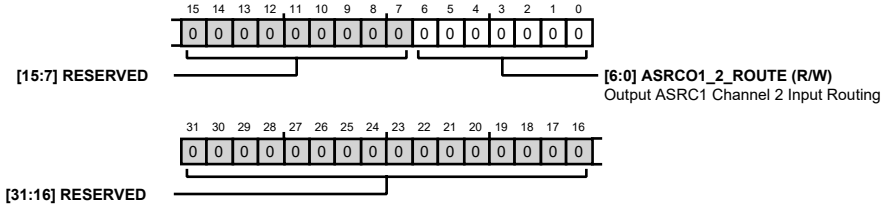


Table 147. Bit Descriptions for ASRCO1_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO1_2_ROUTE	Output ASRC1 Channel 2 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2 0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

OUTPUT ASRC1 CHANNEL 3 INPUT ROUTING REGISTER

Address: 0xF00001B4, Reset: 0x00000000, Name: ASRCO1_ROUTE3

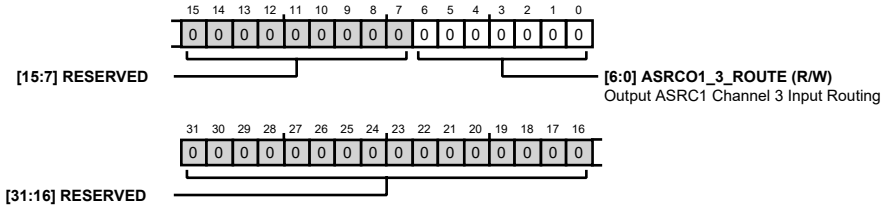


Table 148. Bit Descriptions for ASRCO1_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	ASRCO1_3_ROUTE	Output ASRC1 Channel 3 Input Routing 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: ADC Channel 0 0010001: ADC Channel 1 0010010: ADC Channel 2 0010011: HiFi Core TIE Output 0010100: Digital Microphone Channel 0 0010101: Digital Microphone Channel 1 0010110: Digital Microphone Channel 2 0010111: Digital Microphone Channel 3 0011000: Digital Microphone Channel 4 0011001: Digital Microphone Channel 5 0011010: Digital Microphone Channel 6 0011011: Digital Microphone Channel 7 0011100: Digital Microphone Channel 8 0011101: Digital Microphone Channel 9 0011110: Fast to Slow Decimator Channel 0 0011111: Fast to Slow Decimator Channel 1 0100000: Fast to Slow Decimator Channel 2 0100001: Fast to Slow Decimator Channel 3 0100010: Fast to Slow Decimator Channel 4 0100011: Fast to Slow Decimator Channel 5 0100100: Fast to Slow Decimator Channel 6 0100101: Fast to Slow Decimator Channel 7 0100110: Audio Output DMA 0 Channel 0 0100111: Audio Output DMA 0 Channel 1 0101000: Audio Output DMA 0 Channel 2	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Audio Output DMA 0 Channel 3 0101010: Audio Output DMA 0 Channel 4 0101011: Audio Output DMA 0 Channel 5 0101100: Audio Output DMA 0 Channel 6 0101101: Audio Output DMA 0 Channel 7 0101110: Audio Output DMA 1 Channel 0 0101111: Audio Output DMA 1 Channel 1 0110000: Audio Output DMA 1 Channel 2 0110001: Audio Output DMA 1 Channel 3 0110010: Audio Output DMA 1 Channel 4 0110011: Audio Output DMA 1 Channel 5 0110100: Audio Output DMA 1 Channel 6 0110101: Audio Output DMA 1 Channel 7 0110110: Audio Output DMA 2 Channel 0 0110111: Audio Output DMA 2 Channel 1 0111000: Audio Output DMA 2 Channel 2 0111001: Audio Output DMA 2 Channel 3 0111010: Audio Output DMA 2 Channel 4 0111011: Audio Output DMA 2 Channel 5 0111100: Audio Output DMA 2 Channel 6 0111101: Audio Output DMA 2 Channel 7 0111110: Audio Bus Map Out 0 0111111: Audio Bus Map Out 1 1000000: Audio Bus Map Out 2 1000001: Audio Bus Map Out 3 1000010: Audio Bus Map Out 4 1000011: Audio Bus Map Out 5 1000100: Audio Bus Map Out 6 1000101: Audio Bus Map Out 7 1000110: Audio Bus Map Out 8 1000111: Audio Bus Map Out 9 1001000: Audio Bus Map Out 10 1001001: Audio Bus Map Out 11 1001010: Audio Bus Map Out 12 1001011: Audio Bus Map Out 13 1001100: Audio Bus Map Out 14 1001101: Audio Bus Map Out 15		

FASTDSP RUN REGISTER

Address: 0xF00001B8, Reset: 0x00000000, Name: FDSP_RUN

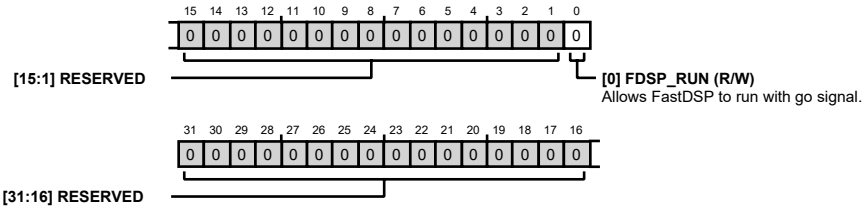


Table 149. Bit Descriptions for FDSP_RUN

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	FDSP_RUN	Allows FastDSP to run with go signal. 0: FastDSP has no go signal. Not running but memories can be loaded if FDSP_EN = 1. 1: FastDSP has a go signal and is running.	0x0	R/W

FASTDSP CORE CLOCK SPEED CONTROL REGISTER

Address: 0xF00001BC, Reset: 0x00000001, Name: FDSP_SPEED

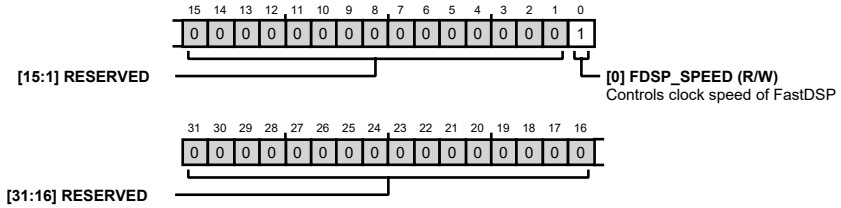


Table 150. Bit Descriptions for FDSP_SPEED

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	FDSP_SPEED	Controls clock speed of FastDSP. 0: 24.576MHz core speed (0.9V or 1.1V DVDD): 64 instructions max at 384kHz. 1: 49.152MHz core speed (1.1V DVDD only): 128 instructions max at 384kHz.	0x1	R/W

FASTDSP CURRENT BANK AND BANK RAMPING CONTROLS REGISTER

Address: 0xF00001C0, Reset: 0x00000070, Name: FDSP_CTRL1

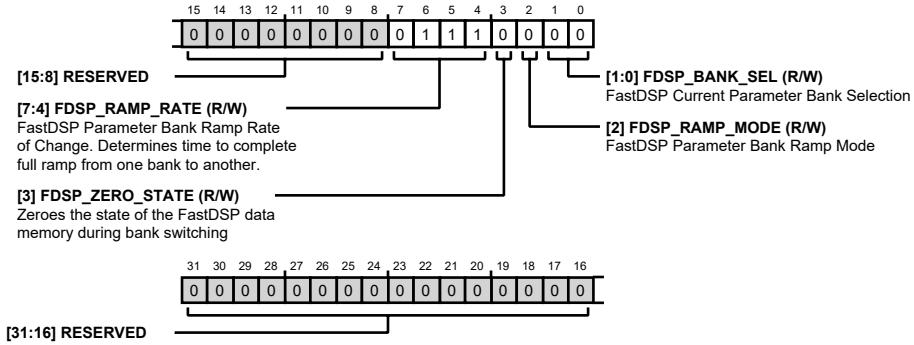


Table 151. Bit Descriptions for FDSP_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:4]	FDSP_RAMP_RATE	FastDSP Parameter Bank Ramp Rate of Change. Determines time to complete full ramp from one bank to another. The rates are shown for 384kHz sample rate. To calculate the ramp time for other sample rates, multiply the values in the table by the ratio (384/sample rate in kHz). 0000: 0.02 sec Ramp 0001: 0.04 sec Ramp 0010: 0.06 sec Ramp 0011: 0.08 sec Ramp 0100: 0.1 sec Ramp 0101: 0.15 sec Ramp 0110: 0.2 sec Ramp 0111: 0.25 sec Ramp 1000: 0.3 sec Ramp 1001: 0.5 sec Ramp 1010: 0.75 sec Ramp 1011: 1 sec Ramp 1100: 1.25 sec Ramp 1101: 1.5 sec Ramp 1110: 1.75 sec Ramp 1111: 2 sec Ramp	0x7	R/W
3	FDSP_ZERO_STATE	Zeroes the state of the FastDSP data memory during bank switching. When switching active parameter banks between two settings, zeroing the state of the bank prevents the new filter settings from being active on old data that is recirculating in filters. Zeroing the state may prevent filter instability or unwanted noises upon bank switching. 0: Do not zero state during bank switch. 1: Zero state during back switch.	0x0	R/W
2	FDSP_RAMP_MODE	FastDSP Parameter Bank Ramp Mode 0: Parameters linearly ramp when the current bank is changed. 1: Parameters instantly change when the current bank is changed.	0x0	R/W
[1:0]	FDSP_BANK_SEL	FastDSP Current Parameter Bank Selection 00: FastDSP uses Parameter Bank A 01: FastDSP uses Parameter Bank B 10: FastDSP uses Parameter Bank C	0x0	R/W

FASTDSP BANK RAMPING STOP POINT REGISTER

Address: 0xF00001C4, Reset: 0x0000003F, Name: FDSP_CTRL2

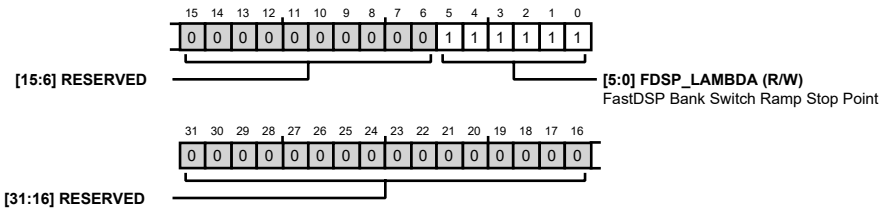


Table 152. Bit Descriptions for FDSP_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
[5:0]	FDSP_LAMBDA	FastDSP Bank Switch Ramp Stop Point. Lambda is a 6-bit value representing the point along the linear interpolation curve between two banks at which the bank ramp switch stops. Where A represents coefficient values in the source bank and B represents coefficient values in the destination bank: 0 = ((63/64) x A + (1/64) x B), 1 = ((62/64) x A + (2/64) x B), …, 62 = ((1/64) x A + (63/64) x B), 63 = B (default) Lambda can be updated "on the fly" via control interface. To complete a bank switch a value of 63 (default setting) must be set. The actual current ramp point (current_lambda: 0-63) can be read via a status register. When this reaches 63, the bank switch is complete, and the current parameters used match the current bank. The actual step size of linear interpolation will be ~12-bits (4096 steps). Parameters in banks that are being ramped between should not change during a bank switch. 000000: Bank switch parameter ramp stops at 1/64 of the full ramp. 000001: Bank switch parameter ramp stops at 2/64 of the full ramp. 111110: Bank switch parameter ramp stops at 63/64 of the full ramp. 111111: Bank switch parameter ramp completes ramp to the current bank.	0x3F	R/W

FASTDSP BANK COPYING REGISTER

Address: 0xF00001C8, Reset: 0x00000000, Name: FDSP_CTRL3

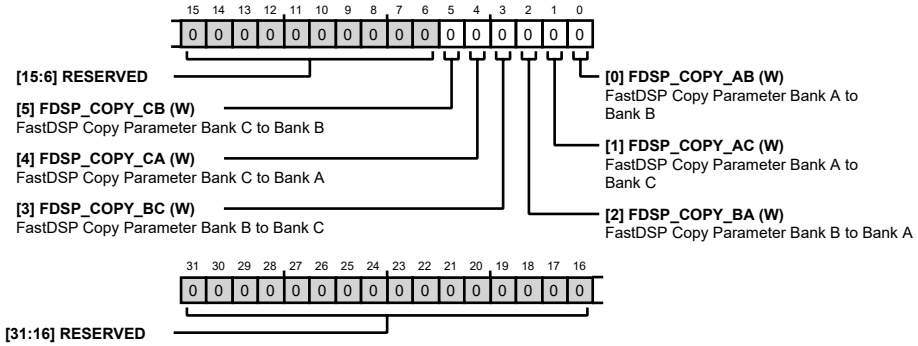


Table 153. Bit Descriptions for FDSP_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
5	FDSP_COPY_CB	FastDSP Copy Parameter Bank C to Bank B 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W
4	FDSP_COPY_CA	FastDSP Copy Parameter Bank C to Bank A 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W
3	FDSP_COPY_BC	FastDSP Copy Parameter Bank B to Bank C 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W

Bits	Bit Name	Description	Reset	Access
2	FDSP_COPY_BA	FastDSP Copy Parameter Bank B to Bank A 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W
1	FDSP_COPY_AC	FastDSP Copy Parameter Bank A to Bank C 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W
0	FDSP_COPY_AB	FastDSP Copy Parameter Bank A to Bank B 0: Normal operation. 1: Writing of 1 copies bank.	0x0	W

FASTDSP FRAME RATE SOURCE REGISTER

Address: 0xF00001CC, Reset: 0x00000000, Name: FDSP_CTRL4

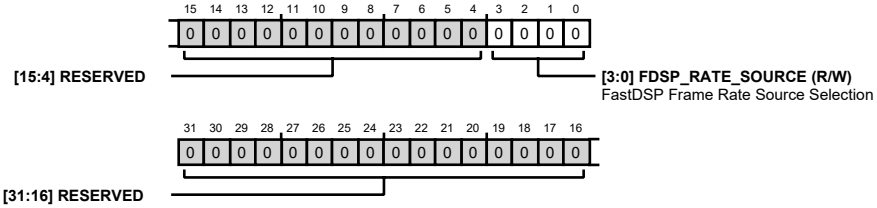


Table 154. Bit Descriptions for FDSP_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved	0x0	R
[3:0]	FDSP_RATE_SOURCE	FastDSP Frame Rate Source Selection 0000: ADC Channel 0 and Channel 1 0001: ADC Channel 2 0010: Digital Microphone Channel 0 and Channel 1 0011: Digital Microphone Channel 2 and Channel 3 0100: Digital Microphone Channel 4 and Channel 5 0101: Digital Microphone Channel 6 and Channel 7 0110: Digital Microphone Channel 8 and Channel 9 0111: Serial Audio Interface 0 1000: Serial Audio Interface 1 1001: Interpolator Channel 0 and Channel 1 1010: Interpolator Channel 2 and Channel 3 1011: Interpolator Channel 4 and Channel 5 1100: Interpolator Channel 6 and Channel 7 1101: Input Asynchronous Sample Rate Converter 0 1110: Input Asynchronous Sample Rate Converter 1 1111: Fixed	0x0	R/W

FASTDSP FIXED RATE DIVISION REGISTER

Address: 0xF00001D0, Reset: 0x0000007F, Name: FDSP_CTRL5

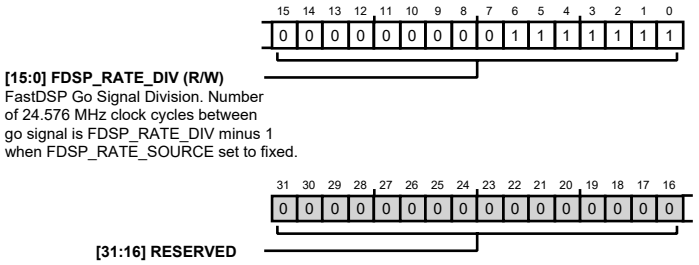


Table 155. Bit Descriptions for FDSP_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	FDSP_RATE_DIV	FastDSP Go Signal Division. Number of 24.576MHz clock cycles between go signal is FDSP_RATE_DIV minus 1 when FDSP_RATE_SOURCE is set to fixed.	0x7F	R/W

FASTDSP MODULO N COUNTER FOR LOWER RATE CONDITIONAL EXECUTION REGISTER

Address: 0xF00001D4, Reset: 0x00000000, Name: FDSP_CTRL6

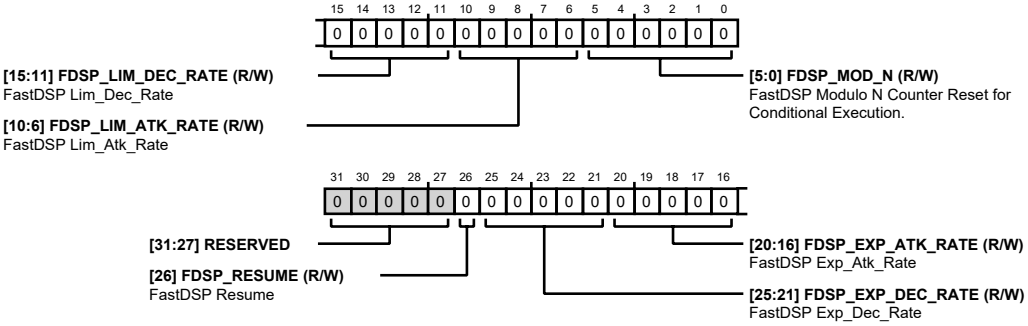


Table 156. Bit Descriptions for FDSP_CTRL6

Bits	Bit Name	Description	Reset	Access
[31:27]	RESERVED	Reserved	0x0	R
26	FDSP_RESUME	FastDSP Resume 0: Normal operation. 1: Resume FDSP operation from pause state.	0x0	R/W
[25:21]	FDSP_EXP_DEC_RATE	FastDSP Exp_Dec_Rate 0: Decay rate as specified. 1: Decay rate slowed by a factor of 2. 31: Decay rate slowed by a factor of 32.	0x0	R/W
[20:16]	FDSP_EXP_ATK_RATE	FastDSP Exp_Atk_Rate 0: Attack rate as specified. 1: Attack rate slowed by a factor of 2. 31: Attack rate slowed by a factor of 32.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[15:11]	FDSP_LIM_DEC_RATE	FastDSP Lim_Dec_Rate 0: Decay rate as specified. 1: Decay rate slowed by a factor of 2. 31: Decay rate slowed by a factor of 32.	0x0	R/W
[10:6]	FDSP_LIM_ATK_RATE	FastDSP Lim_Atk_Rate 0: Attack rate as specified. 1: Attack rate slowed by a factor of 2. 31: Attack rate slowed by a factor of 32.	0x0	R/W
[5:0]	FDSP_MOD_N	FastDSP Modulo N Counter Reset for Conditional Execution 000000: Normal operation. 000001: Modulo 2 operation on M execution condition. 111111: Modulo 64 operation on M execution condition.	0x0	R/W

FASTDSP GENERIC CONDITIONAL EXECUTION REGISTERS

Address: 0xF00001D8, Reset: 0x00000000, Name: FDSP_CTRL7

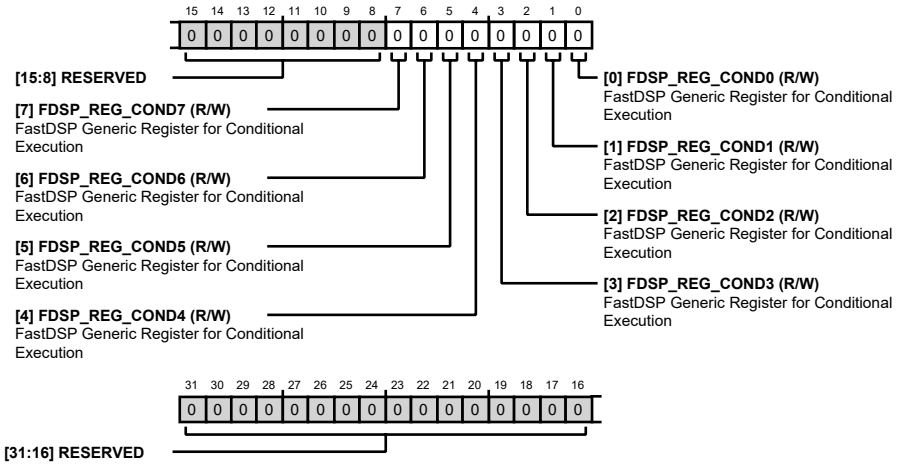


Table 157. Bit Descriptions for FDSP_CTRL7

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	FDSP_REG_COND7	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
6	FDSP_REG_COND6	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
5	FDSP_REG_COND5	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
4	FDSP_REG_COND4	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
3	FDSP_REG_COND3	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
2	FDSP_REG_COND2	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
1	FDSP_REG_COND1	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W
0	FDSP_REG_COND0	FastDSP Generic Register for Conditional Execution. The value of this register can be used for conditional instruction execution in the FastDSP. 0: Conditional register is 0. 1: Conditional register is 1.	0x0	R/W

FAST DSP SAFELOAD ADDRESS REGISTER

Address: 0xF00001DC, Reset: 0x00000000, Name: FDSP_SL_ADDR

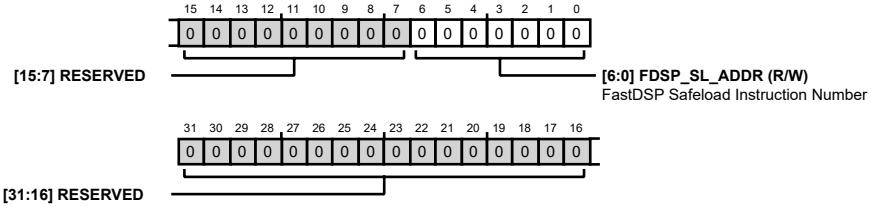


Table 158. Bit Descriptions for FDSP_SL_ADDR

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	FDSP_SL_ADDR	FastDSP Safeload Instruction Number	0x0	R/W

FASTDSP SAFELOAD PARAMETER 0 VALUE REGISTER

Address: 0xF00001E0, Reset: 0x00000000, Name: FDSP_SL_P0

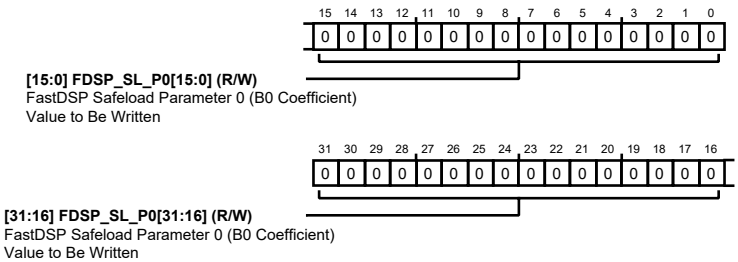


Table 159. Bit Descriptions for FDSP_SL_P0

Bits	Bit Name	Description	Reset	Access
[31:0]	FDSP_SL_P0	FastDSP Safeload Parameter 0 (B0 Coefficient) Value to be Written	0x0	R/W

FASTDSP SAFELOAD PARAMETER 1 VALUE REGISTER

Address: 0xF00001E4, Reset: 0x00000000, Name: FDSP_SL_P1

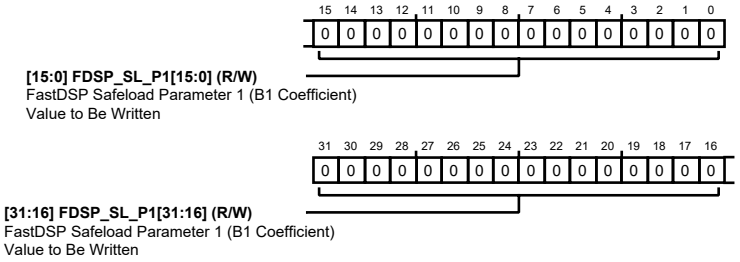


Table 160. Bit Descriptions for FDSP_SL_P1

Bits	Bit Name	Description	Reset	Access
[31:0]	FDSP_SL_P1	FastDSP Safeload Parameter 1 (B1 Coefficient) Value to be Written	0x0	R/W

FASTDSP SAFELOAD PARAMETER 2 VALUE REGISTER

Address: 0xF00001E8, Reset: 0x00000000, Name: FDSP_SL_P2

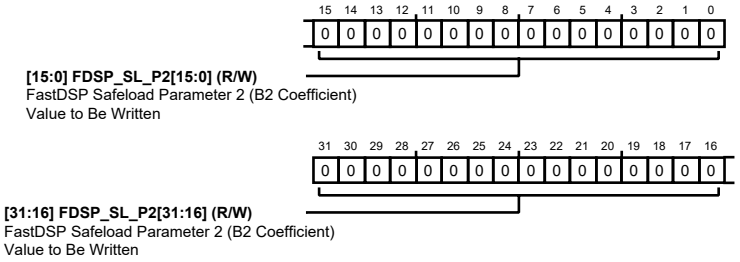


Table 161. Bit Descriptions for FDSP_SL_P2

Bits	Bit Name	Description	Reset	Access
[31:0]	FDSP_SL_P2	FastDSP Safeload Parameter 2 (B2 Coefficient) Value to be Written	0x0	R/W

FASTDSP SAFELOAD PARAMETER 3 VALUE REGISTER

Address: 0xF00001EC, Reset: 0x00000000, Name: FDSP_SL_P3

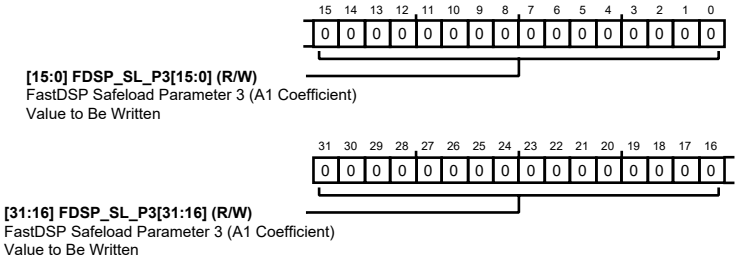


Table 162. Bit Descriptions for FDSP_SL_P3

Bits	Bit Name	Description	Reset	Access
[31:0]	FDSP_SL_P3	FastDSP Safeload Parameter 3 (A1 Coefficient) Value to be Written	0x0	R/W

FASTDSP SAFELOAD PARAMETER 4 VALUE REGISTER

Address: 0xF00001F0, Reset: 0x00000000, Name: FDSP_SL_P4

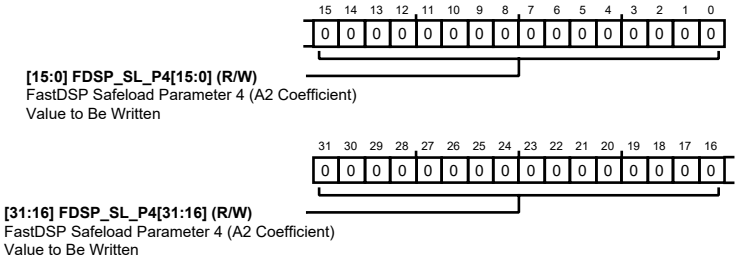


Table 163. Bit Descriptions for FDSP_SL_P4

Bits	Bit Name	Description	Reset	Access
[31:0]	FDSP_SL_P4	FastDSP Safeload Parameter 4 (A2 Coefficient) Value to be Written	0x0	R/W

FASTDSP SAFELOAD UPDATE REGISTER

Address: 0xF00001F4, Reset: 0x00000000, Name: FDSP_SL_UPDATE

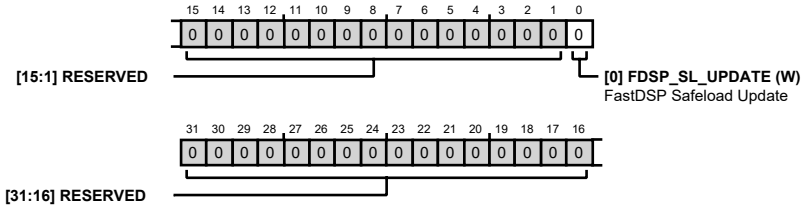


Table 164. Bit Descriptions for FDSP_SL_UPDATE

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	FDSP_SL_UPDATE	FastDSP Safeload Update. Writing a 1 to this register writes the parameter values in the FDSP_SL_Px registers to the addresses in the current bank associated with the instruction number in the FDSP_SL_ADDR register at the beginning of the next frame. 0: No action. 1: Writing of 1 causes an update of safeload parameters at the beginning of the next frame.	0x0	W

HIFI RUN REGISTER

Address: 0xF00001F8, Reset: 0x00000000, Name: HIFI_CTRL1

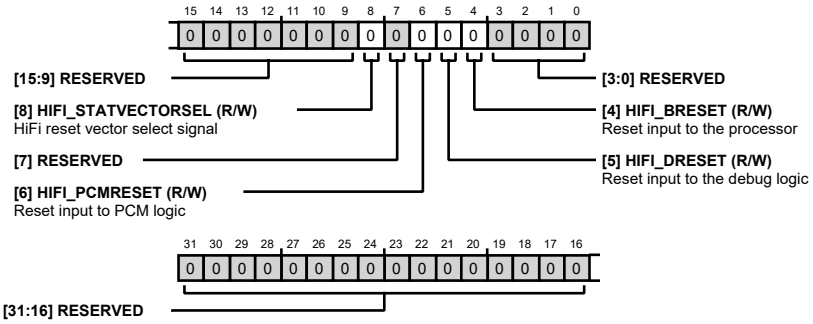


Table 165. Bit Descriptions for HIFI_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	HIFI_STATVECTORSEL	HiFi Reset Vector Select Signal 1: Alternate reset vector. 0: Default reset vector.	0x0	R/W
7	RESERVED	Reserved	0x0	R
6	HIFI_PCMRESET	Reset Input to PCM Logic 0: Normal operation. 1: Reset power control module.	0x0	R/W
5	HIFI_DRESET	Reset Input to the Debug Logic 0: HiFi DReset disabled. 1: HiFi DReset active.	0x0	R/W
4	HIFI_BRESET	Reset Input to the Processor 0: HiFi BReset disabled. 1: HiFi BReset active.	0x0	R/W
[3:0]	RESERVED	Reserved	0x0	R

HIFI SPEED REGISTER

Address: 0xF00001FC, Reset: 0x00000001, Name: HIFI_CTRL2

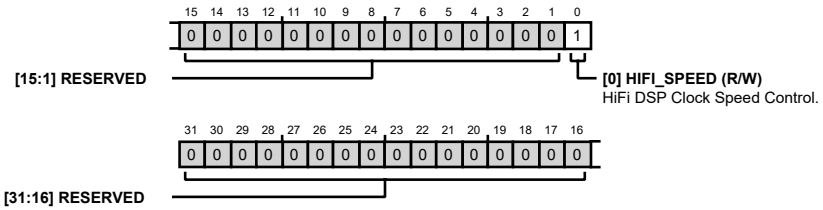


Table 166. Bit Descriptions for HIFI_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	HIFI_SPEED	HiFi DSP Clock Speed Control 0: HiFi DSP low speed, low voltage operation using 49.152MHz core clock. 1: HiFi DSP high speed, high voltage operation using 196.608MHz core clock.	0x1	R/W

HIFI AUDIO INTERRUPTS SOURCE SELECTION 1 REGISTER

Address: 0xF0000200, Reset: 0x00000000, Name: HIFI_INT_CTRL0

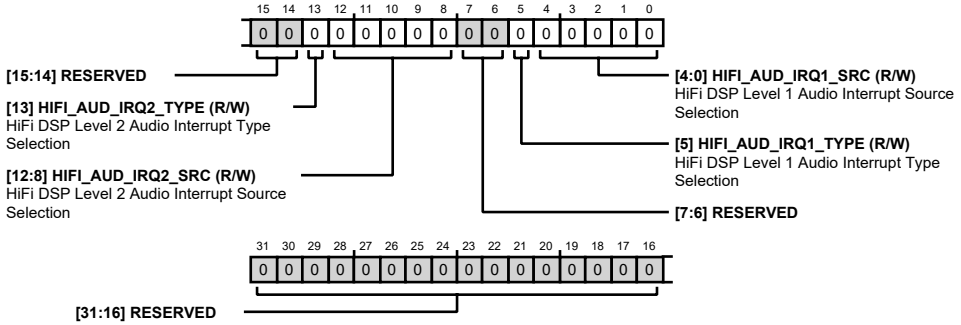


Table 167. Bit Descriptions for HIFI_INT_CTRL0

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved	0x0	R
13	HIFI_AUD_IRQ2_TYPE	HiFi DSP Level 2 Audio Interrupt Type Selection 0: Interrupt will occur every sample. 1: Interrupt will occur every HIFI_AUD_IRQx_CNTR samples.	0x0	R/W
[12:8]	HIFI_AUD_IRQ2_SRC	HiFi DSP Level 2 Audio Interrupt Source Selection 00000: No interrupt source. 00001: ADC0/1 as interrupt source. 00010: ADC2 as interrupt source. 00011: DMIC0/1 as interrupt source. 00100: DMIC2/3 as interrupt source. 00101: DMIC4/5 as interrupt source. 00110: DMIC6/7 as interrupt source. 00111: DMIC8/9 as interrupt source. 01000: SPT0 as interrupt source. 01001: SPT1 as interrupt source. 01010: ASRCI_0 as interrupt source. 01011: ASRCI_1 as interrupt source. 01100: FDSP as interrupt source. 01101: AIRQ1 counter as interrupt source. 01110: FDEC0/1 as interrupt source. 01111: FDEC2/3 as interrupt source. 10000: FDEC4/5 as interrupt source. 10001: FDEC6/7 as interrupt source. 10010: FINT0/1 as interrupt source. 10011: FINT2/3 as interrupt source. 10100: FINT4/5 as interrupt source. 10101: FINT6/7 as interrupt source.	0x0	R/W
[7:6]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
5	HIFI_AUD_IRQ1_TYPE	HiFi DSP Level 1 Audio Interrupt Type Selection 0: Interrupt will occur every sample. 1: Interrupt will occur every HIFI_AUD_IRQx_CNTR samples.	0x0	R/W
[4:0]	HIFI_AUD_IRQ1_SRC	HiFi DSP Level 1 Audio Interrupt Source Selection 00000: No interrupt source. 00001: ADC0/1 as interrupt source. 00010: ADC2 as interrupt source. 00011: DMIC0/1 as interrupt source. 00100: DMIC2/3 as interrupt source. 00101: DMIC4/5 as interrupt source. 00110: DMIC6/7 as interrupt source. 00111: DMIC8/9 as interrupt source. 01000: SPT0 as interrupt source. 01001: SPT1 as interrupt source. 01010: ASRCI_0 as interrupt source. 01011: ASRCI_1 as interrupt source. 01100: FDSP as interrupt source. 01101: AIRQ1 counter as interrupt source. 01110: FDEC0/1 as interrupt source. 01111: FDEC2/3 as interrupt source. 10000: FDEC4/5 as interrupt source. 10001: FDEC6/7 as interrupt source. 10010: FINT0/1 as interrupt source. 10011: FINT2/3 as interrupt source. 10100: FINT4/5 as interrupt source. 10101: FINT6/7 as interrupt source.	0x0	R/W

HIFI AUDIO INTERRUPTS SOURCE SELECTION 2 REGISTER

Address: 0xF0000204, Reset: 0x00000000, Name: HIFI_INT_CTRL1

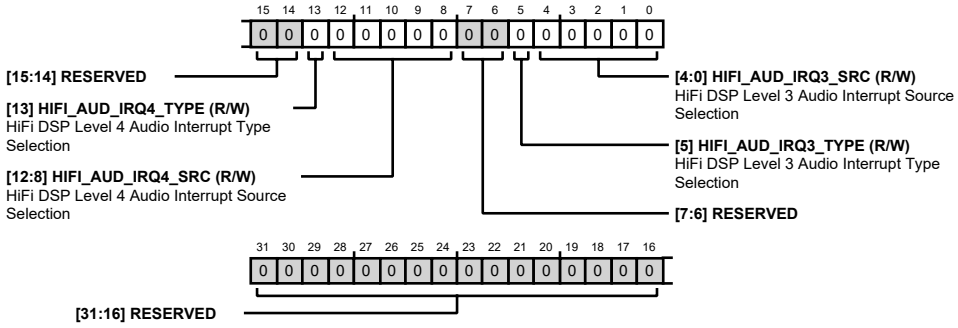


Table 168. Bit Descriptions for HIFI_INT_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:14]	RESERVED	Reserved	0x0	R
13	HIFI_AUD_IRQ4_TYPE	HiFi DSP Level 4 Audio Interrupt Type Selection 0: Interrupt will occur every sample. 1: Interrupt will occur every HIFI_AUD_IRQx_CNTR samples.	0x0	R/W
[12:8]	HIFI_AUD_IRQ4_SRC	HiFi DSP Level 4 Audio Interrupt Source Selection 00000: No interrupt source. 00001: ADC0/1 as interrupt source. 00010: ADC2 as interrupt source. 00011: DMIC0/1 as interrupt source. 00100: DMIC2/3 as interrupt source. 00101: DMIC4/5 as interrupt source. 00110: DMIC6/7 as interrupt source. 00111: DMIC8/9 as interrupt source. 01000: SPT0 as interrupt source. 01001: SPT1 as interrupt source. 01010: ASRCI_0 as interrupt source. 01011: ASRCI_1 as interrupt source. 01100: FDSP as interrupt source. 01101: AIRQ1 counter as interrupt source. 01110: FDEC0/1 as interrupt source. 01111: FDEC2/3 as interrupt source. 10000: FDEC4/5 as interrupt source. 10001: FDEC6/7 as interrupt source. 10010: FINT0/1 as interrupt source. 10011: FINT2/3 as interrupt source. 10100: FINT4/5 as interrupt source. 10101: FINT6/7 as interrupt source.	0x0	R/W
[7:6]	RESERVED	Reserved	0x0	R
5	HIFI_AUD_IRQ3_TYPE	HiFi DSP Level 3 Audio Interrupt Type Selection 0: Interrupt will occur every sample. 1: Interrupt will occur every HIFI_AUD_IRQx_CNTR samples.	0x0	R/W
[4:0]	HIFI_AUD_IRQ3_SRC	HiFi DSP Level 3 Audio Interrupt Source Selection 00000: No interrupt source. 00001: ADC0/1 as interrupt source. 00010: ADC2 as interrupt source. 00011: DMIC0/1 as interrupt source. 00100: DMIC2/3 as interrupt source. 00101: DMIC4/5 as interrupt source. 00110: DMIC6/7 as interrupt source. 00111: DMIC8/9 as interrupt source. 01000: SPT0 as interrupt source. 01001: SPT1 as interrupt source. 01010: ASRCI_0 as interrupt source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: ASRCI_1 as interrupt source. 01100: FDSP as interrupt source. 01101: AIRQ1 counter as interrupt source. 01110: FDEC0/1 as interrupt source. 01111: FDEC2/3 as interrupt source. 10000: FDEC4/5 as interrupt source. 10001: FDEC6/7 as interrupt source. 10010: FINT0/1 as interrupt source. 10011: FINT2/3 as interrupt source. 10100: FINT4/5 as interrupt source. 10101: FINT6/7 as interrupt source.		

HIFI AUDIO INTERRUPTS SOURCE SELECTION 3 REGISTER

Address: 0xF0000208, Reset: 0x00000000, Name: HIFI_INT_CTRL2

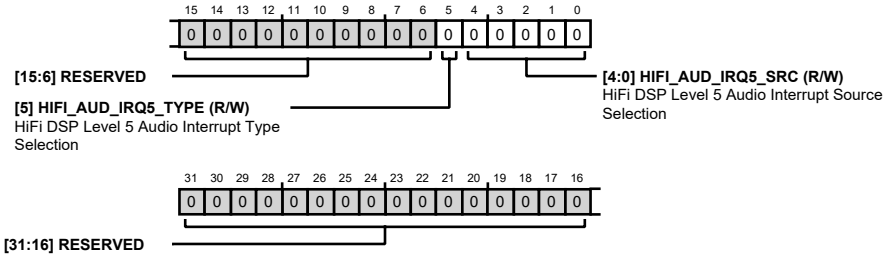


Table 169. Bit Descriptions for HIFI_INT_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
5	HIFI_AUD_IRQ5_TYPE	HiFi DSP Level 5 Audio Interrupt Type Selection 0: Interrupt will occur every sample. 1: Interrupt will occur every HIFI_AUD_IRQx_CNTR samples.	0x0	R/W
[4:0]	HIFI_AUD_IRQ5_SRC	HiFi DSP Level 5 Audio Interrupt Source Selection 00000: No interrupt source. 00001: ADC0/1 as interrupt source. 00010: ADC2 as interrupt source. 00011: DMIC0/1 as interrupt source. 00100: DMIC2/3 as interrupt source. 00101: DMIC4/5 as interrupt source. 00110: DMIC6/7 as interrupt source. 00111: DMIC8/9 as interrupt source. 01000: SPT0 as interrupt source. 01001: SPT1 as interrupt source. 01010: ASRCI_0 as interrupt source. 01011: ASRCI_1 as interrupt source. 01100: FDSP as interrupt source. 01101: AIRQ1 counter as interrupt source. 01110: FDEC0/1 as interrupt source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01111: FDEC2/3 as interrupt source. 10000: FDEC4/5 as interrupt source. 10001: FDEC6/7 as interrupt source. 10010: FINT0/1 as interrupt source. 10011: FINT2/3 as interrupt source. 10100: FINT4/5 as interrupt source. 10101: FINT6/7 as interrupt source.		

HIFI AUDIO INTERRUPT COUNTERS 1 REGISTER

Address: 0xF0000210, Reset: 0x00000000, Name: HIFI_INT_CTRL3

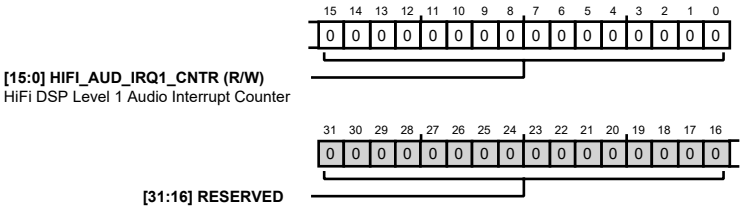


Table 170. Bit Descriptions for HIFI_INT_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	HIFI_AUD_IRQ1_CNTR	HiFi DSP Level 1 Audio Interrupt Counter	0x0	R/W

HIFI AUDIO INTERRUPT COUNTERS 2 REGISTER

Address: 0xF0000218, Reset: 0x00000000, Name: HIFI_INT_CTRL4

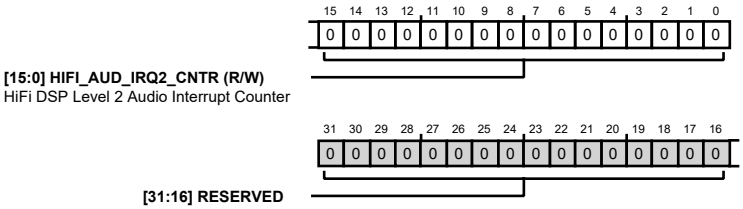


Table 171. Bit Descriptions for HIFI_INT_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	HIFI_AUD_IRQ2_CNTR	HiFi DSP Level 2 Audio Interrupt Counter	0x0	R/W

HIFI AUDIO INTERRUPT COUNTERS 3 REGISTER

Address: 0xF0000220, Reset: 0x00000000, Name: HIFI_INT_CTRL5

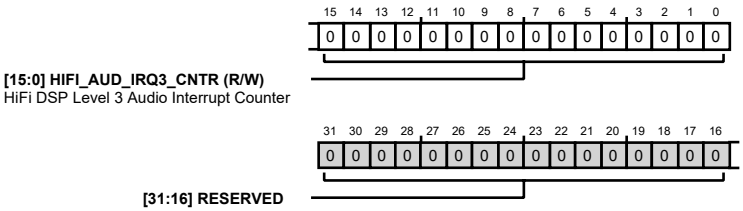


Table 172. Bit Descriptions for HIFI_INT_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	HIFI_AUD_IRQ3_CNTR	HiFi DSP Level 3 Audio Interrupt Counter	0x0	R/W

HIFI AUDIO INTERRUPT COUNTERS 4 REGISTER

Address: 0xF0000228, Reset: 0x00000000, Name: HIFI_INT_CTRL6

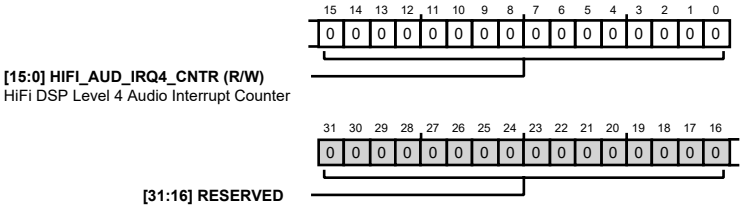


Table 173. Bit Descriptions for HIFI_INT_CTRL6

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	HIFI_AUD_IRQ4_CNTR	HiFi DSP Level 4 Audio Interrupt Counter	0x0	R/W

HIFI AUDIO INTERRUPT COUNTERS 5 REGISTER

Address: 0xF0000230, Reset: 0x00000000, Name: HIFI_INT_CTRL7

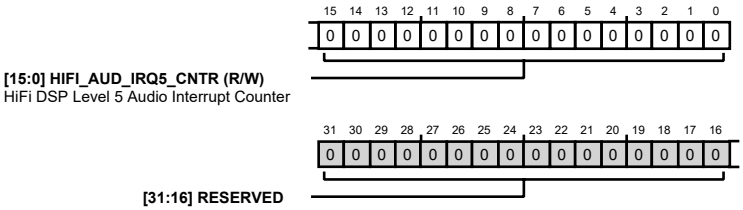


Table 174. Bit Descriptions for HIFI_INT_CTRL7

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	HIFI_AUD_IRQ5_CNTR	HiFi DSP Level 5 Audio Interrupt Counter	0x0	R/W

HIFI MP GPI EDGE SENSITIVE INTERRUPTS SOURCE SELECTION 1 REGISTER

Address: 0xF0000234, Reset: 0x00000000, Name: HIFI_INT_CTRL8

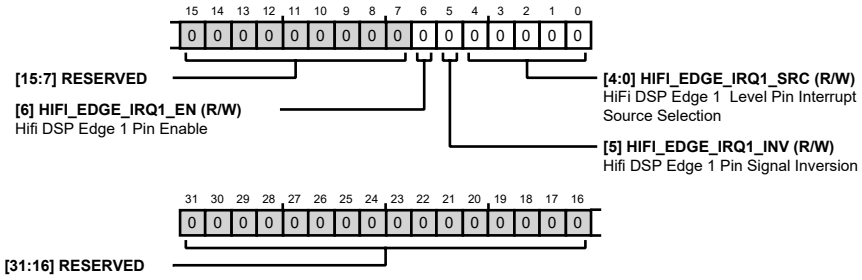


Table 175. Bit Descriptions for HIFI_INT_CTRL8

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_EDGE_IRQ1_EN	HiFi DSP Edge 1 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_EDGE_IRQ1_INV	HiFi DSP Edge 1 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_EDGE_IRQ1_SRC	HiFi DSP Edge 1 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source. 00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source. 01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source. 11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.	0x0	R/W

HIFI MP GPI EDGE SENSITIVE INTERRUPTS SOURCE SELECTION 2 REGISTER

Address: 0xF0000238, Reset: 0x00000000, Name: HIFI_INT_CTRL9

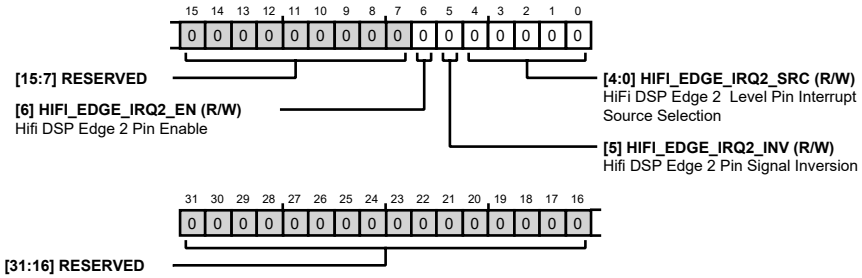


Table 176. Bit Descriptions for HIFI_INT_CTRL9

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_EDGE_IRQ2_EN	HiFi DSP Edge 2 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_EDGE_IRQ2_INV	HiFi DSP Edge 2 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_EDGE_IRQ2_SRC	HiFi DSP Edge 2 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source. 00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source. 01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.		

HIFI MP GPI EDGE SENSITIVE INTERRUPTS SOURCE SELECTION 3 REGISTER

Address: 0xF000023C, Reset: 0x00000000, Name: HIFI_INT_CTRL10

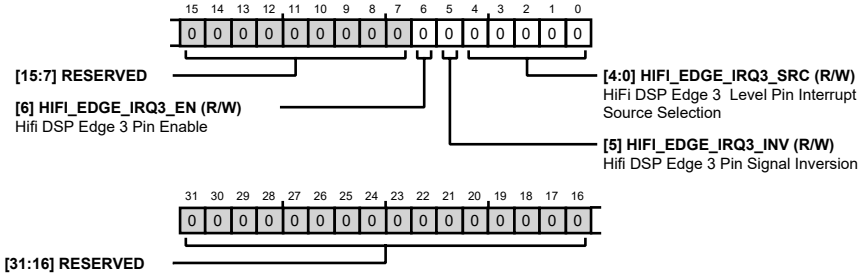


Table 177. Bit Descriptions for HIFI_INT_CTRL10

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_EDGE_IRQ3_EN	HiFi DSP Edge 3 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_EDGE_IRQ3_INV	HiFi DSP Edge 3 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_EDGE_IRQ3_SRC	HiFi DSP Edge 3 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source. 00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source. 11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.		

HIFI MP GPI LEVEL SENSITIVE INTERRUPTS SOURCE SELECTION 1 REGISTER

Address: 0xF0000248, Reset: 0x00000000, Name: HIFI_INT_CTRL11

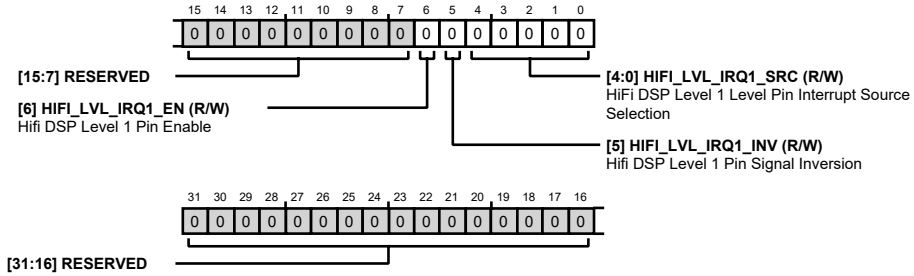


Table 178. Bit Descriptions for HIFI_INT_CTRL11

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_LVL_IRQ1_EN	HiFi DSP Level 1 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_LVL_IRQ1_INV	HiFi DSP Level 1 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_LVL_IRQ1_SRC	HiFi DSP Level 1 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source. 01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source. 11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.		

HIFI MP GPI LEVEL SENSITIVE INTERRUPTS SOURCE SELECTION 2 REGISTER

Address: 0xF000024C, Reset: 0x00000000, Name: HIFI_INT_CTRL12

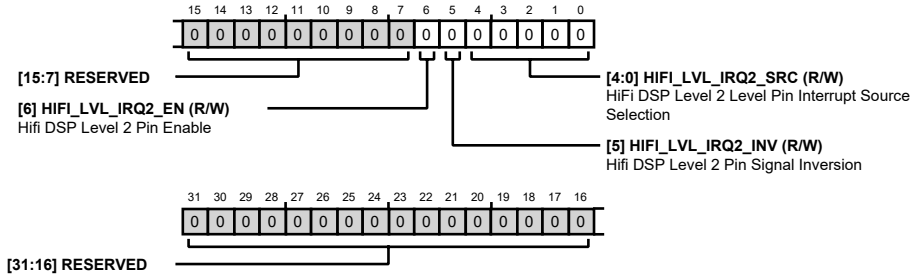


Table 179. Bit Descriptions for HIFI_INT_CTRL12

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_LVL_IRQ2_EN	HiFi DSP Level 2 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_LVL_IRQ2_INV	HiFi DSP Level 2 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_LVL_IRQ2_SRC	HiFi DSP Level 2 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source. 00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source. 01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source. 11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.	0x0	R/W

HIFI MP GPI LEVEL SENSITIVE INTERRUPTS SOURCE SELECTION 3 REGISTER

Address: 0xF0000250, Reset: 0x00000000, Name: HIFI_INT_CTRL13

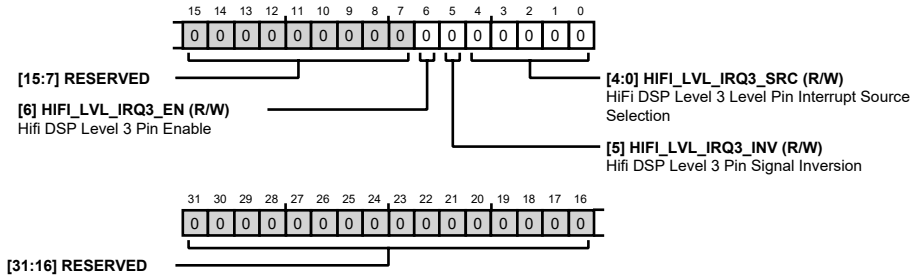


Table 180. Bit Descriptions for HIFI_INT_CTRL13

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	HIFI_LVL_IRQ3_EN	HiFi DSP Level 3 Pin Enable 0: Pin IRQ disabled. 1: Pin IRQ enabled.	0x0	R/W
5	HIFI_LVL_IRQ3_INV	HiFi DSP Level 3 Pin Signal Inversion 0: Pin signal passed to core. 1: Pin signal inverted to core.	0x0	R/W
[4:0]	HIFI_LVL_IRQ3_SRC	HiFi DSP Level 3 Level Pin Interrupt Source Selection 00000: MP0/SDATAO_0 as interrupt pin source. 00001: MP1/SDATAI_0 as interrupt pin source. 00010: MP2/BCLK_0 as interrupt pin source. 00011: MP3/FSYNC_0 as interrupt pin source. 00100: MP4/SDATAO_1 as interrupt pin source. 00101: MP5/SDATAI_1 as interrupt pin source. 00110: MP6/BCLK_1 as interrupt pin source. 00111: MP7/FSYNC_1 as interrupt pin source. 01000: MP8/DMIC01 as interrupt pin source. 01001: MP9/DMIC23 as interrupt pin source. 01010: MP10/DMIC45 as interrupt pin source. 01011: MP11/DMIC67 as interrupt pin source. 01100: MP12/DMIC89 as interrupt pin source. 01101: MP13/DMIC_CLK0 as interrupt pin source. 01110: MP14/DMIC_CLK1 as interrupt pin source. 01111: MP15/QSPIM_CLK as interrupt pin source. 10000: MP16/QSPIM_CS0 as interrupt pin source. 10001: MP17/QSPIM_CS1 as interrupt pin source. 10010: MP18/QSPIM_SDIO0 as interrupt pin source. 10011: MP19/QSPIM_SDIO1 as interrupt pin source. 10100: MP20/QSPIM_SDIO2 as interrupt pin source. 10101: MP21/QSPIM_SDIO3 as interrupt pin source. 10110: MP22/JTAG_TRST as interrupt pin source. 10111: MP23/JTAG_TMS as interrupt pin source. 11000: MP24/JTAG_TCK as interrupt pin source.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		11001: MP25/JTAG_TDI as interrupt pin source. 11010: MP26/JTAG_TDO as interrupt pin source. 11011: MP27/UART_TX as interrupt pin source. 11100: MP28/UART_RX as interrupt pin source. 11101: MP29/UART_RTS as interrupt pin source. 11110: MP30/UART_CTS as interrupt pin source. 11111: MP31/SELFBOOT as interrupt pin source.		

HIFI GENERIC SYSTEM INTERRUPT SOURCES FOR PIN SIGNALLING REGISTER

Address: 0xF0000254, Reset: 0x00000000, Name: HIFI_INT_CTRL14

These interrupts are sources to the nine system interrupt controllers. Their main use is to be able to have a core source for system IRQ outputs on multi-purpose pins

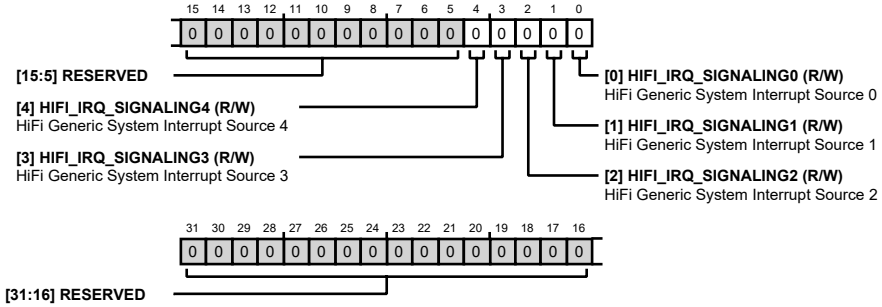


Table 181. Bit Descriptions for HIFI_INT_CTRL14

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	HIFI_IRQ_SIGNALING4	HiFi Generic System Interrupt Source 4 0: No action. 1: Signal generic HiFi system interrupt.	0x0	R/W
3	HIFI_IRQ_SIGNALING3	HiFi Generic System Interrupt Source 3. 0: No action. 1: Signal generic HiFi system interrupt.	0x0	R/W
2	HIFI_IRQ_SIGNALING2	HiFi Generic System Interrupt Source 2. 0: No action. 1: Signal generic HiFi system interrupt.	0x0	R/W
1	HIFI_IRQ_SIGNALING1	HiFi Generic System Interrupt Source 1. 0: No action. 1: Signal generic HiFi system interrupt.	0x0	R/W
0	HIFI_IRQ_SIGNALING0	HiFi Generic System Interrupt Source 0. 0: No action. 1: Signal generic HiFi system interrupt.	0x0	R/W

MULTIPURPOSE PINS 0/1/2/3 MODE SELECT REGISTER

Address: 0xF0000258, Reset: 0x00000000, Name: MP_CTRL1

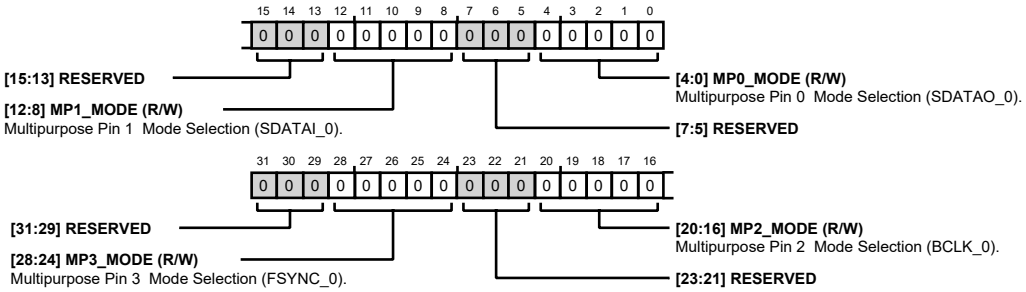


Table 182. Bit Descriptions for MP_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP3_MODE	Multipurpose Pin 3 Mode Selection (FSYNC_0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP2_MODE	Multipurpose Pin 2 Mode Selection (BCLK_0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP1_MODE	Multipurpose Pin 1 Mode Selection (SDATAI_0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP0_MODE	Multipurpose Pin 0 Mode Selection (SDATAO_0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PINS 4/5/6/7 MODE SELECT REGISTER

Address: 0xF000025C, Reset: 0x00000000, Name: MP_CTRL2

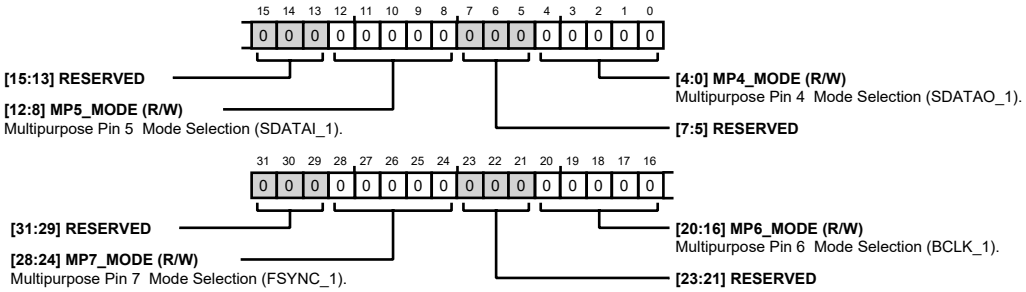


Table 183. Bit Descriptions for MP_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP7_MODE	Multipurpose Pin 7 Mode Selection (FSYNC_1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP6_MODE	Multipurpose Pin 6 Mode Selection (BCLK_1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP5_MODE	Multipurpose Pin 5 Mode Selection (SDATAI_1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP4_MODE	Multipurpose Pin 4 Mode Selection (SDATAO_1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PINS 8/9/10/11 MODE SELECT REGISTER

Address: 0xF0000260, Reset: 0x00000000, Name: MP_CTRL3

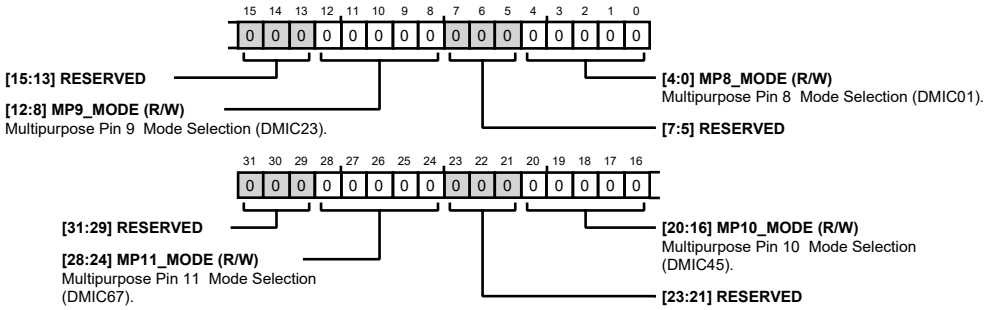


Table 184. Bit Descriptions for MP_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP11_MODE	Multipurpose Pin 11 Mode Selection (DMIC67) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP10_MODE	Multipurpose Pin 10 Mode Selection (DMIC45) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP9_MODE	Multipurpose Pin 9 Mode Selection (DMIC23) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP8_MODE	Multipurpose Pin 8 Mode Selection (DMIC01) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PINS 12/13/14/15 MODE SELECT REGISTER

Address: 0xF0000264, Reset: 0x00000000, Name: MP_CTRL4

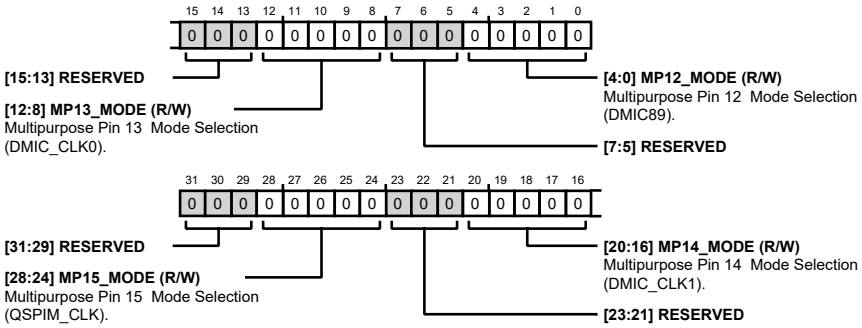


Table 185. Bit Descriptions for MP_CTRL4

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP15_MODE	Multipurpose Pin 15 Mode Selection (QSPIM_CLK) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP14_MODE	Multipurpose Pin 14 Mode Selection (DMIC_CLK1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP13_MODE	Multipurpose Pin 13 Mode Selection (DMIC_CLK0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP12_MODE	Multipurpose Pin 12 Mode Selection (DMIC89) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PINS 16/1718/19 MODE SELECT REGISTER

Address: 0xF0000268, Reset: 0x00000000, Name: MP_CTRL5

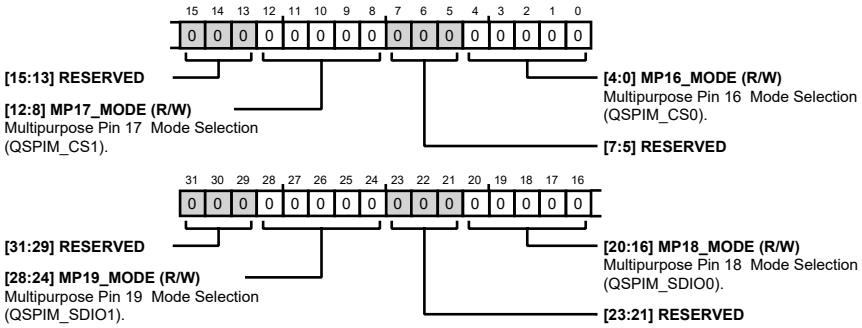


Table 186. Bit Descriptions for MP_CTRL5

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP19_MODE	Multipurpose Pin 19 Mode Selection (QSPIM_SDIO1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP18_MODE	Multipurpose Pin 18 Mode Selection (QSPIM_SDIO0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP17_MODE	Multipurpose Pin 17 Mode Selection (QSPIM_CS1) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP16_MODE	Multipurpose Pin 16 Mode Selection (QSPIM_CS0) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PIN 20/21/22/23 MODE SELECT REGISTER

Address: 0xF000026C, Reset: 0x00000000, Name: MP_CTRL6

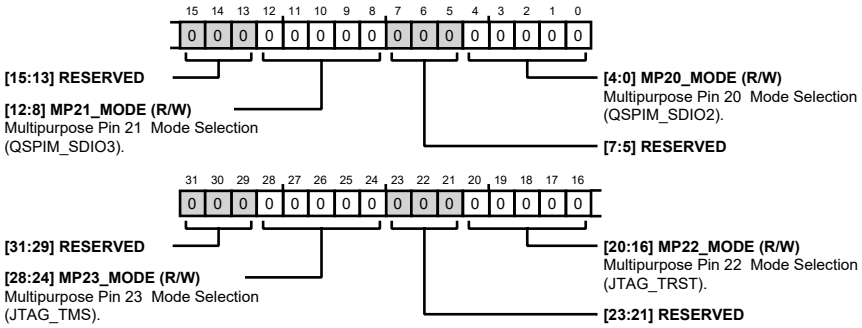


Table 187. Bit Descriptions for MP_CTRL6

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP23_MODE	Multipurpose Pin 23 Mode Selection (JTAG_TMS) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP22_MODE	Multipurpose Pin 22 Mode Selection (JTAG_TRST) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP21_MODE	Multipurpose Pin 21 Mode Selection (QSPIM_SDIO3) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP20_MODE	Multipurpose Pin 20 Mode Selection (QSPIM_SDIO2) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PIN 24/25/26/27 MODE SELECT REGISTER

Address: 0xF0000270, Reset: 0x00000000, Name: MP_CTRL7

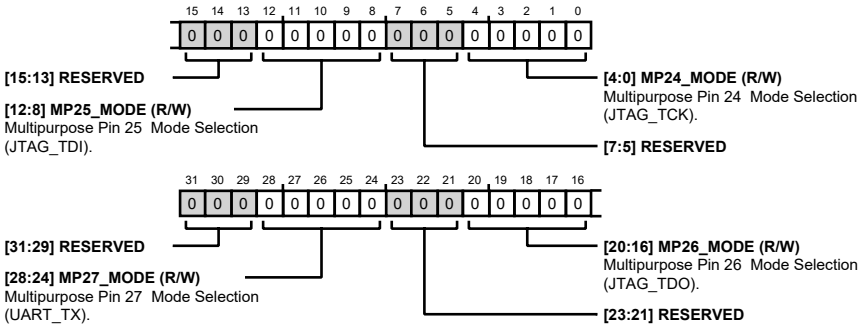


Table 188. Bit Descriptions for MP_CTRL7

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP27_MODE	Multipurpose Pin 27 Mode Selection (UART_TX) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP26_MODE	Multipurpose Pin 26 Mode Selection (JTAG_TDO) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP25_MODE	Multipurpose Pin 25 Mode Selection (JTAG_TDI) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP24_MODE	Multipurpose Pin 24 Mode Selection (JTAG_TCK) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

MULTIPURPOSE PIN 28/29/30/31 MODE SELECT REGISTER

Address: 0xF0000274, Reset: 0x14000000, Name: MP_CTRL8

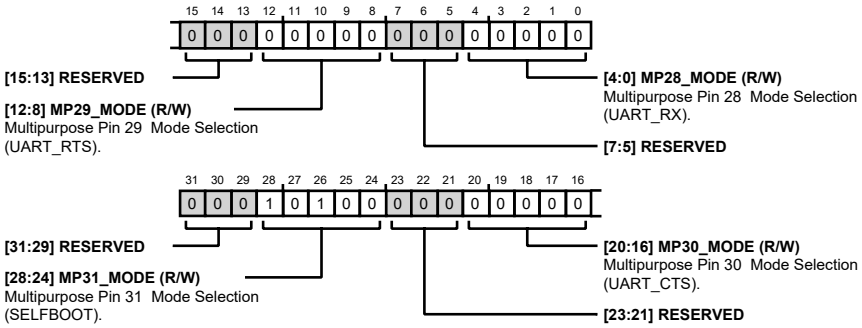


Table 189. Bit Descriptions for MP_CTRL8

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
[28:24]	MP31_MODE	Multipurpose Pin 31 Mode Selection (SELFBOOT) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x14	R/W
[23:21]	RESERVED	Reserved	0x0	R
[20:16]	MP30_MODE	Multipurpose Pin 30 Mode Selection (UART_CTS) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output		
[15:13]	RESERVED	Reserved	0x0	R
[12:8]	MP29_MODE	Multipurpose Pin 29 Mode Selection (UART_RTS) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W
[7:5]	RESERVED	Reserved	0x0	R
[4:0]	MP28_MODE	Multipurpose Pin 28 Mode Selection (UART_RX) 00000: Normal Operation 00001: General-Purpose Input 00010: General-Purpose Output from GPIOx_OUT Bits 00011: Master Clock Output 00100: System IRQ1 Output 00101: System IRQ2 Output 00110: System IRQ3 Output 00111: System IRQ4 Output 01000: System IRQ5 Output 01001: System IRQ6 Output 01010: System IRQ7 Output 01011: System IRQ8 Output 01100: System IRQ9 Output 01101: PDM Clock Output 01110: PDM Data Output 10100: XTAL Direct Output	0x0	R/W

GENERAL-PURPOSE INPUT DEBOUNCE CONTROL AND MASTER CLOCK OUTPUT RATE SELECTION REGISTER

Address: 0xF0000298, Reset: 0x00000010, Name: MP_CTRL9

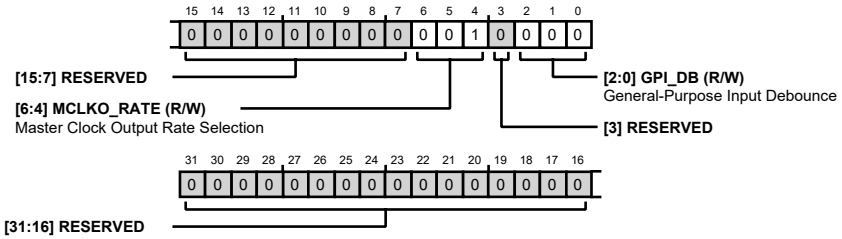


Table 190. Bit Descriptions for MP_CTRL9

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:4]	MCLKO_RATE	Master Clock Output Rate Selection 000: Master Clock Output at 24.576MHz 001: Master Clock Output at 12.288MHz 010: Master Clock Output at 6.144MHz 011: Master Clock Output at 3.072MHz 100: Master Clock Output at 1.536MHz 101: Master Clock Output at 768kHz 110: Master Clock Output at 384kHz 111: Master Clock Output at 192kHz	0x1	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	GPI_DB	General-Purpose Input Debounce 000: GPIO Input without Debounce 001: GPIO Input with Debounce (0.3ms) 010: GPIO Input with Debounce (0.6ms) 011: GPIO Input with Debounce (0.9ms) 100: GPIO Input with Debounce (5ms) 101: GPIO Input with Debounce (10ms) 110: GPIO Input with Debounce (20ms)	0x0	R/W

GENERAL-PURPOSE OUTPUTS CONTROL REGISTER

Address: 0xF000029C, Reset: 0x00000000, Name: MP_CTRL10

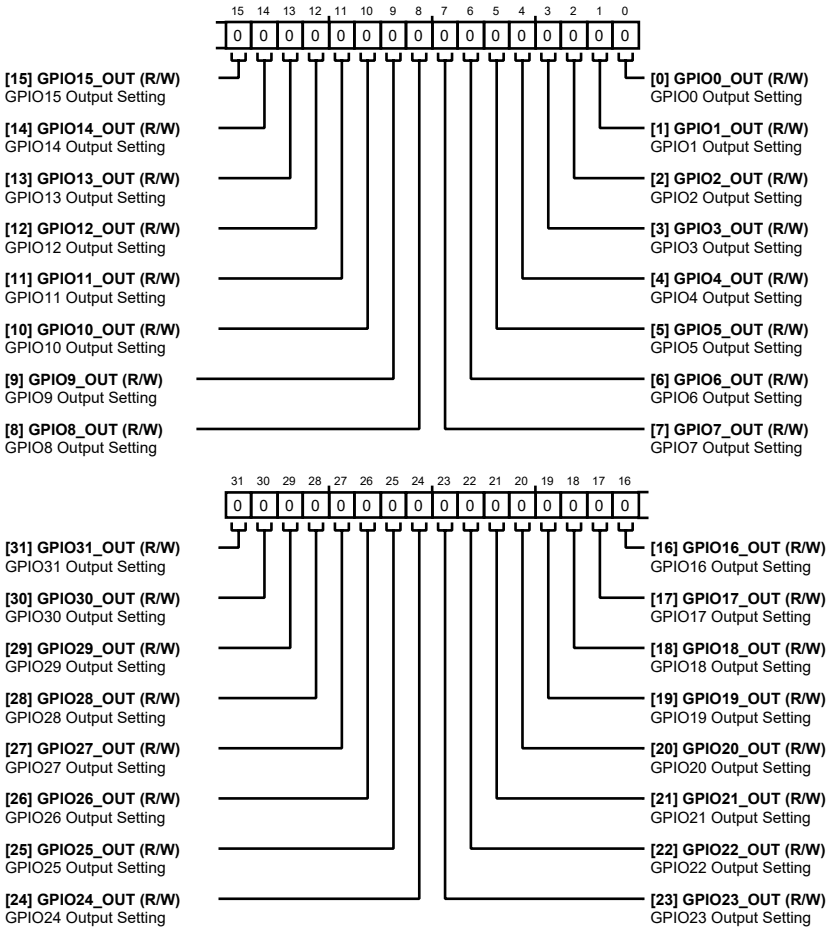


Table 191. Bit Descriptions for MP_CTRL10

Bits	Bit Name	Description	Reset	Access
31	GPIO31_OUT	GPIO31 Output Setting 0: MP31 pin set low when used as general-purpose output. 1: MP31 pin set high when used as general-purpose output.	0x0	R/W
30	GPIO30_OUT	GPIO30 Output Setting 0: MP30 pin set low when used as general-purpose output. 1: MP30 pin set high when used as general-purpose output.	0x0	R/W
29	GPIO29_OUT	GPIO29 Output Setting 0: MP29 pin set low when used as general-purpose output. 1: MP29 pin set high when used as general-purpose output.	0x0	R/W
28	GPIO28_OUT	GPIO28 Output Setting 0: MP28 pin set low when used as general-purpose output. 1: MP28 pin set high when used as general-purpose output.	0x0	R/W
27	GPIO27_OUT	GPIO27 Output Setting 0: MP27 pin set low when used as general-purpose output. 1: MP27 pin set high when used as general-purpose output.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
26	GPIO26_OUT	GPIO26 Output Setting 0: MP26 pin set low when used as general-purpose output. 1: MP26 pin set high when used as general-purpose output.	0x0	R/W
25	GPIO25_OUT	GPIO25 Output Setting 0: MP25 pin set low when used as general-purpose output. 1: MP25 pin set high when used as general-purpose output.	0x0	R/W
24	GPIO24_OUT	GPIO24 Output Setting 0: MP24 pin set low when used as general-purpose output. 1: MP24 pin set high when used as general-purpose output.	0x0	R/W
23	GPIO23_OUT	GPIO23 Output Setting 0: MP23 pin set low when used as general-purpose output. 1: MP23 pin set high when used as general-purpose output.	0x0	R/W
22	GPIO22_OUT	GPIO22 Output Setting 0: MP22 pin set low when used as general-purpose output. 1: MP22 pin set high when used as general-purpose output.	0x0	R/W
21	GPIO21_OUT	GPIO21 Output Setting 0: MP21 pin set low when used as general-purpose output. 1: MP21 pin set high when used as general-purpose output.	0x0	R/W
20	GPIO20_OUT	GPIO20 Output Setting 0: MP20 pin set low when used as general-purpose output. 1: MP20 pin set high when used as general-purpose output.	0x0	R/W
19	GPIO19_OUT	GPIO19 Output Setting 0: MP19 pin set low when used as general-purpose output. 1: MP19 pin set high when used as general-purpose output.	0x0	R/W
18	GPIO18_OUT	GPIO18 Output Setting 0: MP18 pin set low when used as general-purpose output. 1: MP18 pin set high when used as general-purpose output.	0x0	R/W
17	GPIO17_OUT	GPIO17 Output Setting 0: MP17 pin set low when used as general-purpose output. 1: MP17 pin set high when used as general-purpose output.	0x0	R/W
16	GPIO16_OUT	GPIO16 Output Setting 0: MP16 pin set low when used as general-purpose output. 1: MP16 pin set high when used as general-purpose output.	0x0	R/W
15	GPIO15_OUT	GPIO15 Output Setting 0: MP15 pin set low when used as general-purpose output. 1: MP15 pin set high when used as general-purpose output.	0x0	R/W
14	GPIO14_OUT	GPIO14 Output Setting 0: MP14 pin set low when used as general-purpose output. 1: MP14 pin set high when used as general-purpose output.	0x0	R/W
13	GPIO13_OUT	GPIO13 Output Setting 0: MP13 pin set low when used as general-purpose output. 1: MP13 pin set high when used as general-purpose output.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
12	GPIO12_OUT	GPIO12 Output Setting 0: MP12 pin set low when used as general-purpose output. 1: MP12 pin set high when used as general-purpose output.	0x0	R/W
11	GPIO11_OUT	GPIO11 Output Setting 0: MP11 pin set low when used as general-purpose output. 1: MP11 pin set high when used as general-purpose output.	0x0	R/W
10	GPIO10_OUT	GPIO10 Output Setting 0: MP10 pin set low when used as general-purpose output. 1: MP10 pin set high when used as general-purpose output.	0x0	R/W
9	GPIO9_OUT	GPIO9 Output Setting 0: MP9 pin set low when used as general-purpose output. 1: MP9 pin set high when used as general-purpose output.	0x0	R/W
8	GPIO8_OUT	GPIO8 Output Setting 0: MP8 pin set low when used as general-purpose output. 1: MP8 pin set high when used as general-purpose output.	0x0	R/W
7	GPIO7_OUT	GPIO7 Output Setting 0: MP7 pin set low when used as general-purpose output. 1: MP7 pin set high when used as general-purpose output.	0x0	R/W
6	GPIO6_OUT	GPIO6 Output Setting 0: MP6 pin set low when used as general-purpose output. 1: MP6 pin set high when used as general-purpose output.	0x0	R/W
5	GPIO5_OUT	GPIO5 Output Setting 0: MP5 pin set low when used as general-purpose output. 1: MP5 pin set high when used as general-purpose output.	0x0	R/W
4	GPIO4_OUT	GPIO4 Output Setting 0: MP4 pin set low when used as general-purpose output. 1: MP4 pin set high when used as general-purpose output.	0x0	R/W
3	GPIO3_OUT	GPIO3 Output Setting 0: MP3 pin set low when used as general-purpose output. 1: MP3 pin set high when used as general-purpose output.	0x0	R/W
2	GPIO2_OUT	GPIO2 Output Setting 0: MP2 pin set low when used as general-purpose output. 1: MP2 pin set high when used as general-purpose output.	0x0	R/W
1	GPIO1_OUT	GPIO1 Output Setting 0: MP1 pin set low when used as general-purpose output. 1: MP1 pin set high when used as general-purpose output.	0x0	R/W
0	GPIO0_OUT	GPIO0 Output Setting 0: MP0 pin set low when used as general-purpose output. 1: MP0 pin set high when used as general-purpose output.	0x0	R/W

FSYNC_0 PIN CONTROLS REGISTER

Address: 0xF00002A0, Reset: 0x00000005, Name: FSYNC0_CTRL

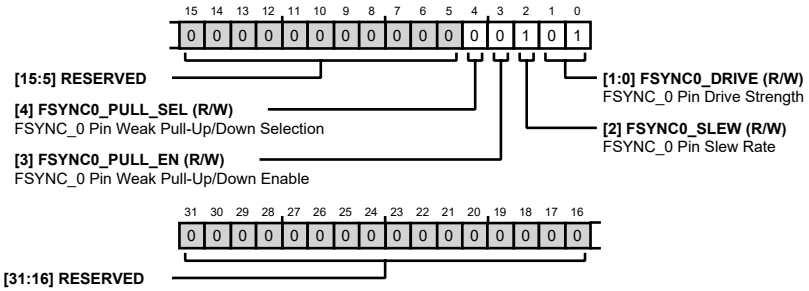


Table 192. Bit Descriptions for FSYNC0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	FSYNC0_PULL_SEL	FSYNC_0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	FSYNC0_PULL_EN	FSYNC_0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by FSYNC0_PULL_SEL bit.	0x0	R/W
2	FSYNC0_SLEW	FSYNC_0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	FSYNC0_DRIVE	FSYNC_0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

BCLK_0 PIN CONTROLS REGISTER

Address: 0xF00002A4, Reset: 0x00000005, Name: BCLK0_CTRL

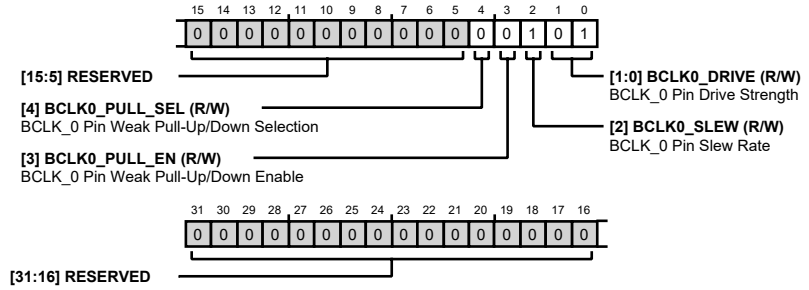


Table 193. Bit Descriptions for BCLK0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	BCLK0_PULL_SEL	BCLK_0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	BCLK0_PULL_EN	BCLK_0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by BCLK0_PULL_SEL bit.	0x0	R/W
2	BCLK0_SLEW	BCLK_0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	BCLK0_DRIVE	BCLK_0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SDATAO_0 PIN CONTROL REGISTER

Address: 0xF00002A8, Reset: 0x00000005, Name: SDATAO0_CTRL

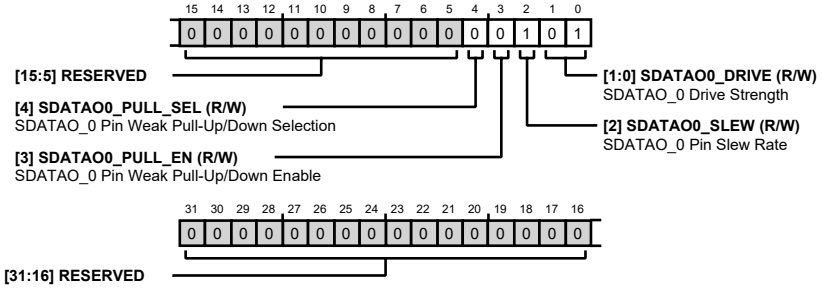


Table 194. Bit Descriptions for SDATAO0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SDATAO0_PULL_SEL	SDATAO_0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	SDATAO0_PULL_EN	SDATAO_0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SDATAO1_PULL_SEL bit.	0x0	R/W
2	SDATAO0_SLEW	SDATAO_0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	SDATAO0_DRIVE	SDATAO_0 Drive Strength 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SDATAI_0 PIN CONTROLS REGISTER

Address: 0xF00002AC, Reset: 0x00000005, Name: SDATAI0_CTRL

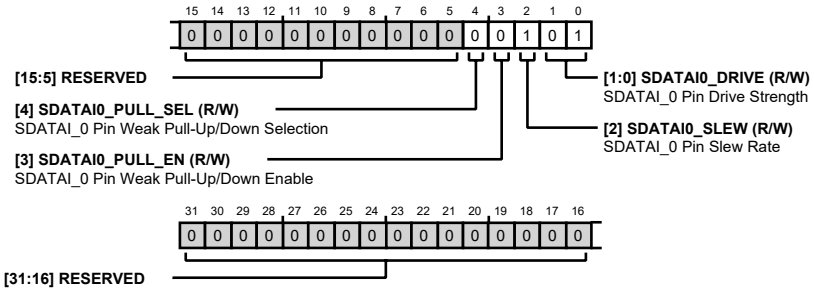


Table 195. Bit Descriptions for SDATAI0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SDATAI0_PULL_SEL	SDATAI_0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	SDATAI0_PULL_EN	SDATAI_0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SDATAI0_PULL_SEL bit.	0x0	R/W
2	SDATAI0_SLEW	SDATAI_0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	SDATAI0_DRIVE	SDATAI_0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

FSYNC_1 PIN CONTROLS REGISTER

Address: 0xF00002B0, Reset: 0x00000005, Name: FSYNC1_CTRL

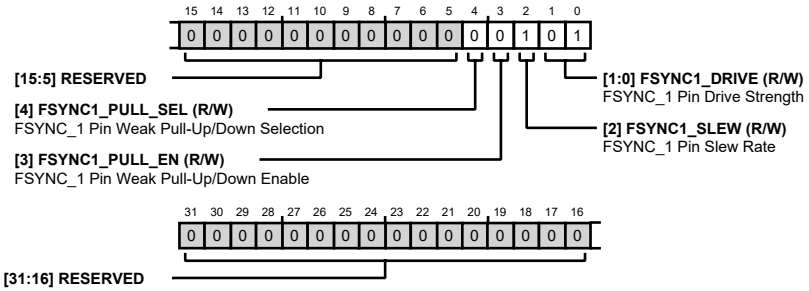


Table 196. Bit Descriptions for FSYNC1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	FSYNC1_PULL_SEL	FSYNC_1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	FSYNC1_PULL_EN	FSYNC_1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by FSYNC1_PULL_SEL bit.	0x0	R/W
2	FSYNC1_SLEW	FSYNC_1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	FSYNC1_DRIVE	FSYNC_1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

BCLK_1 PIN CONTROLS REGISTER

Address: 0xF00002B4, Reset: 0x00000005, Name: BCLK1_CTRL

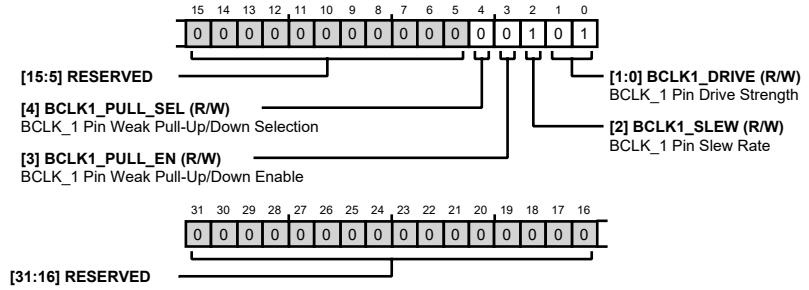


Table 197. Bit Descriptions for BCLK1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	BCLK1_PULL_SEL	BCLK_1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	BCLK1_PULL_EN	BCLK_1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by BCLK1_PULL_SEL bit.	0x0	R/W
2	BCLK1_SLEW	BCLK_1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	BCLK1_DRIVE	BCLK_1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SDATAO_1 PIN CONTROLS REGISTER

Address: 0xF00002B8, Reset: 0x00000005, Name: SDATAO1_CTRL

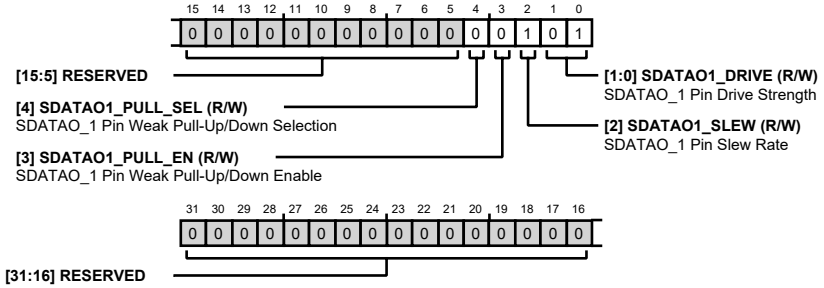


Table 198. Bit Descriptions for SDATAO1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SDATAO1_PULL_SEL	SDATAO_1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	SDATAO1_PULL_EN	SDATAO_1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SDATAO1_PULL_SEL bit.	0x0	R/W
2	SDATAO1_SLEW	SDATAO_1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	SDATAO1_DRIVE	SDATAO_1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SDATAI_1 PIN CONTROLS REGISTER

Address: 0xF00002BC, Reset: 0x00000005, Name: SDATAI1_CTRL

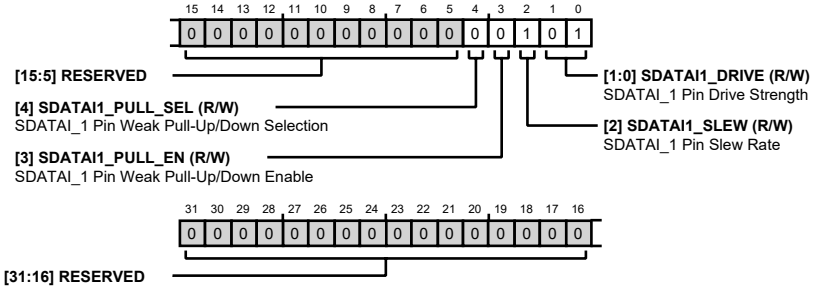


Table 199. Bit Descriptions for SDATAI1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SDATAI1_PULL_SEL	SDATAI_1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	SDATAI1_PULL_EN	SDATAI_1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SDATAI1_PULL_SEL bit.	0x0	R/W
2	SDATAI1_SLEW	SDATAI_1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	SDATAI1_DRIVE	SDATAI_1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC_CLK0 PIN CONTROLS REGISTER

Address: 0xF00002C0, Reset: 0x00000005, Name: DMIC_CLK0_CTRL

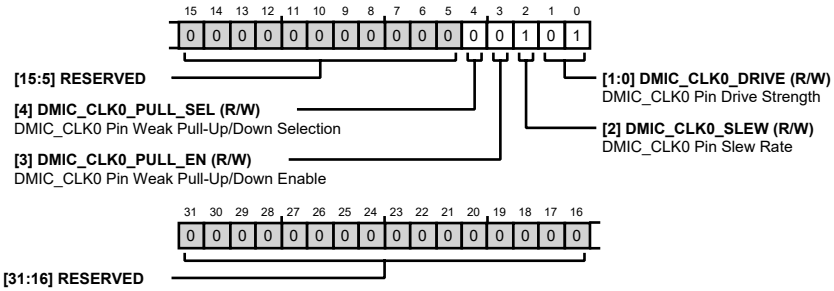


Table 200. Bit Descriptions for DMIC_CLK0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC_CLK0_PULL_SEL	DMIC_CLK0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC_CLK0_PULL_EN	DMIC_CLK0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC_CLK0_PULL_SEL bit.	0x0	R/W
2	DMIC_CLK0_SLEW	DMIC_CLK0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	DMIC_CLK0_DRIVE	DMIC_CLK0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC_CLK1 PIN CONTROLS REGISTER

Address: 0xF00002C4, Reset: 0x00000005, Name: DMIC_CLK1_CTRL

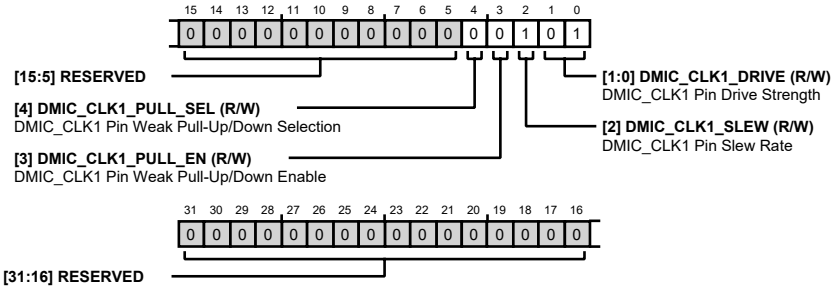


Table 201. Bit Descriptions for DMIC_CLK1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC_CLK1_PULL_SEL	DMIC_CLK1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC_CLK1_PULL_EN	DMIC_CLK1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC_CLK1_PULL_SEL bit.	0x0	R/W
2	DMIC_CLK1_SLEW	DMIC_CLK1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	DMIC_CLK1_DRIVE	DMIC_CLK1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC01 PIN CONTROLS REGISTER

Address: 0xF00002C8, Reset: 0x00000005, Name: DMIC01_CTRL

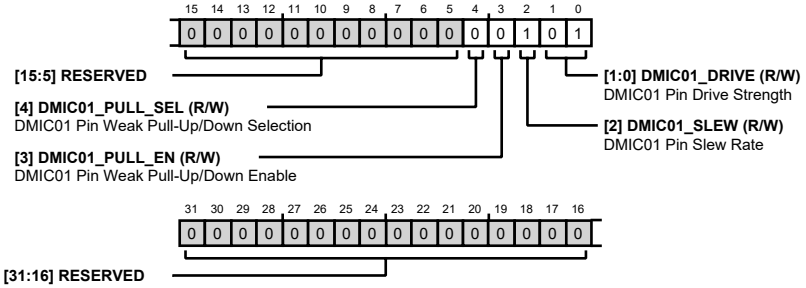


Table 202. Bit Descriptions for DMIC01_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC01_PULL_SEL	DMIC01 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC01_PULL_EN	DMIC01 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	DMIC01_SLEW	DMIC01 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	DMIC01_DRIVE	DMIC01 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC23 PIN CONTROLS REGISTER

Address: 0xF00002CC, Reset: 0x00000005, Name: DMIC23_CTRL

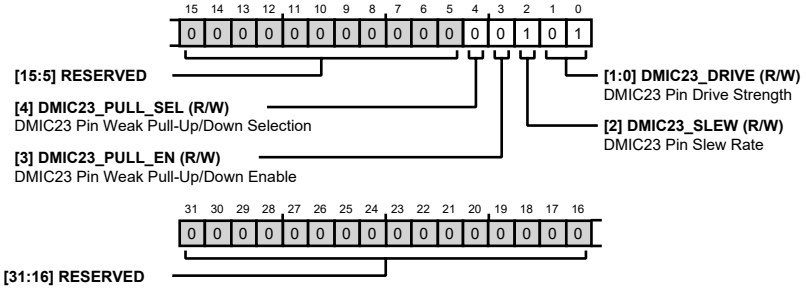


Table 203. Bit Descriptions for DMIC23_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC23_PULL_SEL	DMIC23 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC23_PULL_EN	DMIC23 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC23_PULL_SEL bit.	0x0	R/W
2	DMIC23_SLEW	DMIC23 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	DMIC23_DRIVE	DMIC23 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC45 PIN CONTROLS REGISTER

Address: 0xF00002D0, Reset: 0x00000005, Name: DMIC45_CTRL

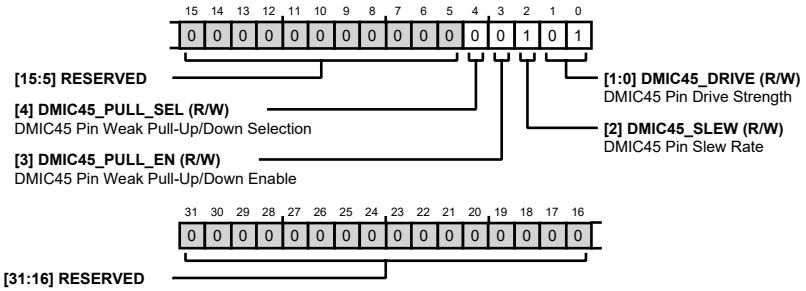


Table 204. Bit Descriptions for DMIC45_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC45_PULL_SEL	DMIC45 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC45_PULL_EN	DMIC45 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC23_PULL_SEL bit.	0x0	R/W
2	DMIC45_SLEW	DMIC45 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	DMIC45_DRIVE	DMIC45 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC67 PIN CONTROLS REGISTER

Address: 0xF00002D4, Reset: 0x00000005, Name: DMIC67_CTRL

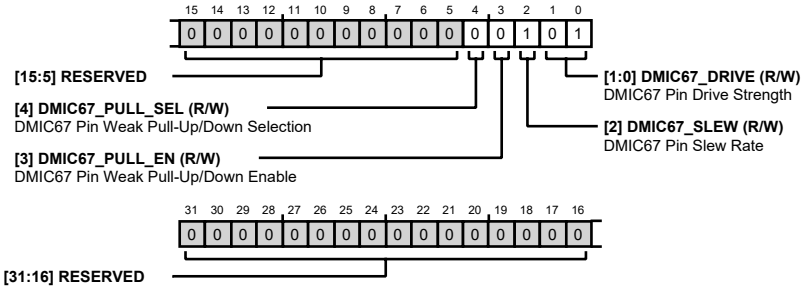


Table 205. Bit Descriptions for DMIC67_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC67_PULL_SEL	DMIC67 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC67_PULL_EN	DMIC67 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC23_PULL_SEL bit.	0x0	R/W
2	DMIC67_SLEW	DMIC67 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	DMIC67_DRIVE	DMIC67 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

DMIC89 PIN CONTROLS REGISTER

Address: 0xF00002D8, Reset: 0x00000005, Name: DMIC89_CTRL

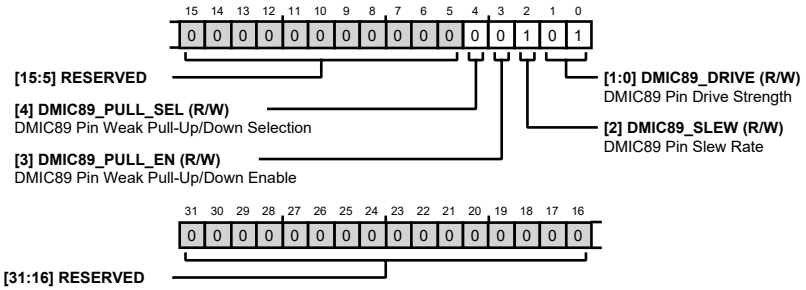


Table 206. Bit Descriptions for DMIC89_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	DMIC89_PULL_SEL	DMIC89 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	DMIC89_PULL_EN	DMIC89 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC23_PULL_SEL bit.	0x0	R/W
2	DMIC89_SLEW	DMIC89 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	DMIC89_DRIVE	DMIC89 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_CLK PIN CONTROLS REGISTER

Address: 0xF00002DC, Reset: 0x00000005, Name: QSPIM_CLK_CTRL

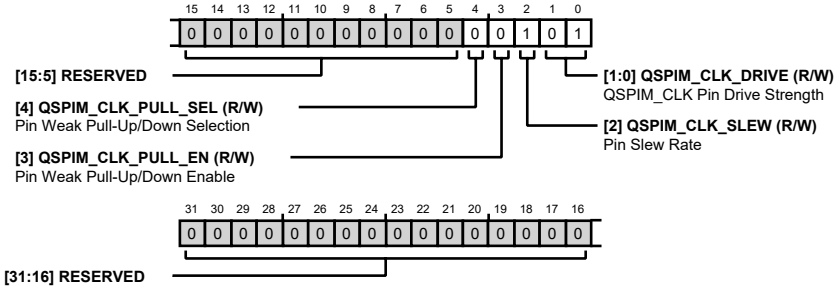


Table 207. Bit Descriptions for QSPIM_CLK_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_CLK_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_CLK_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_CLK_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_CLK_DRIVE	QSPIM_CLK Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_CS0 PIN CONTROLS REGISTER

Address: 0xF00002E0, Reset: 0x00000005, Name: QSPIM_CS0_CTRL

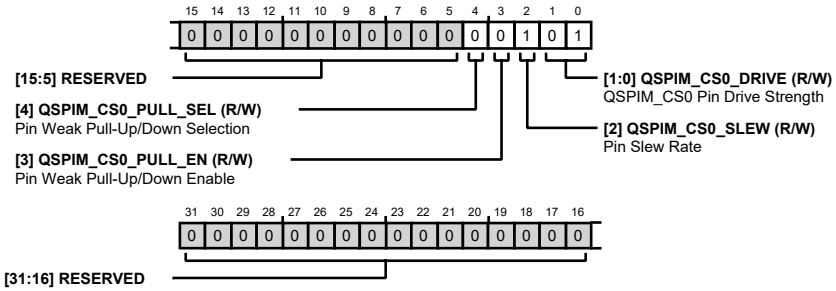


Table 208. Bit Descriptions for QSPIM_CS0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_CS0_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_CS0_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_CS0_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_CS0_DRIVE	QSPIM_CS0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_CS1 PIN CONTROLS REGISTER

Address: 0xF00002E4, Reset: 0x00000005, Name: QSPIM_CS1_CTRL

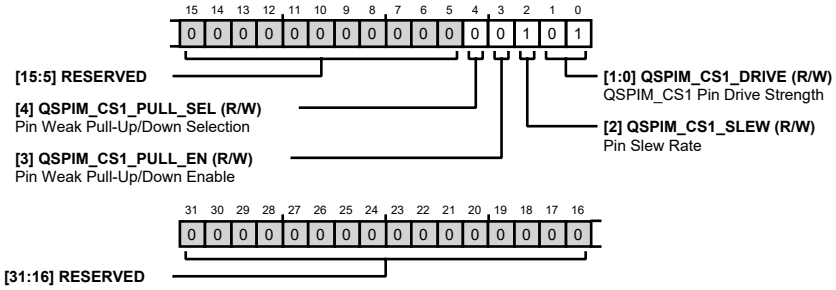


Table 209. Bit Descriptions for QSPIM_CS1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_CS1_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_CS1_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_CS1_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_CS1_DRIVE	QSPIM_CS1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_SDIO0 PIN CONTROLS REGISTER

Address: 0xF00002E8, Reset: 0x00000005, Name: QSPIM_SDIO0_CTRL

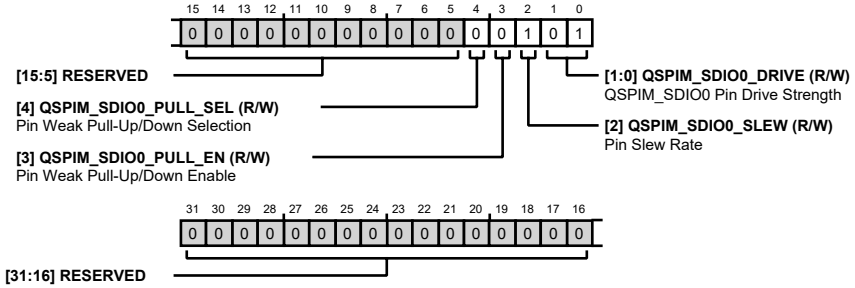


Table 210. Bit Descriptions for QSPIM_SDIO0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_SDIO0_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_SDIO0_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_SDIO0_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	QSPIM_SDIO0_DRIVE	QSPIM_SDIO0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_SDIO1 PIN CONTROLS REGISTER

Address: 0xF00002EC, Reset: 0x00000005, Name: QSPIM_SDIO1_CTRL

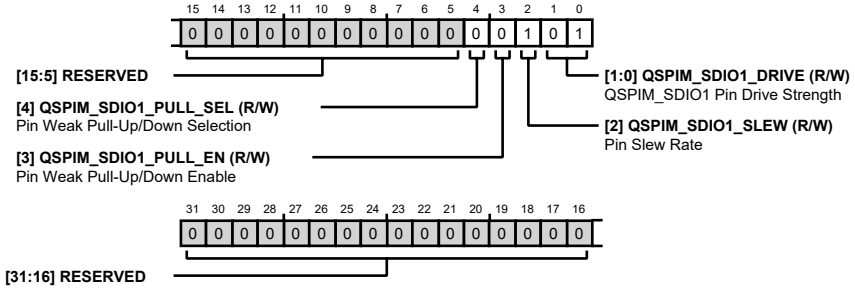


Table 211. Bit Descriptions for QSPIM_SDIO1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_SDIO1_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_SDIO1_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_SDIO1_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_SDIO1_DRIVE	QSPIM_SDIO1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_SDIO2 PIN CONTROLS REGISTER

Address: 0xF00002F0, Reset: 0x00000005, Name: QSPIM_SDIO2_CTRL

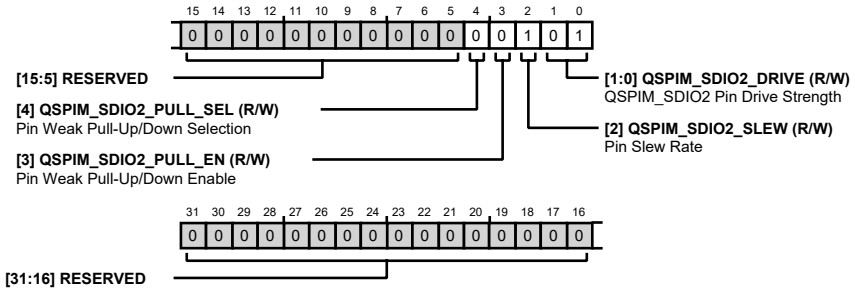


Table 212. Bit Descriptions for QSPIM_SDIO2_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_SDIO2_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_SDIO2_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_SDIO2_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_SDIO2_DRIVE	QSPIM_SDIO2 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

QSPIM_SDIO3 PIN CONTROLS REGISTER

Address: 0xF00002F4, Reset: 0x00000005, Name: QSPIM_SDIO3_CTRL

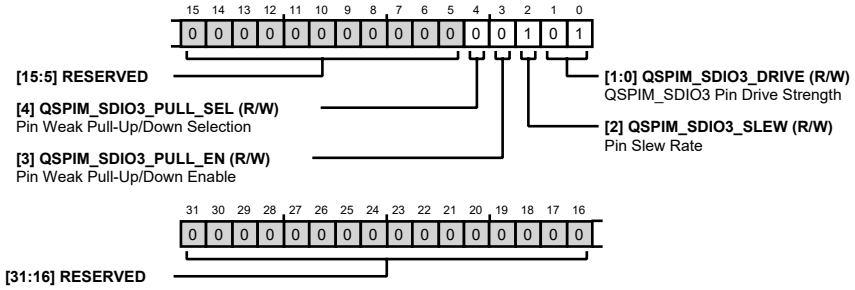


Table 213. Bit Descriptions for QSPIM_SDIO3_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	QSPIM_SDIO3_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	QSPIM_SDIO3_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	QSPIM_SDIO3_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	QSPIM_SDIO3_DRIVE	QSPIM_SDIO3 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

JTAG_TRST PIN CONTROLS REGISTER

Address: 0xF00002F8, Reset: 0x00000005, Name: JTAG_TRST_CTRL

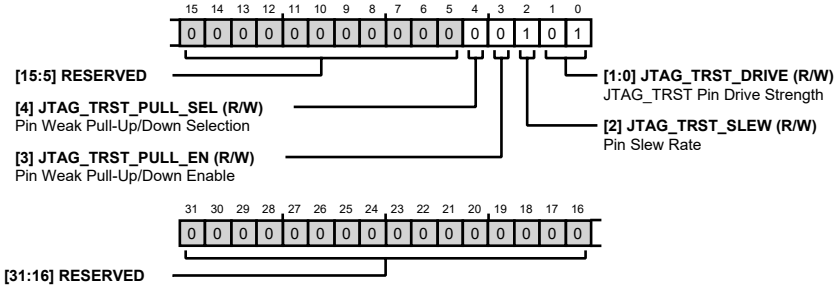


Table 214. Bit Descriptions for JTAG_TRST_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	JTAG_TRST_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	JTAG_TRST_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	JTAG_TRST_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	JTAG_TRST_DRIVE	JTAG_TRST Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

JTAG_TMS PIN CONTROLS REGISTER

Address: 0xF00002FC, Reset: 0x00000005, Name: JTAG_TMS_CTRL

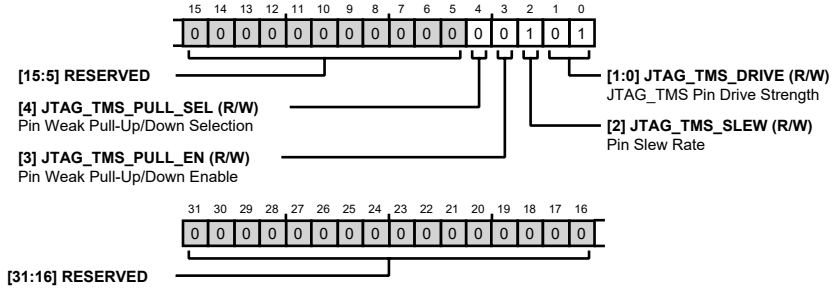


Table 215. Bit Descriptions for JTAG_TMS_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	JTAG_TMS_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	JTAG_TMS_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	JTAG_TMS_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	JTAG_TMS_DRIVE	JTAG_TMS Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

JTAG_TCK PIN CONTROLS REGISTER

Address: 0xF0000300, Reset: 0x00000005, Name: JTAG_TCK_CTRL

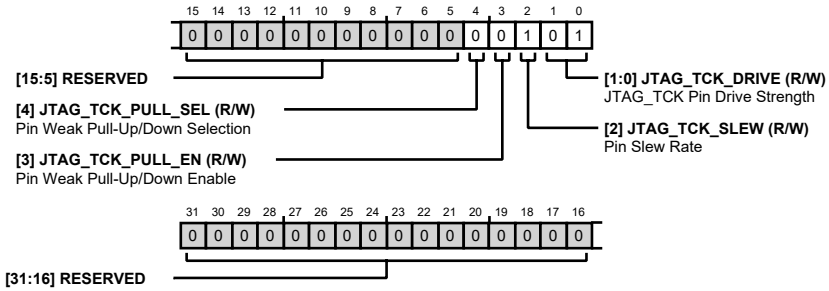


Table 216. Bit Descriptions for JTAG_TCK_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	JTAG_TCK_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	JTAG_TCK_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	JTAG_TCK_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	JTAG_TCK_DRIVE	JTAG_TCK Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

JTAG_TDI PIN CONTROLS REGISTER

Address: 0xF0000304, Reset: 0x00000005, Name: JTAG_TDI_CTRL

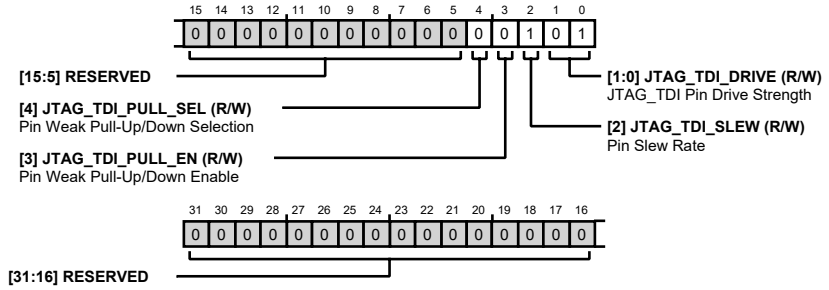


Table 217. Bit Descriptions for JTAG_TDI_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	JTAG_TDI_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	JTAG_TDI_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	JTAG_TDI_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	JTAG_TDI_DRIVE	JTAG_TDI Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

JTAG_TDO PIN CONTROLS REGISTER

Address: 0xF0000308, Reset: 0x00000005, Name: JTAG_TDO_CTRL

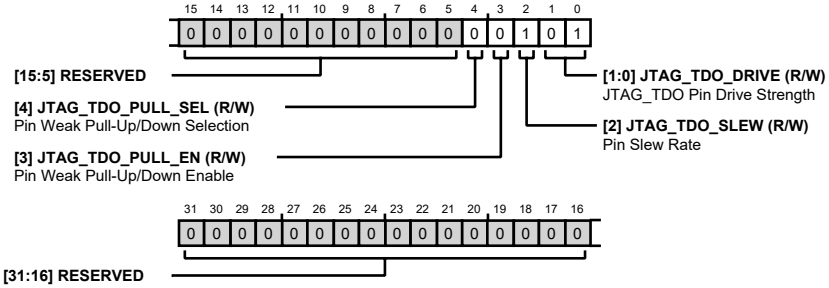


Table 218. Bit Descriptions for JTAG_TDO_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	JTAG_TDO_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	JTAG_TDO_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	JTAG_TDO_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	JTAG_TDO_DRIVE	JTAG_TDO Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

UART_TX PIN CONTROLS REGISTER

Address: 0xF000030C, Reset: 0x00000005, Name: UART_TX_CTRL

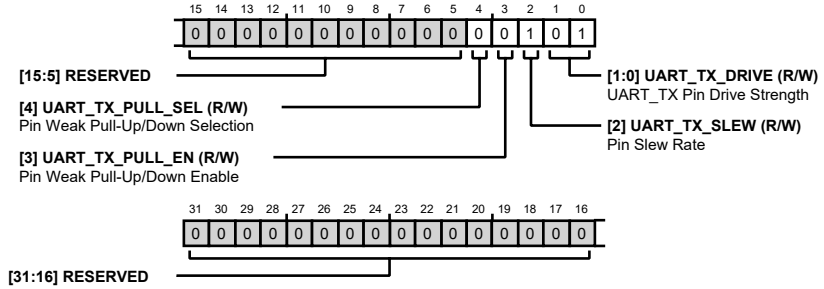


Table 219. Bit Descriptions for UART_TX_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	UART_TX_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	UART_TX_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	UART_TX_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	UART_TX_DRIVE	UART_TX Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

UART_RX PIN CONTROLS REGISTER

Address: 0xF0000310, Reset: 0x00000005, Name: UART_RX_CTRL

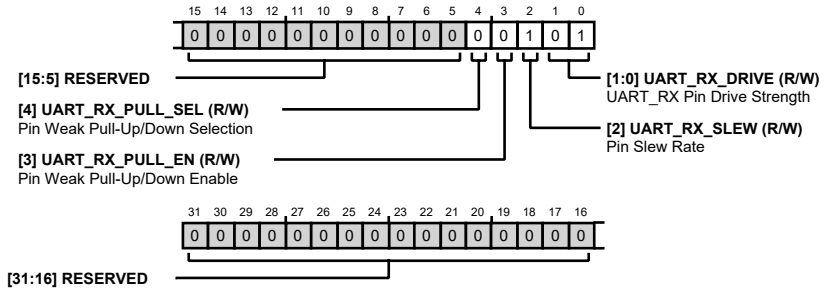


Table 220. Bit Descriptions for UART_RX_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	UART_RX_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	UART_RX_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	UART_RX_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	UART_RX_DRIVE	UART_RX Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

UART_RTS PIN CONTROLS REGISTER

Address: 0xF0000314, Reset: 0x00000005, Name: UART_RTS_CTRL

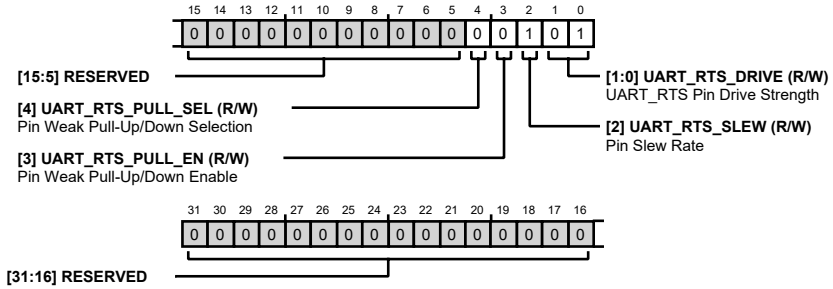


Table 221. Bit Descriptions for UART_RTS_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	UART_RTS_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	UART_RTS_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	UART_RTS_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	UART_RTS_DRIVE	UART_RTS Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

UART_CTS PIN CONTROLS REGISTER

Address: 0xF0000318, Reset: 0x00000005, Name: UART_CTS_CTRL

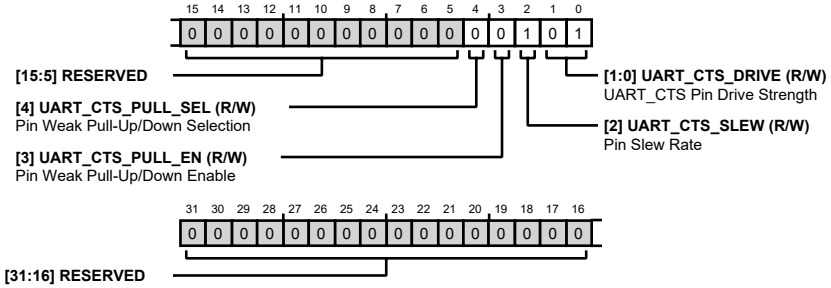


Table 222. Bit Descriptions for UART_CTS_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	UART_CTS_PULL_SEL	Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	UART_CTS_PULL_EN	Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by DMIC01_PULL_SEL bit.	0x0	R/W
2	UART_CTS_SLEW	Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[1:0]	UART_CTS_DRIVE	UART_CTS Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SELFBOOT PIN CONTROLS REGISTER

Address: 0xF000031C, Reset: 0x00000001, Name: SELFBOOT_CTRL

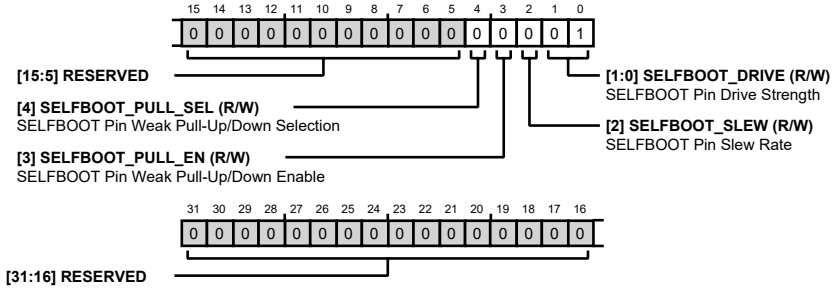


Table 223. Bit Descriptions for SELFBOOT_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SELFBOOT_PULL_SEL	SELFBOOT Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	SELFBOOT_PULL_EN	SELFBOOT Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SELFBOOT_PULL_SEL bit.	0x0	R/W
2	SELFBOOT_SLEW	SELFBOOT Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x0	R/W
[1:0]	SELFBOOT_DRIVE	SELFBOOT Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SCL/SCLK AND SDA/MISO PIN CONTROLS REGISTER

Address: 0xF0000320, Reset: 0x00000000, Name: I2C_SPI_CTRL

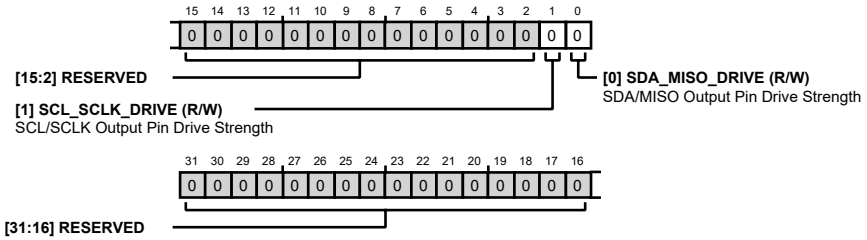


Table 224. Bit Descriptions for I2C_SPI_CTRL

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved	0x0	R
1	SCL_SCLK_DRIVE	SCL/SCLK Output Pin Drive Strength 0: 4mA Drive Strength 1: 20mA Drive Strength. May be required for fast mode plus I^2C operation.	0x0	R/W
0	SDA_MISO_DRIVE	SDA/MISO Output Pin Drive Strength 0: 4mA Drive Strength 1: 20mA Drive Strength. May be required for fast mode plus I^2C operation.	0x0	R/W

SCL1 AND SDA1 PIN CONTROLS REGISTER

Address: 0xF0000324, Reset: 0x00000003, Name: I3C_CTRL

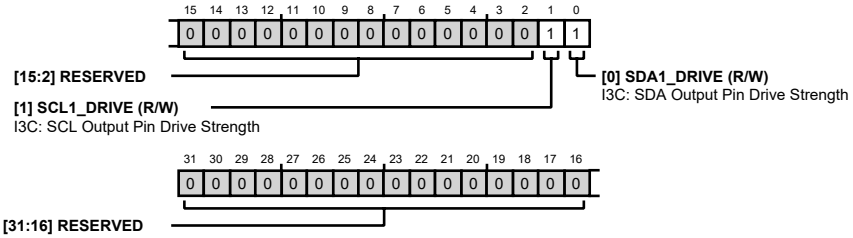


Table 225. Bit Descriptions for I3C_CTRL

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved	0x0	R
1	SCL1_DRIVE	I^3C: SCL Output Pin Drive Strength 0: 4mA drive strength. 1: 20mA Drive Strength. May be required for fast mode plus I^2C operation.	0x1	R/W
0	SDA1_DRIVE	I^3C: SDA Output Pin Drive Strength 0: 4mA Drive Strength. 1: 20mA Drive Strength. May be required for fast mode plus I^2C operation.	0x1	R/W

ADDR0 PIN CONTROLS REGISTER

Address: 0xF0000328, Reset: 0x00000005, Name: ADDR0_CTRL

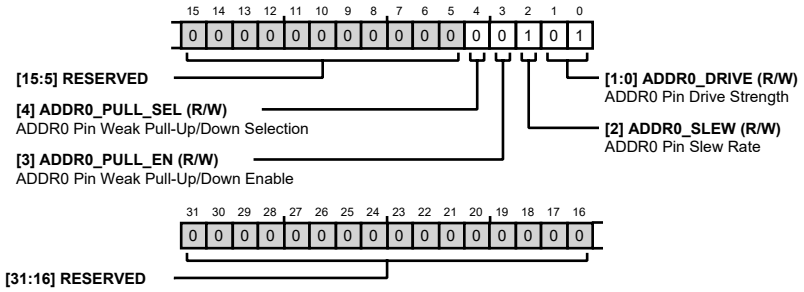


Table 226. Bit Descriptions for ADDR0_CTRL

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	ADDR0_PULL_SEL	ADDR0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	ADDR0_PULL_EN	ADDR0 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SELFBOOT_PULL_SEL bit.	0x0	R/W
2	ADDR0_SLEW	ADDR0 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	ADDR0_DRIVE	ADDR0 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

ADDR1 PIN CONTROLS REGISTER

Address: 0xF000032C, Reset: 0x00000005, Name: ADDR1_CTRL

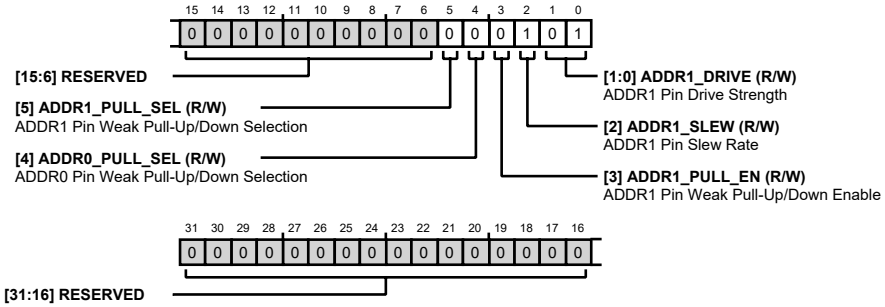


Table 227. Bit Descriptions for ADDR1_CTRL

Bits	Bit Name	Description	Reset	Access
[31:6]	RESERVED	Reserved	0x0	R
5	ADDR1_PULL_SEL	ADDR1 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
4	ADDR0_PULL_SEL	ADDR0 Pin Weak Pull-Up/Down Selection 0: Weak pull-down when enabled. 1: Weak pull-up when enabled.	0x0	R/W
3	ADDR1_PULL_EN	ADDR1 Pin Weak Pull-Up/Down Enable 0: No pull-up or pull-down. 1: Weak pull-up or pull-down set by SELFBOOT_PULL_SEL bit.	0x0	R/W
2	ADDR1_SLEW	ADDR1 Pin Slew Rate. Determines the slew rate of the pin when used as an output. 0: Fast Slew Rate 1: Slow Slew Rate	0x1	R/W
[1:0]	ADDR1_DRIVE	ADDR1 Pin Drive Strength. Determines the drive strength of the pin when used as an output. 00: 2mA Output Drive 01: 4mA Output Drive 10: 8mA Output Drive 11: 12mA Output Drive	0x1	R/W

SYSTEM IRQ MP PIN OUTPUT SIGNALING REGISTER

Address: 0xF0000334, Reset: 0x00000000, Name: IRQ_INVERT

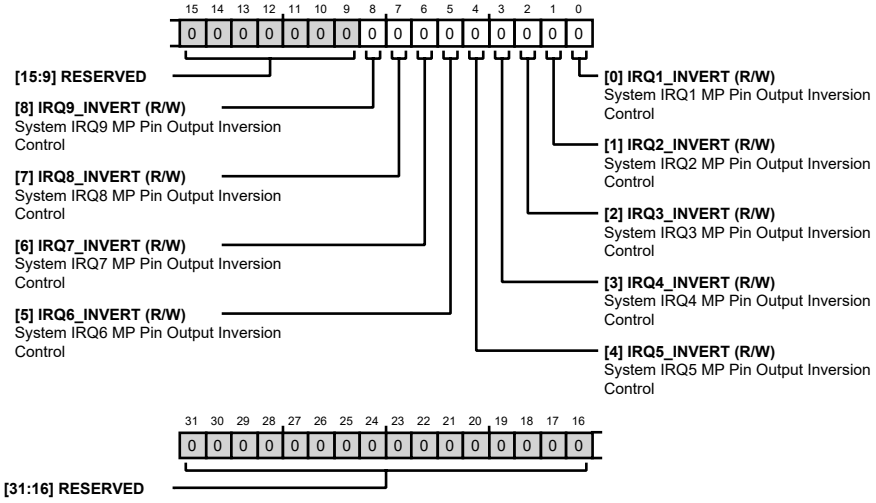


Table 228. Bit Descriptions for IRQ_INVERT

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	IRQ9_INVERT	System IRQ9 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	IRQ8_INVERT	System IRQ8 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
6	IRQ7_INVERT	System IRQ7 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
5	IRQ6_INVERT	System IRQ6 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
4	IRQ5_INVERT	System IRQ5 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
3	IRQ4_INVERT	System IRQ4 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
2	IRQ3_INVERT	System IRQ3 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
1	IRQ2_INVERT	System IRQ2 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W
0	IRQ1_INVERT	System IRQ1 MP Pin Output Inversion Control 0: Active-High Interrupt Signaling on Pin 1: Active-Low Interrupt Signaling on Pin	0x0	R/W

SYSTEM IRQ[N] MASKING REGISTER

Address: 0xF0000338 to 0xF0000398 (Increments of 12), Reset: 0xFFFFFFFF, Name: IRQn_MASK1

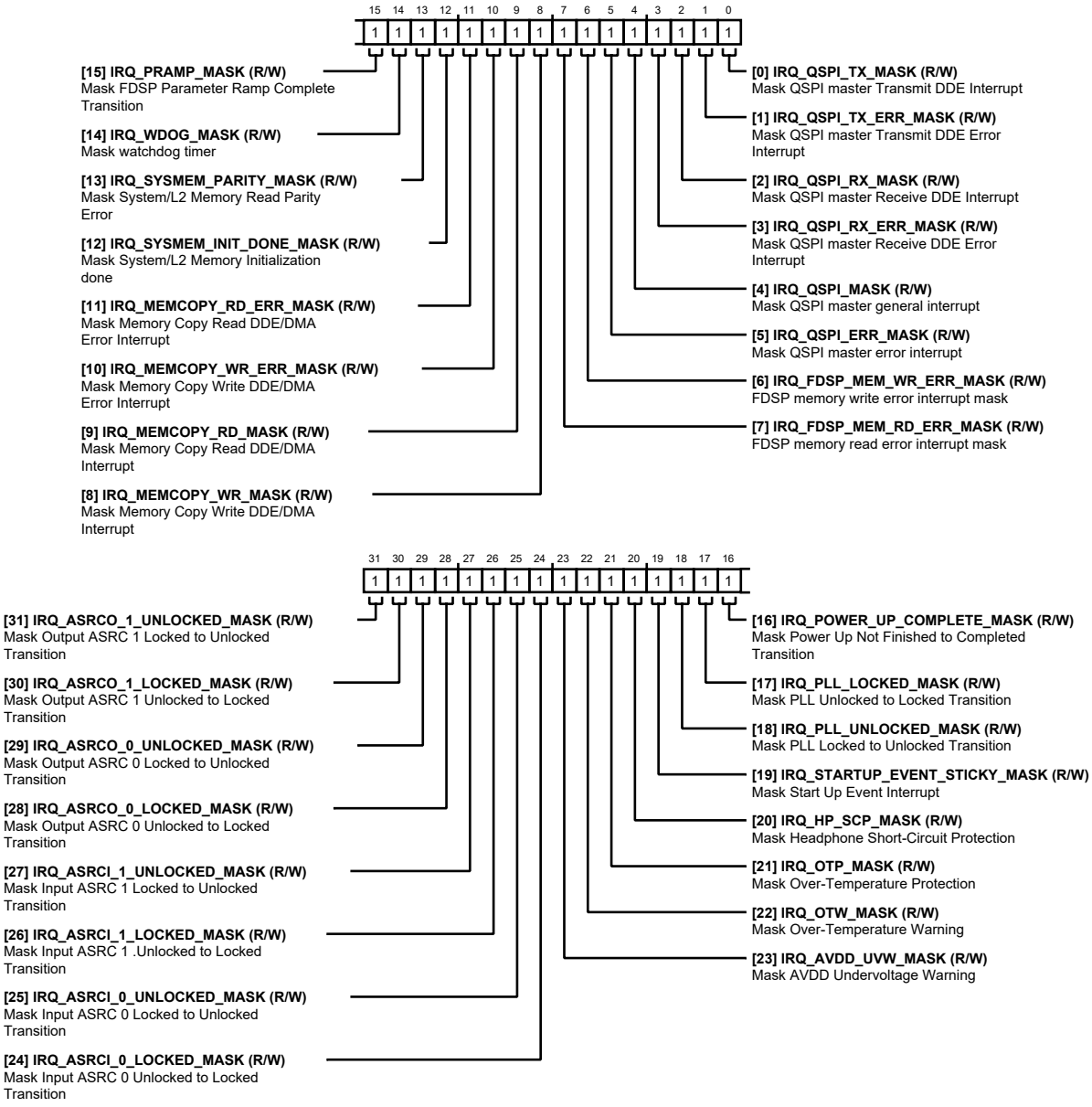


Table 229. Bit Descriptions for IRQn_MASK1

Bits	Bit Name	Description	Reset	Access
31	IRQ_ASRCO_1_UNLOCKED_MASK	Mask Output ASRC 1 Locked to Unlocked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
30	IRQ_ASRCO_1_LOCKED_MASK	Mask Output ASRC 1 Unlocked to Locked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
29	IRQ_ASRCO_0_UNLOCKED_MASK	Mask Output ASRC 0 Locked to Unlocked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
28	IRQ_ASRCO_0_LOCKED_MASK	Mask Output ASRC 0 Unlocked to Locked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
27	IRQ_ASRCI_1_UNLOCKED_MASK	Mask Input ASRC 1 Locked to Unlocked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
26	IRQ_ASRCI_1_LOCKED_MASK	Mask Input ASRC 1 Unlocked to Locked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
25	IRQ_ASRCI_0_UNLOCKED_MASK	Mask Input ASRC 0 Locked to Unlocked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
24	IRQ_ASRCI_0_LOCKED_MASK	Mask Input ASRC 0 Unlocked to Locked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
23	IRQ_AVDD_UVW_MASK	Mask AVDD Undervoltage Warning 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
22	IRQ_OTW_MASK	Mask Over-Temperature Warning 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
21	IRQ_OTP_MASK	Mask Over-Temperature Protection 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
20	IRQ_HP_SCP_MASK	Mask Headphone Short-Circuit Protection 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
19	IRQ_STARTUP_EVENT_STICKY_MASK	Mask Start-Up Event Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
18	IRQ_PLL_UNLOCKED_MASK	Mask PLL Locked to Unlocked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
17	IRQ_PLL_LOCKED_MASK	Mask PLL Unlocked to Locked Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
16	IRQ_POWER_UP_COMPLETE_MASK	Mask Power-Up Not Finished to Completed Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
15	IRQ_PRAMP_MASK	Mask FDSP Parameter Ramp Complete Transition 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
14	IRQ_WDOG_MASK	Mask Watchdog Timer 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
13	IRQ_SYSMEM_PARITY_MASK	Mask System/L2 Memory Read Parity Error 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
12	IRQ_SYSMEM_INIT_DONE_MASK	Mask System/L2 Memory Initialization Done 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
11	IRQ_MEMCOPY_RD_ERR_MASK	Mask Memory Copy Read DDE/DMA Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
10	IRQ_MEMCOPY_WR_ERR_MASK	Mask Memory Copy Write DDE/DMA Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
9	IRQ_MEMCOPY_RD_MASK	Mask Memory Copy Read DDE/DMA Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
8	IRQ_MEMCOPY_WR_MASK	Mask Memory Copy Write DDE/DMA Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
7	IRQ_FDSP_MEM_RD_ERR_MASK	FDSP Memory Read Error Interrupt Mask 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
6	IRQ_FDSP_MEM_WR_ERR_MASK	FDSP Memory Write Error Interrupt Mask 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
5	IRQ_QSPI_ERR_MASK	Mask QSPI Master Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
4	IRQ_QSPI_MASK	Mask QSPI Master General Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
3	IRQ_QSPI_RX_ERR_MASK	Mask QSPI Master Receive DDE Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
2	IRQ_QSPI_RX_MASK	Mask QSPI Master Receive DDE Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
1	IRQ_QSPI_TX_ERR_MASK	Mask QSPI Master Transmit DDE Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
0	IRQ_QSPI_TX_MASK	Mask QSPI Master Transmit DDE Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

SYSTEM IRQ[N] MASKING REGISTER

Address: 0xF000033C to 0xF000039C (Increments of 12), Reset: 0xFFFF3F2F, Name: IRQn_MASK2

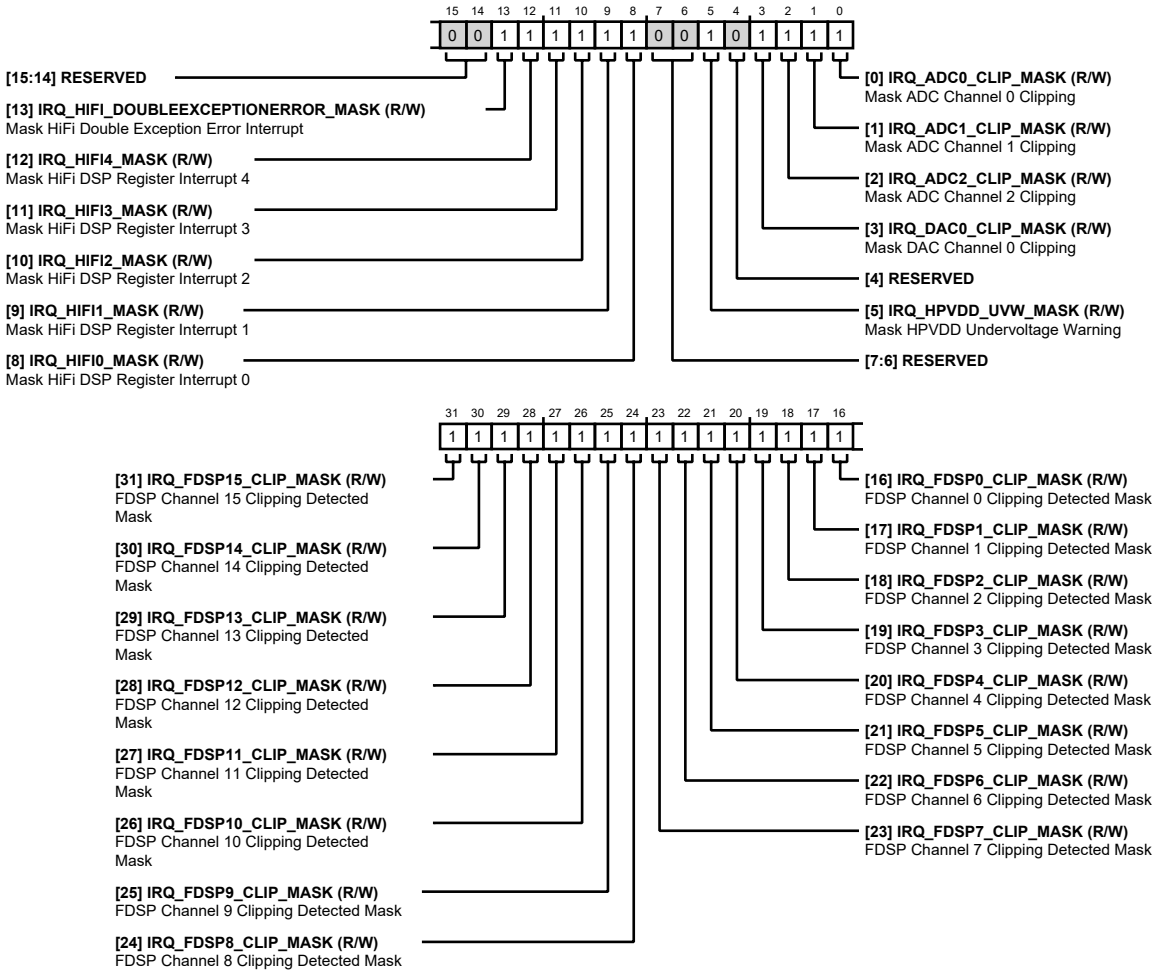


Table 230. Bit Descriptions for IRQn_MASK2

Bits	Bit Name	Description	Reset	Access
31	IRQ_FDSP15_CLIP_MASK	FDSP Channel 15 Clipping Detected Mask	0x1	R/W
30	IRQ_FDSP14_CLIP_MASK	FDSP Channel 14 Clipping Detected Mask	0x1	R/W
29	IRQ_FDSP13_CLIP_MASK	FDSP Channel 13 Clipping Detected Mask	0x1	R/W
28	IRQ_FDSP12_CLIP_MASK	FDSP Channel 12 Clipping Detected Mask	0x1	R/W
27	IRQ_FDSP11_CLIP_MASK	FDSP Channel 11 Clipping Detected Mask	0x1	R/W

Bits	Bit Name	Description	Reset	Access
26	IRQ_FDSP10_CLIP_MASK	FDSP Channel 10 Clipping Detected Mask	0x1	R/W
25	IRQ_FDSP9_CLIP_MASK	FDSP Channel 9 Clipping Detected Mask	0x1	R/W
24	IRQ_FDSP8_CLIP_MASK	FDSP Channel 8 Clipping Detected Mask	0x1	R/W
23	IRQ_FDSP7_CLIP_MASK	FDSP Channel 7 Clipping Detected Mask	0x1	R/W
22	IRQ_FDSP6_CLIP_MASK	FDSP Channel 6 Clipping Detected Mask	0x1	R/W
21	IRQ_FDSP5_CLIP_MASK	FDSP Channel 5 Clipping Detected Mask	0x1	R/W
20	IRQ_FDSP4_CLIP_MASK	FDSP Channel 4 Clipping Detected Mask	0x1	R/W
19	IRQ_FDSP3_CLIP_MASK	FDSP Channel 3 Clipping Detected Mask	0x1	R/W
18	IRQ_FDSP2_CLIP_MASK	FDSP Channel 2 Clipping Detected Mask	0x1	R/W
17	IRQ_FDSP1_CLIP_MASK	FDSP Channel 1 Clipping Detected Mask	0x1	R/W
16	IRQ_FDSP0_CLIP_MASK	FDSP Channel 0 Clipping Detected Mask	0x1	R/W
[15:14]	RESERVED	Reserved	0x0	R
13	IRQ_HIFI_DOUBLEEXCEPTIONERROR_MASK	Mask HiFi Double Exception Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
12	IRQ_HIFI4_MASK	Mask HiFi DSP Register Interrupt 4 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
11	IRQ_HIFI3_MASK	Mask HiFi DSP Register Interrupt 3 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
10	IRQ_HIFI2_MASK	Mask HiFi DSP Register Interrupt 2 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
9	IRQ_HIFI1_MASK	Mask HiFi DSP Register Interrupt 1 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
8	IRQ_HIFI0_MASK	Mask HiFi DSP Register Interrupt 0 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
[7:6]	RESERVED	Reserved	0x0	R
5	IRQ_HPVDD_UVW_MASK	Mask HPVDD Undervoltage Warning 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
4	RESERVED	Reserved	0x0	R
3	IRQ_DAC0_CLIP_MASK	Mask DAC Channel 0 Clipping 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
2	IRQ_ADC2_CLIP_MASK	Mask ADC Channel 2 Clipping 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
1	IRQ_ADC1_CLIP_MASK	Mask ADC Channel 1 Clipping 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
0	IRQ_ADC0_CLIP_MASK	Mask ADC Channel 0 Clipping 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

SYSTEM IRQ[N] MASKING REGISTER

Address: 0xF0000340 to 0xF00003A0 (Increments of 12), Reset: 0x9FF3113F, Name: IRQn_MASK3

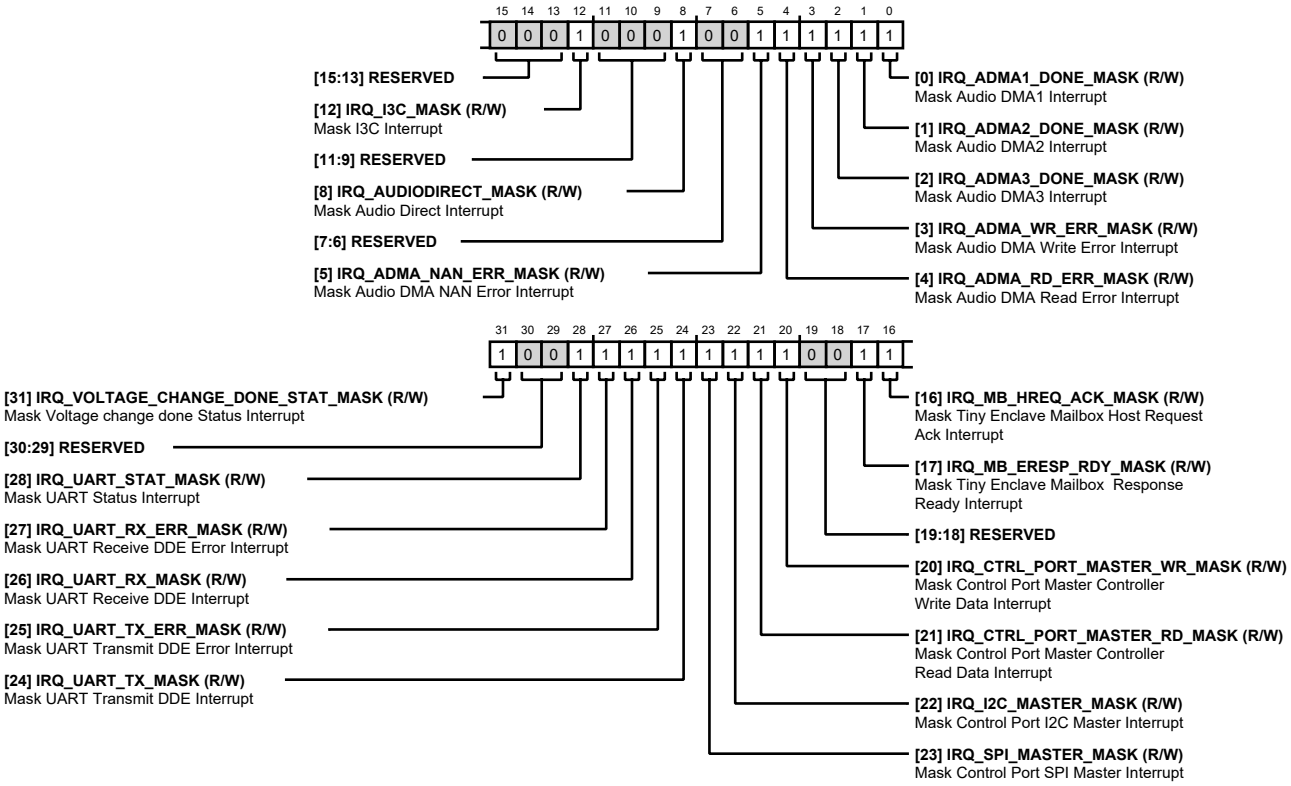


Table 231. Bit Descriptions for IRQn_MASK3

Bits	Bit Name	Description	Reset	Access
31	IRQ_VOLTAGE_CHANGE_DONE_STAT_MASK	Mask Voltage change done Status Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
[30:29]	RESERVED	Reserved.	0x0	R
28	IRQ_UART_STAT_MASK	Mask UART Status Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
27	IRQ_UART_RX_ERR_MASK	Mask UART Receive DDE Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
26	IRQ_UART_RX_MASK	Mask UART Receive DDE Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
25	IRQ_UART_TX_ERR_MASK	Mask UART Transmit DDE Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
24	IRQ_UART_TX_MASK	Mask UART Transmit DDE Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
23	IRQ_SPI_MASTER_MASK	Mask Control Port SPI Master Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
22	IRQ_I2C_MASTER_MASK	Mask Control Port I^2C Master Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
21	IRQ_CTRL_PORT_MASTER_RD_MASK	Mask Control Port Master Controller Read Data Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
20	IRQ_CTRL_PORT_MASTER_WR_MASK	Mask Control Port Master Controller Write Data Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
[19:13]	RESERVED	Reserved.	0x0	R
12	IRQ_I3C_MASK	Mask I3C Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
[11:9]	RESERVED	Reserved	0x0	R
8	IRQ_AUDIODIRECT_MASK	Mask Audio Direct Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
[7:6]	RESERVED	Reserved	0x0	R
5	IRQ_ADMA_NAN_ERR_MASK	Mask Audio DMA NAN Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
4	IRQ_ADMA_RD_ERR_MASK	Mask Audio DMA Read Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
3	IRQ_ADMA_WR_ERR_MASK	Mask Audio DMA Write Error Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
2	IRQ_ADMA3_DONE_MASK	Mask Audio DMA3 Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
1	IRQ_ADMA2_DONE_MASK	Mask Audio DMA2 Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W
0	IRQ_ADMA1_DONE_MASK	Mask Audio DMA1 Interrupt 0: Event causes IRQ. 1: Event masked and does not cause IRQ.	0x1	R/W

SYSTEM IRQ CLEAR 1 REGISTER

Address: 0xF00003A4, Reset: 0x00000000, Name: IRQ_CLR1

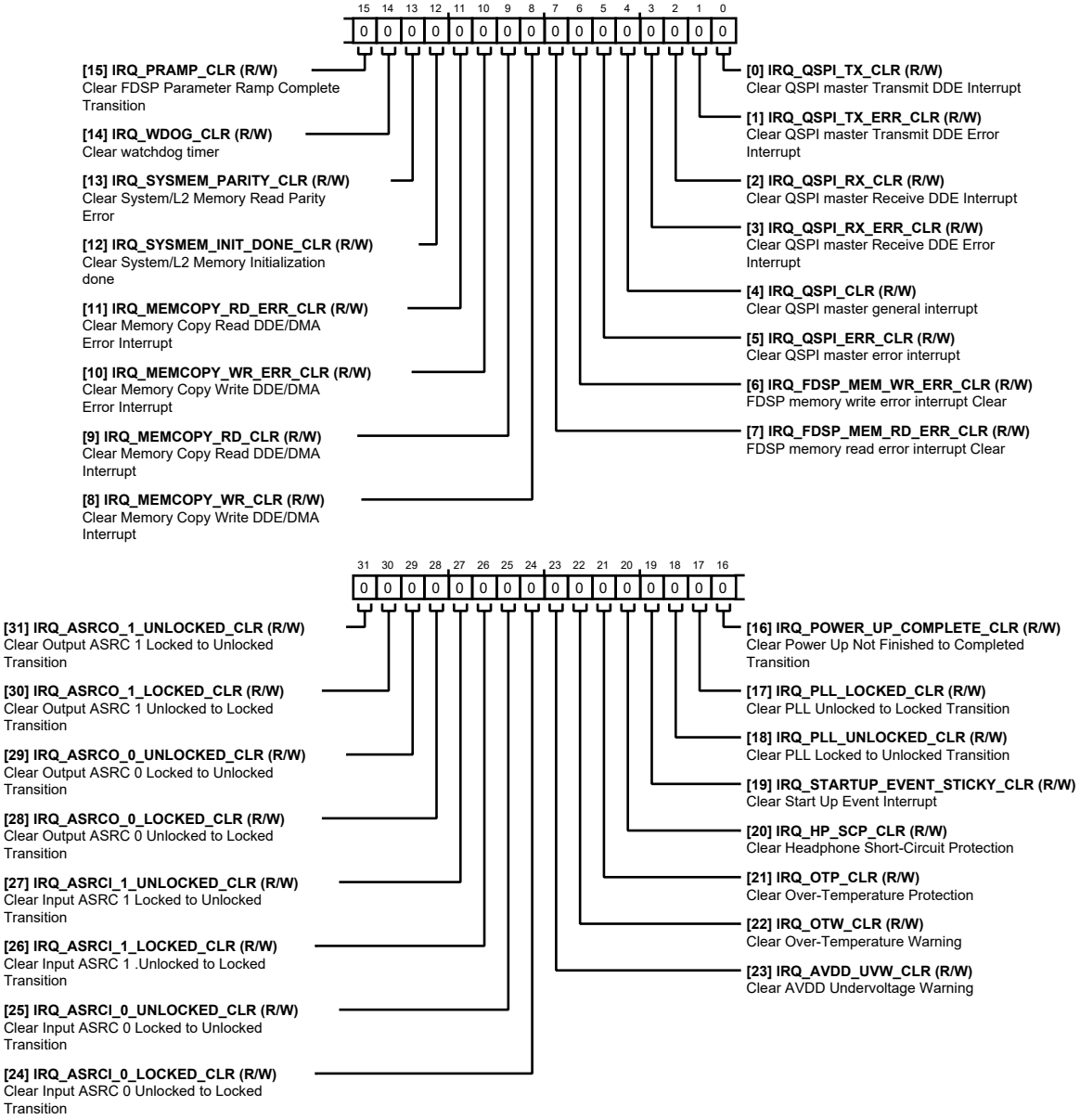


Table 232. Bit Descriptions for IRQ_CLR1

Bits	Bit Name	Description	Reset	Access
31	IRQ_ASRCO_1_UNLOCKED_CLR	Clear Output ASRC 1 Locked to Unlocked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
30	IRQ_ASRCO_1_LOCKED_CLR	Clear Output ASRC 1 Unlocked to Locked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
29	IRQ_ASRCO_0_UNLOCKED_CLR	Clear Output ASRC 0 Locked to Unlocked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
28	IRQ_ASRCO_0_LOCKED_CLR	Clear Output ASRC 0 Unlocked to Locked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
27	IRQ_ASRCI_1_UNLOCKED_CLR	Clear Input ASRC 1 Locked to Unlocked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
26	IRQ_ASRCI_1_LOCKED_CLR	Clear Input ASRC 1. Unlocked to Locked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
25	IRQ_ASRCI_0_UNLOCKED_CLR	Clear Input ASRC 0 Locked to Unlocked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
24	IRQ_ASRCI_0_LOCKED_CLR	Clear Input ASRC 0 Unlocked to Locked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
23	IRQ_AVDD_UVW_CLR	Clear AVDD Undervoltage Warning 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
22	IRQ_OTW_CLR	Clear Over-Temperature Warning 0: Keep Interrupt Status. 1: Clear Interrupt Status.	0x0	R/W
21	IRQ_OTP_CLR	Clear Over-Temperature Protection. 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
20	IRQ_HP_SCP_CLR	Clear Headphone Short-Circuit Protection 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
19	IRQ_STARTUP_EVENT_STICKY_CLR	Clear Start-Up Event Interrupt 1: Clear Interrupt Status. 0: Keep Interrupt Status.	0x0	R/W
18	IRQ_PLL_UNLOCKED_CLR	Clear PLL Locked to Unlocked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

Bits	Bit Name	Description	Reset	Access
17	IRQ_PLL_LOCKED_CLR	Clear PLL Unlocked to Locked Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
16	IRQ_POWER_UP_COMPLETE_CLR	Clear Power-Up Not Finished to Completed Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
15	IRQ_PRAMP_CLR	Clear FDSP Parameter Ramp Complete Transition 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
14	IRQ_WDOG_CLR	Clear Watchdog Timer 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
13	IRQ_SYSMEM_PARITY_CLR	Clear System/L2 Memory Read Parity Error 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
12	IRQ_SYSMEM_INIT_DONE_CLR	Clear System/L2 Memory Initialization done 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
11	IRQ_MEMCOPY_RD_ERR_CLR	Clear Memory Copy Read DDE/DMA Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
10	IRQ_MEMCOPY_WR_ERR_CLR	Clear Memory Copy Write DDE/DMA Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
9	IRQ_MEMCOPY_RD_CLR	Clear Memory Copy Read DDE/DMA Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
8	IRQ_MEMCOPY_WR_CLR	Clear Memory Copy Write DDE/DMA Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
7	IRQ_FDSP_MEM_RD_ERR_CLR	FDSP Memory Read Error Interrupt Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
6	IRQ_FDSP_MEM_WR_ERR_CLR	FDSP memory write error interrupt Clear. 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
5	IRQ_QSPI_ERR_CLR	Clear QSPI Master Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
4	IRQ_QSPI_CLR	Clear QSPI Master General Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

Bits	Bit Name	Description	Reset	Access
3	IRQ_QSPI_RX_ERR_CLR	Clear QSPI Master Receive DDE Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
2	IRQ_QSPI_RX_CLR	Clear QSPI Master Receive DDE Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
1	IRQ_QSPI_TX_ERR_CLR	Clear QSPI Master Transmit DDE Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
0	IRQ_QSPI_TX_CLR	Clear QSPI Master Transmit DDE Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

SYSTEM IRQ CLEAR 2 REGISTER

Address: 0xF00003A8, Reset: 0x00000000, Name: IRQ_CLR2

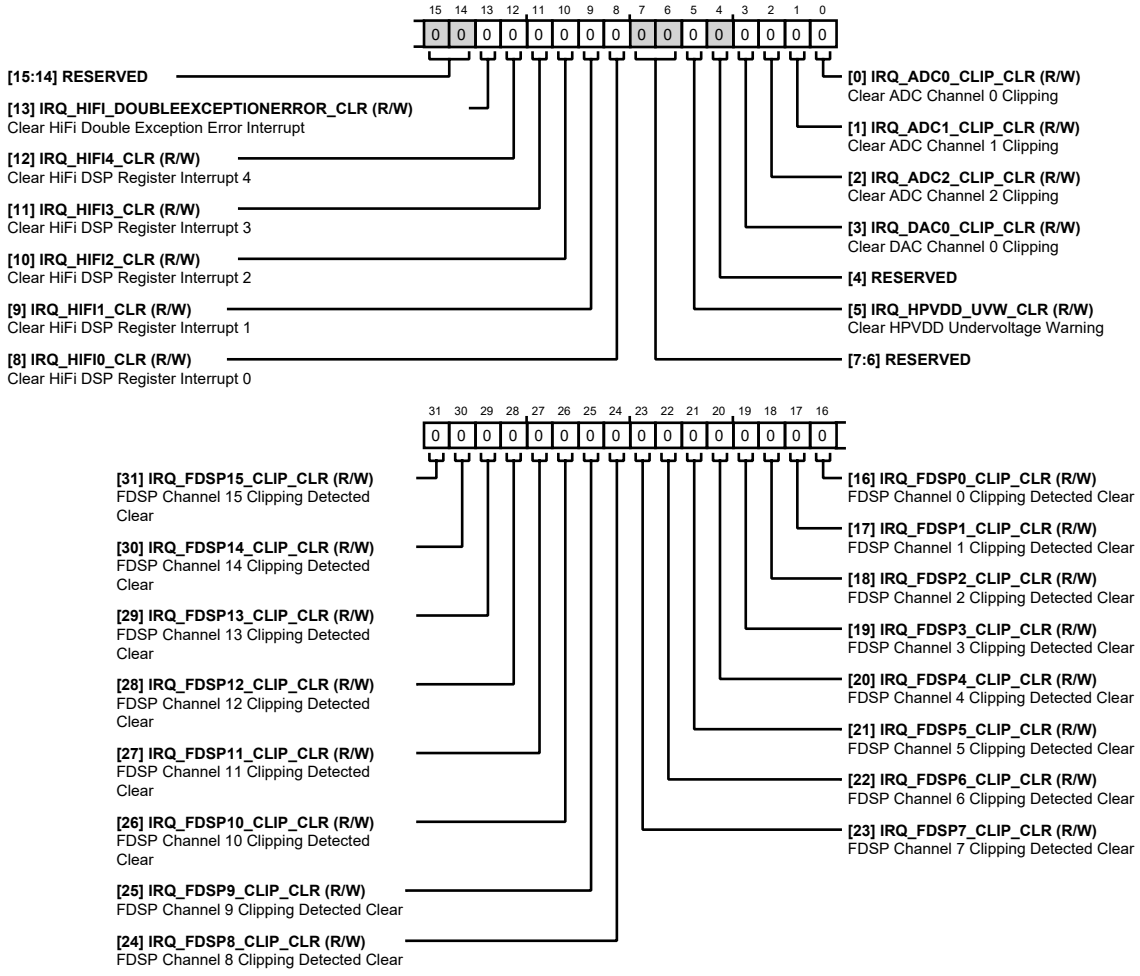


Table 233. Bit Descriptions for IRQ_CLR2

Bits	Bit Name	Description	Reset	Access
31	IRQ_FDSP15_CLIP_CLR	FDSP Channel 15 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
30	IRQ_FDSP14_CLIP_CLR	FDSP Channel 14 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
29	IRQ_FDSP13_CLIP_CLR	FDSP Channel 13 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
28	IRQ_FDSP12_CLIP_CLR	FDSP Channel 12 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
27	IRQ_FDSP11_CLIP_CLR	FDSP Channel 11 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
26	IRQ_FDSP10_CLIP_CLR	FDSP Channel 10 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
25	IRQ_FDSP9_CLIP_CLR	FDSP Channel 9 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
24	IRQ_FDSP8_CLIP_CLR	FDSP Channel 8 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
23	IRQ_FDSP7_CLIP_CLR	FDSP Channel 7 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
22	IRQ_FDSP6_CLIP_CLR	FDSP Channel 6 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
21	IRQ_FDSP5_CLIP_CLR	FDSP Channel 5 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
20	IRQ_FDSP4_CLIP_CLR	FDSP Channel 4 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
19	IRQ_FDSP3_CLIP_CLR	FDSP Channel 3 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
18	IRQ_FDSP2_CLIP_CLR	FDSP Channel 2 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

Bits	Bit Name	Description	Reset	Access
17	IRQ_FDSP1_CLIP_CLR	FDSP Channel 1 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
16	IRQ_FDSP0_CLIP_CLR	FDSP Channel 0 Clipping Detected Clear 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[15:14]	RESERVED	Reserved.	0x0	R
13	IRQ_HIFI_DOUBLEEXCEPTIONERROR_CLR	Clear HiFi Double Exception Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
12	IRQ_HIFI4_CLR	Clear HiFi DSP Register Interrupt 4 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
11	IRQ_HIFI3_CLR	Clear HiFi DSP Register Interrupt 3 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
10	IRQ_HIFI2_CLR	Clear HiFi DSP Register Interrupt 2 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
9	IRQ_HIFI1_CLR	Clear HiFi DSP Register Interrupt 1 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
8	IRQ_HIFI0_CLR	Clear HiFi DSP Register Interrupt 0 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[7:6]	RESERVED	Reserved.	0x0	R
5	IRQ_HPVDD_UVW_CLR	Clear HPVDD Undervoltage Warning 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
4	RESERVED	Reserved.	0x0	R
3	IRQ_DAC0_CLIP_CLR	Clear DAC Channel 0 Clipping 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
2	IRQ_ADC2_CLIP_CLR	Clear ADC Channel 2 Clipping 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
1	IRQ_ADC1_CLIP_CLR	Clear ADC Channel 1 Clipping 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
0	IRQ_ADC0_CLIP_CLR	Clear ADC Channel 0 Clipping 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

SYSTEM IRQ CLEAR 3 REGISTER

Address: 0xF00003AC, Reset: 0x00000000, Name: IRQ_CLR3

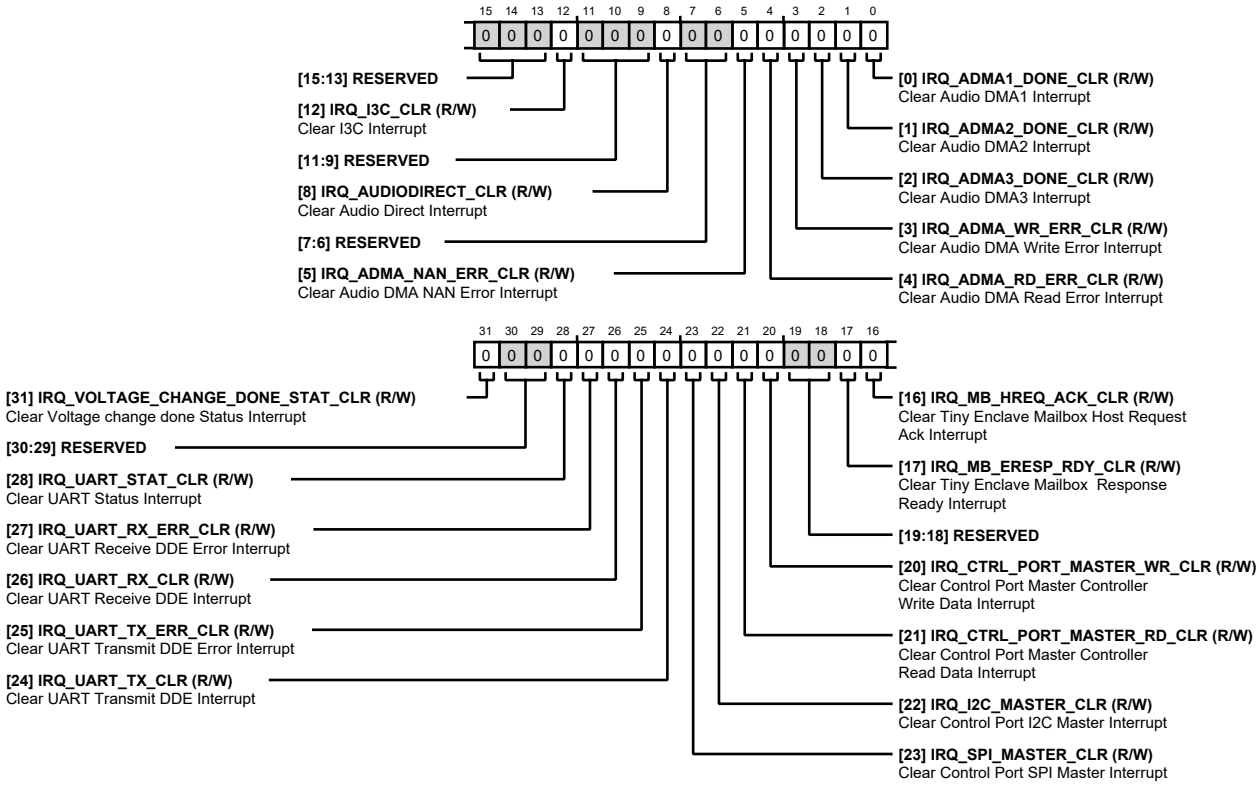


Table 234. Bit Descriptions for IRQ_CLR3

Bits	Bit Name	Description	Reset	Access
31	IRQ_VOLTAGE_CHANGE_DONE_STAT_CLR	Clear Voltage Change Done Status Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[30:29]	RESERVED	Reserved	0x0	R
28	IRQ_UART_STAT_CLR	Clear UART Status Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
27	IRQ_UART_RX_ERR_CLR	Clear UART Receive DDE Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
26	IRQ_UART_RX_CLR	Clear UART Receive DDE Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
25	IRQ_UART_TX_ERR_CLR	Clear UART Transmit DDE Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
24	IRQ_UART_TX_CLR	Clear UART Transmit DDE Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

Bits	Bit Name	Description	Reset	Access
23	IRQ_SPI_MASTER_CLR	Clear Control Port SPI Master Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
22	IRQ_I2C_MASTER_CLR	Clear Control Port I^2C Master Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
21	IRQ_CTRL_PORT_MASTER_RD_CLR	Clear Control Port Master Controller Read Data Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
20	IRQ_CTRL_PORT_MASTER_WR_CLR	Clear Control Port Master Controller Write Data Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[19:13]	RESERVED	Reserved.	0x0	R
12	IRQ_I3C_CLR	Clear I^3C Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[11:9]	RESERVED	Reserved	0x0	R
8	IRQ_AUDIODIRECT_CLR	Clear Audio Direct Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
[7:6]	RESERVED	Reserved.	0x0	R
5	IRQ_ADMA_NAN_ERR_CLR	Clear Audio DMA NAN Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
4	IRQ_ADMA_RD_ERR_CLR	Clear Audio DMA Read Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
3	IRQ_ADMA_WR_ERR_CLR	Clear Audio DMA Write Error Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
2	IRQ_ADMA3_DONE_CLR	Clear Audio DMA3 Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
1	IRQ_ADMA2_DONE_CLR	Clear Audio DMA2 Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W
0	IRQ_ADMA1_DONE_CLR	Clear Audio DMA1 Interrupt 0: Keep Interrupt Status 1: Clear Interrupt Status	0x0	R/W

CHIP RESETS REGISTER

Address: 0xF0000400, Reset: 0x00000000, Name: RESETS

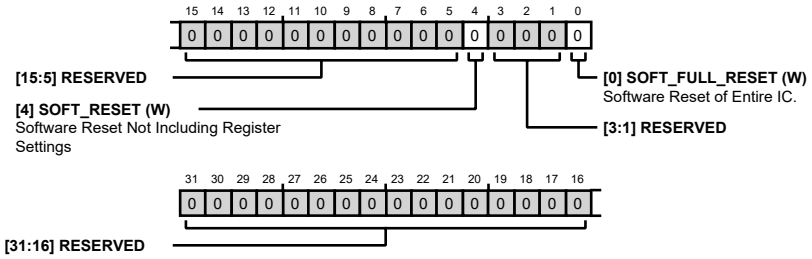


Table 235. Bit Descriptions for RESETS

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	SOFT_RESET	Software Reset Not Including Register Settings 0: Not applicable. 1: Write 1 once to soft reset.	0x0	W
[3:1]	RESERVED	Reserved	0x0	R
0	SOFT_FULL_RESET	Software Reset of Entire IC 0: Not applicable. 1: Write 1 once to soft full reset.	0x0	W

FASTDSP CURRENT LAMBDA REGISTER

Address: 0xF0000404, Reset: 0x0000003F, Name: FDSP_STATUS

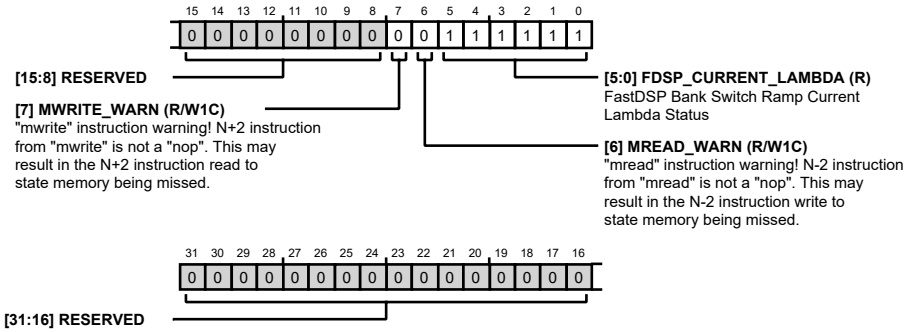


Table 236. Bit Descriptions for FDSP_STATUS

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	MWRITE_WARN	"mwrite" instruction warning! N+2 instruction from "mwrite" is not a "nop". This may result in the N+2 instruction read-to-state memory being missed.	0x0	R/W1C
6	MREAD_WARN	"mread" instruction warning! N-2 instruction from "mread" is not a "nop". This may result in the N-2 instruction write-to-state memory being missed.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
[5:0]	FDSP_CURRENT_LAMBDA	FastDSP Bank Switch Ramp Current Lambda Status. Lambda is a 6-bit value representing the point along the linear interpolation curve between two banks at which the bank ramp switch stops. Where A represents coefficient values in the source bank and B represents coefficient values in the destination bank: 0 = ((63/64) x A + (1/64) x B), 1 = ((62/64) x A + (2/64) x B), …, 62 = ((1/64) x A + (63/64) x B), 63 = B (default) Lambda can be updated "on the fly" via control interface. To complete a bank switch, a value of 63 (default setting) must be set. Actual current ramp point (current_lambda: 0-63) can be read via a status register. When this reaches 63, the bank switch is complete, and the current parameters used match the current bank. Actual step size of linear interpolation will be ~12 bits (4096 steps). Parameters in banks being ramped between should not change during a bank switch. 0: Bank switch parameter ramp is at 1/64 of full ramp. 1: Bank switch parameter ramp is at 2/64 of full ramp. 62: Bank switch parameter ramp is at 63/64 of full ramp. 63: Bank switch parameter ramp is complete.	0x3F	R

CHIP STATUS 1 REGISTER

Address: 0xF0000408, Reset: 0x00000000, Name: STATUS1

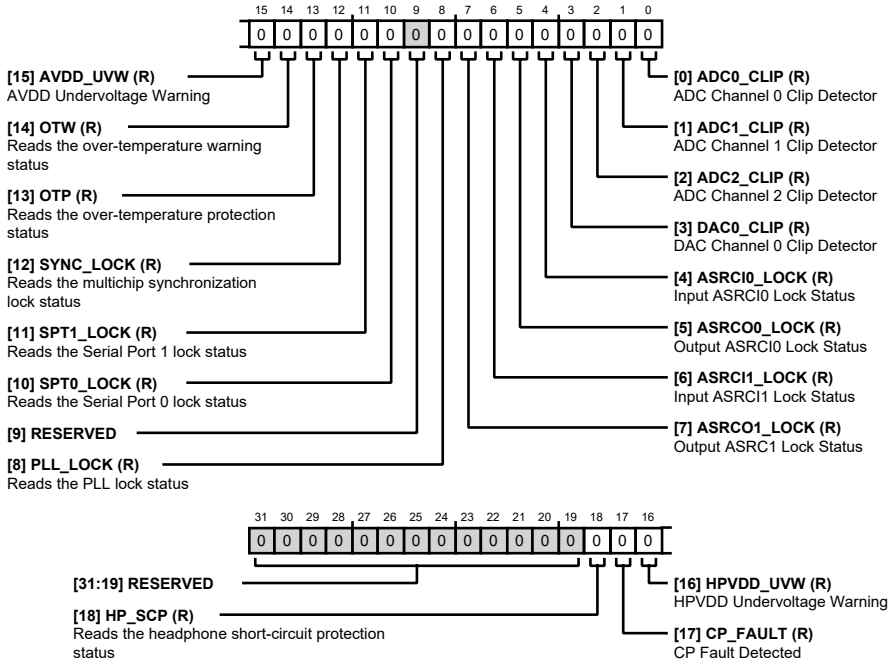


Table 237. Bit Descriptions for STATUS1

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved	0x0	R
18	HP_SCP	Reads the headphone short-circuit protection status. 0: Normal Operation 1: Condition Detected	0x0	R

Bits	Bit Name	Description	Reset	Access
17	CP_FAULT	CP Fault Detected 0: Normal Operation 1: Undervoltage on AVDD Detected	0x0	R
16	HPVDD_UVW	HPVDD Undervoltage Warning 0: Normal Operation 1: Undervoltage on AVDD Detected	0x0	R
15	AVDD_UVW	AVDD Undervoltage Warning 0: Normal Operation 1: Undervoltage on AVDD Detected	0x0	R
14	OTW	Reads the over-temperature warning status. 0: Normal Operation 1: Condition Detected	0x0	R
13	OTP	Reads the over-temperature protection status. 0: Normal Operation 1: Condition Detected	0x0	R
12	SYNC_LOCK	Reads the multichip synchronization lock status. 0: Sync source unlocked. 1: Sync source locked.	0x0	R
11	SPT1_LOCK	Reads the Serial Port 1 lock status. 0: SPT1 synchronization unlocked. 1: SPT1 synchronization locked.	0x0	R
10	SPT0_LOCK	Reads the Serial Port 0 lock status. 0: SPT0 synchronization unlocked. 1: SPT0 synchronization locked.	0x0	R
9	RESERVED	Reserved	0x0	R
8	PLL_LOCK	Reads the PLL Lock Status 0: PLL is not locked. 1: PLL is locked.	0x0	R
7	ASRCO1_LOCK	Output ASRC1 Lock Status 0: ASRC currently unlocked. 1: ASRC currently locked.	0x0	R
6	ASRCI1_LOCK	Input ASRCI1 Lock Status 0: ASRC currently unlocked. 1: ASRC currently locked.	0x0	R
5	ASRCO0_LOCK	Output ASRCI0 Lock Status 0: ASRC currently unlocked. 1: ASRC currently locked.	0x0	R
4	ASRCI0_LOCK	Input ASRCI0 Lock Status 0: ASRC currently unlocked. 1: ASRC currently locked.	0x0	R
3	DAC0_CLIP	DAC Channel 0 Clip Detector 0: Normal Operation 1: Clipping Detected	0x0	R

Bits	Bit Name	Description	Reset	Access
2	ADC2_CLIP	ADC Channel 2 Clip Detector 0: Normal Operation 1: Amplifier Clipping Detected	0x0	R
1	ADC1_CLIP	ADC Channel 1 Clip Detector 0: Normal Operation 1: Amplifier Clipping Detected	0x0	R
0	ADC0_CLIP	ADC Channel 0 Clip Detector 0: Normal Operation 1: Amplifier Clipping Detected	0x0	R

DIGITAL POWER SUPPLY STATUS REGISTER

Address: 0xF000040C, Reset: 0x00000000, Name: DVDD_STATUS

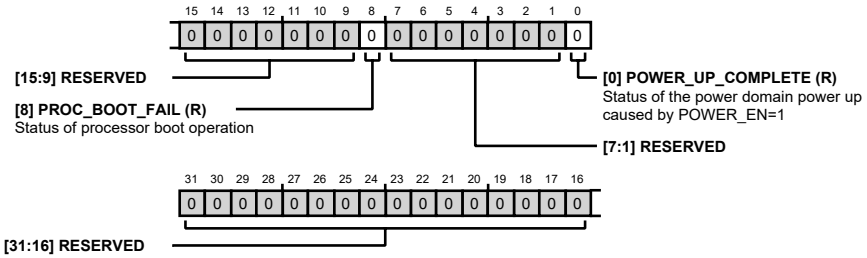


Table 238. Bit Descriptions for DVDD_STATUS

Bits	Bit Name	Description	Reset	Access
[31:9]	RESERVED	Reserved	0x0	R
8	PROC_BOOT_FAIL	Status of processor boot operation.	0x0	R
[7:1]	RESERVED	Reserved	0x0	R
0	POWER_UP_COMPLETE	Status of the power domain power-up caused by POWER_EN = 1. 0: Power-up not yet complete. 1: Power-up is complete.	0x0	R

GENERAL-PURPOSE INPUT READ 0 TO INPUT READ 31 REGISTER

Address: 0xF0000414, Reset: 0x00000000, Name: GPI1

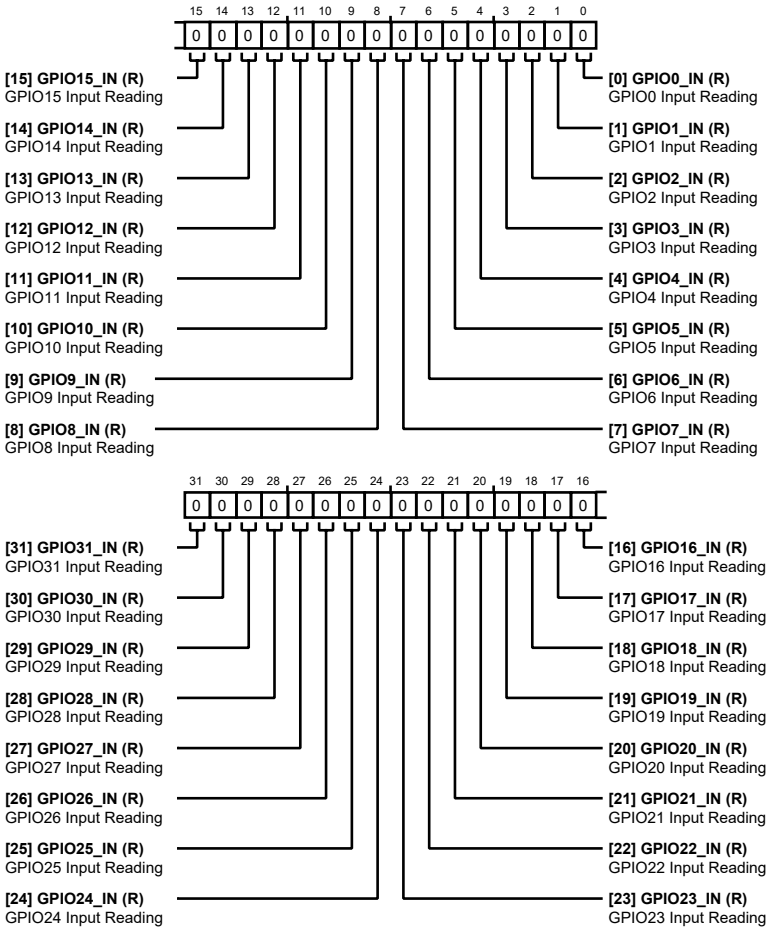


Table 239. Bit Descriptions for GPI1

Bits	Bit Name	Description	Reset	Access
31	GPIO31_IN	GPIO31 Input Reading 0: MP31 (set as GPIO 31) is low. 1: MP31 (set as GPIO 31) is high.	0x0	R
30	GPIO30_IN	GPIO30 Input Reading 0: MP30 (set as GPIO 30) is low. 1: MP30 (set as GPIO 30) is high.	0x0	R
29	GPIO29_IN	GPIO29 Input Reading 0: MP29 (set as GPIO 29) is low. 1: MP29 (set as GPIO 29) is high.	0x0	R
28	GPIO28_IN	GPIO28 Input Reading 0: MP28 (set as GPIO 28) is low. 1: MP28 (set as GPIO 28) is high.	0x0	R
27	GPIO27_IN	GPIO27 Input Reading 0: MP27 (set as GPIO 27) is low. 1: MP27 (set as GPIO 27) is high.	0x0	R

Bits	Bit Name	Description	Reset	Access
26	GPIO26_IN	GPIO26 Input Reading 0: MP26 (set as GPIO 26) is low. 1: MP26 (set as GPIO 26) is high.	0x0	R
25	GPIO25_IN	GPIO25 Input Reading 0: MP25 (set as GPIO 25) is low. 1: MP25 (set as GPIO 25) is high.	0x0	R
24	GPIO24_IN	GPIO24 Input Reading 0: MP24 (set as GPIO 24) is low. 1: MP24 (set as GPIO 24) is high.	0x0	R
23	GPIO23_IN	GPIO23 Input Reading 0: MP23 (set as GPIO 23) is low. 1: MP23 (set as GPIO 23) is high.	0x0	R
22	GPIO22_IN	GPIO22 Input Reading 0: MP22 (set as GPIO 22) is low. 1: MP22 (set as GPIO 22) is high.	0x0	R
21	GPIO21_IN	GPIO21 Input Reading 0: MP21 (set as GPIO 21) is low. 1: MP21 (set as GPIO 21) is high.	0x0	R
20	GPIO20_IN	GPIO20 Input Reading 0: MP20 (set as GPIO 20) is low. 1: MP20 (set as GPIO 20) is high.	0x0	R
19	GPIO19_IN	GPIO19 Input Reading 0: MP19 (set as GPIO 19) is low. 1: MP19 (set as GPIO 19) is high.	0x0	R
18	GPIO18_IN	GPIO18 Input Reading 0: MP18 (set as GPIO 18) is low. 1: MP18 (set as GPIO 18) is high.	0x0	R
17	GPIO17_IN	GPIO17 Input Reading 0: MP17 (set as GPIO 17) is low. 1: MP17 (set as GPIO 17) is high.	0x0	R
16	GPIO16_IN	GPIO16 Input Reading 0: MP16 (set as GPIO 16) is low. 1: MP16 (set as GPIO 16) is high.	0x0	R
15	GPIO15_IN	GPIO15 Input Reading 0: MP15 (set as GPIO 15) is low. 1: MP15 (set as GPIO 15) is high.	0x0	R
14	GPIO14_IN	GPIO14 Input Reading 0: MP14 (set as GPIO 14) is low. 1: MP14 (set as GPIO 14) is high.	0x0	R
13	GPIO13_IN	GPIO13 Input Reading 0: MP13 (set as GPIO 13) is low. 1: MP13 (set as GPIO 13) is high.	0x0	R

Bits	Bit Name	Description	Reset	Access
12	GPIO12_IN	GPIO12 Input Reading 0: MP12 (set as GPIO 12) is low. 1: MP12 (set as GPIO 12) is high.	0x0	R
11	GPIO11_IN	GPIO11 Input Reading 0: MP11 (set as GPIO 11) is low. 1: MP11 (set as GPIO 11) is high.	0x0	R
10	GPIO10_IN	GPIO10 Input Reading 0: MP10 (set as GPIO10) is low. 1: MP10 (set as GPIO 10) is high.	0x0	R
9	GPIO9_IN	GPIO9 Input Reading 0: MP9 (set as GPIO 9) is low. 1: MP9 (set as GPIO 9) is high.	0x0	R
8	GPIO8_IN	GPIO8 Input Reading 0: MP8 (set as GPIO 8) is low. 1: MP8 (set as GPIO 8) is high.	0x0	R
7	GPIO7_IN	GPIO7 Input Reading 0: MP7 (set as GPIO 7) is low. 1: MP7 (set as GPIO 7) is high.	0x0	R
6	GPIO6_IN	GPIO6 Input Reading 0: MP6 (set as GPIO 6) is low. 1: MP6 (set as GPIO 6) is high.	0x0	R
5	GPIO5_IN	GPIO5 Input Reading 0: MP5 (set as GPIO 5) is low. 1: MP5 (set as GPIO 5) is high.	0x0	R
4	GPIO4_IN	GPIO4 Input Reading 0: MP4 (set as GPIO 4) is low. 1: MP4 (set as GPIO 4) is high.	0x0	R
3	GPIO3_IN	GPIO3 Input Reading 0: MP3 (set as GPIO 3) is low. 1: MP3 (set as GPIO 3) is high.	0x0	R
2	GPIO2_IN	GPIO2 Input Reading 0: MP2 (set as GPIO 2) is low. 1: MP2 (set as GPIO 2) is high.	0x0	R
1	GPIO1_IN	GPIO1 Input Reading 0: MP1 (set as GPIO 1) is low. 1: MP1 (set as GPIO 1) is high.	0x0	R
0	GPIO0_IN	GPIO0 Input Reading 0: MP0 (set as GPIO 0) is low. 1: MP0 (set as GPIO 0) is high.	0x0	R

SYSTEM IRQ STATUS 1 REGISTER

Address: 0xF0000424, Reset: 0x00000000, Name: IRQ_STATUS1

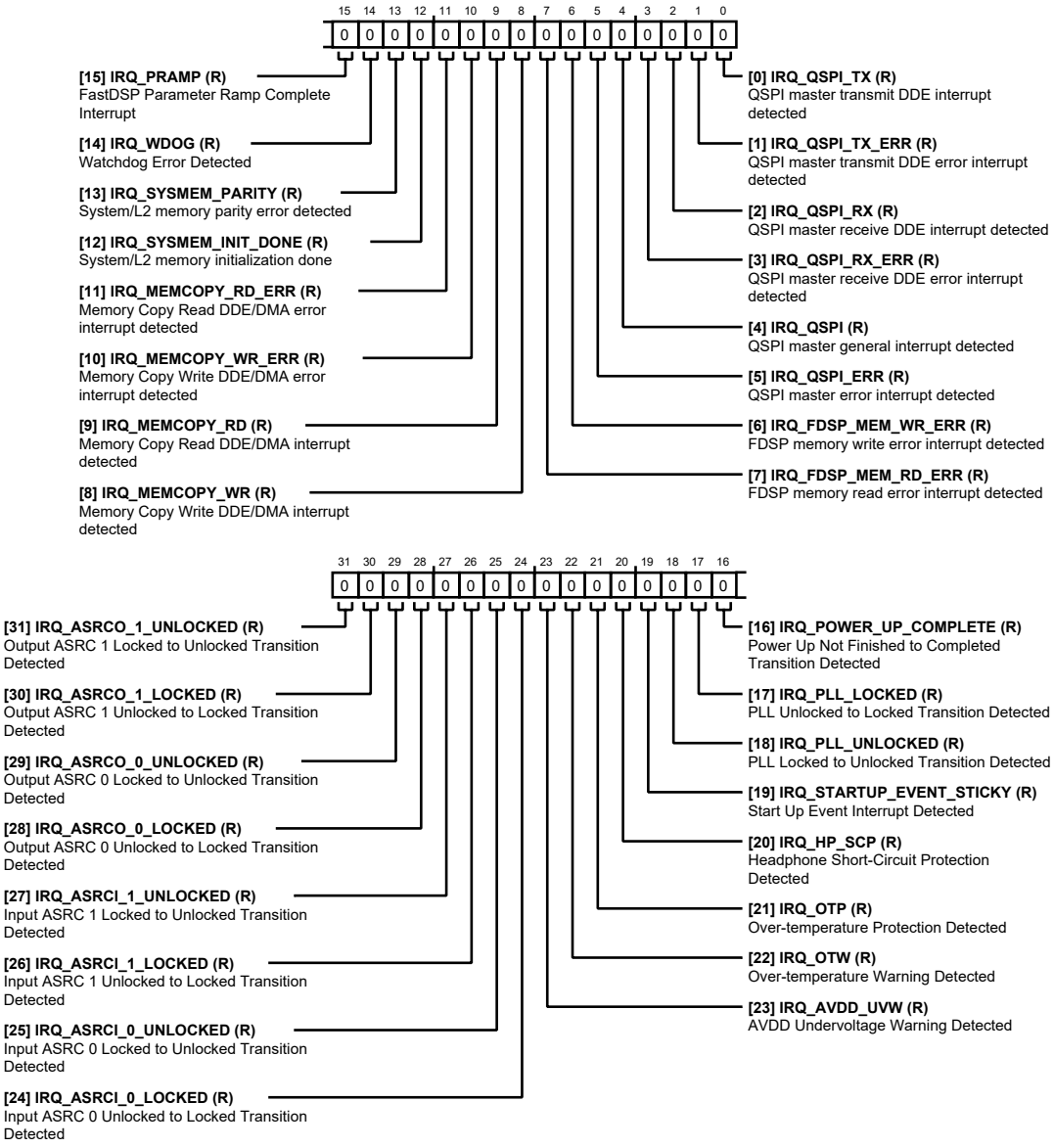


Table 240. Bit Descriptions for IRQ_STATUS1

Bits	Bit Name	Description	Reset	Access
31	IRQ_ASRCO_1_UNLOCKED	Output ASRC 1 Locked to Unlocked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
30	IRQ_ASRCO_1_LOCKED	Output ASRC 1 Unlocked to Locked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
29	IRQ_ASRCO_0_UNLOCKED	Output ASRC 0 Locked to Unlocked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R

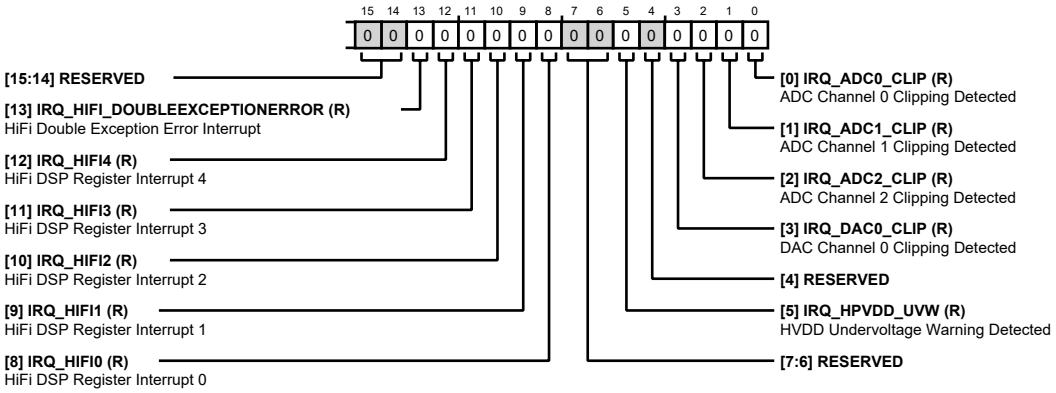
Bits	Bit Name	Description	Reset	Access
28	IRQ_ASRCO_0_LOCKED	Output ASRC 0 Unlocked to Locked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
27	IRQ_ASRCI_1_UNLOCKED	Input ASRC 1 Locked to Unlocked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
26	IRQ_ASRCI_1_LOCKED	Input ASRC 1 Unlocked to Locked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
25	IRQ_ASRCI_0_UNLOCKED	Input ASRC 0 Locked to Unlocked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
24	IRQ_ASRCI_0_LOCKED	Input ASRC 0 Unlocked to Locked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: Unlocked to locked transition detected.	0x0	R
23	IRQ_AVDD_UVW	AVDD Undervoltage Warning Detected 0: Interrupt not triggered. 1: AVDD undervoltage warning detected.	0x0	R
22	IRQ_OTW	Over-Temperature Warning Detected 0: Interrupt not triggered. 1: Over-temperature warning detected.	0x0	R
21	IRQ_OTP	Over-Temperature Protection Detected 0: Interrupt not triggered. 1: Over-temperature protection detected.	0x0	R
20	IRQ_HP_SCP	Headphone Short-Circuit Protection Detected 0: Interrupt not triggered. 1: Headphone Short-Circuit Protection Detected.	0x0	R
19	IRQ_STARTUP_EVENT_STICKY	Start-Up Event Interrupt Detected 0: Interrupt not triggered by power-up complete event. 1: Power-up complete transition detected.	0x0	R
18	IRQ_PLL_UNLOCKED	PLL Locked to Unlocked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: PLL unlocked to locked transition detected.	0x0	R
17	IRQ_PLL_LOCKED	PLL Unlocked to Locked Transition Detected 0: Interrupt not triggered by PLL lock event. 1: PLL unlocked to locked transition detected.	0x0	R
16	IRQ_POWER_UP_COMPLETE	Power-Up Not Finished to Completed Transition Detected 0: Interrupt not triggered by power-up complete event. 1: Power-up complete transition detected.	0x0	R
15	IRQ_PRAMP	FastDSP Parameter Ramp Complete Interrupt 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R

Bits	Bit Name	Description	Reset	Access
14	IRQ_WDOG	Watchdog Error Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
13	IRQ_SYSMEM_PARITY	System/L2 Memory Parity Error Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
12	IRQ_SYSMEM_INIT_DONE	System/L2 Memory Initialization Done 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
11	IRQ_MEMCOPY_RD_ERR	Memory Copy Read DDE/DMA Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
10	IRQ_MEMCOPY_WR_ERR	Memory Copy Write DDE/DMA Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
9	IRQ_MEMCOPY_RD	Memory Copy Read DDE/DMA Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
8	IRQ_MEMCOPY_WR	Memory Copy Write DDE/DMA Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
7	IRQ_FDSP_MEM_RD_ERR	FDSP Memory Read Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
6	IRQ_FDSP_MEM_WR_ERR	FDSP Memory Write Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
5	IRQ_QSPI_ERR	QSPI Master Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
4	IRQ_QSPI	QSPI Master General Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
3	IRQ_QSPI_RX_ERR	QSPI Master Receive DDE Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
2	IRQ_QSPI_RX	QSPI Master Receive DDE Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R

Bits	Bit Name	Description	Reset	Access
1	IRQ_QSPI_TX_ERR	QSPI Master Transmit DDE Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
0	IRQ_QSPI_TX	QSPI Master Transmit DDE Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R

SYSTEM IRQ STATUS 2 REGISTER

Address: 0xF0000428, Reset: 0x00000000, Name: IRQ_STATUS2



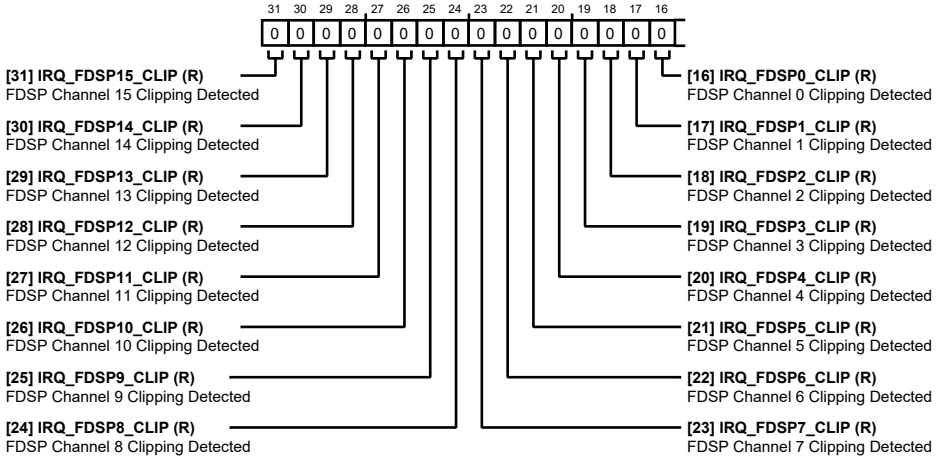


Table 241. Bit Descriptions for IRQ_STATUS2

Bits	Bit Name	Description	Reset	Access
31	IRQ_FDSP15_CLIP	FDSP Channel 15 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
30	IRQ_FDSP14_CLIP	FDSP Channel 14 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R

Bits	Bit Name	Description	Reset	Access
29	IRQ_FDSP13_CLIP	FDSP Channel 13 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
28	IRQ_FDSP12_CLIP	FDSP Channel 12 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
27	IRQ_FDSP11_CLIP	FDSP Channel 11 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
26	IRQ_FDSP10_CLIP	FDSP Channel 10 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
25	IRQ_FDSP9_CLIP	FDSP Channel 9 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
24	IRQ_FDSP8_CLIP	FDSP Channel 8 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
23	IRQ_FDSP7_CLIP	FDSP Channel 7 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
22	IRQ_FDSP6_CLIP	FDSP Channel 6 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
21	IRQ_FDSP5_CLIP	FDSP Channel 5 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
20	IRQ_FDSP4_CLIP	FDSP Channel 4 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
19	IRQ_FDSP3_CLIP	FDSP Channel 3 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
18	IRQ_FDSP2_CLIP	FDSP Channel 2 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
17	IRQ_FDSP1_CLIP	FDSP Channel 1 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
16	IRQ_FDSP0_CLIP	FDSP Channel 0 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
[15:14]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
13	IRQ_HIFI_DOUBLEEXCEPTIONERROR	HiFi Double Exception Error Interrupt 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
12	IRQ_HIFI4	HiFi DSP Register Interrupt 4 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
11	IRQ_HIFI3	HiFi DSP Register Interrupt 3 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
10	IRQ_HIFI2	HiFi DSP Register Interrupt 2 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
9	IRQ_HIFI1	HiFi DSP Register Interrupt 1 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
8	IRQ_HIFI0	HiFi DSP Register Interrupt 0 0: Interrupt not triggered. 1: Interrupt triggered.	0x0	R
[7:6]	RESERVED	Reserved	0x0	R
5	IRQ_HPVDD_UVW	HVDD Undervoltage Warning Detected 0: Interrupt not triggered. 1: AVDD undervoltage warning detected.	0x0	R
4	RESERVED	Reserved	0x0	R
3	IRQ_DAC0_CLIP	DAC Channel 0 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
2	IRQ_ADC2_CLIP	ADC Channel 2 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
1	IRQ_ADC1_CLIP	ADC Channel 1 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R
0	IRQ_ADC0_CLIP	ADC Channel 0 Clipping Detected 0: Interrupt not triggered. 1: Clipping detected.	0x0	R

SYSTEM IRQ STATUS 3 REGISTER

Address: 0xF000042C, Reset: 0x00000000, Name: IRQ_STATUS3

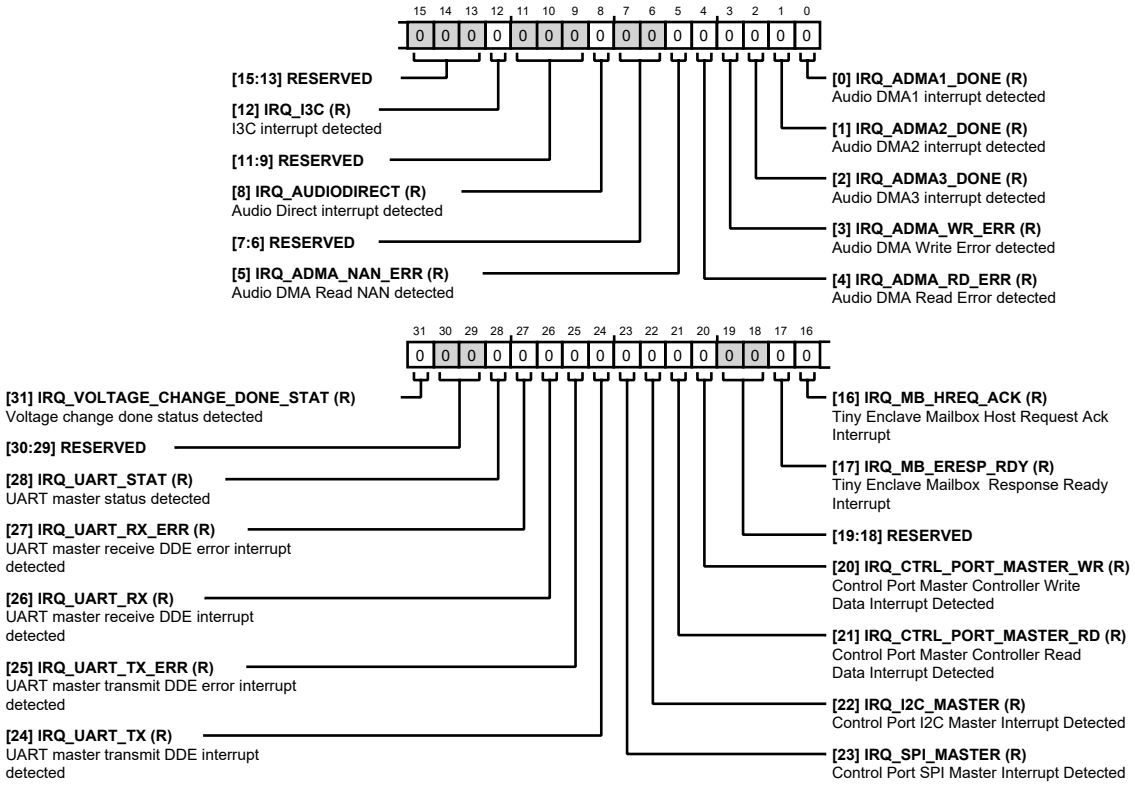


Table 242. Bit Descriptions for IRQ_STATUS3

Bits	Bit Name	Description	Reset	Access
31	IRQ_VOLTAGE_CHANGE_DONE_STAT	Voltage Change Done Status Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
[30:29]	RESERVED	Reserved	0x0	R
28	IRQ_UART_STAT	UART Master Status Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
27	IRQ_UART_RX_ERR	UART Master Receive DDE Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
26	IRQ_UART_RX	UART Master Receive DDE Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
25	IRQ_UART_TX_ERR	UART Master Transmit DDE Error Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
24	IRQ_UART_TX	UART Master Transmit DDE Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R

Bits	Bit Name	Description	Reset	Access
23	IRQ_SPI_MASTER	Control Port SPI Master Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
22	IRQ_I2C_MASTER	Control Port I^2C Master Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
21	IRQ_CTRL_PORT_MASTER_RD	Control Port Master Controller Read Data Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
20	IRQ_CTRL_PORT_MASTER_WR	Control Port Master Controller Write Data Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
[19:13]	RESERVED	Reserved	0x0	R
12	IRQ_I3C	I^3C Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
[11:9]	RESERVED	Reserved	0x0	R
8	IRQ_AUDIODIRECT	Audio Direct Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
[7:6]	RESERVED	Reserved.	0x0	R
5	IRQ_ADMA_NAN_ERR	Audio DMA Read NAN Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
4	IRQ_ADMA_RD_ERR	Audio DMA Read Error Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
3	IRQ_ADMA_WR_ERR	Audio DMA Write Error Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
2	IRQ_ADMA3_DONE	Audio DMA3 Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
1	IRQ_ADMA2_DONE	Audio DMA2 Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R
0	IRQ_ADMA1_DONE	Audio DMA1 Interrupt Detected 0: Interrupt not triggered. 1: Interrupt detected.	0x0	R

SERIAL PORT 0 CONTROL 1 REGISTER

Address: 0xF0000500, Reset: 0x00000000, Name: SPT0_CTRL1

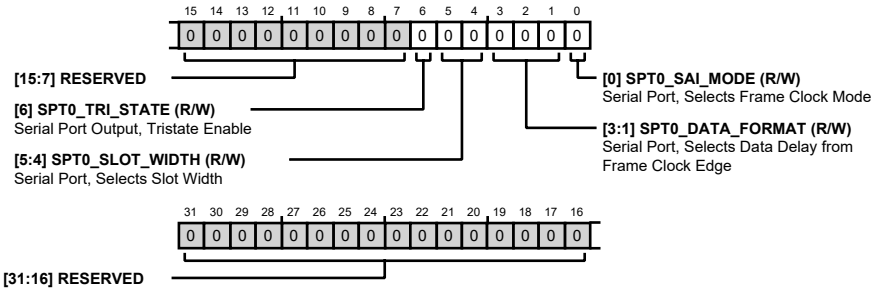


Table 243. Bit Descriptions for SPT0_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	SPT0_TRI_STATE	Serial Port Output, Tristate Enable 1: Tristate Enable 0: Tristate Disable	0x0	R/W
[5:4]	SPT0_SLOT_WIDTH	Serial Port, Selects Slot Width 00: 32 BCLKs per Slot 01: 16 BCLKs per Slot 10: 24 BCLKs per Slot	0x0	R/W
[3:1]	SPT0_DATA_FORMAT	Serial Port, Selects Data Delay from Frame Clock Edge 001: Left-Justified, Delay by 0 000: Typical I^2S Mode, Delay by 1 010: Delay by 8 011: Delay by 12 100: Delay by 16	0x0	R/W
0	SPT0_SAI_MODE	Serial Port, Selects Frame Clock Mode 0: Stereo. 50% duty cycle frame clock (I^2S, left-justified, or right-justified). 1: TDM. Frame clock is single bit clock wide pulse.	0x0	R/W

SERIAL PORT 0 CONTROL 2 REGISTER

Address: 0xF0000504, Reset: 0x00000000, Name: SPT0_CTRL2

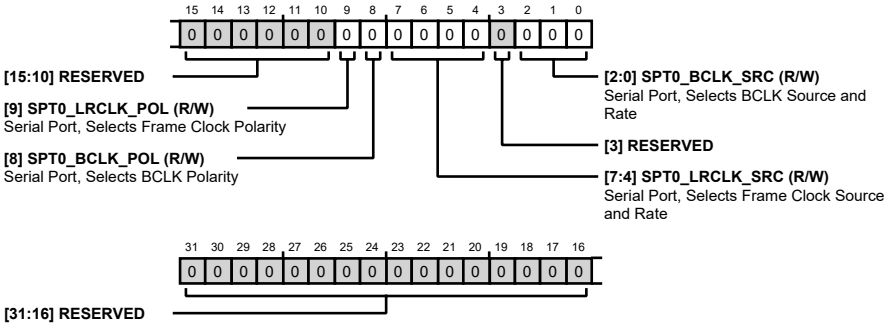


Table 244. Bit Descriptions for SPT0_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	SPT0_LRCLK_POL	Serial Port, Selects Frame Clock Polarity 0: Normal Polarity 1: Inverted Polarity	0x0	R/W
8	SPT0_BCLK_POL	Serial Port, Selects BCLK Polarity 0: Captured on rising edge. 1: Captured on falling edge.	0x0	R/W
[7:4]	SPT0_LRCLK_SRC	Serial Port, Selects Frame Clock Source and Rate 0000: Frame clock is from external source. 0001: Generates frame clock with 48kHz. 0010: Generates frame clock with 96kHz. 0011: Generates frame clock with 192kHz. 0100: Generates frame clock with 12kHz. 0101: Generates frame clock with 24kHz. 0110: Generates frame clock with 384kHz. 0111: Generates frame clock with 768kHz. 1000: Generates frame clock with 8kHz. 1001: Generates frame clock with 16kHz.	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	SPT0_BCLK_SRC	Serial Port, Selects BCLK Source and Rate 000: BCLK is from external source. 001: Generates BCLK at 3.072MHz. 010: Generates BCLK at 6.144MHz. 011: Generates BCLK at 12.288MHz. 100: Generates BCLK at 24.576MHz.	0x0	R/W

SERIAL PORT 0 OUTPUT ROUTING SLOT 0 (LEFT) REGISTER

Address: 0xF0000508, Reset: 0x00000010, Name: SPT0_ROUTE0

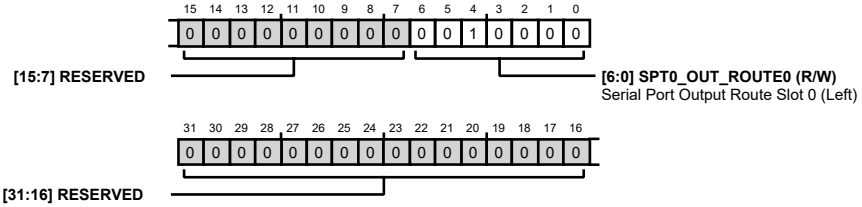


Table 245. Bit Descriptions for SPT0_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE0	Serial Port Output Route Slot 0 (Left) 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1		

Bits	Bit Name	Description	Reset	Access
		0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 1 (RIGHT) REGISTER

Address: 0xF000050C, Reset: 0x00000011, Name: SPT0_ROUTE1

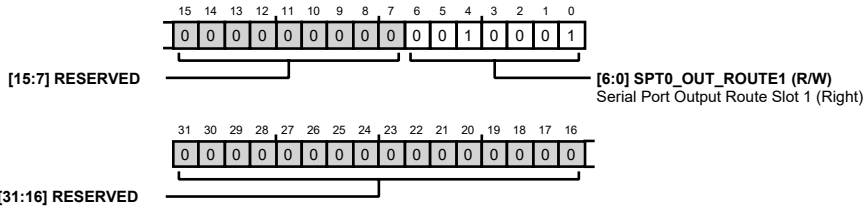


Table 246. Bit Descriptions for SPT0_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE1	Serial Port Output Route Slot 1 (Right) 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4	0x11	R/W

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 2 REGISTER

Address: 0xF0000510, Reset: 0x00000012, Name: SPT0_ROUTE2

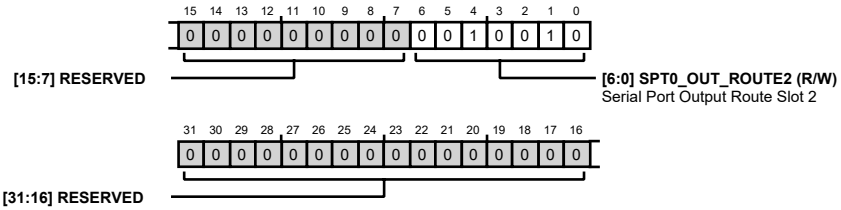


Table 247. Bit Descriptions for SPT0_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE2	Serial Port Output Route Slot 2 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0	0x12	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2		

Bits	Bit Name	Description	Reset	Access
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 3 REGISTER

Address: 0xF0000514, Reset: 0x00000013, Name: SPT0_ROUTE3

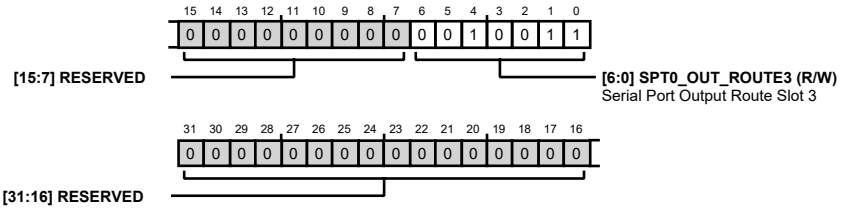


Table 248. Bit Descriptions for SPT0_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE3	Serial Port Output Route Slot 3	0x13	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		
		0000011: FastDSP Channel 3		
		0000100: FastDSP Channel 4		
		0000101: FastDSP Channel 5		
		0000110: FastDSP Channel 6		
		0000111: FastDSP Channel 7		
		0001000: FastDSP Channel 8		

Bits	Bit Name	Description	Reset	Access
		0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6		

Bits	Bit Name	Description	Reset	Access
		0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 4 REGISTER

Address: 0xF0000518, Reset: 0x00000014, Name: SPT0_ROUTE4

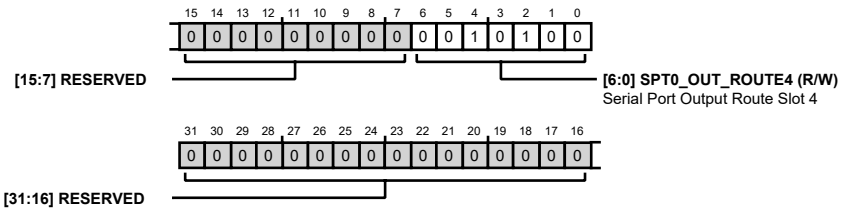


Table 249. Bit Descriptions for SPT0_ROUTE4

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE4	Serial Port Output Route Slot 4 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2	0x14	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12		

Bits	Bit Name	Description	Reset	Access
		1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 5 REGISTER

Address: 0xF000051C, Reset: 0x00000015, Name: SPT0_ROUTE5

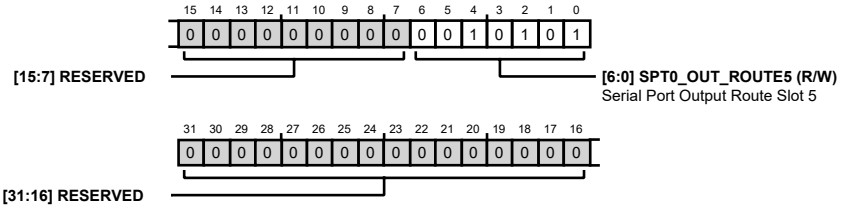


Table 250. Bit Descriptions for SPT0_ROUTE5

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE5	Serial Port Output Route Slot 5 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2	0x15	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 6 REGISTER

Address: 0xF0000520, Reset: 0x00000016, Name: SPT0_ROUTE6

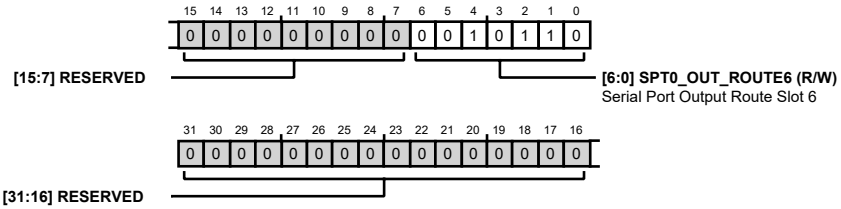


Table 251. Bit Descriptions for SPT0_ROUTE6

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE6	Serial Port Output Route Slot 6 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14	0x16	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4		

Bits	Bit Name	Description	Reset	Access
		0111011: Audio Output DMA 1 Channel 5		
		0111100: Audio Output DMA 1 Channel 6		
		0111101: Audio Output DMA 1 Channel 7		
		0111110: Audio Output DMA 2 Channel 0		
		0111111: Audio Output DMA 2 Channel 1		
		1000000: Audio Output DMA 2 Channel 2		
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 7 REGISTER

Address: 0xF0000524, Reset: 0x00000017, Name: SPT0_ROUTE7

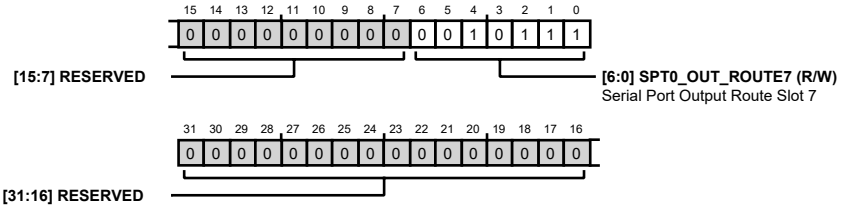


Table 252. Bit Descriptions for SPT0_ROUTE7

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE7	Serial Port Output Route Slot 7	0x17	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		

Bits	Bit Name	Description	Reset	Access
		0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0		

Bits	Bit Name	Description	Reset	Access
		0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 8 REGISTER

Address: 0xF0000528, Reset: 0x00000018, Name: SPT0_ROUTE8

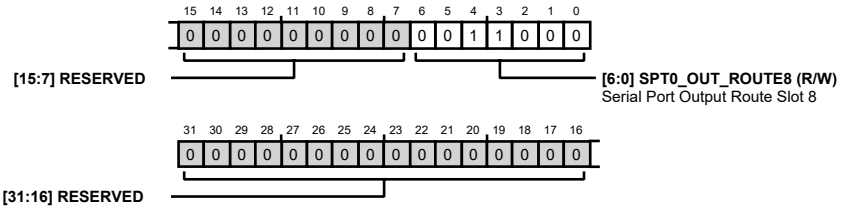


Table 253. Bit Descriptions for SPT0_ROUTE8

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved.	0x0	R
[6:0]	SPT0_OUT_ROUTE8	Serial Port Output Route Slot 8	0x18	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		
		0000011: FastDSP Channel 3		
		0000100: FastDSP Channel 4		
		0000101: FastDSP Channel 5		
		0000110: FastDSP Channel 6		
		0000111: FastDSP Channel 7		
		0001000: FastDSP Channel 8		
		0001001: FastDSP Channel 9		
		0001010: FastDSP Channel 10		
		0001011: FastDSP Channel 11		
		0001100: FastDSP Channel 12		
		0001101: FastDSP Channel 13		
		0001110: FastDSP Channel 14		
		0001111: FastDSP Channel 15		
		0010000: Output ASRC 0 Channel 0		
		0010001: Output ASRC 0 Channel 1		
		0010010: Output ASRC 0 Channel 2		
		0010011: Output ASRC 0 Channel 3		
		0010100: Output ASRC 1 Channel 0		
		0010101: Output ASRC 1 Channel 1		
		0010110: Output ASRC 1 Channel 2		
		0010111: Output ASRC 1 Channel 3		
		0011000: ADC Channel 0		
		0011001: ADC Channel 1		
		0011010: ADC Channel 2		
		0011011: HiFi TIE Output		
		0011100: Digital Microphone Channel 0		
		0011101: Digital Microphone Channel 1		
		0011110: Digital Microphone Channel 2		
		0011111: Digital Microphone Channel 3		
		0100000: Digital Microphone Channel 4		

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 9 REGISTER

Address: 0xF000052C, Reset: 0x00000019, Name: SPT0_ROUTE9

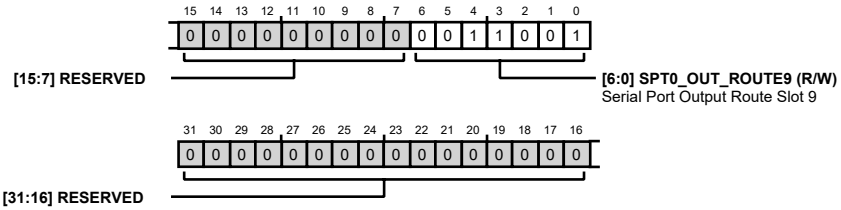


Table 254. Bit Descriptions for SPT0_ROUTE9

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE9	Serial Port Output Route Slot 9 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0	0x19	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2		

Bits	Bit Name	Description	Reset	Access
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 10 REGISTER

Address: 0xF0000530, Reset: 0x0000001A, Name: SPT0_ROUTE10

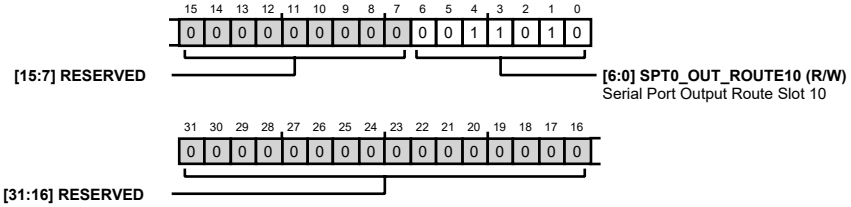


Table 255. Bit Descriptions for SPT0_ROUTE10

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE10	Serial Port Output Route Slot 10	0x1A	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		
		0000011: FastDSP Channel 3		
		0000100: FastDSP Channel 4		
		0000101: FastDSP Channel 5		
		0000110: FastDSP Channel 6		
		0000111: FastDSP Channel 7		
		0001000: FastDSP Channel 8		

Bits	Bit Name	Description	Reset	Access
		0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6		

Bits	Bit Name	Description	Reset	Access
		0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 11 REGISTER

Address: 0xF0000534, Reset: 0x0000001B, Name: SPT0_ROUTE11

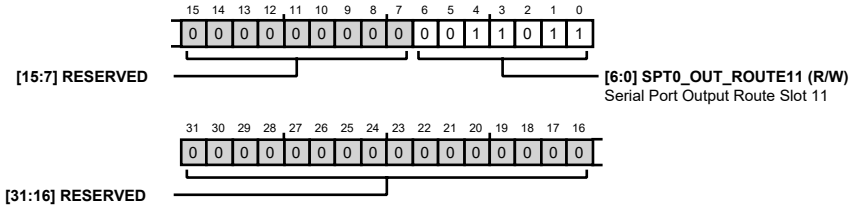


Table 256. Bit Descriptions for SPT0_ROUTE11

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE11	Serial Port Output Route Slot 11 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2	0x1B	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12		

Bits	Bit Name	Description	Reset	Access
		1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 12 REGISTER

Address: 0xF0000538, Reset: 0x0000001C, Name: SPT0_ROUTE12

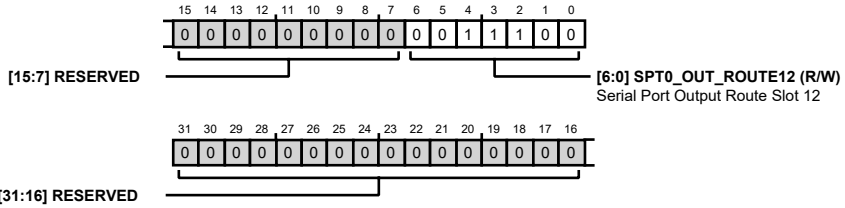


Table 257. Bit Descriptions for SPT0_ROUTE12

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE12	Serial Port Output Route Slot 12 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2	0x1C	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 13 REGISTER

Address: 0xF000053C, Reset: 0x0000001D, Name: SPT0_ROUTE13

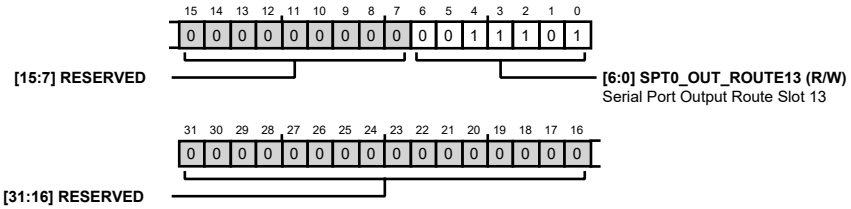


Table 258. Bit Descriptions for SPT0_ROUTE13

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE13	Serial Port Output Route Slot 13 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14	0x1D	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4		

Bits	Bit Name	Description	Reset	Access
		0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 14 REGISTER

Address: 0xF0000540, Reset: 0x0000001E, Name: SPT0_ROUTE14

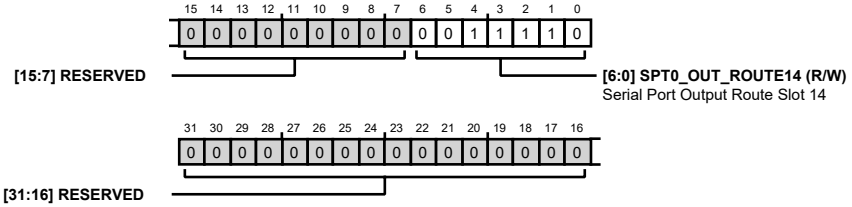


Table 259. Bit Descriptions for SPT0_ROUTE14

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE14	Serial Port Output Route Slot 14 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2	0x1E	R/W

Bits	Bit Name	Description	Reset	Access
		0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0		

Bits	Bit Name	Description	Reset	Access
		0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 0 OUTPUT ROUTING SLOT 15 REGISTER

Address: 0xF0000544, Reset: 0x0000001F, Name: SPT0_ROUTE15

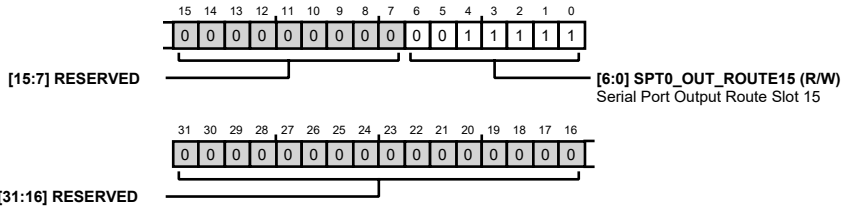


Table 260. Bit Descriptions for SPT0_ROUTE15

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT0_OUT_ROUTE15	Serial Port Output Route Slot 15 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4	0x1F	R/W

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 CONTROL 1 REGISTER

Address: 0xF0000548, Reset: 0x00000000, Name: SPT1_CTRL1

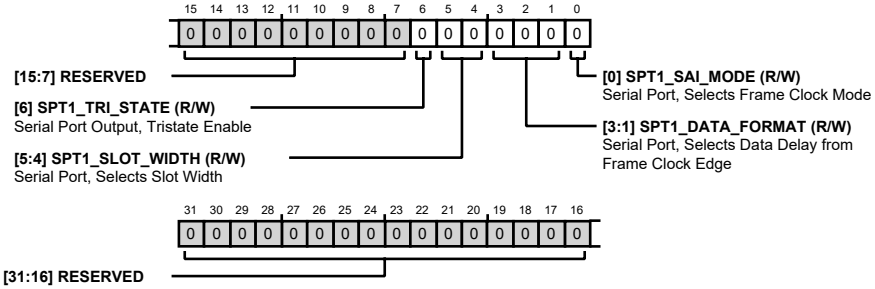


Table 261. Bit Descriptions for SPT1_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	SPT1_TRI_STATE	Serial Port Output, Tristate Enable 1: Tristate Enable 0: Tristate Disable	0x0	R/W
[5:4]	SPT1_SLOT_WIDTH	Serial Port, Selects Slot Width 00: 32 BCLKs per Slot 01: 16 BCLKs per Slot 10: 24 BCLKs per Slot	0x0	R/W
[3:1]	SPT1_DATA_FORMAT	Serial Port, Selects Data Delay from Frame Clock Edge 001: Left-Justified, Delay by 0 000: Typical I^2S Mode, Delay by 1 010: Delay by 8 011: Delay by 12 100: Delay by 16	0x0	R/W
0	SPT1_SAI_MODE	Serial Port, Selects Frame Clock Mode 0: Stereo. 50% duty cycle frame clock (I^2S, left-justified, or right-justified). 1: TDM. Frame clock is single bit clock wide pulse.	0x0	R/W

SERIAL PORT 1 CONTROL 2 REGISTER

Address: 0xF000054C, Reset: 0x00000000, Name: SPT1_CTRL2

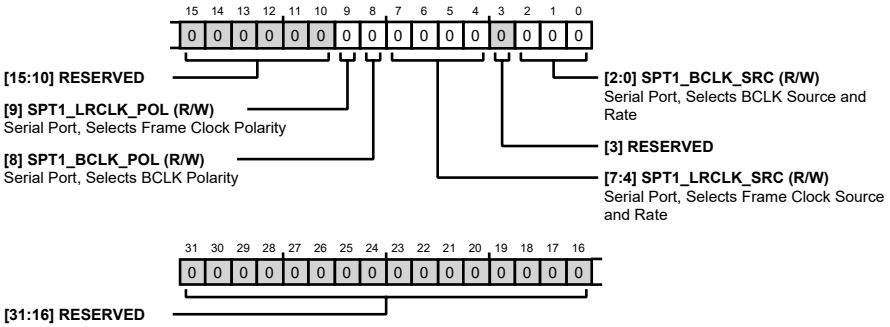


Table 262. Bit Descriptions for SPT1_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	SPT1_LRCLK_POL	Serial Port, Selects Frame Clock Polarity 0: Normal Polarity 1: Inverted Polarity	0x0	R/W
8	SPT1_BCLK_POL	Serial Port, Selects BCLK Polarity 0: Captured on rising edge. 1: Captured on falling edge.	0x0	R/W
[7:4]	SPT1_LRCLK_SRC	Serial Port, Selects Frame Clock Source and Rate 0000: Frame clock is from an external source. 0001: Generates frame clock with 48kHz. 0010: Generates frame clock with 96kHz. 0011: Generates frame clock with 192kHz. 0100: Generates frame clock with 12kHz. 0101: Generates frame clock with 24kHz. 0110: Generates frame clock with 384kHz. 0111: Generates frame clock with 76 kHz. 1000: Generates frame clock with 8kHz. 1001: Generates frame clock with 16kHz.	0x0	R/W
3	RESERVED	Reserved	0x0	R
[2:0]	SPT1_BCLK_SRC	Serial Port, Selects BCLK Source and Rate 000: BCLK is from an external source. 001: Generates BCLK at 3.072MHz. 010: Generates BCLK at 6.144MHz. 011: Generates BCLK at 12.288MHz. 100: Generates BCLK at 24.576MHz.	0x0	R/W

SERIAL PORT 1 OUTPUT ROUTING SLOT 0 (LEFT) REGISTER

Address: 0xF0000550, Reset: 0x00000010, Name: SPT1_ROUTE0

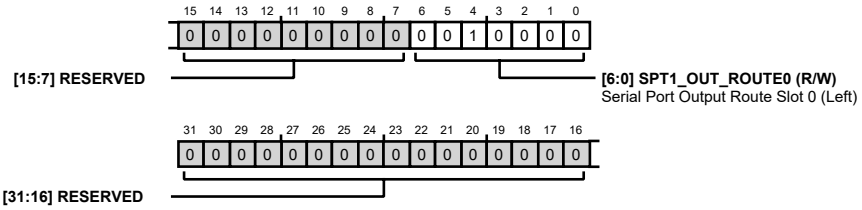


Table 263. Bit Descriptions for SPT1_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved.	0x0	R
[6:0]	SPT1_OUT_ROUTE0	Serial Port Output Route Slot 0 (Left) 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 1 (RIGHT) REGISTER

Address: 0xF0000554, Reset: 0x00000010, Name: SPT1_ROUTE1

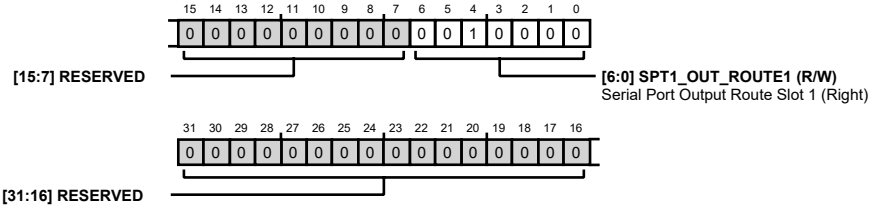


Table 264. Bit Descriptions for SPT1_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE1	Serial Port Output Route Slot 1 (Right) 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2		

Bits	Bit Name	Description	Reset	Access
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 2 REGISTER

Address: 0xF0000558, Reset: 0x00000010, Name: SPT1_ROUTE2

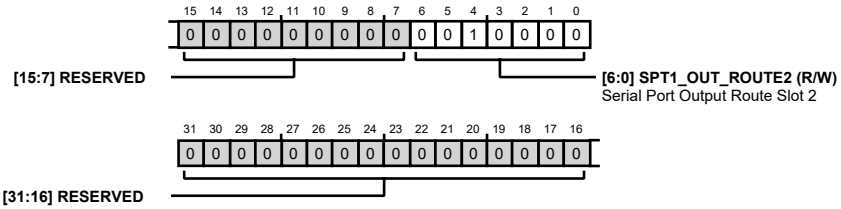


Table 265. Bit Descriptions for SPT1_ROUTE2

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE2	Serial Port Output Route Slot 2	0x10	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		
		0000011: FastDSP Channel 3		
		0000100: FastDSP Channel 4		
		0000101: FastDSP Channel 5		
		0000110: FastDSP Channel 6		
		0000111: FastDSP Channel 7		
		0001000: FastDSP Channel 8		

Bits	Bit Name	Description	Reset	Access
		0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6		

Bits	Bit Name	Description	Reset	Access
		0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 3 REGISTER

Address: 0xF000055C, Reset: 0x00000010, Name: SPT1_ROUTE3

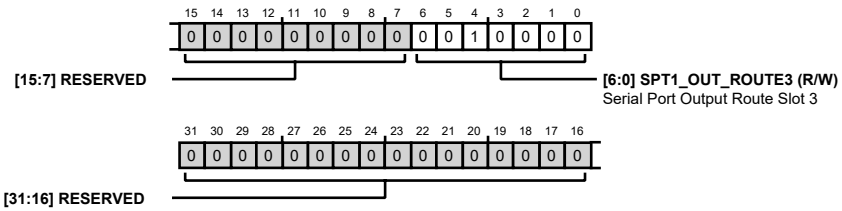


Table 266. Bit Descriptions for SPT1_ROUTE3

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE3	Serial Port Output Route Slot 3 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12		

Bits	Bit Name	Description	Reset	Access
		1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 4 REGISTER

Address: 0xF0000560, Reset: 0x00000010, Name: SPT1_ROUTE4

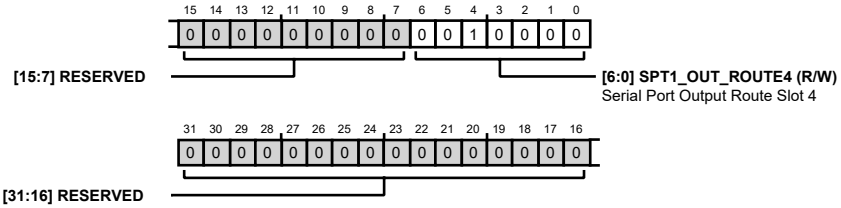


Table 267. Bit Descriptions for SPT1_ROUTE4

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE4	Serial Port Output Route Slot 4 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 5 REGISTER

Address: 0xF0000564, Reset: 0x00000010, Name: SPT1_ROUTE5

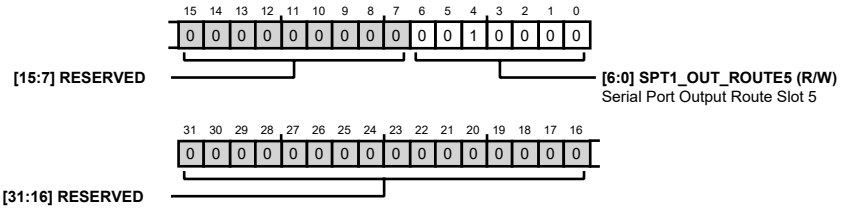


Table 268. Bit Descriptions for SPT1_ROUTE5

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE5	Serial Port Output Route Slot 5 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4		

Bits	Bit Name	Description	Reset	Access
		0111011: Audio Output DMA 1 Channel 5		
		0111100: Audio Output DMA 1 Channel 6		
		0111101: Audio Output DMA 1 Channel 7		
		0111110: Audio Output DMA 2 Channel 0		
		0111111: Audio Output DMA 2 Channel 1		
		1000000: Audio Output DMA 2 Channel 2		
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 6 REGISTER

Address: 0xF0000568, Reset: 0x00000010, Name: SPT1_ROUTE6

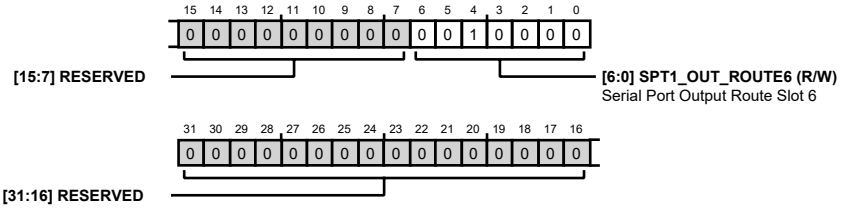


Table 269. Bit Descriptions for SPT1_ROUTE6

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE6	Serial Port Output Route Slot 6	0x10	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		

Bits	Bit Name	Description	Reset	Access
		0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0		

Bits	Bit Name	Description	Reset	Access
		0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 7 REGISTER

Address: 0xF000056C, Reset: 0x00000010, Name: SPT1_ROUTE7

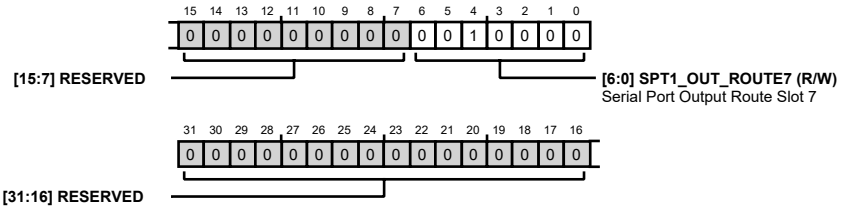


Table 270. Bit Descriptions for SPT1_ROUTE7

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE7	Serial Port Output Route Slot 7 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 8 REGISTER

Address: 0xF0000570, Reset: 0x00000010, Name: SPT1_ROUTE8

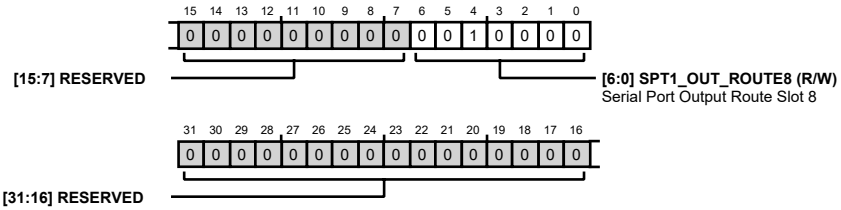


Table 271. Bit Descriptions for SPT1_ROUTE8

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE8	Serial Port Output Route Slot 8 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2		

Bits	Bit Name	Description	Reset	Access
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 9 REGISTER

Address: 0xF0000574, Reset: 0x00000010, Name: SPT1_ROUTE9

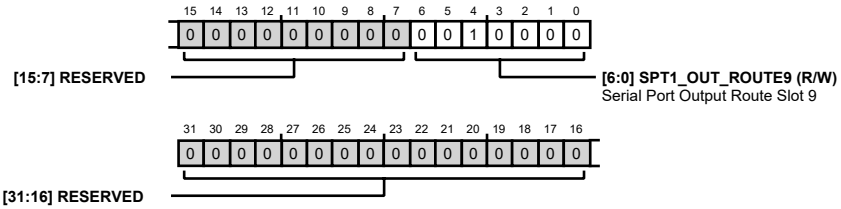


Table 272. Bit Descriptions for SPT1_ROUTE9

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE9	Serial Port Output Route Slot 9	0x10	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		
		0000011: FastDSP Channel 3		
		0000100: FastDSP Channel 4		
		0000101: FastDSP Channel 5		
		0000110: FastDSP Channel 6		
		0000111: FastDSP Channel 7		
		0001000: FastDSP Channel 8		

Bits	Bit Name	Description	Reset	Access
		0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6		

Bits	Bit Name	Description	Reset	Access
		0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 10 REGISTER

Address: 0xF0000578, Reset: 0x00000010, Name: SPT1_ROUTE10

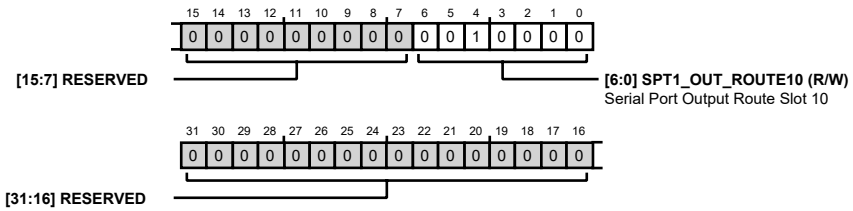


Table 273. Bit Descriptions for SPT1_ROUTE10

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE10	Serial Port Output Route Slot 10 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12		

Bits	Bit Name	Description	Reset	Access
		1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 11 REGISTER

Address: 0xF000057C, Reset: 0x00000010, Name: SPT1_ROUTE11

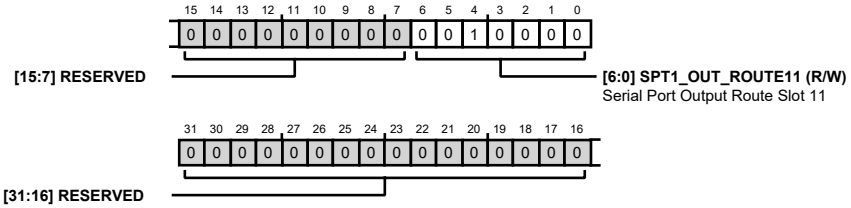


Table 274. Bit Descriptions for SPT1_ROUTE11

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE11	Serial Port Output Route Slot 11 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0		

Bits	Bit Name	Description	Reset	Access
		1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 12 REGISTER

Address: 0xF0000580, Reset: 0x00000010, Name: SPT1_ROUTE12

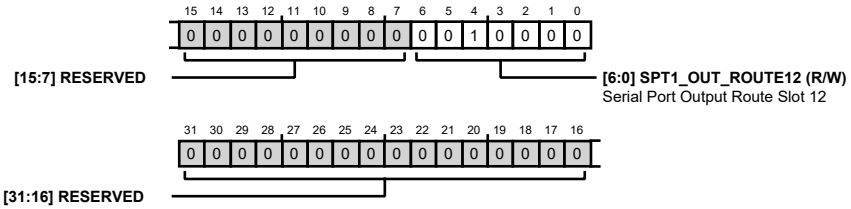


Table 275. Bit Descriptions for SPT1_ROUTE12

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE12	Serial Port Output Route Slot 12 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4		

Bits	Bit Name	Description	Reset	Access
		0111011: Audio Output DMA 1 Channel 5		
		0111100: Audio Output DMA 1 Channel 6		
		0111101: Audio Output DMA 1 Channel 7		
		0111110: Audio Output DMA 2 Channel 0		
		0111111: Audio Output DMA 2 Channel 1		
		1000000: Audio Output DMA 2 Channel 2		
		1000001: Audio Output DMA 2 Channel 3		
		1000010: Audio Output DMA 2 Channel 4		
		1000011: Audio Output DMA 2 Channel 5		
		1000100: Audio Output DMA 2 Channel 6		
		1000101: Audio Output DMA 2 Channel 7		
		1000110: Audio Bus Map Out 0		
		1000111: Audio Bus Map Out 1		
		1001000: Audio Bus Map Out 2		
		1001001: Audio Bus Map Out 3		
		1001010: Audio Bus Map Out 4		
		1001011: Audio Bus Map Out 5		
		1001100: Audio Bus Map Out 6		
		1001101: Audio Bus Map Out 7		
		1001110: Audio Bus Map Out 8		
		1001111: Audio Bus Map Out 9		
		1010000: Audio Bus Map Out 10		
		1010001: Audio Bus Map Out 11		
		1010010: Audio Bus Map Out 12		
		1010011: Audio Bus Map Out 13		
		1010100: Audio Bus Map Out 14		
		1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 13 REGISTER

Address: 0xF0000584, Reset: 0x00000010, Name: SPT1_ROUTE13

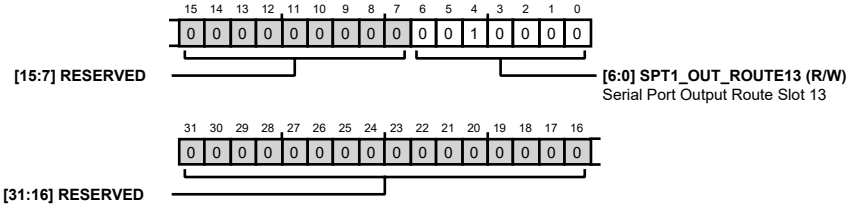


Table 276. Bit Descriptions for SPT1_ROUTE13

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE13	Serial Port Output Route Slot 13	0x10	R/W
		0000000: FastDSP Channel 0		
		0000001: FastDSP Channel 1		
		0000010: FastDSP Channel 2		

Bits	Bit Name	Description	Reset	Access
		0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0		

Bits	Bit Name	Description	Reset	Access
		0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 14 REGISTER

Address: 0xF0000588, Reset: 0x00000010, Name: SPT1_ROUTE14

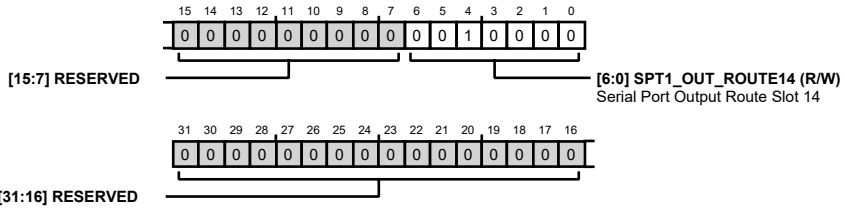


Table 277. Bit Descriptions for SPT1_ROUTE14

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE14	Serial Port Output Route Slot 14 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0 0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2 1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6		

Bits	Bit Name	Description	Reset	Access
		1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

SERIAL PORT 1 OUTPUT ROUTING SLOT 15 REGISTER

Address: 0xF000058C, Reset: 0x00000010, Name: SPT1_ROUTE15

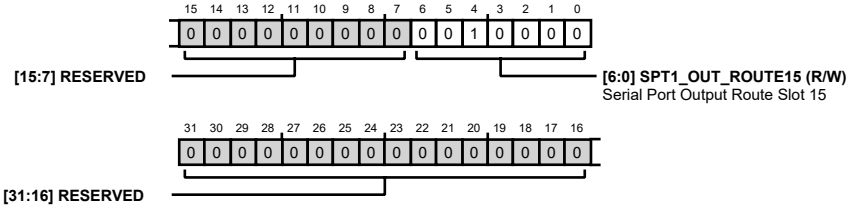


Table 278. Bit Descriptions for SPT1_ROUTE15

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	SPT1_OUT_ROUTE15	Serial Port Output Route Slot 15 0000000: FastDSP Channel 0 0000001: FastDSP Channel 1 0000010: FastDSP Channel 2 0000011: FastDSP Channel 3 0000100: FastDSP Channel 4 0000101: FastDSP Channel 5 0000110: FastDSP Channel 6 0000111: FastDSP Channel 7 0001000: FastDSP Channel 8 0001001: FastDSP Channel 9 0001010: FastDSP Channel 10 0001011: FastDSP Channel 11 0001100: FastDSP Channel 12 0001101: FastDSP Channel 13 0001110: FastDSP Channel 14 0001111: FastDSP Channel 15 0010000: Output ASRC 0 Channel 0 0010001: Output ASRC 0 Channel 1 0010010: Output ASRC 0 Channel 2 0010011: Output ASRC 0 Channel 3 0010100: Output ASRC 1 Channel 0	0x10	R/W

Bits	Bit Name	Description	Reset	Access
		0010101: Output ASRC 1 Channel 1 0010110: Output ASRC 1 Channel 2 0010111: Output ASRC 1 Channel 3 0011000: ADC Channel 0 0011001: ADC Channel 1 0011010: ADC Channel 2 0011011: HiFi TIE Output 0011100: Digital Microphone Channel 0 0011101: Digital Microphone Channel 1 0011110: Digital Microphone Channel 2 0011111: Digital Microphone Channel 3 0100000: Digital Microphone Channel 4 0100001: Digital Microphone Channel 5 0100010: Digital Microphone Channel 6 0100011: Digital Microphone Channel 7 0100100: Digital Microphone Channel 8 0100101: Digital Microphone Channel 9 0100110: Fast to Slow Decimator Channel 0 0100111: Fast to Slow Decimator Channel 1 0101000: Fast to Slow Decimator Channel 2 0101001: Fast to Slow Decimator Channel 3 0101010: Fast to Slow Decimator Channel 4 0101011: Fast to Slow Decimator Channel 5 0101100: Fast to Slow Decimator Channel 6 0101101: Fast to Slow Decimator Channel 7 0101110: Audio Output DMA 0 Channel 0 0101111: Audio Output DMA 0 Channel 1 0110000: Audio Output DMA 0 Channel 2 0110001: Audio Output DMA 0 Channel 3 0110010: Audio Output DMA 0 Channel 4 0110011: Audio Output DMA 0 Channel 5 0110100: Audio Output DMA 0 Channel 6 0110101: Audio Output DMA 0 Channel 7 0110110: Audio Output DMA 1 Channel 0 0110111: Audio Output DMA 1 Channel 1 0111000: Audio Output DMA 1 Channel 2 0111001: Audio Output DMA 1 Channel 3 0111010: Audio Output DMA 1 Channel 4 0111011: Audio Output DMA 1 Channel 5 0111100: Audio Output DMA 1 Channel 6 0111101: Audio Output DMA 1 Channel 7 0111110: Audio Output DMA 2 Channel 0 0111111: Audio Output DMA 2 Channel 1 1000000: Audio Output DMA 2 Channel 2		

Bits	Bit Name	Description	Reset	Access
		1000001: Audio Output DMA 2 Channel 3 1000010: Audio Output DMA 2 Channel 4 1000011: Audio Output DMA 2 Channel 5 1000100: Audio Output DMA 2 Channel 6 1000101: Audio Output DMA 2 Channel 7 1000110: Audio Bus Map Out 0 1000111: Audio Bus Map Out 1 1001000: Audio Bus Map Out 2 1001001: Audio Bus Map Out 3 1001010: Audio Bus Map Out 4 1001011: Audio Bus Map Out 5 1001100: Audio Bus Map Out 6 1001101: Audio Bus Map Out 7 1001110: Audio Bus Map Out 8 1001111: Audio Bus Map Out 9 1010000: Audio Bus Map Out 10 1010001: Audio Bus Map Out 11 1010010: Audio Bus Map Out 12 1010011: Audio Bus Map Out 13 1010100: Audio Bus Map Out 14 1010101: Audio Bus Map Out 15		

PDM SAMPLE RATE AND FILTERING CONTROL REGISTER

Address: 0xF0000590, Reset: 0x00000004, Name: PDM_CTRL1

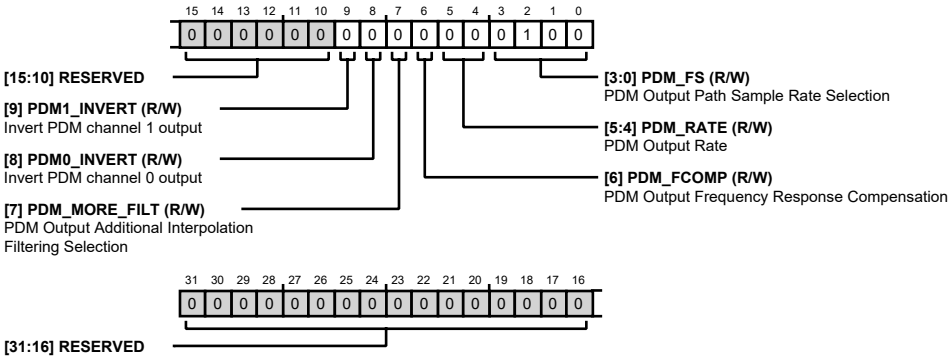


Table 279. Bit Descriptions for PDM_CTRL1

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	PDM1_INVERT	Invert PDM Channel 1 Output 0: PDM channel 1 not inverted. 1: PDM channel 1 inverted.	0x0	R/W
8	PDM0_INVERT	Invert PDM Channel 0 Output 0: PDM channel 0 not inverted. 1: PDM channel 0 inverted.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	PDM_MORE_FILT	PDM Output Additional Interpolation Filtering Selection 0: Less Interpolation Filtering: Lower Delay 1: More Interpolation Filtering: Higher Delay	0x0	R/W
6	PDM_FCOMP	PDM Output Frequency Response Compensation 0: High frequency response is not compensated (lower delay). 1: High frequency response is compensated for samples rates of 192kHz or lower when PDM_MORE_FILT = 1 (higher delay).	0x0	R/W
[5:4]	PDM_RATE	PDM Output Rate 01: 6.144MHz PDM Output Rate 10: 3.072MHz PDM Output Rate 00: 12.288MHz PDM Output Rate	0x0	R/W
[3:0]	PDM_FS	PDM Output Path Sample Rate Selection 0000: 12kHz Sample Rate 0001: 12kHz Sample Rate 0010: 12kHz Sample Rate 0011: 24kHz Sample Rate 0100: 48kHz Sample Rate 0101: 96kHz Sample Rate 0110: 192kHz Sample Rate 0111: 384kHz Sample Rate 1000: 768kHz Sample Rate	0x4	R/W

PDM MUTING, HIGHPASS, AND VOLUME OPTIONS REGISTER

Address: 0xF0000594, Reset: 0x000000C4, Name: PDM_CTRL2

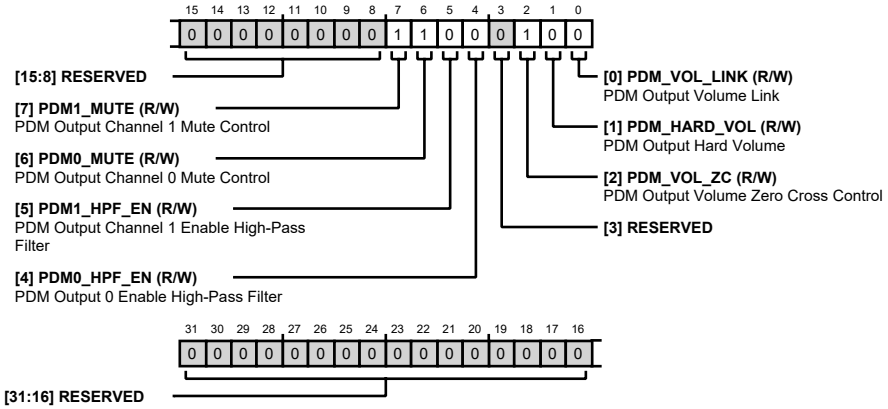


Table 280. Bit Descriptions for PDM_CTRL2

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
7	PDM1_MUTE	PDM Output Channel 1 Mute Control 0: PDM Output Unmuted 1: PDM Output Muted	0x1	R/W

Bits	Bit Name	Description	Reset	Access
6	PDM0_MUTE	PDM Output Channel 0 Mute Control 0: PDM Output Unmuted 1: PDM Output Muted	0x1	R/W
5	PDM1_HPF_EN	PDM Output Channel 1 Enable Highpass Filter 0: PDM Output Highpass Filter Off 1: PDM Output Highpass Filter On	0x0	R/W
4	PDM0_HPF_EN	PDM Output 0 Enable Highpass Filter 0: PDM Output Highpass Filter Off 1: PDM Output Highpass Filter On	0x0	R/W
3	RESERVED	Reserved	0x0	R
2	PDM_VOL_ZC	PDM Output Volume Zero Cross Control 0: Volume change occurs at any time. 1: Volume change only occurs at zero crossing.	0x1	R/W
1	PDM_HARD_VOL	PDM Output Hard Volume 0: Soft Volume Ramping 1: Hard/Immediate Volume Change	0x0	R/W
0	PDM_VOL_LINK	PDM Output Volume Link 0: Each ADC channel uses its respective volume value. 1: All ADC channels use Channel 0 volume value.	0x0	R/W

PDM HIGHPASS FILTER CUTOFF CONTROL REGISTER

Address: 0xF0000598, Reset: 0x0000000D, Name: PDM_CTRL3

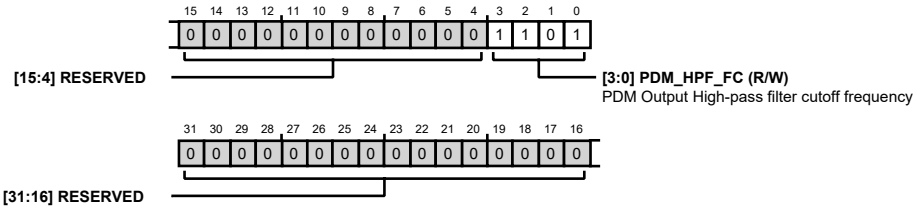


Table 281. Bit Descriptions for PDM_CTRL3

Bits	Bit Name	Description	Reset	Access
[31:4]	RESERVED	Reserved	0x0	R
[3:0]	PDM_HPF_FC	PDM Output Highpass Filter Cutoff Frequency 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: Reserved 0101: 241Hz 0110: 120Hz 0111: 60Hz 1000: 30Hz 1001: 15Hz 1010: 7Hz	0xD	R/W

Bits	Bit Name	Description	Reset	Access
		1011: 4Hz 1100: 2Hz 1101: 1Hz 1110: 0.5Hz 1111: 0.25Hz		

PDM OUTPUT CHANNEL 0 VOLUME REGISTER

Address: 0xF000059C, Reset: 0x00000040, Name: PDM_VOL0

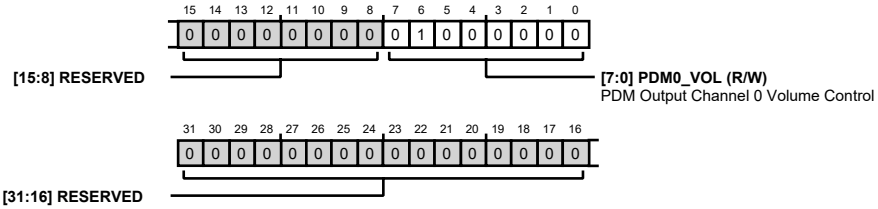


Table 282. Bit Descriptions for PDM_VOL0

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	PDM0_VOL	PDM Output Channel 0 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

PDM OUTPUT CHANNEL 1 VOLUME REGISTER

Address: 0xF00005A0, Reset: 0x00000040, Name: PDM_VOL1

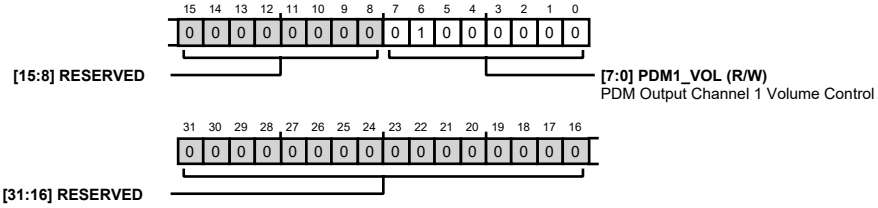


Table 283. Bit Descriptions for PDM_VOL1

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	PDM1_VOL	PDM Output Channel 1 Volume Control 00000000: +24dB 00000001: +23.625dB 00000010: +23.25dB 00000011: +22.875dB 00000100: +22.5dB ... 00111111: +0.375dB 01000000: 0dB 01000001: -0.375dB ... 11111101: -70.875dB 11111110: -71.25dB 11111111: Mute	0x40	R/W

PDM OUTPUT CHANNEL 0 ROUTING REGISTER

Address: 0xF00005A4, Reset: 0x00000000, Name: PDM_ROUTE0

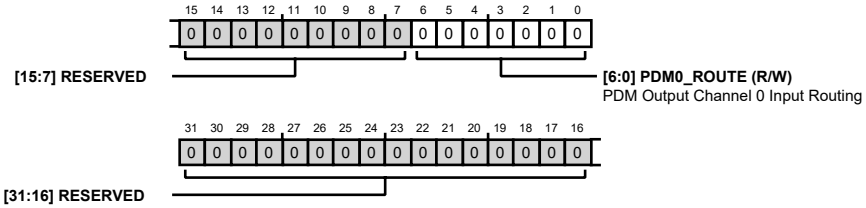


Table 284. Bit Descriptions for PDM_ROUTE0

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	PDM0_ROUTE	PDM Output Channel 0 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0		

Bits	Bit Name	Description	Reset	Access
		0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: HiFi Core TIE Output 0111100: Digital Microphone Channel 0 0111101: Digital Microphone Channel 1 0111110: Digital Microphone Channel 2 0111111: Digital Microphone Channel 3 1000000: Digital Microphone Channel 4 1000001: Digital Microphone Channel 5 1000010: Digital Microphone Channel 6 1000011: Digital Microphone Channel 7 1000100: Digital Microphone Channel 8 1000101: Digital Microphone Channel 9 1000110: Audio Output DMA 0 Channel 0 1000111: Audio Output DMA 0 Channel 1 1001000: Audio Output DMA 0 Channel 2 1001001: Audio Output DMA 0 Channel 3 1001010: Audio Output DMA 0 Channel 4 1001011: Audio Output DMA 0 Channel 5 1001100: Audio Output DMA 0 Channel 6 1001101: Audio Output DMA 0 Channel 7 1001110: Audio Output DMA 1 Channel 0 1001111: Audio Output DMA 1 Channel 1 1010000: Audio Output DMA 1 Channel 2 1010001: Audio Output DMA 1 Channel 3 1010010: Audio Output DMA 1 Channel 4 1010011: Audio Output DMA 1 Channel 5 1010100: Audio Output DMA 1 Channel 6 1010101: Audio Output DMA 1 Channel 7 1010110: Audio Output DMA 2 Channel 0 1010111: Audio Output DMA 2 Channel 1 1011000: Audio Output DMA 2 Channel 2 1011001: Audio Output DMA 2 Channel 3 1011010: Audio Output DMA 2 Channel 4 1011011: Audio Output DMA 2 Channel 5 1011100: Audio Output DMA 2 Channel 6 1011101: Audio Output DMA 2 Channel 7 1011110: Slow to Fast Interpolator Channel 0 1011111: Slow to Fast Interpolator Channel 1 1100000: Slow to Fast Interpolator Channel 2 1100001: Slow to Fast Interpolator Channel 3 1100010: Slow to Fast Interpolator Channel 4 1100011: Slow to Fast Interpolator Channel 5 1100100: Slow to Fast Interpolator Channel 6		

Bits	Bit Name	Description	Reset	Access
		1100101: Slow to Fast Interpolator Channel 7 1100110: Audio Bus Map Out 0 1100111: Audio Bus Map Out 1 1101000: Audio Bus Map Out 2 1101001: Audio Bus Map Out 3 1101010: Audio Bus Map Out 4 1101011: Audio Bus Map Out 5 1101100: Audio Bus Map Out 6 1101101: Audio Bus Map Out 7 1101110: Audio Bus Map Out 8 1101111: Audio Bus Map Out 9 1110000: Audio Bus Map Out 10 1110001: Audio Bus Map Out 11 1110010: Audio Bus Map Out 12 1110011: Audio Bus Map Out 13 1110100: Audio Bus Map Out 14 1110101: Audio Bus Map Out 15		

PDM OUTPUT CHANNEL 1 ROUTING REGISTER

Address: 0xF00005A8, Reset: 0x00000000, Name: PDM_ROUTE1

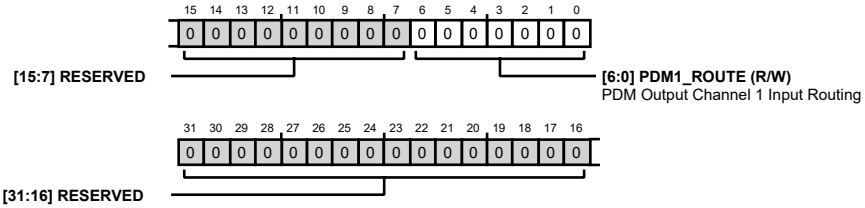


Table 285. Bit Descriptions for PDM_ROUTE1

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
[6:0]	PDM1_ROUTE	PDM Output Channel 1 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0		

Bits	Bit Name	Description	Reset	Access
		0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: HiFi Core TIE Output 0111100: Digital Microphone Channel 0 0111101: Digital Microphone Channel 1 0111110: Digital Microphone Channel 2 0111111: Digital Microphone Channel 3 1000000: Digital Microphone Channel 4 1000001: Digital Microphone Channel 5 1000010: Digital Microphone Channel 6 1000011: Digital Microphone Channel 7 1000100: Digital Microphone Channel 8 1000101: Digital Microphone Channel 9 1000110: Audio Output DMA 0 Channel 0 1000111: Audio Output DMA 0 Channel 1 1001000: Audio Output DMA 0 Channel 2 1001001: Audio Output DMA 0 Channel 3 1001010: Audio Output DMA 0 Channel 4 1001011: Audio Output DMA 0 Channel 5 1001100: Audio Output DMA 0 Channel 6 1001101: Audio Output DMA 0 Channel 7 1001110: Audio Output DMA 1 Channel 0 1001111: Audio Output DMA 1 Channel 1 1010000: Audio Output DMA 1 Channel 2 1010001: Audio Output DMA 1 Channel 3 1010010: Audio Output DMA 1 Channel 4 1010011: Audio Output DMA 1 Channel 5 1010100: Audio Output DMA 1 Channel 6 1010101: Audio Output DMA 1 Channel 7 1010110: Audio Output DMA 2 Channel 0 1010111: Audio Output DMA 2 Channel 1 1011000: Audio Output DMA 2 Channel 2 1011001: Audio Output DMA 2 Channel 3 1011010: Audio Output DMA 2 Channel 4 1011011: Audio Output DMA 2 Channel 5 1011100: Audio Output DMA 2 Channel 6 1011101: Audio Output DMA 2 Channel 7 1011110: Slow to Fast Interpolator Channel 0 1011111: Slow to Fast Interpolator Channel 1 1100000: Slow to Fast Interpolator Channel 2 1100001: Slow to Fast Interpolator Channel 3 1100010: Slow to Fast Interpolator Channel 4 1100011: Slow to Fast Interpolator Channel 5 1100100: Slow to Fast Interpolator Channel 6		

Bits	Bit Name	Description	Reset	Access
		1100101: Slow to Fast Interpolator Channel 7 1100110: Audio Bus Map Out 0 1100111: Audio Bus Map Out 1 1101000: Audio Bus Map Out 2 1101001: Audio Bus Map Out 3 1101010: Audio Bus Map Out 4 1101011: Audio Bus Map Out 5 1101100: Audio Bus Map Out 6 1101101: Audio Bus Map Out 7 1101110: Audio Bus Map Out 8 1101111: Audio Bus Map Out 9 1110000: Audio Bus Map Out 10 1110001: Audio Bus Map Out 11 1110010: Audio Bus Map Out 12 1110011: Audio Bus Map Out 13 1110100: Audio Bus Map Out 14 1110101: Audio Bus Map Out 15		

AUDIO DMA INPUT FORMAT SELECT REGISTER

Address: 0xF0000600 to 0xF0000608 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CONFIGn

Specifies the format conversion of the channel data to the ADMA write data buffer. Data is converted from 1.23 to the selected type. The format conversion is per ADMA engine, so all channels processed by the same ADMA Engine undergo the same format conversion.

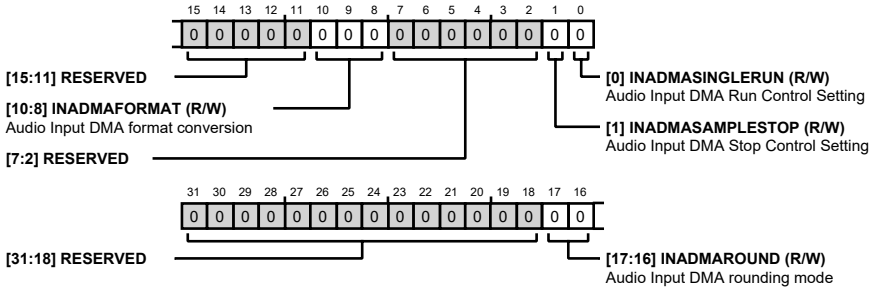


Table 286. Bit Descriptions for ADMA_IN_CONFIGn

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved	0x0	R
[17:16]	INADMAROUND	Audio Input DMA Rounding Mode 00: Round down. Number is rounded down. Unused bits are truncated. 01: Round half to even. If integer value is even, round down (unused bits are truncated). If integer value is odd and the fractional value is ≥ 0.5, round up, else round down. ex. 23.5 -> 24 ex. 24.5 -> 24 ex. -23.5 -> 24 ex. -24.5 -> 24 10: Round half to zero. If the fractional value is ≤ 0.5 round toward the nearest integer value closest to 0 on a number line. Else, round toward the nearest integer value furthest from zero on a number line. ex. 23.5 becomes 23, ex. -23.5 becomes -23	0x0	R/W
[15:11]	RESERVED	Reserved	0x0	R
[10:8]	INADMAFORMAT	Audio Input DMA Format Conversion 000: Destination format is 1.31. 001: Destination format is 1.15. 010: Destination format is 9.23. 011: Destination format is 1.23. 101: Destination format is FLOAT.	0x0	R/W
[7:2]	RESERVED	Reserved	0x0	R
1	INADMASAMPLESTOP	Audio Input DMA Stop Control Setting. Block or Sample stop mode. Determines how the Engine will respond to the inAdmaStop bit. In Block stop mode, engine will run until the end of the current block and then stop and indicate the done state. This only applies to Continuous run mode because block stop is the normal mode for Single Block run In Sample stop mode, engine will stop almost immediately. It will process the current sample, then wait only for any pending AXI transactions to finish and stop without finishing the current frame or block of data. Default is Block stop mode. 0: Stop continuous ADMA operation on a block boundary. 1: Stop continuous ADMA operation on a sample boundary.	0x0	R/W
0	INADMASINGLERUN	Audio Input DMA Run Control Setting. Continuous or Single Block run mode. In Continuous run mode, engine will run continuously until inAdmaStop is asserted. Memory addressing is determined by inCBegin and inCEnd. In Single Block run mode, engine will stop at the end of a block and indicate the done state. Memory addressing starts at the inSingleBlockAddr register setting. Default is Continuous mode. 0: Engine will run continuously until inAdmaStop is asserted. 1: Engine will stop at the end of a block.	0x0	R/W

AUDIO DMA OUTPUT FORMAT SELECT REGISTER

Address: 0xF0000610 to 0xF0000618 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CONFIGn

Specifies the format conversion of the ADMA read data to the channel data in the Audio DMA output registers. Data is converted from the selected type to 1.23. The format conversion is per ADMA engine, so all channels processed by the same

ADMA Engine undergo the same format conversion.

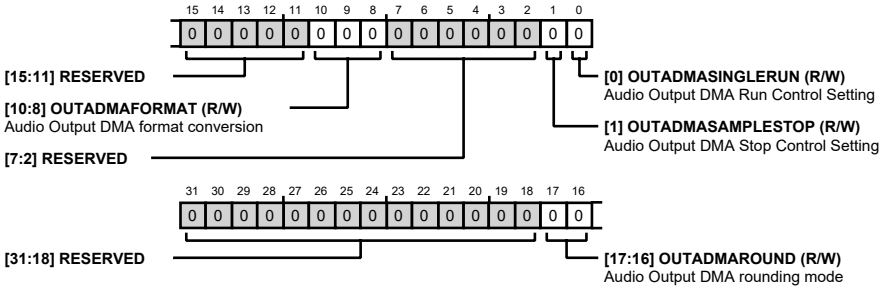


Table 287. Bit Descriptions for ADMA_OUT_CONFIGn

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved	0x0	R
[17:16]	OUTADMAROUND	Audio Output DMA Rounding Mode 00: Round down. Number is rounded down. Unused bits are truncated. 01: Round half to even. If integer value is even, round down (unused bits are truncated). If integer value is odd and the fractional value is ≥ 0.5, round up, else round down. ex. 23.5 -> 24 ex. 24.5 -> 24 ex. -23.5 -> 24 ex. -24.5 -> 24 10: Round half to zero. If the fractional value is ≤ 0.5 round toward the nearest integer value closest to 0 on a number line. Else, round toward the nearest integer value furthest from zero on a number line. ex. 23.5 becomes 23, ex. -23.5 becomes -23	0x0	R/W
[15:11]	RESERVED	Reserved	0x0	R
[10:8]	OUTADMAFORMAT	Audio Output DMA Format Conversion 000: Source format is 1.31. 001: Source format is 1.15. 010: Source format is 9.23. 011: Source format is 1.23. 101: Source format is FLOAT.	0x0	R/W
[7:2]	RESERVED	Reserved	0x0	R
1	OUTADMASAMPLESTOP	Audio Output DMA Stop Control Setting. Block or Sample stop mode. Determines how the Engine will respond to the outAdmaStop bit. In Block stop mode, engine will run until the end of the current block and then stop and indicate the done state. This only applies to Continuous run mode because block stop is the normal mode for Single Block run mode. In Sample stop mode, engine will stop almost immediately. It will process the current sample, then wait only for any pending AXI transactions to finish and stop without finishing the current frame or block of data. Default is Block stop mode. 0: Stop continuous ADMA operation on a block boundary. 1: Stop continuous ADMA operation on a sample boundary.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
0	OUTADMASINGLERUN	Audio Output DMA Run Control Setting. Continuous or Single Block run mode. In Continuous run mode, engine will run continuously until inAdmaStop is asserted. Memory addressing is determined by outCBegin and outCEnd. In Single Block run mode, engine will stop at the end of a block and indicate the done state. Memory addressing starts at the outSingleBlockAddr register setting. Default is Continuous mode. 0: Engine will run continuously until inAdmaStop is asserted. 1: Engine will stop at the end of a block.	0x0	R/W

AUDIO DMA AUDIO FS SELECT REGISTER

Address: 0xF0000620 to 0xF0000628 (Increments of 4), Reset: 0x00000000, Name: ADMA_FS_SELECTn

Selects from one of 70 FSs generated by audio sources for generation of frame sync interrupt, or masks FS interrupt generation.

Setting this register to values greater than 6'h47 or 6'h00 selects 1'b0 as a frame sync reference thereby masking the generation of an interrupt.

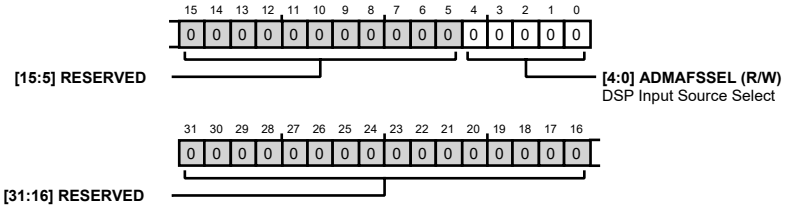


Table 288. Bit Descriptions for ADMA_FS_SELECTn

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
[4:0]	ADMAFSSEL	DSP Input Source Select 00000: Serial Port 0 00001: Serial Port 1 00010: Fast DSP 00011: Input ASRC 0 00100: Input ASRC 1 00101: ADC01 00110: ADC2 00111: Digital Microphone01 01000: Digital Microphone23 01001: Digital Microphone45 01010: Digital Microphone67 01011: Digital Microphone89 01100: Fast to Slow Decimator01 01101: Fast to Slow Decimator23 01110: Fast to Slow Decimator45 01111: Fast to Slow Decimator67 10000: Slow to Fast Interpolator01 10001: Slow to Fast Interpolator23	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		10010: Slow to Fast Interpolator45 10011: Slow to Fast Interpolator67 10100: Do Not Select Any Source		

AUDIO DMA INPUT MASK CHANNEL ENABLE/MASK REGISTER

Address: 0xF0000640 to 0xF0000648 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_MASKn

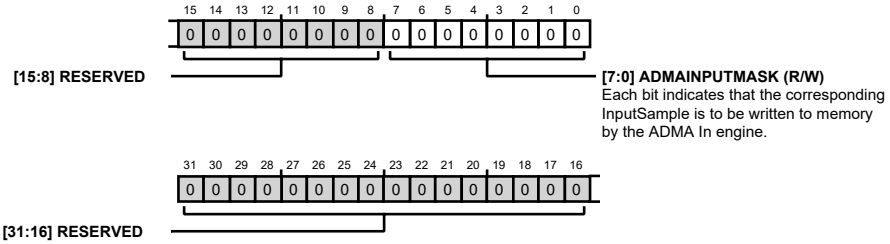


Table 289. Bit Descriptions for ADMA_IN_MASKn

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	ADMAINPUTMASK	Each bit indicates that the corresponding InputSample is to be written to memory by the ADMA In engine.	0x0	R/W

AUDIO INPUT DMA CIRCULAR BUFFER BEGIN ADDRESS REGISTER

Address: 0xF0000650 to 0xF0000658 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CBEGINn

Beginning address of the memory region used as a circular buffer for the Input ADMA Engine, when running in Continuous mode. Ignored in Single Block mode.

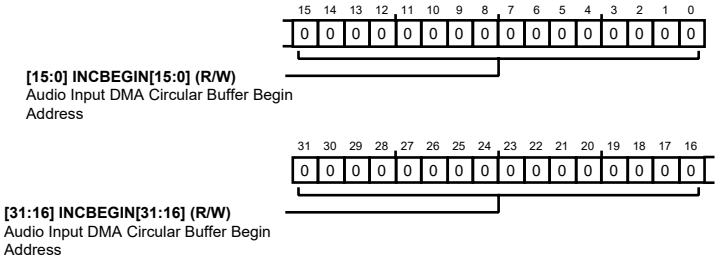


Table 290. Bit Descriptions for ADMA_IN_CBEGINn

Bits	Bit Name	Description	Reset	Access
[31:0]	INCBEGIN	Audio Input DMA Circular Buffer Begin Address	0x0	R/W

AUDIO INPUT DMA CIRCULAR BUFFER END ADDRESS REGISTER

Address: 0xF0000660 to 0xF0000668 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CENDn

Ending (last) address of the memory region used as a circular buffer for the Input ADMA Engine, when running in Continuous mode. Ignored in Single Block mode.

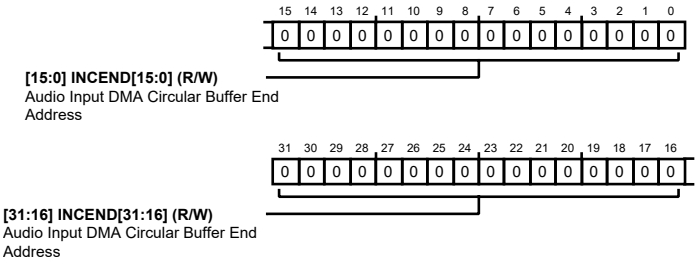


Table 291. Bit Descriptions for ADMA_IN_CENDn

Bits	Bit Name	Description	Reset	Access
[31:0]	INCEND	Audio Input DMA Circular Buffer End Address	0x0	R/W

AUDIO INPUT DMA CHANNEL STRIDE REGISTER

Address: 0xF0000670 to 0xF0000678 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CHAN_STRIDEn

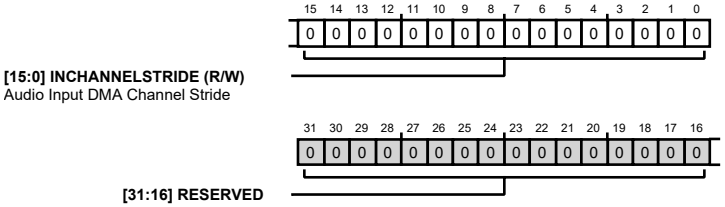


Table 292. Bit Descriptions for ADMA_IN_CHAN_STRIDEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	INCHANNELSTRIDE	Audio Input DMA Channel Stride. Determines the Input ADMA Engine memory address increment after each channel is written. The units are sample counts, which are translated to bytes in the Engine (each sample count increment can be 2-4 bytes, as determined by the DMA_IN_FORMAT register). Can be a negative number (2's complement format). Specified as an increment from the address of the previous channel, so the default is 1. Normally it will be 1 for channel interleaved mode, or equal to inBlockSize for non-interleaved mode. In circular buffer mode, the magnitude of the stride must be less than or equal to the size of the circular buffer, abs(CEnd-CBegin).	0x0	R/W

AUDIO INPUT DMA FRAME STRIDE REGISTER

Address: 0xF0000680 to 0xF0000688 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_FRAME_STRIDEn

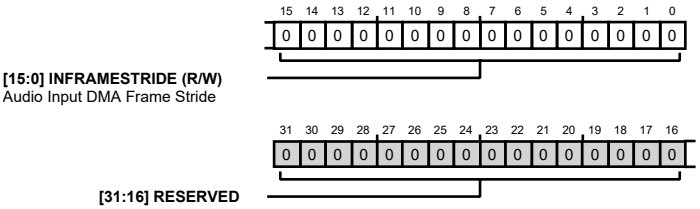


Table 293. Bit Descriptions for ADMA_IN_FRAME_STRIDEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	INFRAMESTRIDE	Audio Input DMA Frame Stride. Determines the Input ADMA Engine memory address increment after each frame. (A frame is defined as the set of channels processed by an engine between frame sync pulses). The units are sample counts, which are translated to bytes in the Engine (each sample count increment can be 2-4 bytes, as determined by the ADMA_IN_FORMAT register). Can be a negative number (2's complement format). Specified as an increment from the starting address of the previous frame. The default is 0, which means each frame overwrites the previous frame. In circular buffer mode, the magnitude of the stride must be less than or equal to the size of the circular buffer, abs(CEnd-CBegin).	0x0	R/W

AUDIO INPUT DMA BLOCK SIZE REGISTER

Address: 0xF0000690 to 0xF0000698 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_BLOCK_SIZEn

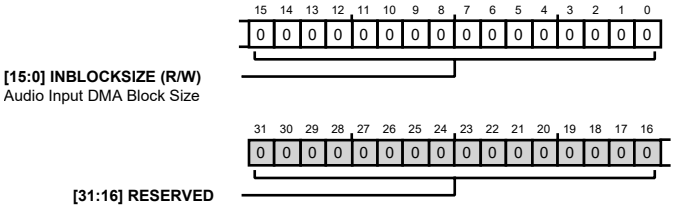


Table 294. Bit Descriptions for ADMA_IN_BLOCK_SIZEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	INBLOCKSIZE	Audio Input DMA Block Size. Specifies the number of frame syncs processed by the Input ADMA Engine for a "block" of data. At the end of the block, the Done signal is asserted, and an interrupt is triggered (if enabled). The amount of actual memory used by the ADMA Engine depends also on the data format (ADMA_IN_FORMAT) and the stride settings (ADMA_IN_CHAN_STRIDE, ADMA_IN_BLOCK_STRIDE).	0x0	R/W

AUDIO INPUT DMA CURRENT BLOCK ADDRESS REGISTER

Address: 0xF00006A0 to 0xF00006A8 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CURR_BLOCK_ADDRn

Starting memory address of the current block of data in process.

Table 295. Bit Descriptions for ADMA_IN_CURR_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	INCURRBLOCKADDR	Audio Input DMA Current Block Address	0x0	R

AUDIO INPUT DMA PREVIOUS BLOCK ADDRESS REGISTER

Address: 0xF00006B0 to 0xF00006B8 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_PREV_BLOCK_ADDRn

Starting memory address of the most recently completed block of data.

Table 296. Bit Descriptions for ADMA_IN_PREV_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	INPREVBLOCKADDR	Audio Input DMA Previous Block Address	0x0	R

AUDIO INPUT DMA SINGLE MODE BLOCK ADDRESS REGISTER

Address: 0xF00006C0 to 0xF00006C8 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_SINGLE_BLOCK_ADDRn

Designates the starting memory address of the next block of samples to be written in Single Block mode only (ignored in Continuous mode).

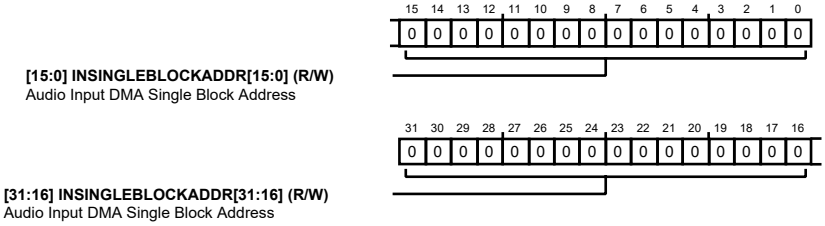


Table 297. Bit Descriptions for ADMA_IN_SINGLE_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	INSINGLEBLOCKADDR	Audio Input DMA Single Block Address	0x0	R/W

AUDIO INPUT DMA BLOCK ADDRESS REGISTER

Address: 0xF00006D0 to 0xF00006D8 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_WRITE_ADDRn

Latest memory address to be used by the Input DMA Engine.

Latency of the system including the AXI bus will determine when this address is accessed in memory.

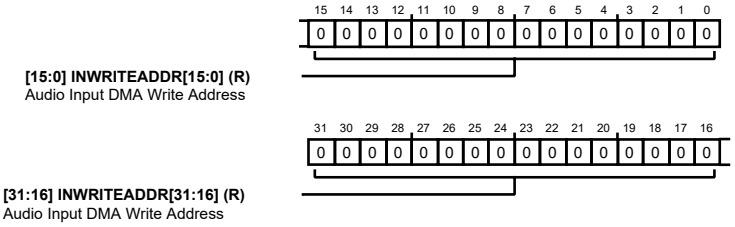


Table 298. Bit Descriptions for ADMA_IN_WRITE_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	INWRITEADDR	Audio Input DMA Write Address	0x0	R

AUDIO OUTPUT DMA CIRCULAR BUFFER BEGIN ADDRESS REGISTER

Address: 0xF00006E0 to 0xF00006E8 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CBEGINn

Beginning address of the memory region used as a circular buffer for the Output ADMA Engine, when running in Continuous mode. Ignored in Single Block mode.

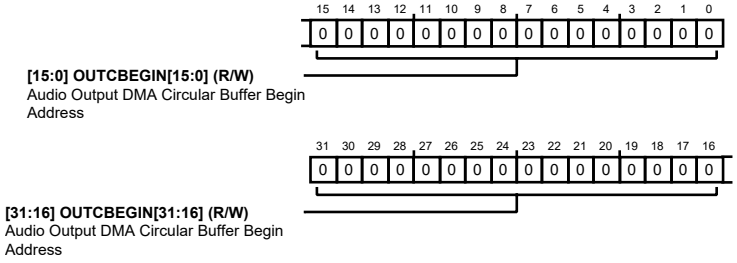


Table 299. Bit Descriptions for ADMA_OUT_CBEGINn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTCBEGIN	Audio Output DMA Circular Buffer Begin Address	0x0	R/W

AUDIO OUTPUT DMA CIRCULAR BUFFER END ADDRESS REGISTER

Address: 0xF00006F0 to 0xF00006F8 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CENDn

Ending (last) address of the memory region used as a circular buffer for the Output ADMA Engine, when running in Continuous mode. Ignored in Single Block mode.

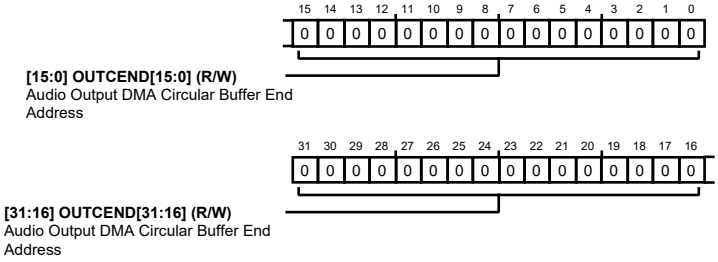


Table 300. Bit Descriptions for ADMA_OUT_CENDn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTCEND	Audio Output DMA Circular Buffer End Address	0x0	R/W

AUDIO OUTPUT DMA CHANNEL STRIDE REGISTER

Address: 0xF0000700 to 0xF0000708 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CHAN_STRIDEn

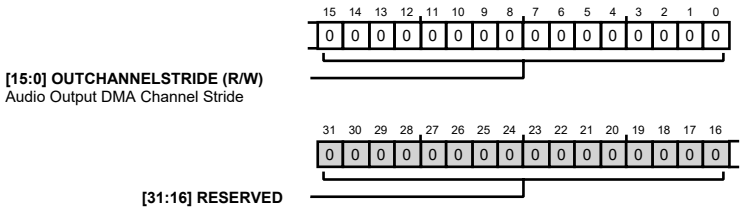


Table 301. Bit Descriptions for ADMA_OUT_CHAN_STRIDEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	OUTCHANNELSTRIDE	Audio Output DMA Channel Stride. Determines the Output ADMA Engine memory address increment after each channel is read. The units are sample counts, which are translated to bytes in the Engine (each sample count increment can be 2-4 bytes, as determined by the ADMA_IN_FORMAT register). Can be a negative number (2's complement format). Specified as an increment from the address of the previous channel, so the default is 1. Normally it will be 1 for channel interleaved mode, or equal to outBlockSize for non-interleaved mode. In circular buffer mode, the magnitude of the stride must be less than or equal to the size of the circular buffer, abs(CEnd-CBegin).	0x0	R/W

AUDIO OUTPUT DMA FRAME STRIDE REGISTER

Address: 0xF0000710 to 0xF0000718 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_FRAME_STRIDEn

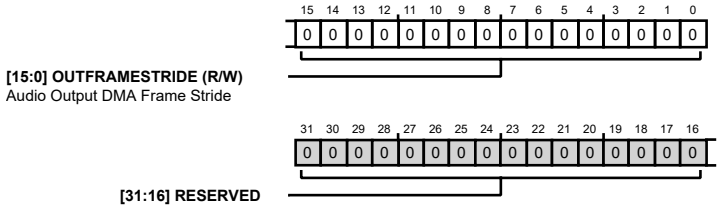


Table 302. Bit Descriptions for ADMA_OUT_FRAME_STRIDEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	OUTFRAMESTRIDE	Audio Output DMA Frame Stride. Determines the Output ADMA Engine memory address increment after each frame. (A frame is defined as the set of channels processed by an engine between frame sync pulses). The units are sample counts, which are translated to bytes in the Engine (each sample count increment can be 2-4 bytes, as determined by the ADMA_IN_FORMAT register). Can be a negative number (2's complement format). Specified as an increment from the starting address of the previous frame. The default is 0, which means each frame is read from the same memory locations as the previous frame. In circular buffer mode, the magnitude of the stride must be less than or equal to the size of the circular buffer, abs(CEnd-CBegin).	0x0	R/W

AUDIO OUTPUT DMA BLOCK SIZE REGISTER

Address: 0xF0000720 to 0xF0000728 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_BLOCK_SIZEn

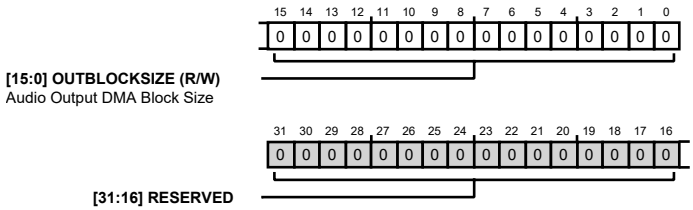


Table 303. Bit Descriptions for ADMA_OUT_BLOCK_SIZEn

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	OUTBLOCKSIZE	Audio Output DMA Block Size. Specifies the number of frame syncs processed by the Output ADMA Engine for a "block" of data. At the end of the block, the Done signal is asserted, and an interrupt is triggered (if enabled). The amount of actual memory accessed by the ADMA Engine depends also on the data format (ADMA_OUT_FORMAT) and the stride settings (ADMA_OUT_CHAN_STRIDE, ADMA_OUT_BLOCK_STRIDE).	0x0	R/W

AUDIO OUTPUT DMA BLOCK ADDRESS REGISTER

Address: 0xF0000730 to 0xF0000738 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_READ_ADDRn

Latest memory address to be accessed by the Output ADMA Engine.

Latency of the system including the AXI bus will determine when this address is actually accessed in memory.

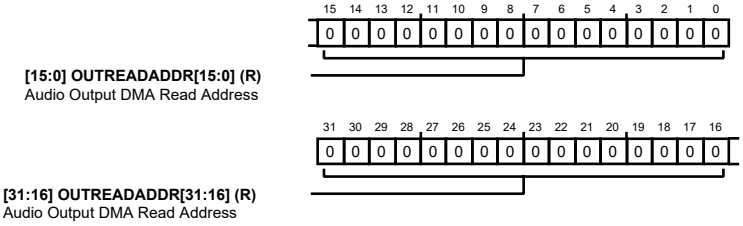


Table 304. Bit Descriptions for ADMA_OUT_READ_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTREADADDR	Audio Output DMA Read Address	0x0	R

AUDIO OUTPUT DMA CURRENT BLOCK ADDRESS REGISTER

Address: 0xF0000740 to 0xF0000748 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CURR_BLOCK_ADDRn

Starting memory address of the current block of data in process.

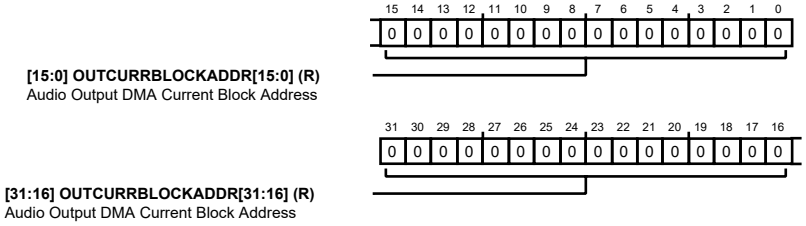


Table 305. Bit Descriptions for ADMA_OUT_CURR_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTCURRBLOCKADDR	Audio Output DMA Current Block Address	0x0	R

AUDIO OUTPUT DMA SINGLE MODE BLOCK ADDRESS REGISTER

Address: 0xF0000750 to 0xF0000758 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_SINGLE_BLOCK_ADDRn

Designates the starting memory address of the next block of samples to be read in Single Block mode only (ignored in Continuous mode).

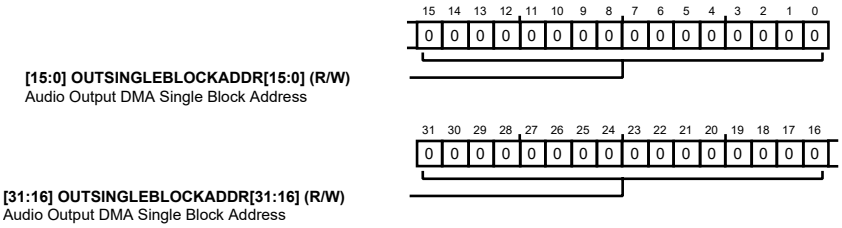


Table 306. Bit Descriptions for ADMA_OUT_SINGLE_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTSINGLEBLOCKADDR	Audio Output DMA Single Block Address	0x0	R/W

AUDIO OUTPUT DMA PREVIOUS BLOCK ADDRESS REGISTER

Address: 0xF0000760 to 0xF0000768 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_PREV_BLOCK_ADDRn

Starting memory address of the most recently completed block of data.

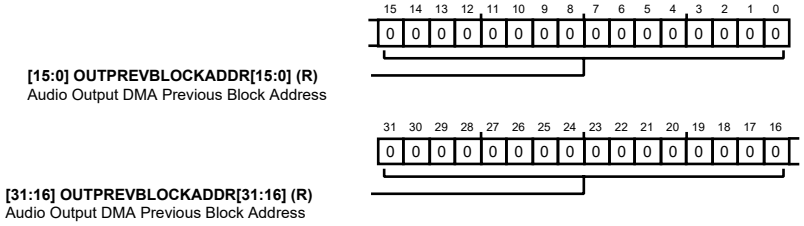


Table 307. Bit Descriptions for ADMA_OUT_PREV_BLOCK_ADDRn

Bits	Bit Name	Description	Reset	Access
[31:0]	OUTPREVBLOCKADDR	Audio Output DMA Previous Block Address	0x0	R

AUDIO DMA OUTPUT MASK REGISTER

Address: 0xF0000770 to 0xF0000778 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_MASKn

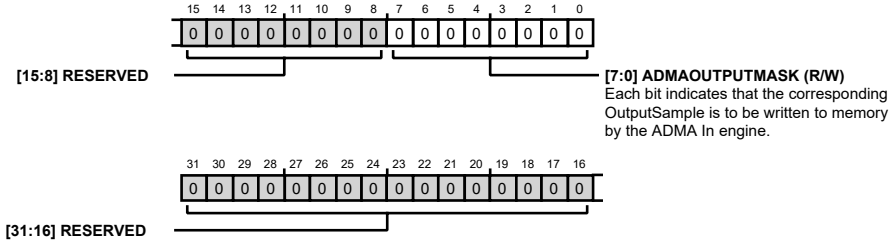


Table 308. Bit Descriptions for ADMA_OUT_MASKn

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	ADMAOUTPUTMASK	Each bit indicates that the corresponding OutputSample is to be written to memory by the ADMA In engine.	0x0	R/W

AUDIO DMA INPUT CONTROL REGISTER

Address: 0xF0000790 to 0xF0000798 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_CONTROLn

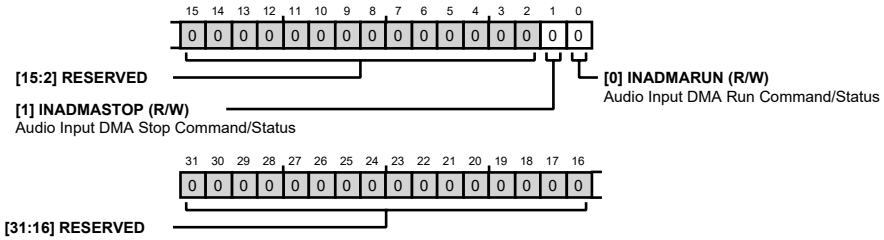


Table 309. Bit Descriptions for ADMA_IN_CONTROLn

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved	0x0	R
1	INADMASTOP	Audio Input DMA Stop Command/Status. Writing a 1 generates a pulse that initiates stopping the corresponding Audio DMA engine. The stop mode, Block or Sample, is determined by the inAdmaSingleRun bit. Reading the bit can be used to acknowledge the pulse. The Engine will stop when the program stop mode conditions are met according to inAdmaSampleStop. Note the bit may be asserted for a very short time, depending on the Engine configuration. 0: No stop signal has been received, or the Engine is not running. 1: Engine is still running, but the engine has received stop signal.	0x0	R/W
0	INADMARUN	Audio Input DMA Run Command/Status. Writing a 1 generates a pulse that starts the corresponding Audio DMA engine. The run mode, continuous or single block, is determined by the inAdmaSingleRun bit. Reading the bit indicates the engine status. This is a live bit for reading and not a sticky bit, in contrast to the inAdmaDone bit. The starting state is always the same, independent of the stopping mode or conditions. The starting address will be either inCBegin or inSingleBlockAddr depending on inAdmaSingleRun. The first channel processed will correspond to the lowest indexed asserted bit in admaInputMask, independent of the last channel processed when stopping. 0: Engine is not running, acknowledging the inAdmaStop pulse. 1: Engine is running, acknowledging the inAdmaRun pulse.	0x0	R/W

AUDIO DMA OUTPUT CONTROL REGISTER

Address: 0xF00007A0 to 0xF00007A8 (Increments of 4), Reset: 0x00000000, Name: ADMA_OUT_CONTROLn

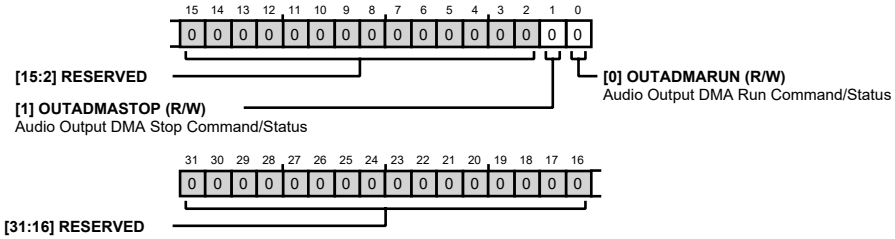


Table 310. Bit Descriptions for ADMA_OUT_CONTROLn

Bits	Bit Name	Description	Reset	Access
[31:2]	RESERVED	Reserved	0x0	R
1	OUTADMASTOP	Audio Output DMA Stop Command/Status. Writing a 1 generates a pulse that initiates stopping the corresponding Audio DMA engine. The stop mode, Block or Sample, is determined by the outAdmaSingleRun bit. Reading the bit can be used to acknowledge the pulse. The Engine will stop when the program stop mode conditions are met according to outAdmaSampleStop. Note the bit may be asserted for a very short time, depending on the Engine configuration. 0: No stop signal has been received, or the Engine is not running. 1: Engine is still running, but the engine has received stop signal.	0x0	R/W
0	OUTADMARUN	Audio Output DMA Run Command/Status. Writing a 1 generates a pulse that starts the corresponding Audio DMA engine. The run mode, continuous or single block, is determined by the outAdmaSingleRun bit. Reading the bit indicates the engine status. This is a live bit for reading and not a sticky bit, in contrast to the outAdmaDone bit. The starting state is always the same, independent of the stopping mode or conditions. The starting address will be either outCBegin or outSingleBlockAddr depending on outAdmaSingleRun. The first channel processed will correspond to the lowest indexed asserted bit in admaOutputMask, independent of the last channel processed when stopping. 0: Engine is not running, acknowledging the outAdmaStop pulse. 1: Engine is running, acknowledging the outAdmaRun pulse.	0x0	R/W

AUDIO DMA INTERRUPT CONTROL REGISTER

Address: 0xF00007B0, Reset: 0x00000000, Name: ADMA_INTERRUPT_CONTROL

Controls interrupts generated by Audio DMA, including combining Input and Output Engine interrupts.

Enabled interrupts are triggered when a block completes, defined as the number of frame syncs processed equal to the in/outBlockSize register. Completion includes waiting for pending AXI transactions associated with the corresponding Engine.

Note the admaOR signals are not used. OR'ing the Input and Output interrupts is accomplished by enabling the Input or Output interrupt. The AND signal requires both Input and Output interrupts to be enabled to work properly.

The interrupts are level-sensitive and stay asserted after the first block done signal from the corresponding Engine. Interrupts are cleared by writing to the ADMA_INTERRUPT_STATUS register.

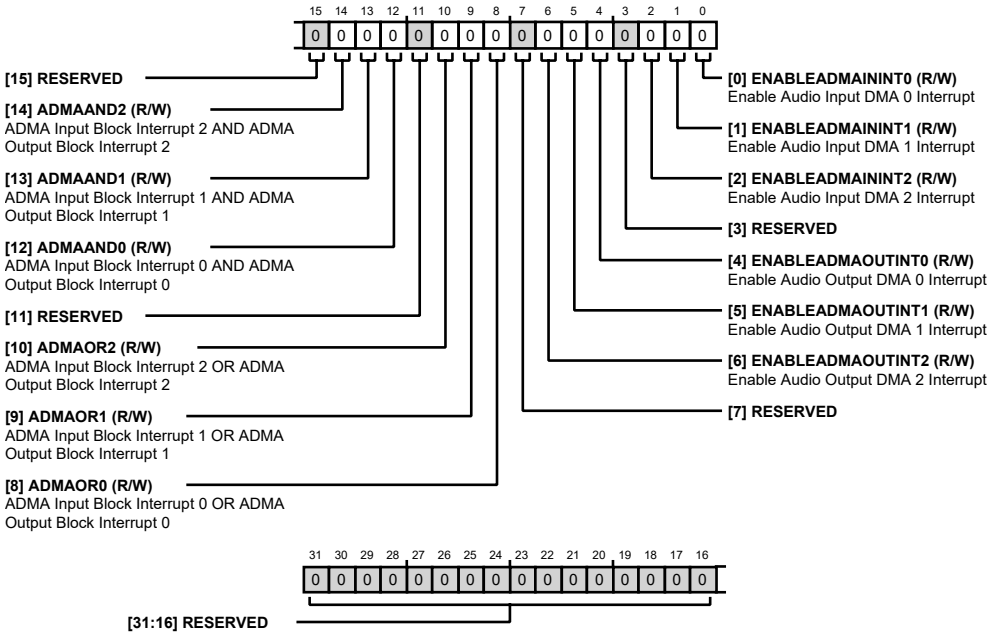


Table 311. Bit Descriptions for ADMA_INTERRUPT_CONTROL

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved	0x0	R
14	ADMAAND2	ADMA Input Block Interrupt 2 AND ADMA Output Block Interrupt 2	0x0	R/W
13	ADMAAND1	ADMA Input Block Interrupt 1 AND ADMA Output Block Interrupt 1	0x0	R/W
12	ADMAAND0	ADMA Input Block Interrupt 0 AND ADMA Output Block Interrupt 0	0x0	R/W
11	RESERVED	Reserved	0x0	R
10	ADMAOR2	ADMA Input Block Interrupt 2 OR ADMA Output Block Interrupt 2	0x0	R/W
9	ADMAOR1	ADMA Input Block Interrupt 1 OR ADMA Output Block Interrupt 1	0x0	R/W
8	ADMAOR0	ADMA Input Block Interrupt 0 OR ADMA Output Block Interrupt 0	0x0	R/W
7	RESERVED	Reserved	0x0	R
6	ENABLEADMAOUTINT2	Enable Audio Output DMA 2 Interrupt	0x0	R/W
5	ENABLEADMAOUTINT1	Enable Audio Output DMA 1 Interrupt	0x0	R/W
4	ENABLEADMAOUTINT0	Enable Audio Output DMA 0 Interrupt	0x0	R/W
3	RESERVED	Reserved	0x0	R
2	ENABLEADMAININT2	Enable Audio Input DMA 2 Interrupt	0x0	R/W
1	ENABLEADMAININT1	Enable Audio Input DMA 1 Interrupt	0x0	R/W
0	ENABLEADMAININT0	Enable Audio Input DMA 0 Interrupt	0x0	R/W

AUDIO DMA INTERRUPT STATUS REGISTER

Address: 0xF00007C0, Reset: 0x00000000, Name: ADMA_INTERRUPT_STATUS

Indicates a block of data completed, and the corresponding interrupt was enabled.

The signals exactly match the interrupt signals to the DSP.

Cleared by software (write-1-to-clear), which also clears the interrupt.

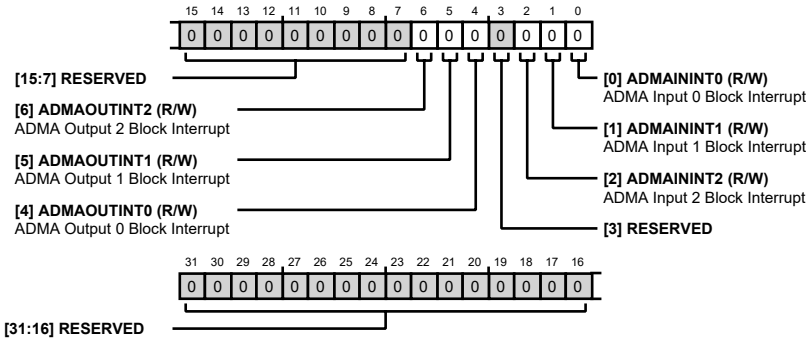


Table 312. Bit Descriptions for ADMA_INTERRUPT_STATUS

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	ADMAOUTINT2	ADMA Output 2 Block Interrupt	0x0	R/W
5	ADMAOUTINT1	ADMA Output 1 Block Interrupt	0x0	R/W
4	ADMAOUTINT0	ADMA Output 0 Block Interrupt	0x0	R/W
3	RESERVED	Reserved	0x0	R
2	ADMAININT2	ADMA Input 2 Block Interrupt	0x0	R/W
1	ADMAININT1	ADMA Input 1 Block Interrupt	0x0	R/W
0	ADMAININT0	ADMA Input 0 Block Interrupt	0x0	R/W

AUDIO DMA DONE STATUS REGISTER

Address: 0xF00007D0, Reset: 0x00000000, Name: ADMA_DONE_STATUS

Indicates a block of data completed by the corresponding Audio DMA Engine.

A block is defined as the number of frame syncs processed equal to the in/outBlockSize register. Block completion includes waiting for pending AXI transactions associated with the corresponding Engine.

Cleared by software (write-1-to-clear).

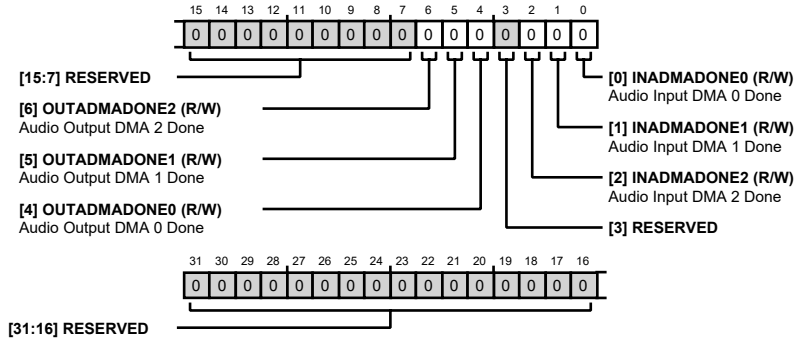


Table 313. Bit Descriptions for ADMA_DONE_STATUS

Bits	Bit Name	Description	Reset	Access
[31:7]	RESERVED	Reserved	0x0	R
6	OUTADMADONE2	Audio Output DMA 2 Done	0x0	R/W
5	OUTADMADONE1	Audio Output DMA 1 Done	0x0	R/W
4	OUTADMADONE0	Audio Output DMA 0 Done	0x0	R/W
3	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
2	INADMADONE2	Audio Input DMA 2 Done	0x0	R/W
1	INADMADONE1	Audio Input DMA 1 Done	0x0	R/W
0	INADMADONE0	Audio Input DMA 0 Done	0x0	R/W

AUDIO INPUT DMA CHANNELS 0 TO 3 ROUTING REGISTER

Address: 0xF0000800 to 0xF0000808 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_ROUTE0n

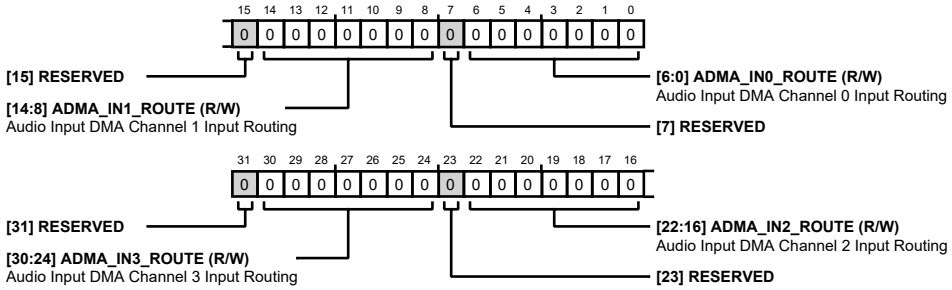


Table 314. Bit Descriptions for ADMA_IN_ROUTE0n

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved	0x0	R
[30:24]	ADMA_IN3_ROUTE	Audio Input DMA Channel 3 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9		

Bits	Bit Name	Description	Reset	Access
		1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
23	RESERVED	Reserved	0x0	R
[22:16]	ADMA_IN2_ROUTE	Audio Input DMA Channel 2 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0		

Bits	Bit Name	Description	Reset	Access
		1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
15	RESERVED	Reserved	0x0	R
[14:8]	ADMA_IN1_ROUTE	Audio Input DMA Channel 1 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1		

Bits	Bit Name	Description	Reset	Access
		1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
7	RESERVED	Reserved.	0x0	R
[6:0]	ADMA_IN0_ROUTE	Audio Input DMA Channel 0 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2		

Bits	Bit Name	Description	Reset	Access
		1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		

AUDIO INPUT DMA CHANNELS 4 TO 7 ROUTING REGISTER

Address: 0xF0000810 to 0xF0000818 (Increments of 4), Reset: 0x00000000, Name: ADMA_IN_ROUTE1n

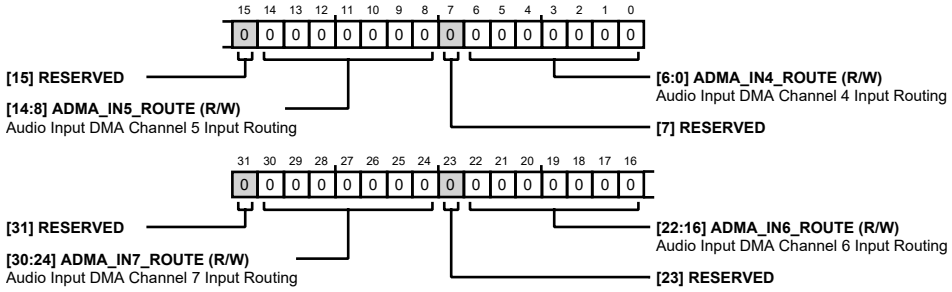


Table 315. Bit Descriptions for ADMA_IN_ROUTE1n

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved	0x0	R
[30:24]	ADMA_IN7_ROUTE	Audio Input DMA Channel 7 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 0111010: ADC Channel 2.		

Bits	Bit Name	Description	Reset	Access
		0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
23	RESERVED	Reserved	0x0	R
[22:16]	ADMA_IN6_ROUTE	Audio Input DMA Channel 6 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0		

Bits	Bit Name	Description	Reset	Access
		0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
15	RESERVED	Reserved	0x0	R
[14:8]	ADMA_IN5_ROUTE	Audio Input DMA Channel 5 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1		

Bits	Bit Name	Description	Reset	Access
		0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		
7	RESERVED	Reserved	0x0	R
[6:0]	ADMA_IN4_ROUTE	Audio Input DMA Channel 4 Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6 0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2		

Bits	Bit Name	Description	Reset	Access
		0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4 1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		

AUDIO DMA WRITE ERROR CODE (AXI WRITE TRANSACTION ADDRESS) REGISTER

Address: 0xF000081C, Reset: 0x00000000, Name: ADMA_WR_ERR_CODE

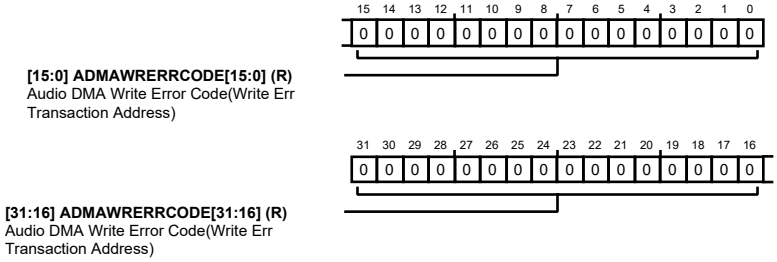


Table 316. Bit Descriptions for ADMA_WR_ERR_CODE

Bits	Bit Name	Description	Reset	Access
[31:0]	ADMAWRERRCODE	Audio DMA Write Error Code (Write Err Transaction Address)	0x0	R

AUDIO DMA READ ERROR CODE (AXI READ TRANSACTION ADDRESS) REGISTER

Address: 0xF0000820, Reset: 0x00000000, Name: ADMA_RD_ERR_CODE

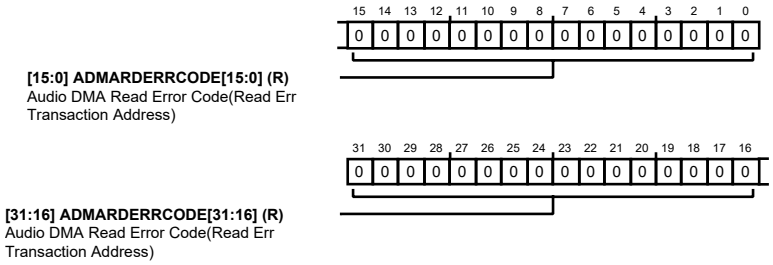


Table 317. Bit Descriptions for ADMA_RD_ERR_CODE

Bits	Bit Name	Description	Reset	Access
[31:0]	ADMARDERRCODE	Audio DMA Read Error Code (Read Err Transaction Address)	0x0	R

AUDIO DMA NAN ERROR CODE (FRACTION NAN VALUE) REGISTER

Address: 0xF0000824, Reset: 0x00000000, Name: ADMA_NAN_ERR_CODE

{sign_bit, fraction, 1'b0, eng_ix_samp, chan_ix_samp} {1 bit, 23 bits, 1 bit, 2 bits, 5 bits}

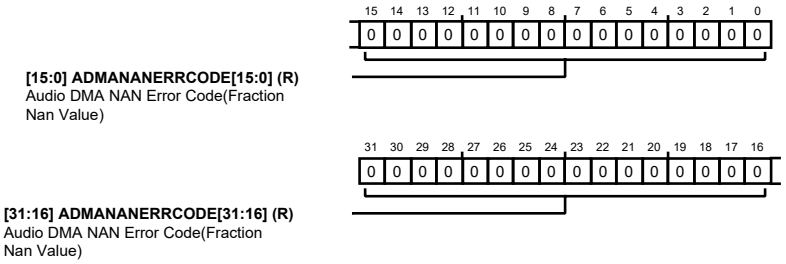


Table 318. Bit Descriptions for ADMA_NAN_ERR_CODE

Bits	Bit Name	Description	Reset	Access
[31:0]	ADMANANERRCODE	Audio DMA NAN Error Code (Fraction Nan Value)	0x0	R

AUDIO DMA ERROR ACKNOWLEDGE REGISTER

Address: 0xF0000828, Reset: 0x00000000, Name: ADMA_ERR_ACK

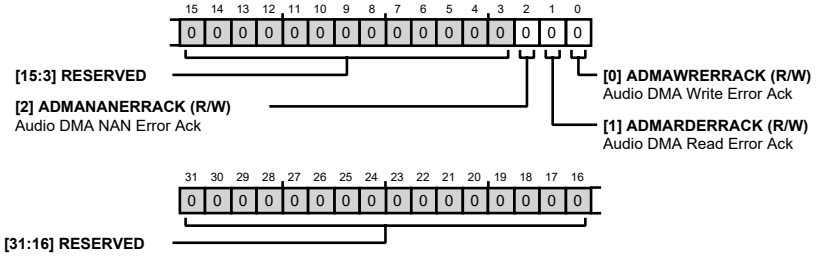


Table 319. Bit Descriptions for ADMA_ERR_ACK

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved	0x0	R
2	ADMANANERRACK	Audio DMA NAN Error Ack. (Auto Sync Clear bit)	0x0	R/W
1	ADMARDERRACK	Audio DMA Read Error Ack. (Auto Sync Clear bit)	0x0	R/W
0	ADMAWRERRACK	Audio DMA Write Error Ack. (Auto Sync Clear bit)	0x0	R/W

HOST INFORMATION REGISTER

Address: 0xF0000C68, Reset: 0x00100000, Name: HOST_INFO

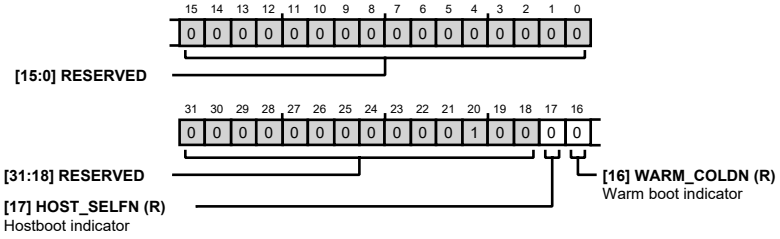


Table 320. Bit Descriptions for HOST_INFO

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved	0x4	R
17	HOST_SELFN	Host Boot Indicator 0: Self boot. 1: Host boot.	0x0	R
16	WARM_COLDN	Warm Boot Indicator 0: Cold boot. 1: Warm boot.	0x0	R
[15:0]	RESERVED	Reserved	0x0	R

FIFO_RESET_N REGISTER

Address: 0xF0000D00, Reset: 0xFFFFFFFF, Name: AMAP_FIFO_RESET_REG

This register is used to give reset to the FIFO used inside. Its asynchronous reset and active low.

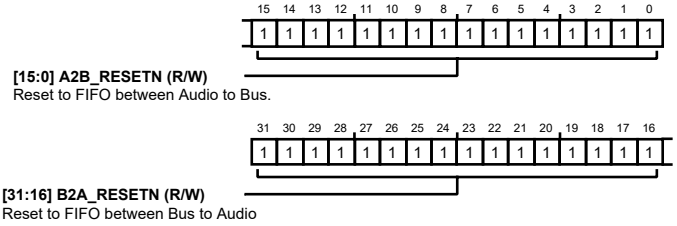


Table 321. Bit Descriptions for AMAP_FIFO_RESET_REG

Bits	Bit Name	Description	Reset	Access
[31:16]	B2A_RESETN	Reset to FIFO between Bus to Audio.	0xFFFF	R/W
[15:0]	A2B_RESETN	Reset to FIFO between Audio to Bus.	0xFFFF	R/W

CHANNEL_SEL REGISTER

Address: 0xF0000D04, Reset: 0x00000000, Name: AMAP_CHANNEL_SEL_REG

This Register is used to Mask data between Audio Peripherals and FIFO

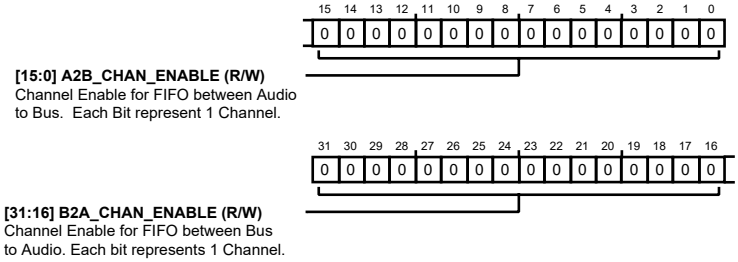


Table 322. Bit Descriptions for AMAP_CHANNEL_SEL_REG

Bits	Bit Name	Description	Reset	Access
[31:16]	B2A_CHAN_ENABLE	Channel Enable for FIFO between Bus to Audio. Each bit represents 1 Channel. 1: Enable 0: Disable	0x0	R/W
[15:0]	A2B_CHAN_ENABLE	Channel Enable for FIFO between Audio to Bus. Each Bit represents 1 Channel. 1: Enable 0: Disable	0x0	R/W

AMAP_FLAG_THRESHOLD REGISTER

Address: 0xF0000D08 to 0xF0000D44 (Increments of 4), Reset: 0x00006262, Name: AMAP_FLAG_THRESHOLD_REGn

This Register is used to Provide Threshold for Almost Empty and Almost full Flag

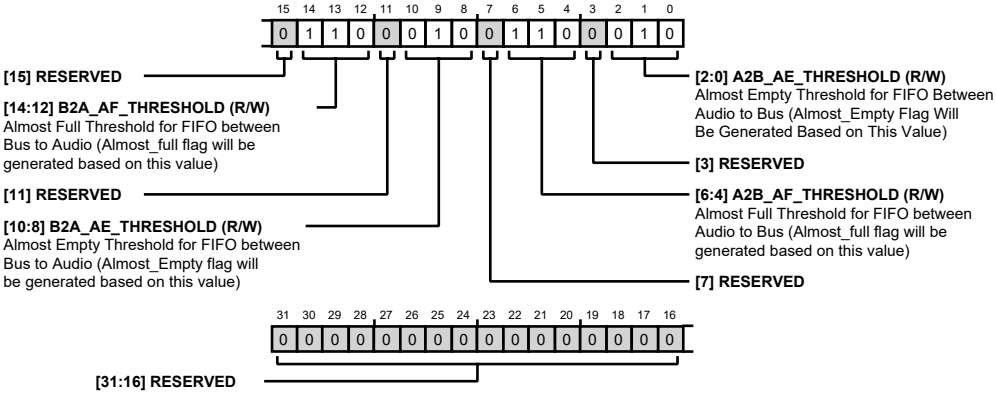


Table 323. Bit Descriptions for AMAP_FLAG_THRESHOLD_REGn

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved	0x0	R
[14:12]	B2A_AF_THRESHOLD	Almost Full Threshold for FIFO Between Bus to Audio (Almost_full flag will be generated based on this value).	0x6	R/W
11	RESERVED	Reserved.	0x0	R
[10:8]	B2A_AE_THRESHOLD	Almost Empty Threshold for FIFO Between Bus to Audio (Almost_Empty flag will be generated based on this value).	0x2	R/W
7	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
[6:4]	A2B_AF_THRESHOLD	Almost Full Threshold for FIFO Between Audio to Bus (Almost_full flag will be generated based on this value).	0x6	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	A2B_AE_THRESHOLD	Almost Empty Threshold for FIFO Between Audio to Bus (Almost_Empty Flag will be generated based on this value).	0x2	R/W

CONFIG_REG REGISTER

Address: 0xF0000D48 to 0xF0000D84 (Increments of 4), Reset: 0x00000303, Name: AMAP_CONFIG_REGn

This Register is used to configure format of Each FIFO.

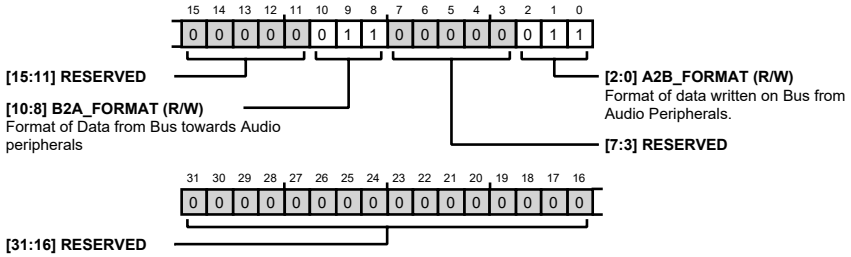


Table 324. Bit Descriptions for AMAP_CONFIG_REGn

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved	0x0	R
[10:8]	B2A_FORMAT	Format of Data from Bus towards Audio peripherals. 000: 1D31 001: 1D15 010: 9D23 011: 1D23 101: FLOAT	0x3	R/W
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	A2B_FORMAT	Format of data written on Bus from Audio Peripherals. 000: 1D31 001: 1D15 010: 9D23 011: 1D23 101: FLOAT	0x3	R/W

FLAG REGISTER

Address: 0xF0000D88 to 0xF0000DC4 (Increments of 4), Reset: 0x00000303, Name: AMAP_FLAG_REGn

This is Error status register of FIFO. Depth of FIFO used is 8. All flags are being calculated based on this.

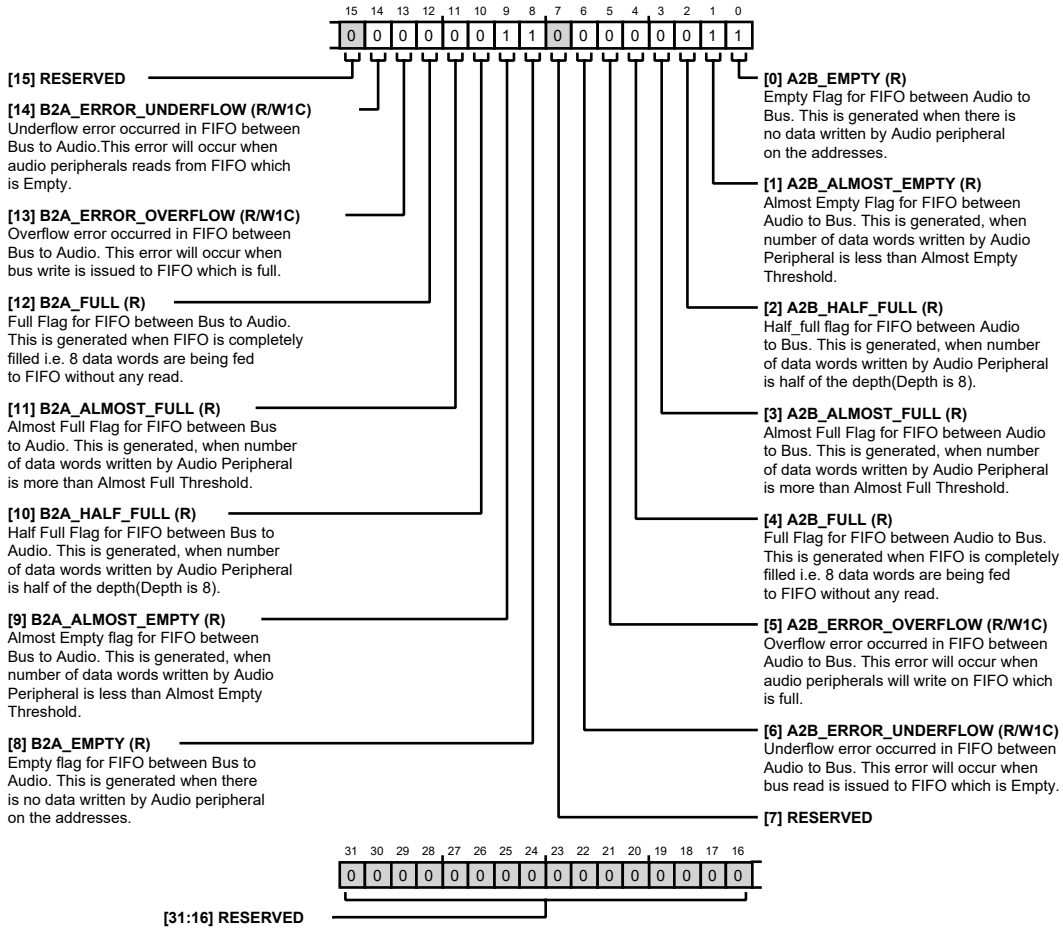


Table 325. Bit Descriptions for AMAP_FLAG_REGn

Bits	Bit Name	Description	Reset	Access
[31:15]	RESERVED	Reserved	0x0	R
14	B2A_ERROR_UNDERFLOW	Underflow error occurred in FIFO between Bus to Audio. This error will occur when audio peripherals read from FIFO which is Empty.	0x0	R/W1C
13	B2A_ERROR_OVERFLOW	Overflow error occurred in FIFO between Bus to Audio. This error will occur when bus write is issued to FIFO which is full.	0x0	R/W1C
12	B2A_FULL	Full Flag for FIFO between Bus to Audio. This is generated when FIFO is filled i.e., 8 data words are being fed to FIFO without any read.	0x0	R
11	B2A_ALMOST_FULL	Almost Full Flag for FIFO between Bus to Audio. This is generated, when number of data words written by Audio Peripheral is more than Almost Full Threshold.	0x0	R
10	B2A_HALF_FULL	Half Full Flag for FIFO between Bus to Audio. This is generated, when number of data words written by Audio Peripheral is half of the depth (Depth is 8).	0x0	R
9	B2A_ALMOST_EMPTY	Almost Empty flag for FIFO between Bus to Audio. This is generated, when number of data words written by Audio Peripheral is less than Almost Empty Threshold.	0x1	R

Bits	Bit Name	Description	Reset	Access
8	B2A_EMPTY	Empty flag for FIFO between Bus to Audio. This is generated when there is no data written by Audio peripheral on the addresses.	0x1	R
7	RESERVED	Reserved	0x0	R
6	A2B_ERROR_UNDERFLOW	Underflow error occurred in FIFO between Audio to Bus. This error will occur when bus read is issued to FIFO which is Empty.	0x0	R/W1C
5	A2B_ERROR_OVERFLOW	Overflow error occurred in FIFO between Audio to Bus. This error will occur when audio peripherals write on FIFO which is full.	0x0	R/W1C
4	A2B_FULL	Full Flag for FIFO between Audio to Bus. This is generated when FIFO is filled i.e., 8 data words are being fed to FIFO without any read.	0x0	R
3	A2B_ALMOST_FULL	Almost Full Flag for FIFO between Audio to Bus. This is generated, when number of data words written by Audio Peripheral is more than Almost Full Threshold.	0x0	R
2	A2B_HALF_FULL	Half full flag for FIFO between Audio to Bus. This is generated, when number of data words written by Audio Peripheral is half of the depth (Depth is 8).	0x0	R
1	A2B_ALMOST_EMPTY	Almost Empty Flag for FIFO between Audio to Bus. This is generated, when number of data words written by Audio Peripheral is less than Almost Empty Threshold.	0x1	R
0	A2B_EMPTY	Empty Flag for FIFO between Audio to Bus. This is generated when there is no data written by Audio peripheral on the addresses.	0x1	R

ROUTE REGISTER

Address: 0xF0000E08 to 0xF0000E44 (Increments of 4), Reset: 0x00000900, Name: AMAP_ROUTE_REGn

IN/OUT Route Select Register

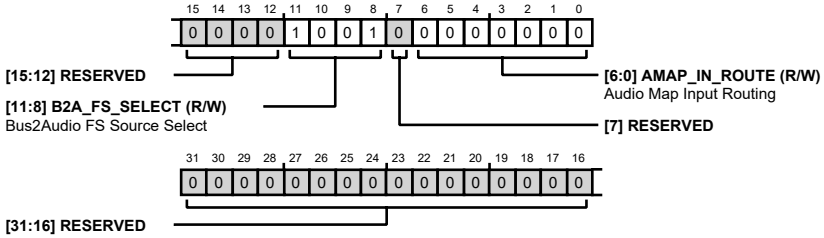


Table 326. Bit Descriptions for AMAP_ROUTE_REGn

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
[11:8]	B2A_FS_SELECT	Bus2Audio FS Source Select 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected		
7	RESERVED	Reserved	0x0	R
[6:0]	AMAP_IN_ROUTE	Audio Map Input Routing 0000000: Serial Port 0 Channel 0 0000001: Serial Port 0 Channel 1 0000010: Serial Port 0 Channel 2 0000011: Serial Port 0 Channel 3 0000100: Serial Port 0 Channel 4 0000101: Serial Port 0 Channel 5 0000110: Serial Port 0 Channel 6 0000111: Serial Port 0 Channel 7 0001000: Serial Port 0 Channel 8 0001001: Serial Port 0 Channel 9 0001010: Serial Port 0 Channel 10 0001011: Serial Port 0 Channel 11 0001100: Serial Port 0 Channel 12 0001101: Serial Port 0 Channel 13 0001110: Serial Port 0 Channel 14 0001111: Serial Port 0 Channel 15 0010000: Serial Port 1 Channel 0 0010001: Serial Port 1 Channel 1 0010010: Serial Port 1 Channel 2 0010011: Serial Port 1 Channel 3 0010100: Serial Port 1 Channel 4 0010101: Serial Port 1 Channel 5 0010110: Serial Port 1 Channel 6 0010111: Serial Port 1 Channel 7 0011000: Serial Port 1 Channel 8 0011001: Serial Port 1 Channel 9 0011010: Serial Port 1 Channel 10 0011011: Serial Port 1 Channel 11 0011100: Serial Port 1 Channel 12 0011101: Serial Port 1 Channel 13 0011110: Serial Port 1 Channel 14 0011111: Serial Port 1 Channel 15 0100000: FastDSP Channel 0 0100001: FastDSP Channel 1 0100010: FastDSP Channel 2 0100011: FastDSP Channel 3 0100100: FastDSP Channel 4 0100101: FastDSP Channel 5 0100110: FastDSP Channel 6	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0100111: FastDSP Channel 7 0101000: FastDSP Channel 8 0101001: FastDSP Channel 9 0101010: FastDSP Channel 10 0101011: FastDSP Channel 11 0101100: FastDSP Channel 12 0101101: FastDSP Channel 13 0101110: FastDSP Channel 14 0101111: FastDSP Channel 15 0110000: Input ASRC 0 Channel 0 0110001: Input ASRC 0 Channel 1 0110010: Input ASRC 0 Channel 2 0110011: Input ASRC 0 Channel 3 0110100: Input ASRC 1 Channel 0 0110101: Input ASRC 1 Channel 1 0110110: Input ASRC 1 Channel 2 0110111: Input ASRC 1 Channel 3 0111000: ADC Channel 0 0111001: ADC Channel 1 0111010: ADC Channel 2 0111011: Digital Microphone Channel 0 0111100: Digital Microphone Channel 1 0111101: Digital Microphone Channel 2 0111110: Digital Microphone Channel 3 0111111: Digital Microphone Channel 4 1000000: Digital Microphone Channel 5 1000001: Digital Microphone Channel 6 1000010: Digital Microphone Channel 7 1000011: Digital Microphone Channel 8 1000100: Digital Microphone Channel 9 1000101: Fast to Slow Decimator Channel 0 1000110: Fast to Slow Decimator Channel 1 1000111: Fast to Slow Decimator Channel 2 1001000: Fast to Slow Decimator Channel 3 1001001: Fast to Slow Decimator Channel 4 1001010: Fast to Slow Decimator Channel 5 1001011: Fast to Slow Decimator Channel 6 1001100: Fast to Slow Decimator Channel 7 1001101: Slow to Fast Interpolator Channel 0 1001110: Slow to Fast Interpolator Channel 1 1001111: Slow to Fast Interpolator Channel 2 1010000: Slow to Fast Interpolator Channel 3 1010001: Slow to Fast Interpolator Channel 4		

Bits	Bit Name	Description	Reset	Access
		1010010: Slow to Fast Interpolator Channel 5 1010011: Slow to Fast Interpolator Channel 6 1010100: Slow to Fast Interpolator Channel 7		

ERROR STATUS REGISTER

Address: 0xF0000E48, Reset: 0x00000000, Name: AMAP_ERROR_STATUS_REG

Error Status Register

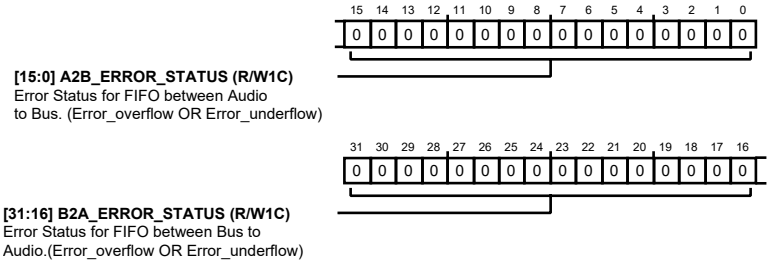


Table 327. Bit Descriptions for AMAP_ERROR_STATUS_REG

Bits	Bit Name	Description	Reset	Access
[31:16]	B2A_ERROR_STATUS	Error Status for FIFO between Bus to Audio. (Error_overflow OR Error_underflow). 0: Normal operation. 1: Error occurred.	0x0	R/W1C
[15:0]	A2B_ERROR_STATUS	Error Status for FIFO between Audio to Bus. (Error_overflow OR Error_underflow). 0: Normal operation. 1: Error occurred.	0x0	R/W1C

INTERRUPT MASK REGISTER

Address: 0xF0000E4C, Reset: 0x00000000, Name: AMAP_INTERRUPT_MASK_REG

Interrupt Mask Register

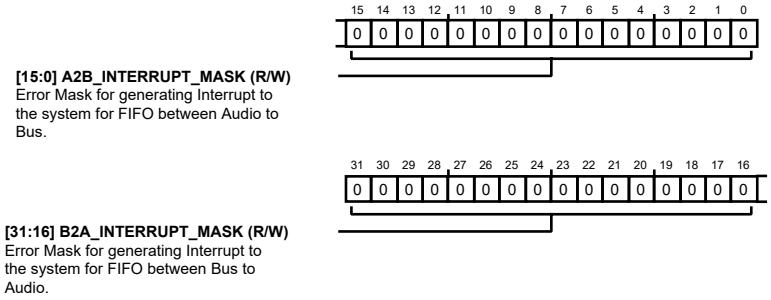


Table 328. Bit Descriptions for AMAP_INTERRUPT_MASK_REG

Bits	Bit Name	Description	Reset	Access
[31:16]	B2A_INTERRUPT_MASK	Error Mask for generating Interrupt to the system for FIFO between Bus to Audio. 0: Interrupt disable. 1: Interrupt enable.	0x0	R/W
[15:0]	A2B_INTERRUPT_MASK	Error Mask for generating Interrupt to the system for FIFO between Audio to Bus. 0: Interrupt disable. 1: Interrupt enable.	0x0	R/W

INTERRUPT STATUS REGISTER

Address: 0xF0000E50, Reset: 0x00000000, Name: AMAP_INTERRUPT_STATUS_REG

Interrupt Status Register

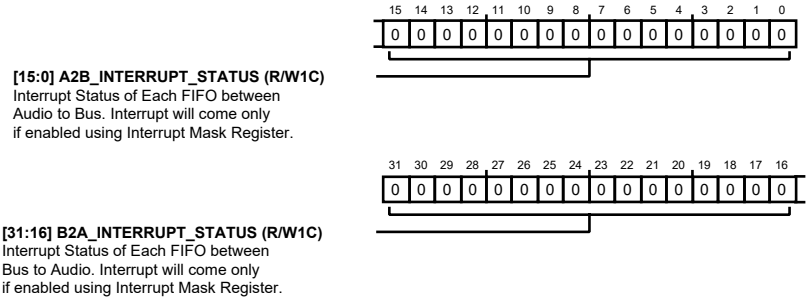


Table 329. Bit Descriptions for AMAP_INTERRUPT_STATUS_REG

Bits	Bit Name	Description	Reset	Access
[31:16]	B2A_INTERRUPT_STATUS	Interrupt Status of Each FIFO between Bus to Audio. Interrupt will come only if enabled using Interrupt Mask Register.	0x0	R/W1C
[15:0]	A2B_INTERRUPT_STATUS	Interrupt Status of Each FIFO between Audio to Bus. Interrupt will come only if enabled using Interrupt Mask Register.	0x0	R/W1C

ADMA POWER CONTROLS FOR ADMA0,1,2 REGISTER

Address: 0xF0000F00, Reset: 0x00000000, Name: ADMA_PWR

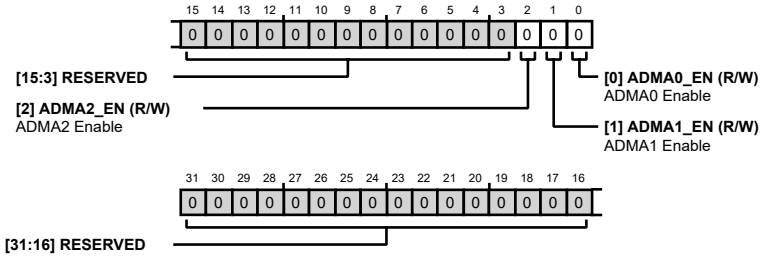


Table 330. Bit Descriptions for ADMA_PWR

Bits	Bit Name	Description	Reset	Access
[31:3]	RESERVED	Reserved	0x0	R
2	ADMA2_EN	ADMA2 Enable 0: ADC Channel 0 Powered Off 1: ADC Channel 0 Powered On	0x0	R/W
1	ADMA1_EN	ADMA1 Enable 0: ADC Channel 0 Powered Off 1: ADC Channel 0 Powered On	0x0	R/W
0	ADMA0_EN	ADMA0 Enable 0: ADC Channel 0 Powered Off 1: ADC Channel 0 Powered On	0x0	R/W

AMAP CLK ENABLE REGISTER

Address: 0xF0000F04, Reset: 0x00000000, Name: AMAP_PWR

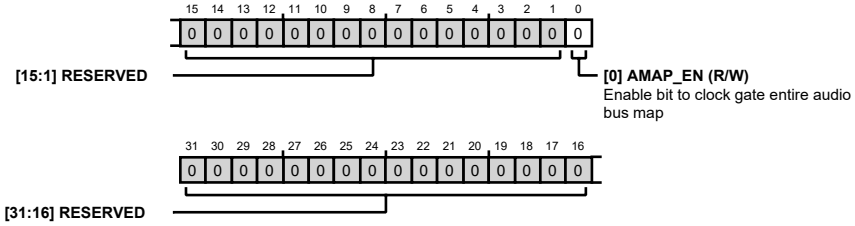


Table 331. Bit Descriptions for AMAP_PWR

Bits	Bit Name	Description	Reset	Access
[31:1]	RESERVED	Reserved	0x0	R
0	AMAP_EN	Enable bit to clock gate entire audio bus map.	0x0	R/W

SAMPLE RATE SELECT REGISTER1 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F50, Reset: 0x00090909, Name: FS_SELECT_REG1

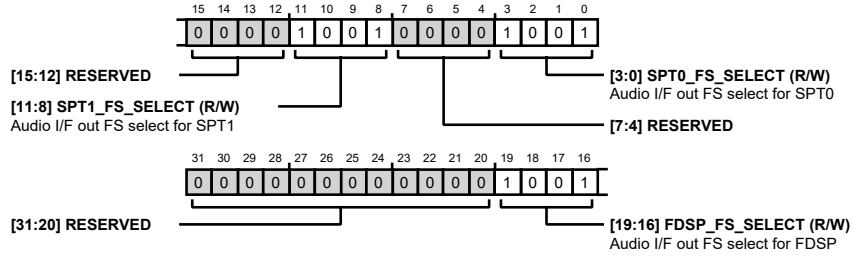


Table 332. Bit Descriptions for FS_SELECT_REG1

Bits	Bit Name	Description	Reset	Access
[31:20]	RESERVED	Reserved	0x0	R
[19:16]	FDSP_FS_SELECT	Audio I/F out FS select for FDSP 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected		
[15:12]	RESERVED	Reserved	0x0	R
[11:8]	SPT1_FS_SELECT	Audio I/F Out FS Select for SPT1 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	SPT0_FS_SELECT	Audio I/F Out FS Select for SPT0 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER2 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F54, Reset: 0x00000909, Name: FS_SELECT_REG2

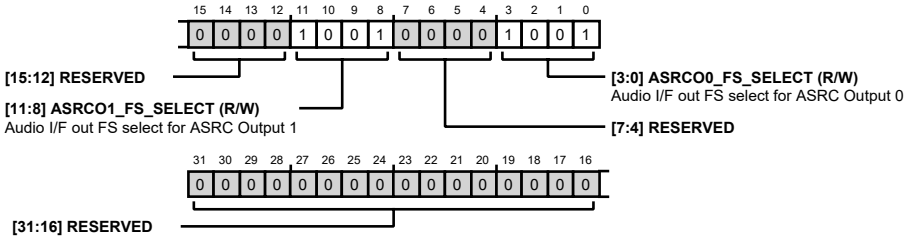


Table 333. Bit Descriptions for FS_SELECT_REG2

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
[11:8]	ASRCO1_FS_SELECT	Audio I/F Out FS Select for ASRC Output 1 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	ASRCO0_FS_SELECT	Audio I/F Out FS Select for ASRC Output 0 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER3 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F58, Reset: 0x09090909, Name: FS_SELECT_REG3

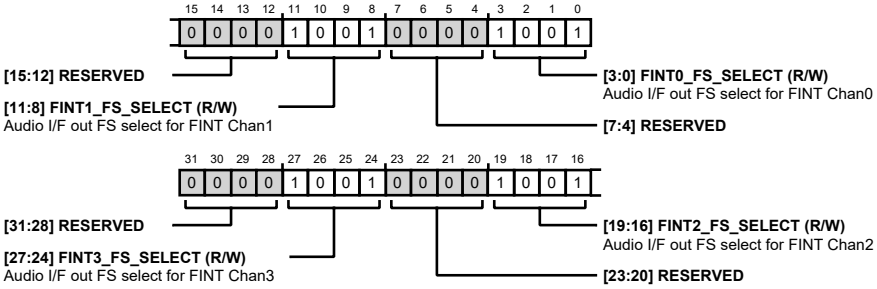


Table 334. Bit Descriptions for FS_SELECT_REG3

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved	0x0	R
[27:24]	FINT3_FS_SELECT	Audio I/F Out FS Select for FINT Chan3 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected		
[23:20]	RESERVED	Reserved	0x0	R
[19:16]	FINT2_FS_SELECT	Audio I/F Out FS Select for FINT Chan2 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[15:12]	RESERVED	Reserved	0x0	R
[11:8]	FINT1_FS_SELECT	Audio I/F Out FS Select for FINT Chan1 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	FINT0_FS_SELECT	Audio I/F Out FS Select for FINT Chan0 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER4 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F5C, Reset: 0x09090909, Name: FS_SELECT_REG4

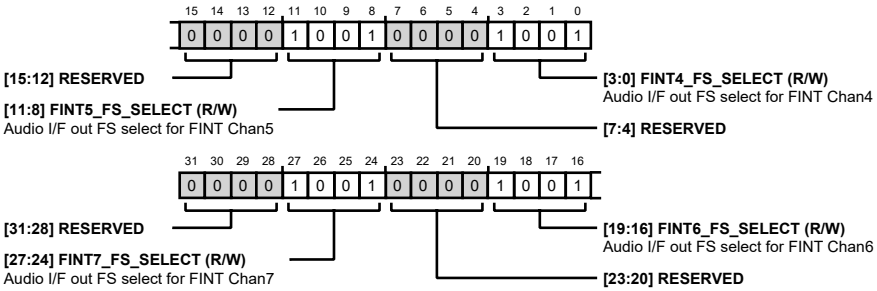


Table 335. Bit Descriptions for FS_SELECT_REG4

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved	0x0	R
[27:24]	FINT7_FS_SELECT	Audio I/F Out FS Select for FINT Chan7 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[23:20]	RESERVED	Reserved	0x0	R
[19:16]	FINT6_FS_SELECT	Audio I/F Out FS Select for FINT Chan6 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[15:12]	RESERVED	Reserved	0x0	R
[11:8]	FINT5_FS_SELECT	Audio I/F Out FS Select for FINT Chan5 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected		
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	FINT4_FS_SELECT	Audio I/F Out FS Select for FINT Chan4 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER5 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F60, Reset: 0x09090909, Name: FS_SELECT_REG5

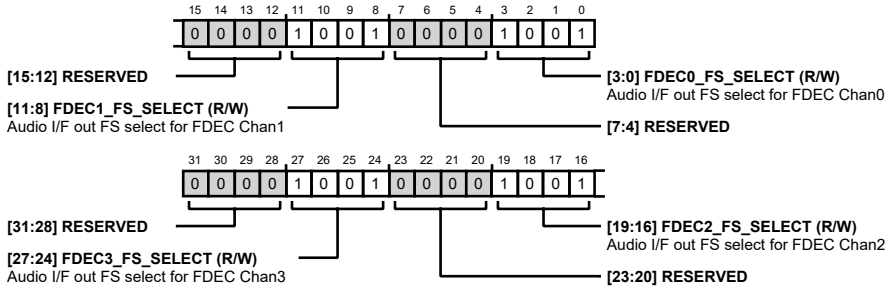


Table 336. Bit Descriptions for FS_SELECT_REG5

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved	0x0	R
[27:24]	FDEC3_FS_SELECT	Audio I/F Out FS Select for FDEC Chan3 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[23:20]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
[19:16]	FDEC2_FS_SELECT	Audio I/F Out FS Select for FDEC Chan2 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[15:12]	RESERVED	Reserved	0x0	R
[11:8]	FDEC1_FS_SELECT	Audio I/F Out FS Select for FDEC Chan1 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	FDEC0_FS_SELECT	Audio I/F Out FS Select for FDEC Chan0 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER6 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F64, Reset: 0x09090909, Name: FS_SELECT_REG6

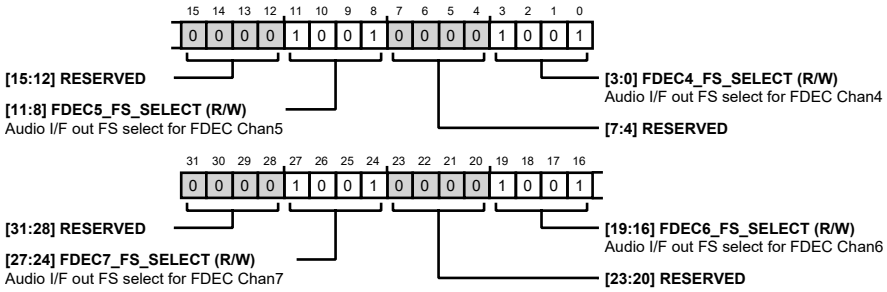


Table 337. Bit Descriptions for FS_SELECT_REG6

Bits	Bit Name	Description	Reset	Access
[31:28]	RESERVED	Reserved	0x0	R
[27:24]	FDEC7_FS_SELECT	Audio I/F Out FS Select for FDEC Chan7 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[23:20]	RESERVED	Reserved	0x0	R
[19:16]	FDEC6_FS_SELECT	Audio I/F Out FS Select for FDEC Chan6 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[15:12]	RESERVED	Reserved	0x0	R
[11:8]	FDEC5_FS_SELECT	Audio I/F Out FS Select for FDEC Chan5 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate	0x9	R/W

Bits	Bit Name	Description	Reset	Access
		0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected		
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	FDEC4_FS_SELECT	Audio I/F Out FS Select for FDEC Chan4 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

SAMPLE RATE SELECT REGISTER7 FOR AUDIO INTERFACE FROM XTENSA

Address: 0xF0000F68, Reset: 0x00090909, Name: FS_SELECT_REG7

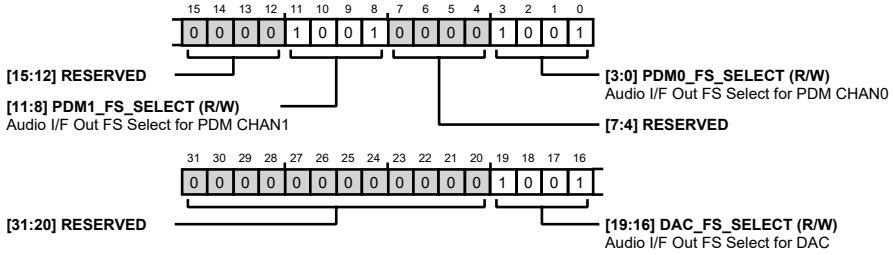


Table 338. Bit Descriptions for FS_SELECT_REG7

Bits	Bit Name	Description	Reset	Access
[31:20]	RESERVED	Reserved	0x0	R
[19:16]	DAC_FS_SELECT	Audio I/F Out FS Select for DAC 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[15:12]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
[11:8]	PDM1_FS_SELECT	Audio I/F Out FS Select for PDM CHAN1 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	PDM0_FS_SELECT	Audio I/F Out FS Select for PDM CHAN0 0000: 8KHz Sample Rate 0001: 12KHz Sample Rate 0010: 16KHz Sample Rate 0011: 24KHz Sample Rate 0100: 48KHz Sample Rate 0101: 96KHz Sample Rate 0110: 192KHz Sample Rate 0111: 384KHz Sample Rate 1000: 768KHz Sample Rate 1001: FS Source Not Connected	0x9	R/W

WATCHDOG MAXIMUM COUNT AND PRESCALE REGISTER

Address: 0xF00011FC, Reset: 0x00000000, Name: WATCHDOG

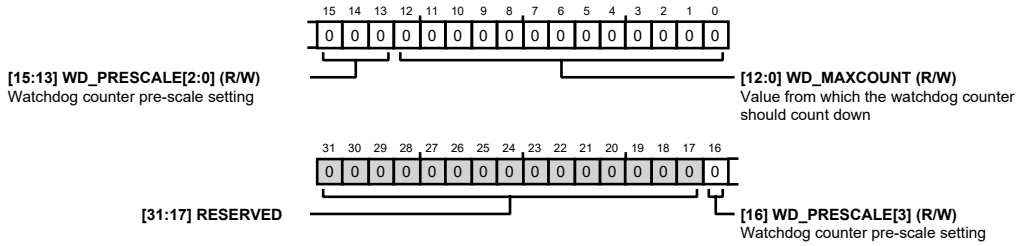


Table 339. Bit Descriptions for WATCHDOG

Bits	Bit Name	Description	Reset	Access
[31:17]	RESERVED	Reserved	0x0	R
[16:13]	WD_PRESCALE	Watchdog Counter Pre-Scale Setting 0000: Increment every 64 clock cycles. 0001: Increment every 128 clock cycles. 0010: Increment every 256 clock cycles. 0011: Increment every 512 clock cycles. 0100: Increment every 1024 clock cycles. 0101: Increment every 2048 clock cycles.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		0110: Increment every 4096 clock cycles. 0111: Increment every 8k clock cycles. 1000: Increment every 16k clock cycles. 1001: Increment every 32k clock cycles. 1010: Increment every 65k clock cycles. 1011: Increment every 131k clock cycles.		
[12:0]	WD_MAXCOUNT	Value from which the watchdog counter should count down.	0x0	R/W

REGISTER DETAILS: SERIAL PERIPHERAL INTERFACE (SPI)

CONTROL REGISTER

Address: 0xF0010004, Reset: 0x00000040, Name: CTL

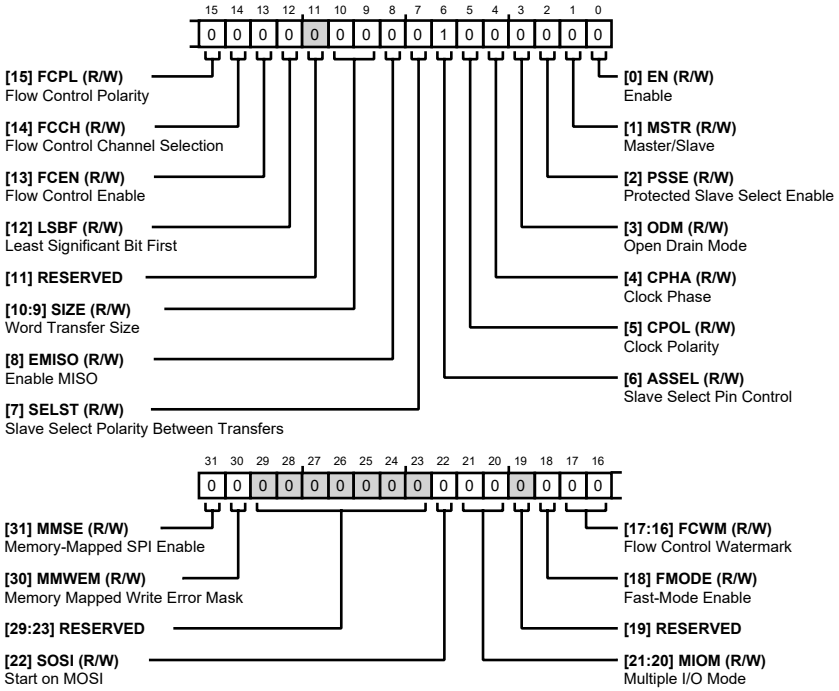


Table 340. Bit Descriptions for CTL

Bits	Bit Name	Description	Reset	Access
31	MMSE	Memory-Mapped SPI Enable 0: Hardware automated access of memory-mapped SPI memory disabled. 1: Hardware-automated access of memory-mapped SPI memory enabled.	0x0	R/W
30	MMWEM	Memory Mapped Write Error Mask 0: Write error response returned upon write attempts to memory-mapped SPI memory. 1: Write error response masked (not returned) upon write attempts to memory-mapped SPI memory.	0x0	R/W
[29:23]	RESERVED	Reserved	0x0	R
22	SOSI	Start on MOSI. This bit is valid only when MIOM is enabled for either DIOM or QIOM, and this bit selects the starting pin and the bit placement on pins for these modes. 0: Start on MISO (DIOM) or start on SPIQ3 (QSPI). 1: Start on MOSI.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[21:20]	MIOM	Multiple I/O Mode. These bits enable SPI operation in dual I/O mode (DIOM) or quad I/O mode (QIOM). 00: No MIOM (disabled). 01: DIOM operation. 10: QIOM operation. 11: Reserved	0x0	R/W
19	RESERVED	Reserved	0x0	R
18	FMODE	Fast-Mode Enable. This bit enables fast mode operation for SPI receive transfers. 0: Disable 1: Enable	0x0	R/W
[17:16]	FCWM	Flow Control Watermark. These bits select the watermark level of the transmit channel (SPI_TFIFO buffer) or receive channel (SPI_RFIFO buffer) that triggers flow control operation. 00: TFIFO empty or RFIFO full. 01: TFIFO 75% or more empty, or RFIFO 75% or more full. 10: TFIFO 50% or more empty, or RFIFO 50% or more full. 11: Reserved	0x0	R/W
15	FCPL	Flow Control Polarity. This bit selects flow control polarity for the RDY pin when flow control is enabled. 0: Active-low RDY 1: Active-high RDY	0x0	R/W
14	FCCH	Flow Control Channel Selection. This bit selects whether the SPI applies flow control to the transmit channel (SPI_TFIFO buffer) or receive channel (SPI_RFIFO buffer). 0: Flow control on RX buffer. 1: Flow control on TX buffer.	0x0	R/W
13	FCEN	Flow Control Enable. This bit enables SPI flow control operation, which permits slow slave devices to interface with fast master devices. This bit controls operation of the RDY pin. 0: Disable 1: Enable	0x0	R/W
12	LSBF	Least Significant Bit First. This bit selects whether the SPI transmits/receives data as LSB first (little endian) or MSB first (big endian). This bit may only be changed when the SPI is disabled. 0: MSB sent/received first (big endian). 1: LSB sent/received first (little endian).	0x0	R/W
11	RESERVED	Reserved	0x0	R
[10:9]	SIZE	Word Transfer Size. These bits select the SPI transfer word size as 8-, 16-, or 32-bits. To ensure correct operation, both the master and slave must be configured with the same word size. This bit may only be changed when the SPI is disabled. 00: 8-bit word. 01: 16-bit word. 10: 32-bit word. 11: Reserved	0x0	R/W

Bits	Bit Name	Description	Reset	Access
8	EMISO	Enable MISO. This bit enables master-in-slave-out (MISO, DQ1_QMST) mode. This SPI mode is applicable only when the SPI is a slave. 0: Disable 1: Enable	0x0	R/W
7	SELST	Slave Select Polarity Between Transfers 0: De-assert slave select (high) 1: Assert slave select (low)	0x0	R/W
6	ASSEL	Slave Select Pin Control 0: Software Slave Select Control 1: Hardware Slave Select Control	0x1	R/W
5	CPOL	Clock Polarity. This bit selects whether the SPI uses an active-low or active-high signal for the SPI clock. 0: Active-high SPI CLK 1: Active-low SPI CLK	0x0	R/W
4	CPHA	Clock Phase. This bit selects whether the SPI starts toggling the signal for the SPI clock from the start of the first data bit or from the middle of the first data bit. 0: SPI CLK toggles from middle. 1: SPI CLK toggles from start.	0x0	R/W
3	ODM	Open Drain Mode. This bit configures the data output pins to behave as open drain outputs, which prevents contention and possible damage to pin drivers in multi-master or multi-slave SPI systems. 0: Disable 1: Enable	0x0	R/W
2	PSSE	Protected Slave Select Enable 0: Disable 1: Enable	0x0	R/W
1	MSTR	Master/Slave. This bit may only be changed when the SPI is disabled. 0: Slave 1: Master	0x0	R/W
0	EN	Enable. This bit enables SPI operation. 0: Disable SPI Module 1: Enable	0x0	R/W

RECEIVE CONTROL REGISTER

Address: 0xF0010008, Reset: 0x00000000, Name: RXCTL

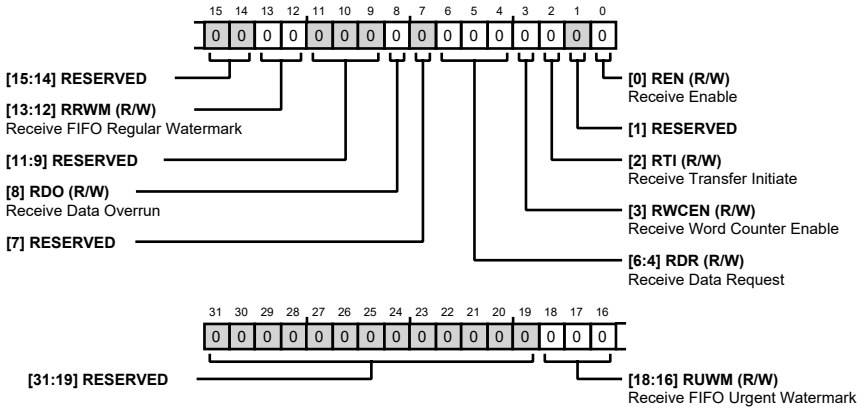


Table 341. Bit Descriptions for RXCTL

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved	0x0	R
[18:16]	RUWM	Receive FIFO Urgent Watermark. These bits select the receive FIFO watermark level for urgent data bus requests. 000: Disabled 001: 25% full RFIFO 010: 50% full RFIFO 011: 75% full RFIFO 100: Full RFIFO 101: Reserved 110: Reserved 111: Reserved	0x0	R/W
[15:14]	RESERVED	Reserved	0x0	R
[13:12]	RRWM	Receive FIFO Regular Watermark. These bits select the receive FIFO watermark level for regular data bus requests. 00: Empty RFIFO 01: RFIFO less than 25% full. 10: RFIFO less than 50% full. 11: RFIFO less than 75% full.	0x0	R/W
[11:9]	RESERVED	Reserved	0x0	R
8	RDO	Receive Data Overrun. This bit selects handling for receive data requests when the receive buffer is full. 0: Discard incoming data if SPI_RFIFO is full. 1: Overwrite old data if SPI_RFIFO is full.	0x0	R/W
7	RESERVED	Reserved	0x0	R
[6:4]	RDR	Receive Data Request. These bits select receive FIFO watermark conditions that direct the SPI to generate a receive data request. 000: Disabled 001: Not empty RFIFO. 010: 25% full RFIFO. 011: 50% full RFIFO.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		100: 75% full RFIFO. 101: Full RFIFO. 110: Reserved 111: Reserved		
3	RWCEN	Receive Word Counter Enable 0: Disable 1: Enable	0x0	R/W
2	RTI	Receive Transfer Initiate 0: Disable 1: Enable	0x0	R/W
1	RESERVED	Reserved	0x0	R
0	REN	Receive Enable. This bit enables SPI receive channel operation. 0: Disable 1: Enable	0x0	R/W

TRANSMIT CONTROL REGISTER

Address: 0xF001000C, Reset: 0x00000000, Name: TXCTL

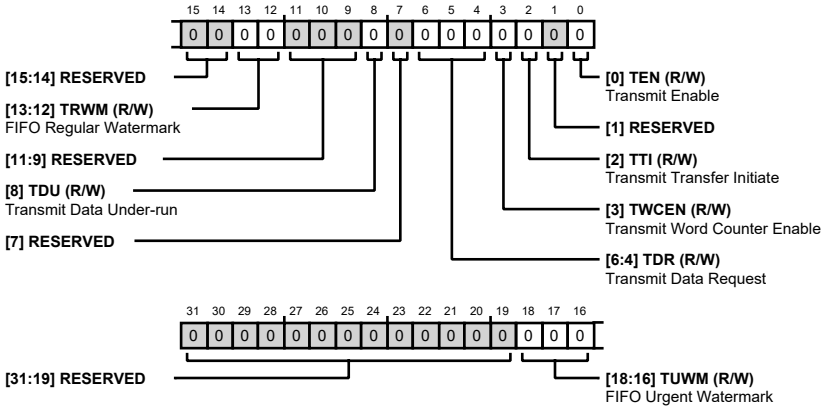


Table 342. Bit Descriptions for TXCTL

Bits	Bit Name	Description	Reset	Access
[31:19]	RESERVED	Reserved	0x0	R
[18:16]	TUWM	FIFO Urgent Watermark. These bits select the transmit FIFO watermark level for urgent data bus requests. 000: Disabled 001: 25% empty TFIFO. 010: 50% empty TFIFO. 011: 75% empty TFIFO. 100: Empty TFIFO	0x0	R/W
[15:14]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
[13:12]	TRWM	FIFO Regular Watermark. These bits select the transmit FIFO watermark level for regular data bus requests. 00: Full TFIFO 01: TFIFO less than 25% empty. 10: TFIFO less than 50% empty. 11: TFIFO less than 75% empty.	0x0	R/W
[11:9]	RESERVED	Reserved	0x0	R
8	TDU	Transmit Data Under-run. This bit selects handling for transmit data requests when the transmit buffer is empty. 0: Send last word when SPI_TFIFO is empty. 1: Send zeros when SPI_TFIFO is empty.	0x0	R/W
7	RESERVED	Reserved.	0x0	R
[6:4]	TDR	Transmit Data Request. These bits select transmit FIFO watermark conditions that direct the SPI to generate a transmit status interrupt. 000: Disabled 001: Not full TFIFO. 010: 25% empty TFIFO. 011: 50% empty TFIFO. 100: 75% empty TFIFO. 101: Empty TFIFO.	0x0	R/W
3	TWCEN	Transmit Word Counter Enable 0: Disable 1: Enable	0x0	R/W
2	TTI	Transmit Transfer Initiate 0: Disable 1: Enable	0x0	R/W
1	RESERVED	Reserved	0x0	R
0	TEN	Transmit Enable. This bit enables SPI transmit channel operation. 0: Disable 1: Enable	0x0	R/W

CLOCK RATE REGISTER

Address: 0xF0010010, Reset: 0x00000003, Name: CLK

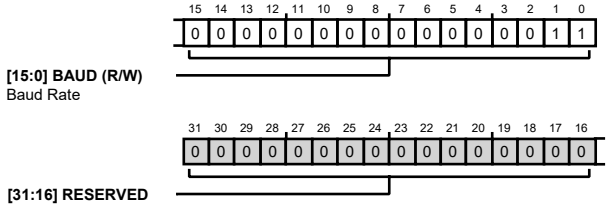


Table 343. Bit Descriptions for CLK

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	BAUD	Baud Rate. These bits set the SPI baud rate according to the formula: BAUD = (SCLK / SCK) -1, where SCLK = system clock and SCK = SPI serial clock.	0x3	R/W

DELAY REGISTER

Address: 0xF0010014, Reset: 0x00000301, Name: DLY

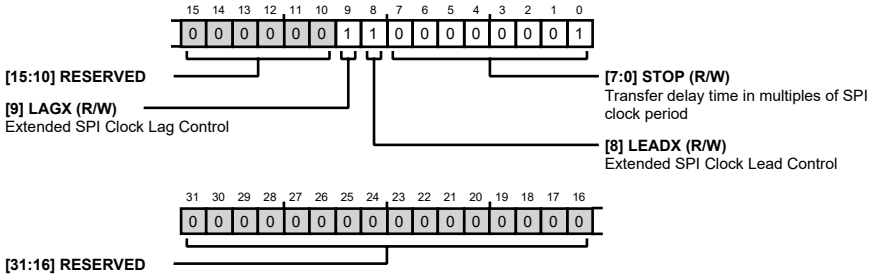


Table 344. Bit Descriptions for DLY

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	LAGX	Extended SPI Clock Lag Control 0: Disable 1: Enable	0x1	R/W
8	LEADX	Extended SPI Clock Lead Control 0: Disable 1: Enable	0x1	R/W
[7:0]	STOP	Transfer delay time in multiples of SPI clock period. These bits select a delay (number of stop bits in multiples of SPI Clock duration) at the end of each SPI transfer.	0x1	R/W

SLAVE SELECT REGISTER

Address: 0xF0010018, Reset: 0x0000FE00, Name: SLVSEL

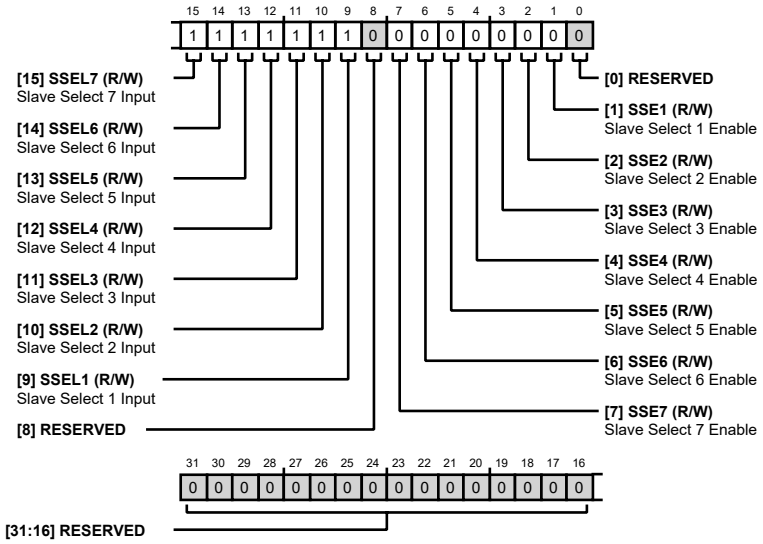


Table 345. Bit Descriptions for SLVSEL

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
15	SSEL7	Slave Select 7 Input 0: Low 1: High	0x1	R/W
14	SSEL6	Slave Select 6 Input 0: Low 1: High	0x1	R/W
13	SSEL5	Slave Select 5 Input 0: Low 1: High	0x1	R/W
12	SSEL4	Slave Select 4 Input 0: Low 1: High	0x1	R/W
11	SSEL3	Slave Select 3 Input 0: Low 1: High	0x1	R/W
10	SSEL2	Slave Select 2 Input 0: Low 1: High	0x1	R/W
9	SSEL1	Slave Select 1 Input 0: Low 1: High	0x1	R/W
8	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
7	SSE7	Slave Select 7 Enable 0: Disable 1: Enable	0x0	R/W
6	SSE6	Slave Select 6 Enable 0: Disable 1: Enable	0x0	R/W
5	SSE5	Slave Select 5 Enable 0: Disable 1: Enable	0x0	R/W
4	SSE4	Slave Select 4 Enable 0: Disable 1: Enable	0x0	R/W
3	SSE3	Slave Select 3 Enable 0: Disable 1: Enable	0x0	R/W
2	SSE2	Slave Select 2 Enable 0: Disable 1: Enable	0x0	R/W
1	SSE1	Slave Select 1 Enable 0: Disable 1: Enable	0x0	R/W
0	RESERVED	Reserved	0x0	R

RECEIVED WORD COUNT REGISTER

Address: 0xF001001C, Reset: 0x00000000, Name: RWC

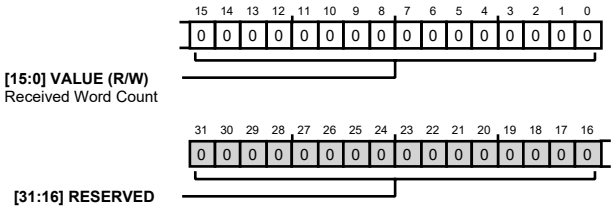


Table 346. Bit Descriptions for RWC

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Received Word Count	0x0	R/W

RECEIVED WORD COUNT RELOAD REGISTER

Address: 0xF0010020, Reset: 0x00000000, Name: RWCR

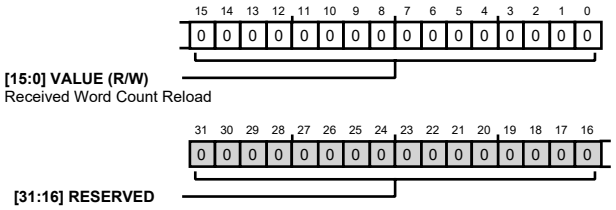


Table 347. Bit Descriptions for RWCR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Received Word Count Reload	0x0	R/W

TRANSMITTED WORD COUNT REGISTER

Address: 0xF0010024, Reset: 0x00000000, Name: TWC

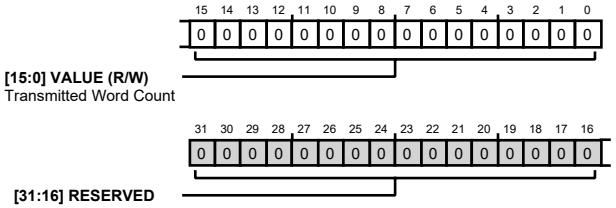


Table 348. Bit Descriptions for TWC

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Transmitted Word Count	0x0	R/W

TRANSMITTED WORD COUNT RELOAD REGISTER

Address: 0xF0010028, Reset: 0x00000000, Name: TWCR

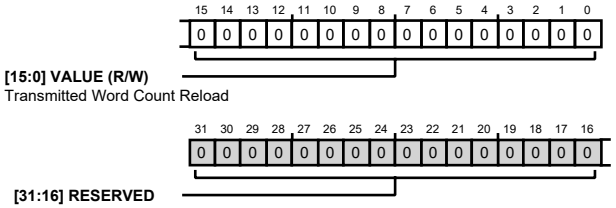


Table 349. Bit Descriptions for TWCR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Transmitted Word Count Reload	0x0	R/W

INTERRUPT MASK REGISTER

Address: 0xF0010030, Reset: 0x00000000, Name: IMSK

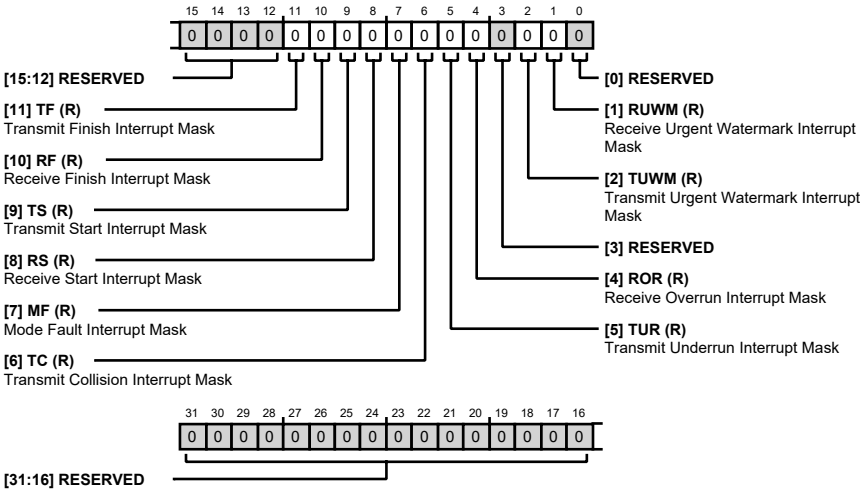


Table 350. Bit Descriptions for IMSK

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
11	TF	Transmit Finish Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
10	RF	Receive Finish Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
9	TS	Transmit Start Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
8	RS	Receive Start Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
7	MF	Mode Fault Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
6	TC	Transmit Collision Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
5	TUR	Transmit Underrun Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
4	ROR	Receive Overrun Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
3	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
2	TUWM	Transmit Urgent Watermark Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
1	RUWM	Receive Urgent Watermark Interrupt Mask 0: Disable (mask) interrupt. 1: Enable (unmask) interrupt.	0x0	R
0	RESERVED	Reserved	0x0	R

INTERRUPT MASK CLEAR REGISTER

Address: 0xF0010034, Reset: 0x00000000, Name: IMSK_CLR

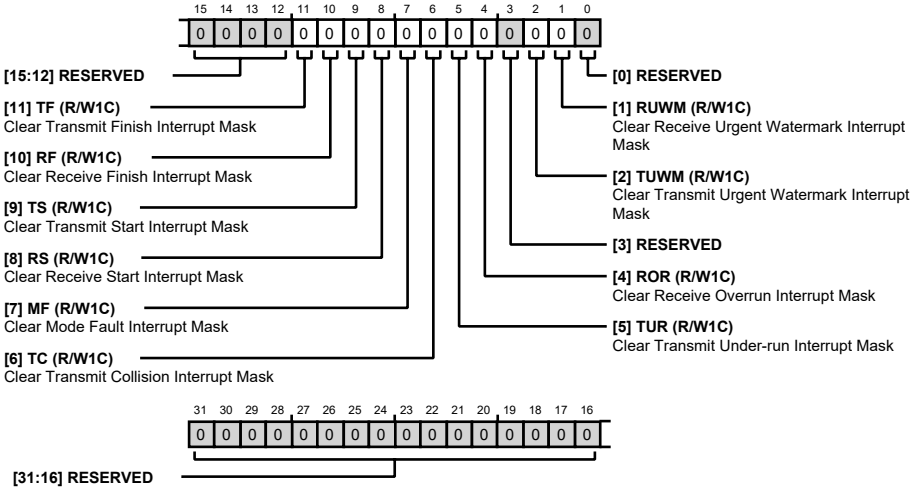


Table 351. Bit Descriptions for IMSK_CLR

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
11	TF	Clear Transmit Finish Interrupt Mask	0x0	R/W1C
10	RF	Clear Receive Finish Interrupt Mask	0x0	R/W1C
9	TS	Clear Transmit Start Interrupt Mask	0x0	R/W1C
8	RS	Clear Receive Start Interrupt Mask	0x0	R/W1C
7	MF	Clear Mode Fault Interrupt Mask	0x0	R/W1C
6	TC	Clear Transmit Collision Interrupt Mask	0x0	R/W1C
5	TUR	Clear Transmit Under-run Interrupt Mask	0x0	R/W1C
4	ROR	Clear Receive Overrun Interrupt Mask	0x0	R/W1C
3	RESERVED	Reserved	0x0	R
2	TUWM	Clear Transmit Urgent Watermark Interrupt Mask	0x0	R/W1C
1	RUWM	Clear Receive Urgent Watermark Interrupt Mask	0x0	R/W1C
0	RESERVED	Reserved	0x0	R

INTERRUPT MASK SET REGISTER

Address: 0xF0010038, Reset: 0x00000000, Name: IMSK_SET

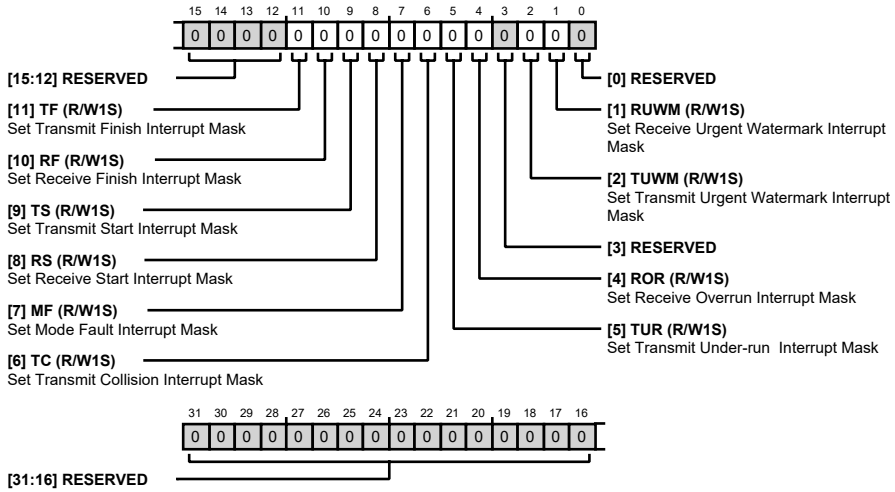


Table 352. Bit Descriptions for IMSK_SET

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
11	TF	Set Transmit Finish Interrupt Mask	0x0	R/W1S
10	RF	Set Receive Finish Interrupt Mask	0x0	R/W1S
9	TS	Set Transmit Start Interrupt Mask	0x0	R/W1S
8	RS	Set Receive Start Interrupt Mask	0x0	R/W1S
7	MF	Set Mode Fault Interrupt Mask	0x0	R/W1S
6	TC	Set Transmit Collision Interrupt Mask	0x0	R/W1S
5	TUR	Set Transmit Under-run Interrupt Mask	0x0	R/W1S
4	ROR	Set Receive Overrun Interrupt Mask	0x0	R/W1S
3	RESERVED	Reserved	0x0	R
2	TUWM	Set Transmit Urgent Watermark Interrupt Mask	0x0	R/W1S
1	RUWM	Set Receive Urgent Watermark Interrupt Mask	0x0	R/W1S
0	RESERVED	Reserved	0x0	R

STATUS REGISTER

Address: 0xF0010040, Reset: 0x00440001, Name: STAT

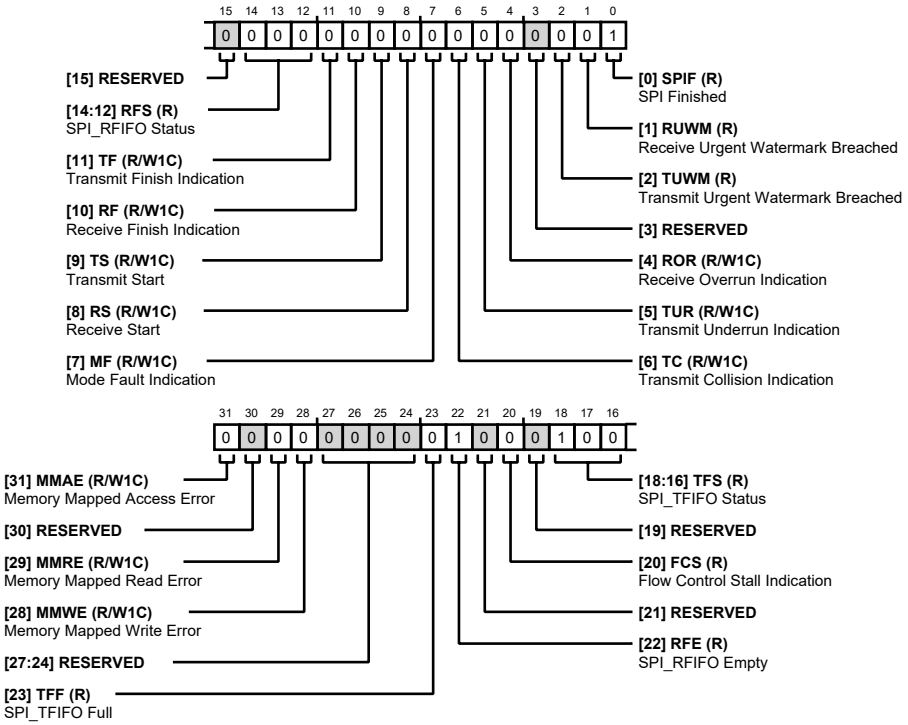


Table 353. Bit Descriptions for STAT

Bits	Bit Name	Description	Reset	Access
31	MMAE	Memory Mapped Access Error	0x0	R/W1C
30	RESERVED	Reserved	0x0	R
29	MMRE	Memory Mapped Read Error	0x0	R/W1C
28	MMWE	Memory Mapped Write Error	0x0	R/W1C
[27:24]	RESERVED	Reserved	0x0	R
23	TFF	SPI_TFIFO Full 0: Not Full Tx FIFO. 1: Full Tx FIFO.	0x0	R
22	RFE	SPI_RFIFO Empty 0: RX FIFO not empty. 1: RX FIFO empty.	0x1	R
21	RESERVED	Reserved	0x0	R
20	FCS	Flow Control Stall Indication. This bit indicates whether a slave has de-asserted the RDY pin to stall the SPI master while the slave is unable to service the SPI master's request. 0: No Stall (RDY pin asserted) 1: Stall (RDY pin de-asserted)	0x0	R
19	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
[18:16]	TFS	SPI_TFIFO Status. The SPI uses this status when evaluating transmit watermark conditions. 000: Full TFIFO. 001: 25% empty TFIFO. 010: 50% empty TFIFO. 011: 75% empty TFIFO. 100: Empty TFIFO.	0x4	R
15	RESERVED	Reserved	0x0	R
[14:12]	RFS	SPI_RFIFO Status. The SPI uses this status when evaluating receive watermark conditions. 000: Empty RFIFO. 001: 25% full RFIFO. 010: 50% full RFIFO. 011: 75% full RFIFO. 100: Full RFIFO.	0x0	R
11	TF	Transmit Finish Indication. This bit indicates that the SPI has detected the finish of a transmit burst transfer. 0: No status. 1: Transmit finish detected.	0x0	R/W1C
10	RF	Receive Finish Indication. This bit indicates that the SPI has detected the finish of a receive burst transfer. 0: No status. 1: Receive finish detected.	0x0	R/W1C
9	TS	Transmit Start. This bit indicates that the SPI has detected the start of a transmit burst transfer. 0: No status. 1: Transmit start detected.	0x0	R/W1C
8	RS	Receive Start. This bit indicates that the SPI has detected the start of a receive burst transfer. 0: No status. 1: Receive start detected.	0x0	R/W1C
7	MF	Mode Fault Indication. This bit, when SPI is a master and PSSE is enabled, indicates that multiple masters have asserted slave select inputs. 0: No status. 1: Mode fault occurred.	0x0	R/W1C
6	TC	Transmit Collision Indication. This bit, when SPI is a slave, indicates that the load of data into the shift register has occurred too close to the first transmitting edge of the SPI Clock. 0: No status. 1: Transmit collision occurred.	0x0	R/W1C
5	TUR	Transmit Underrun Indication. This bit, when the transmit FIFO is empty, indicates that the last word in the transmit FIFO has been re-sent as transmit data. Alternately, it indicates that zero has been sent as transmit data. 0: No status. 1: Transmit underrun occurred.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
4	ROR	Receive Overrun Indication. This bit, when the receive FIFO is full, indicates that a word in the receive FIFO has been overwritten with incoming receive data. Alternately, it indicates that incoming receive data has been discarded. 0: No status. 1: Receive overrun occurred.	0x0	R/W1C
3	RESERVED	Reserved	0x0	R
2	TUWM	Transmit Urgent Watermark Breached. This bit indicates that the transmit urgent watermark has been reached. This condition is cleared when the transmit FIFO fills enough to reach the transmit regular watermark. 0: TX regular watermark reached. 1: TX urgent watermark breached.	0x0	R
1	RUWM	Receive Urgent Watermark Breached. This bit indicates that the receive urgent watermark has been reached. This condition is cleared when the receive FIFO empties enough to reach the receive regular watermark. 0: RX regular watermark reached. 1: RX urgent watermark breached.	0x0	R
0	SPIF	SPI Finished. This bit indicates that a single word transfer is complete. 0: No status. 1: Completed single-word transfer.	0x1	R

MASKED INTERRUPT CONDITION REGISTER

Address: 0xF0010044, Reset: 0x00000000, Name: ILAT

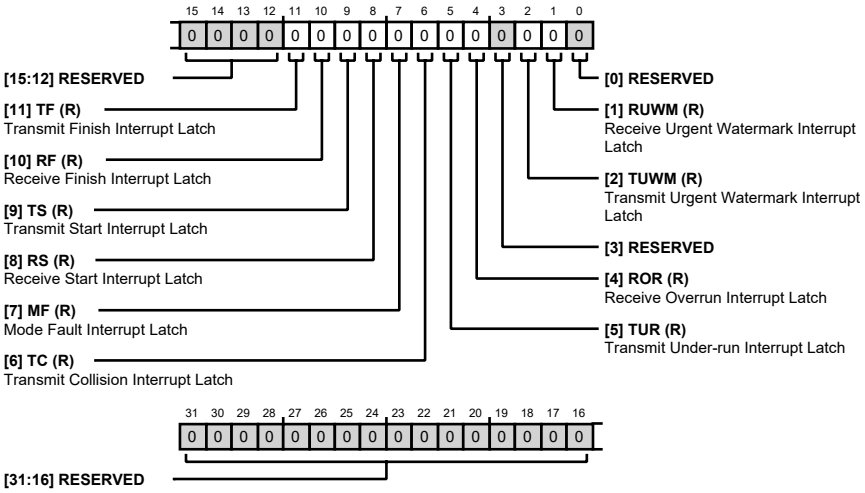


Table 354. Bit Descriptions for ILAT

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
11	TF	Transmit Finish Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R

Bits	Bit Name	Description	Reset	Access
10	RF	Receive Finish Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
9	TS	Transmit Start Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
8	RS	Receive Start Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
7	MF	Mode Fault Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
6	TC	Transmit Collision Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
5	TUR	Transmit Under-run Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
4	ROR	Receive Overrun Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
3	RESERVED	Reserved	0x0	R
2	TUWM	Transmit Urgent Watermark Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
1	RUWM	Receive Urgent Watermark Interrupt Latch 0: No interrupt. 1: Latched interrupt.	0x0	R
0	RESERVED	Reserved	0x0	R

MASKED INTERRUPT CLEAR REGISTER

Address: 0xF0010048, Reset: 0x00000000, Name: ILAT_CLR

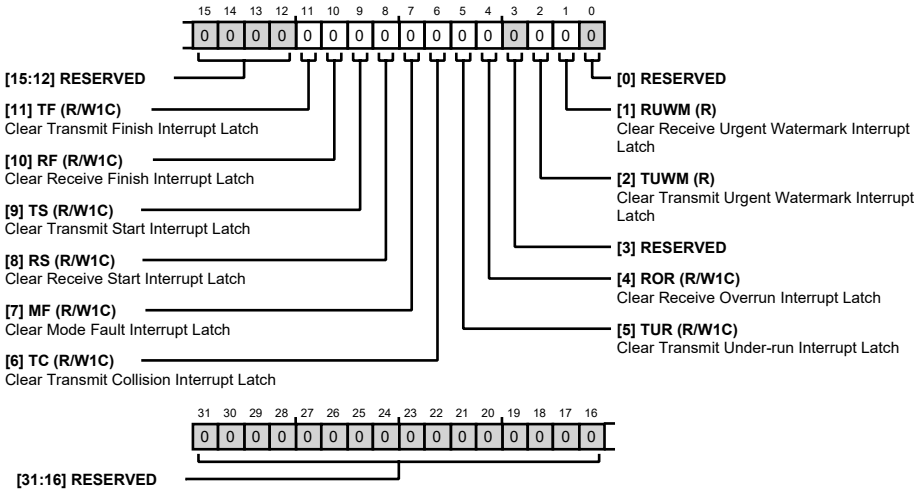


Table 355. Bit Descriptions for ILAT_CLR

Bits	Bit Name	Description	Reset	Access
[31:12]	RESERVED	Reserved	0x0	R
11	TF	Clear Transmit Finish Interrupt Latch	0x0	R/W1C
10	RF	Clear Receive Finish Interrupt Latch	0x0	R/W1C
9	TS	Clear Transmit Start Interrupt Latch	0x0	R/W1C
8	RS	Clear Receive Start Interrupt Latch	0x0	R/W1C
7	MF	Clear Mode Fault Interrupt Latch	0x0	R/W1C
6	TC	Clear Transmit Collision Interrupt Latch	0x0	R/W1C
5	TUR	Clear Transmit Underrun Interrupt Latch	0x0	R/W1C
4	ROR	Clear Receive Overrun Interrupt Latch	0x0	R/W1C
3	RESERVED	Reserved	0x0	R
2	TUWM	Clear Transmit Urgent Watermark Interrupt Latch	0x0	R
1	RUWM	Clear Receive Urgent Watermark Interrupt Latch	0x0	R
0	RESERVED	Reserved	0x0	R

RECEIVE FIFO DATA REGISTER

Address: 0xF0010050, Reset: 0x00000000, Name: RFIFO

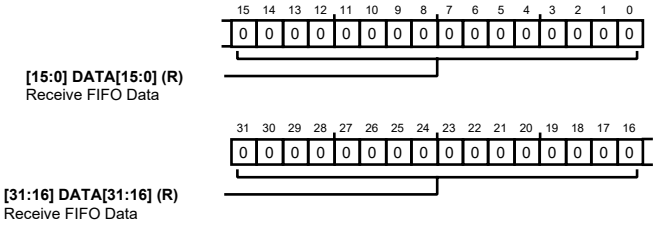


Table 356. Bit Descriptions for RFIFO

Bits	Bit Name	Description	Reset	Access
[31:0]	DATA	Receive FIFO Data	0x0	R

TRANSMIT FIFO DATA REGISTER

Address: 0xF0010058, Reset: 0x00000000, Name: TFIFO

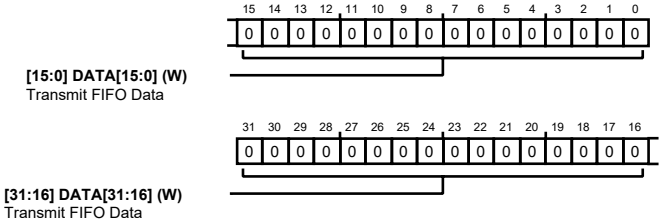


Table 357. Bit Descriptions for TFIFO

Bits	Bit Name	Description	Reset	Access
[31:0]	DATA	Transmit FIFO Data	0x0	W

MEMORY MAPPED READ HEADER REGISTER

Address: 0xF0010060, Reset: 0x00000000, Name: MMRDH

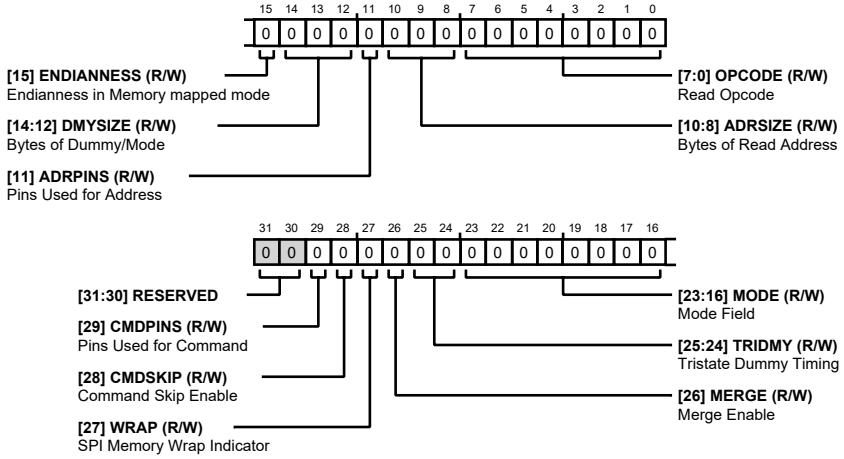


Table 358. Bit Descriptions for MMRDH

Bits	Bit Name	Description	Reset	Access
[31:30]	RESERVED	Reserved	0x0	R
29	CMDPINS	Pins Used for Command. This bit specifies the number of pins to be used for command transmission. 0: Use only one pin: MOSI (overrides MIOM bits in register SPI_CTL). 1: Use pins specified by MIOM bits in register SPI_CTL.	0x0	R/W
28	CMDSKIP	Command Skip Enable. This bit enables command skip mode where the address is sent first, and the OPCODE field is not sent (CMDSKIP =1). 0: OPCODE field is sent first followed by address. 1: OPCODE field is not sent; address is sent first.	0x0	R/W
27	WRAP	SPI Memory Wrap Indicator 0: SPI Memory auto increments address purely sequentially. 1: SPI Memory auto increments address but wraps within 32 Byte lines.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
26	MERGE	Merge Enable. When this bit is set, SPI hardware combines the two successive transfers. This increases the throughput rate when accessing many sequential memory locations. 0: Merge disabled. 1: Merge enabled.	0x0	R/W
[25:24]	TRIDMY	Tristate Dummy Timing 00: Tristate outputs immediately. 01: Tristate outputs after 4 bits of dummy/mode are transmitted. 10: Tristate outputs after 8 bits of dummy/mode are transmitted. 11: Never Tristate outputs never (previously specified output state is held).	0x0	R/W
[23:16]	MODE	Mode Field	0x0	R/W
15	ENDIANNESS	Endianness in Memory Mapped Mode 0: Transmits/receives data as big endian (MSB first) in Memory mapped mode. 1: Transmits/receives data as little endian (LSB first) in Memory mapped mode.	0x0	R/W
[14:12]	DMYSIZE	Bytes of Dummy Mode. These bits specify the number of bytes separating address transmission and read data return. 000: 0 Bytes 001: 1 Bytes 010: 2 Bytes 011: 3 Bytes 100: 4 Bytes 101: 5 Bytes 110: 6 Bytes 111: 7 Bytes	0x0	R/W
11	ADRPINS	Pins Used for Address. This bit specifies the number of pins to be used for address transmission. 0: Use only one pin: MOSI (overrides MIOM bits). 1: Use pins specified by MIOM bits.	0x0	R/W
[10:8]	ADRSIZE	Bytes of Read Address. These bits define the number of bytes used to specify the read address. 000: 1 Byte 001: 1 Byte 010: 2 Bytes 011: 3 Bytes 100: 4 Bytes	0x0	R/W
[7:0]	OPCODE	Read Opcode. These bits specify the initial bits transmitted in response to a read request of SPI memory. Although any opcode may be sent, values 0x03, 0x0B, 0x3B, 0x6B, 0xBB, and 0xEB are likely to be the most used.	0x0	R/W

SPI MEMORY TOP ADDRESS REGISTER

Address: 0xF0010064, Reset: 0x00000000, Name: MMTOP

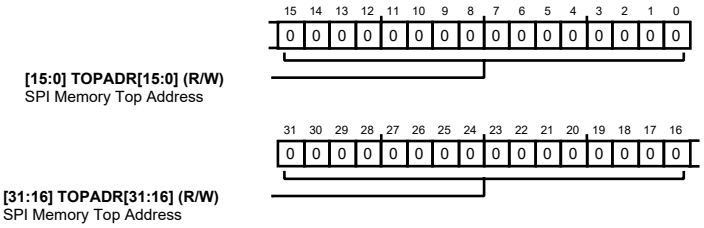


Table 359. Bit Descriptions for MMTOP

Bits	Bit Name	Description	Reset	Access
[31:0]	TOPADR	SPI Memory Top Address. These bits specify the top populated address of a connected SPI memory device. Attempts to access SPI memory are not blocked if this address is exceeded and an error is generated as part of the read response.	0x0	R/W

REGISTER DETAILS: DMA CHANNEL (DDE)

POINTER TO NEXT INITIAL DESCRIPTOR REGISTER

Address: 0x00, Reset: 0x00000000, Name: DSCPTR_NXT

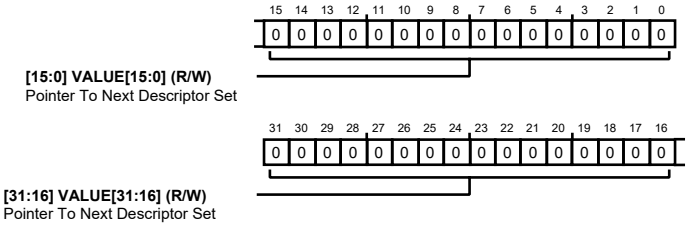


Table 360. Bit Descriptions for DSCPTR_NXT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer To Next Descriptor Set	0x0	R/W

START ADDRESS OF CURRENT BUFFER REGISTER

Address: 0x04, Reset: 0x00000000, Name: ADDRSTART

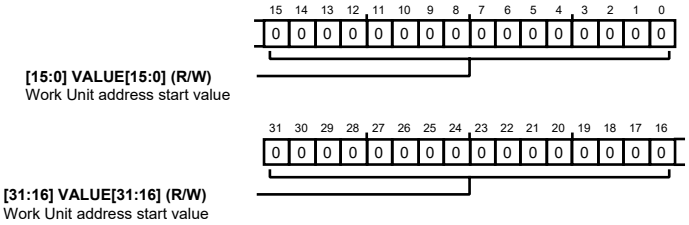


Table 361. Bit Descriptions for ADDRSTART

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Address Start Value	0x0	R/W

CONFIGURATION REGISTER

Address: 0x08, Reset: 0x00000000, Name: CFG

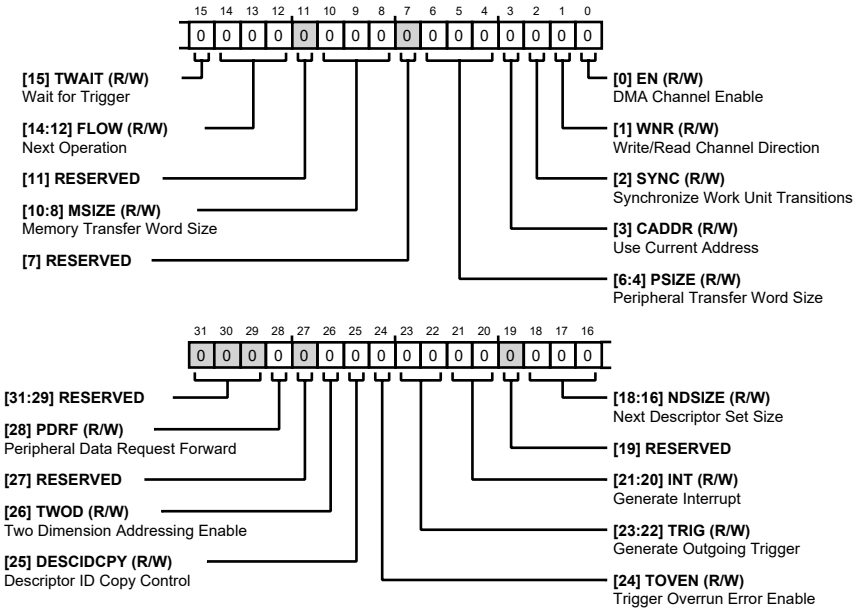


Table 362. Bit Descriptions for CFG

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
28	PDRF	Peripheral Data Request Forward. This bit defines how the DDE handles data requests from the peripheral while in idle state after a stop mode or memory read work unit. 0: Peripheral data request not forwarded. 1: Peripheral data request forwarded.	0x0	R/W
27	RESERVED	Reserved	0x0	R
26	TWOD	Two Dimension Addressing Enable. This bit selects whether the DMA addressing involves only DDE_XCNT and DDE_XMOD (one-dimensional DMA) or also involves DDE_YCNT and DDE_YMOD (two-dimensional DMA). 0: One-dimensional addressing. 1: Two-dimensional addressing.	0x0	R/W
25	DESCIDCPY	Descriptor ID Copy Control. This bit specifies when to copy the initial descriptor pointer to the DDE_DSCPTR_PRV register. 0: Never copy. 1: Copy on work unit complete.	0x0	R/W
24	TOVEN	Trigger Overrun Error Enable. A trigger overrun occurs if more than one trigger was received before the DDE reached the trigger wait state. If DDE_CFG.TOVEN is set, a trigger overrun causes the DDE to flag an error. In cases where a trigger overrun is not a problem, clearing DDE_CFG.TOVEN prevents the overrun from causing an error and halting the DDE. The DDE_CFG.TOVEN operates independently of the DDE_CFG.TWAIT bit selection. 0: Ignore trigger overrun. 1: Error on trigger overrun.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[23:22]	TRIG	Generate Outgoing Trigger. These bits select whether the DDE issues an outgoing trigger, based on the work unit counter values. 00: Never assert Trigger. 01: Trigger when XCNTCUR reaches 0. 10: Trigger when YCNTCUR reaches 0. 11: Reserved	0x0	R/W
[21:20]	INT	Generate Interrupt. These bits select whether an interrupt is sent to the core based on work unit status or peripheral interrupt request. 00: Never assert Interrupt. 01: Interrupt when X count expires. 10: Interrupt when Y count expires. 11: Peripheral Interrupt	0x0	R/W
19	RESERVED	Reserved	0x0	R
[18:16]	NDSIZE	Next Descriptor Set Size. These bits specify the number of descriptor elements in memory to load during the next descriptor fetch. 000: Fetch one descriptor element. 001: Fetch two descriptor elements. 010: Fetch three descriptor elements. 011: Fetch four descriptor elements. 100: Fetch five descriptor elements. 101: Fetch six descriptor elements. 110: Fetch seven descriptor elements. 111: Reserved	0x0	R/W
15	TWAIT	Wait for Trigger. This bit controls whether the DDE waits for an incoming trigger from another channel or user. 0: Begin Work Unit Automatically (No Wait) 1: Wait for Trigger (Halt before Work Unit)	0x0	R/W
[14:12]	FLOW	Next Operation. These bits select descriptor handling options. 000: STOP—Stop. When the current work unit completes, the DMA channel stops automatically, after signaling an interrupt (if selected). specifying the next work unit. 001: AUTO—Auto-buffer. In this mode, no descriptors in memory are used. Instead, DMA is performed in a continuous circular buffer fashion based on user programmed DMA MMR settings. 010: Reserved 011: Reserved 100: DSCL—Descriptor List. This mode fetches a descriptor Set from memory that includes DDE_DSCPTR_NXT, allowing maximum flexibility in locating descriptors in memory.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		101: DSCA—Descriptor Array. This mode fetches a descriptor set from memory that does not include the DDE_DSCPTR_NXT element. Because the descriptor set does not contain a next descriptor pointer entry, the DDE defaults to using the DDE_DSCPTR_CUR register to step through descriptors, allowing a group of descriptors sets to follow one another in memory as an array. 110: Descriptor On Demand List. This mode fetches a descriptor set from memory that includes DDE_DSCPTR_NXT. At the end of the work unit, if the channel has not been triggered, the work unit is repeated. But, if the channel has been triggered before the end of the work unit, the DDE fetches a new descriptor set. 111: Descriptor On Demand Array. This mode fetches a descriptor set from memory that does not include DDE_DSCPTR_NXT. At the end of the work unit, if the channel has not been triggered, the work unit is repeated. But, if the channel has been triggered before the end of the work unit, the DDE fetches a new descriptor set is fetched.		
11	RESERVED	Reserved	0x0	R
[10:8]	MSIZE	Memory Transfer Word Size 000: 1 Byte 001: 2 Bytes 010: 4 Bytes 011: 8 Bytes 100: 16 Bytes 101: 32 Bytes	0x0	R/W
7	RESERVED	Reserved	0x0	R
[6:4]	PSIZE	Peripheral Transfer Word Size 000: 1 Byte 001: 2 Bytes 010: 4 Bytes 011: 8 Bytes	0x0	R/W
3	CADDR	Use Current Address. If this bit is cleared, the DDE loads the DDE_ADDRSTART register on the first access of the work unit. If this bit is set, the DDE uses the DDE_ADDR_CUR register value for the starting address for the work unit and writes the same value to the DDE_ADDRSTART register. 0: Load Starting Address 1: Use Current Address	0x0	R/W
2	SYNC	Synchronize Work Unit Transitions. Setting this bit clears the DMA FIFO and pointers before starting the first Work Unit of a Work Unit Chain. 0: No Synchronization 1: Synchronize Channel	0x0	R/W
1	WNR	Write/Read Channel Direction 0: Transmit (Read from memory) 1: Receive (Write to memory)	0x0	R/W
0	EN	DMA Channel Enable. This bit enables the selected DMA Channel. 0: Disable 1: Enable	0x0	R/W

INNER LOOP COUNT START VALUE REGISTER

Address: 0x0C, Reset: 0x00000000, Name: XCNT

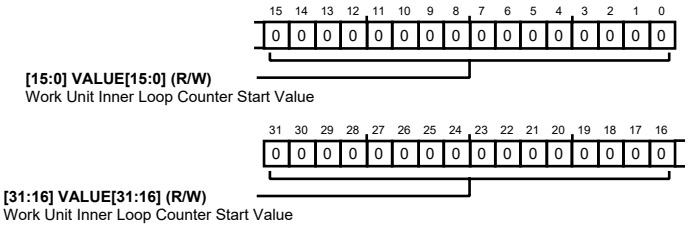


Table 363. Bit Descriptions for XCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Start Value	0x0	R/W

INNER LOOP ADDRESS INCREMENT REGISTER

Address: 0x10, Reset: 0x00000000, Name: XMOD

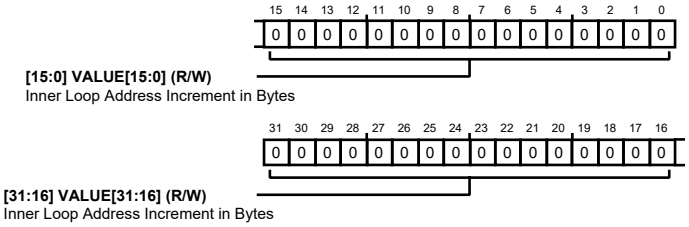


Table 364. Bit Descriptions for XMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Inner Loop Address Increment in Bytes	0x0	R/W

OUTER LOOP COUNT START VALUE (2D ONLY) REGISTER

Address: 0x14, Reset: 0x00000000, Name: YCNT

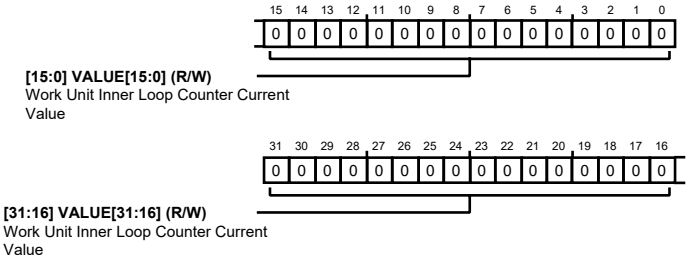


Table 365. Bit Descriptions for YCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Current Value	0x0	R/W

OUTER LOOP ADDRESS INCREMENT (2D ONLY) REGISTER

Address: 0x18, Reset: 0x00000000, Name: YMOD

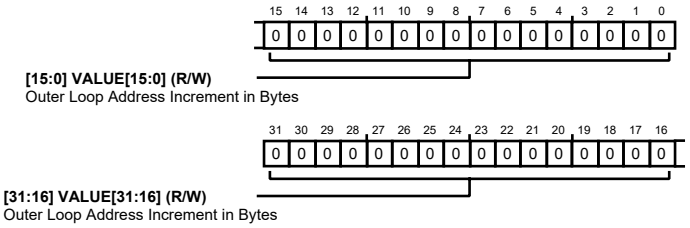


Table 366. Bit Descriptions for YMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Outer Loop Address Increment in Bytes	0x0	R/W

CURRENT DESCRIPTOR POINTER REGISTER

Address: 0x24, Reset: 0x00000000, Name: DSCPTR_CUR

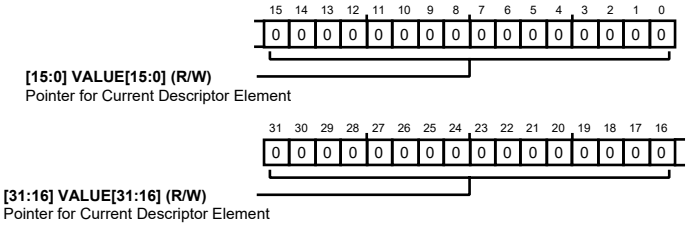


Table 367. Bit Descriptions for DSCPTR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer for Current Descriptor Element	0x0	R/W

PREVIOUS INITIAL DESCRIPTOR POINTER REGISTER

Address: 0x28, Reset: 0x00000000, Name: DSCPTR_PRV

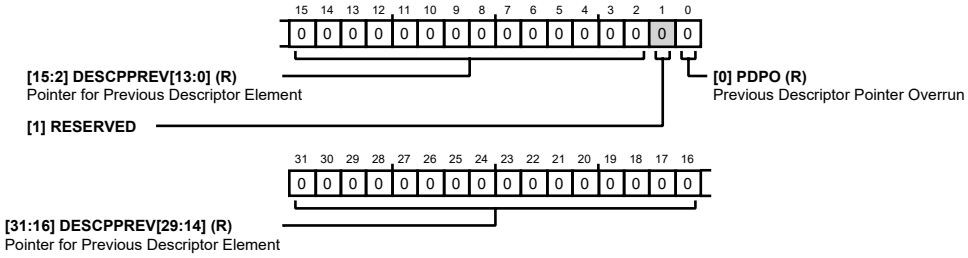


Table 368. Bit Descriptions for DSCPTR_PRV

Bits	Bit Name	Description	Reset	Access
[31:2]	DESCPPREV	Pointer for Previous Descriptor Element	0x0	R
1	RESERVED	Reserved	0x0	R
0	PDPO	Previous Descriptor Pointer Overrun	0x0	R

CURRENT ADDRESS REGISTER

Address: 0x2C, Reset: 0x00000000, Name: ADDR_CUR

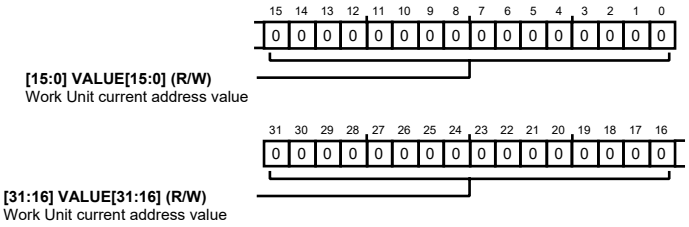


Table 369. Bit Descriptions for ADDR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Current Address Value	0x0	R/W

STATUS REGISTER

Address: 0x30, Reset: 0x00006000, Name: STAT

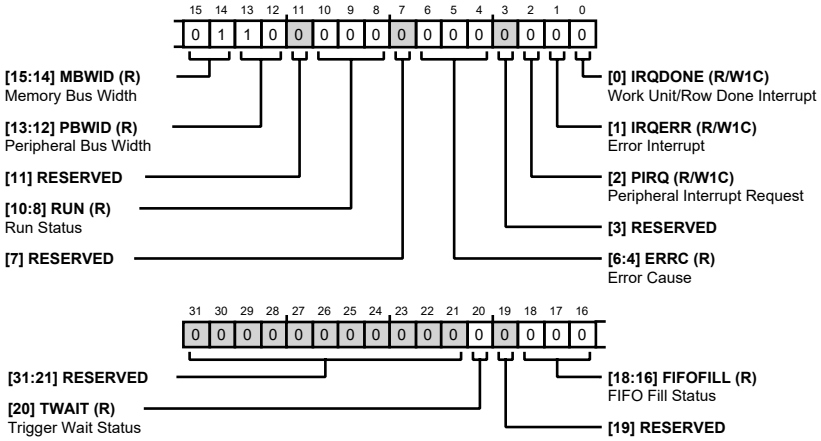


Table 370. Bit Descriptions for STAT

Bits	Bit Name	Description	Reset	Access
[31:21]	RESERVED	Reserved	0x0	R
20	TWAIT	Trigger Wait Status. This bit indicates whether the DDE has or has not received a trigger. 0: No trigger received. 1: Trigger received.	0x0	R
19	RESERVED	Reserved.	0x0	R
[18:16]	FIFOFILL	FIFO Fill Status. These bits report the quantity of data in the FIFO relative to available space. 000: Empty 001: Empty < FIFO = 1/4 Full 010: 1/4 Full < FIFO = 1/2 Full 011: 1/2 Full < FIFO = 3/4 Full 100: 3/4 Full < FIFO = Full	0x0	R

Bits	Bit Name	Description	Reset	Access
		101: Reserved 110: Reserved 111: Full		
[15:14]	MBWID	Memory Bus Width. These bits indicate the width of the memory bus connected to this DDE. 00: 2 Bytes 01: 4 Bytes 10: 8 Bytes 11: 16 Bytes	0x1	R
[13:12]	PBWID	Peripheral Bus Width. These bits indicate the width of the peripheral bus connected to this DDE. 00: 1 Byte 01: 2 Bytes 10: 4 Bytes 11: 8 Bytes	0x2	R
11	RESERVED	Reserved	0x0	R
[10:8]	RUN	Run Status. These bits report the DDE's current operational state. 000: Idle/Stop State 001: Descriptor Fetch 010: Data Transfer 011: Waiting for Trigger 100: Waiting for Write ACK/FIFO Drain to Peripheral 101: Reserved 110: Reserved 111: Reserved	0x0	R
7	RESERVED	Reserved	0x0	R
[6:4]	ERRC	Error Cause. When an interrupt request error occurs, the DDE updates ERRC to identify the type of error. 000: Configuration Error 001: Illegal Write Occurred While Channel Running 010: Address Alignment Error 011: Memory Access/Fabric Error 100: Reserved 101: Trigger Overrun 110: Bandwidth Monitor Error 111: Reserved	0x0	R
3	RESERVED	Reserved	0x0	R
2	PIRQ	Peripheral Interrupt Request. This bit indicates an interrupt has been caused by the peripheral. 0: No Interrupt 1: Interrupt Signaled by Peripheral	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
1	IRQERR	Error Interrupt. This bit indicates that the DDE has detected a documented rule violations during DMA programming or operation. 0: No Error 1: Error Occurred	0x0	R/W1C
0	IRQDONE	Work Unit/Row Done Interrupt. This bit indicates the DDE has detected the completion of a work unit or row (inner loop count) and has issued an interrupt. 0: Inactive 1: Active	0x0	R/W1C

CURRENT COUNT(1D) OR INTRA-ROW XCNT (2D) REGISTER

Address: 0x34, Reset: 0x00000000, Name: XCNT_CUR

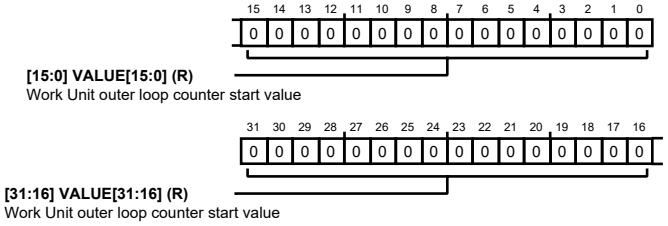


Table 371. Bit Descriptions for XCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Outer Loop Counter Start Value	0x0	R

CURRENT ROW COUNT (2D ONLY) REGISTER

Address: 0x38, Reset: 0x00000000, Name: YCNT_CUR

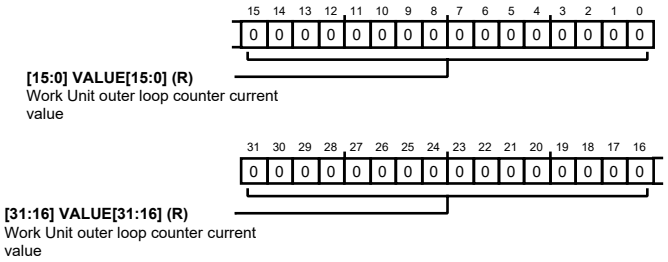


Table 372. Bit Descriptions for YCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Outer Loop Counter Current Value	0x0	R

BANDWIDTH LIMIT COUNT REGISTER

Address: 0x40, Reset: 0x00000000, Name: BWLCNT

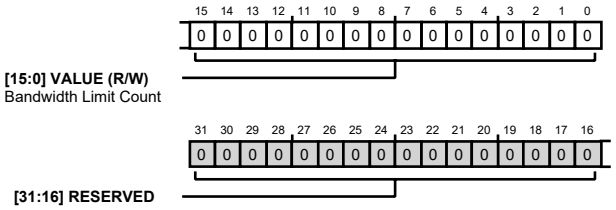


Table 373. Bit Descriptions for BWLCNT

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Bandwidth Limit Count	0x0	R/W

BANDWIDTH LIMIT COUNT CURRENT REGISTER

Address: 0x44, Reset: 0x00000000, Name: BWLCNT_CUR

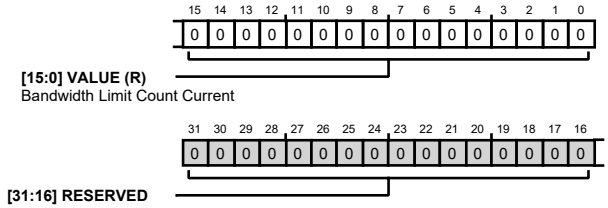


Table 374. Bit Descriptions for BWLCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	Bandwidth Limit Count Current	0x0	R

BANDWIDTH MONITOR COUNT REGISTER

Address: 0x48, Reset: 0x00000000, Name: BWMCNT

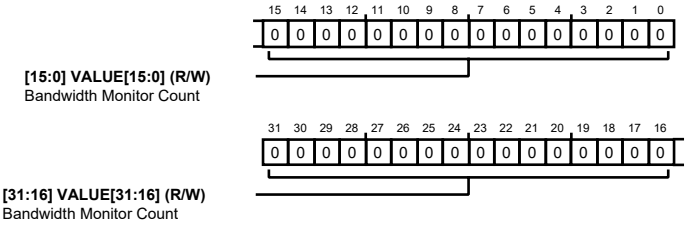


Table 375. Bit Descriptions for BWMCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count	0x0	R/W

BANDWIDTH MONITOR COUNT CURRENT REGISTER

Address: 0x4C, Reset: 0x00000000, Name: BWMCNT_CUR

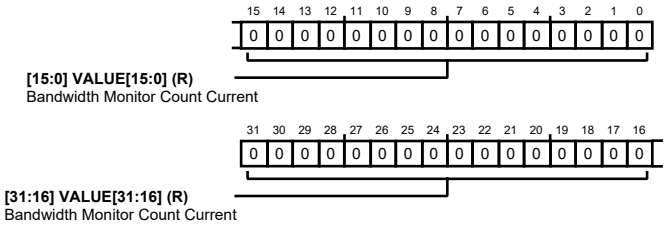


Table 376. Bit Descriptions for BWMCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count Current	0x0	R

REGISTER DETAILS: UART (UART)

CONTROL REGISTER

Address: 0xF0012004, Reset: 0x00000000, Name: CTL

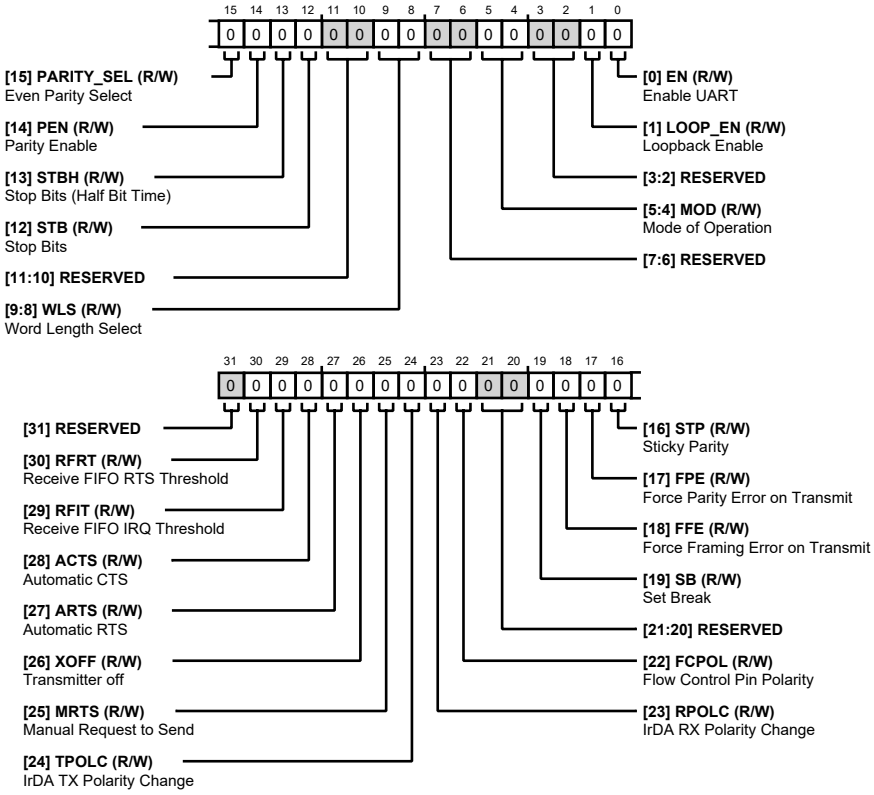


Table 377. Bit Descriptions for CTL

Bits	Bit Name	Description	Reset	Access
31	RESERVED	Reserved	0x0	R/W
30	RFRT	Receive FIFO RTS Threshold 0: De-assert RTS if RX FIFO word count greater than 4; assert if less than or equal to 4. 1: De-assert RTS if RX FIFO word count greater than 7; assert if less than or equal to 7.	0x0	R/W
29	RFIT	Receive FIFO IRQ Threshold 0: Set RFCS = 1 if RX FIFO count ≥ 4. 1: Set RFCS = 1 if RX FIFO count ≥ 7.	0x0	R/W
28	ACTS	Automatic CTS 0: Disable Tx handshaking protocol. 1: Enable Tx handshaking protocol.	0x0	R/W
27	ARTS	Automatic RTS 0: Disable Rx handshaking protocol. 1: Enable Rx handshaking protocol.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
26	XOFF	Transmitter Off 0: Transmission ON, if ACTS = 0. 1: Transmission OFF, if ACTS = 0.	0x0	R/W
25	MRTS	Manual Request to Send 0: De-assert RTS pin when ARTS = 0. 1: Assert RTS pin when ARTS = 0.	0x0	R/W
24	TPOLC	IrDA Tx Polarity Change 0: Active-low Tx polarity setting. 1: Active-high Tx polarity setting.	0x0	R/W
23	RPOLC	IrDA Rx Polarity Change 0: Active-low Rx polarity setting. 1: Active-high Rx polarity setting.	0x0	R/W
22	FCPOL	Flow Control Pin Polarity 0: Active low CTS/RTS. 1: Active high CTS/RTS.	0x0	R/W
[21:20]	RESERVED	Reserved	0x0	R/W
19	SB	Set Break 0: No force. 1: Force Tx pin to 0.	0x0	R/W
18	FFE	Force Framing Error on Transmit 0: Normal operation. 1: Force error.	0x0	R/W
17	FPE	Force Parity Error on Transmit 0: Normal operation. 1: Force parity error.	0x0	R/W
16	STP	Sticky Parity 0: No forced parity. 1: Force (Stick) parity to defined value (if PEN = 1).	0x0	R/W
15	PARITY_SEL	Even Parity Select 0: Odd parity. 1: Even parity.	0x0	R/W
14	PEN	Parity Enable 0: Disable 1: Enable parity transmit and check.	0x0	R/W
13	STBH	Stop Bits (Half Bit Time) 0: 0 half-bit-time stop bit. 1: 1 half-bit-time stop bit.	0x0	R/W
12	STB	Stop Bits. This bit controls how many stop bits are appended to transmitted data. 0: 1 stop bit. 1: 2 stop bits.	0x0	R/W
[11:10]	RESERVED	Reserved	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[9:8]	WLS	Word Length Select 00: 5-Bit Word 01: 6-Bit Word 10: 7-Bit Word 11: 8-Bit Word	0x0	R/W
[7:6]	RESERVED	Reserved	0x0	R/W
[5:4]	MOD	Mode of Operation. This bit selects the UART operation mode (UMOD). 00: UART Mode 01: MDB Mode 10: IrDA SIR Mode	0x0	R/W
[3:2]	RESERVED	Reserved	0x0	R/W
1	LOOP_EN	Loopback Enable 0: Disable 1: Enable	0x0	R/W
0	EN	Enable UART 0: Disable 1: Enable	0x0	R/W

STATUS REGISTER

Address: 0xF0012008, Reset: 0x000000A0, Name: STAT

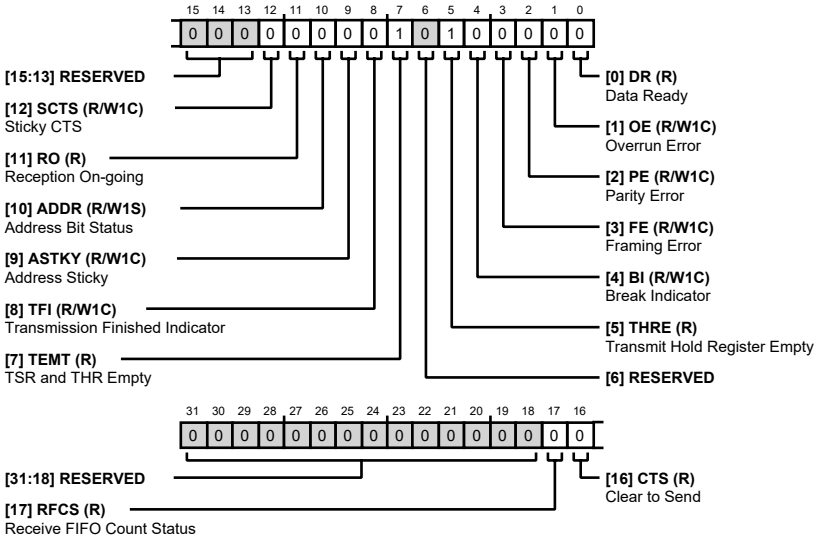


Table 378. Bit Descriptions for STAT

Bits	Bit Name	Description	Reset	Access
[31:18]	RESERVED	Reserved	0x0	R
17	RFCS	Receive FIFO Count Status 0: Rx FIFO has less than 4 (7) entries when RFIT = 0 (1). 1: Rx FIFO has at least 4 (7) entries when RFIT = 0 (1).	0x0	R

Bits	Bit Name	Description	Reset	Access
16	CTS	Clear to Send 0: Not clear to send (External device not ready to receive). 1: Clear to send (External device ready to receive).	0x0	R
[15:13]	RESERVED	Reserved	0x0	R
12	SCTS	Sticky CTS 0: CTS has not transitioned from low to high. 1: CTS has transitioned from low to high.	0x0	R/W1C
11	RO	Reception On-going 0: No data reception in progress. 1: Data reception in progress.	0x0	R
10	ADDR	Address Bit Status 0: Address bit is low. 1: Address bit is high.	0x0	R/W1S
9	ASTKY	Address Sticky 0: ADDR bit has not been set. 1: ADDR bit has been set.	0x0	R/W1C
8	TFI	Transmission Finished Indicator 0: TEMT did not transition from 0 to 1. 1: TEMT transition from 0 to 1.	0x0	R/W1C
7	TEMT	TSR and THR Empty 0: Not empty TSR/THR. 1: TSR/THR empty.	0x1	R
6	RESERVED	Reserved	0x0	R
5	THRE	Transmit Hold Register Empty 0: Not empty THR/TAIP. 1: Empty THR/TAIP.	0x1	R
4	BI	Break Indicator 0: No break interrupt. 1: Break interrupt. this indicates UARTxRX was held low (RPOLC = 0) / high (RPOLC = 1) for more than the maximum word length.	0x0	R/W1C
3	FE	Framing Error 0: No error. 1: Invalid stop bit error.	0x0	R/W1C
2	PE	Parity Error 0: No parity error. 1: Parity error.	0x0	R/W1C
1	OE	Overrun Error 0: No overrun. 1: Overrun error.	0x0	R/W1C
0	DR	Data Ready 0: No new data. 1: New data in RBR.	0x0	R

CLOCK RATE REGISTER

Address: 0xF0012010, Reset: 0x0000FFFF, Name: CLK

The UART_CLK register divides the system clock (SCLK) down to the bit clock.

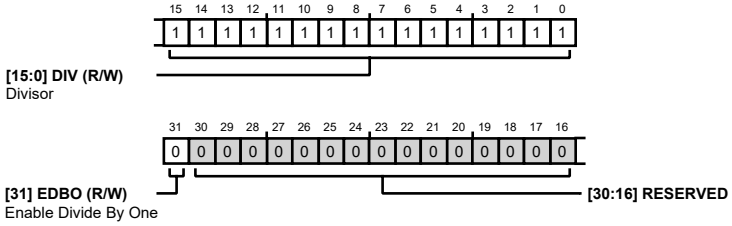


Table 379. Bit Descriptions for CLK

Bits	Bit Name	Description	Reset	Access
31	EDBO	Enable Divide by One. This bit enables bypassing of the divide-by-16 prescaler in bit clock generation. This improves bit rate granularity, especially at high bit rates. Do not set this bit in IrDA mode. 0: Bit clock prescaler = 16. 1: Bit clock prescaler = 1.	0x0	R/W
[30:16]	RESERVED	Reserved	0x0	R
[15:0]	DIV	Divisor. These bits set the divisor for the UART's clock bit rate calculation. The bit rate is defined by the formula: Bit Rate = SCLK / $16^{(1\text{-EDBo})}$ x DIV, where SCLK = system clock.	0xFFFF	R/W

INTERRUPT MASK REGISTER

Address: 0xF0012014, Reset: 0x00000000, Name: IMSK

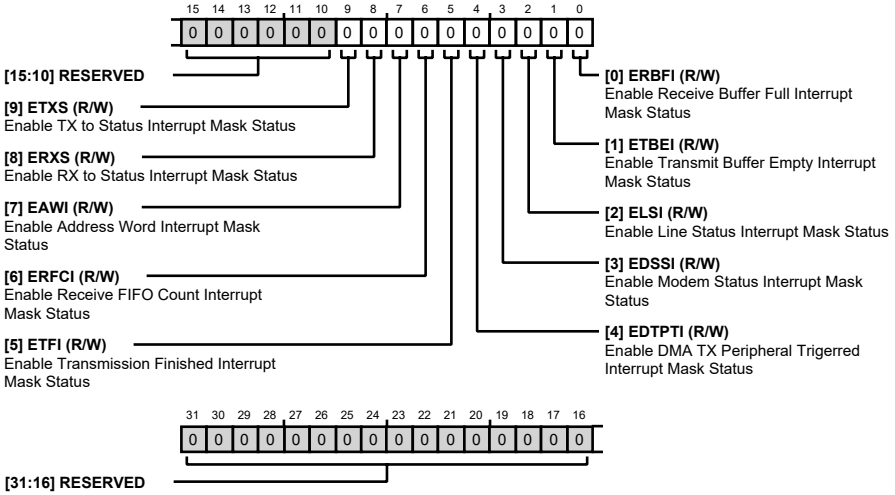


Table 380. Bit Descriptions for IMSK

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	ETXS	Enable Tx to Status Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
8	ERXS	Enable Rx to Status Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
7	EAWI	Enable Address Word Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
6	ERFCI	Enable Receive FIFO Count Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
5	ETFI	Enable Transmission Finished Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
4	EDTPTI	Enable DMA Tx Peripheral Triggered Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
3	EDSSI	Enable Modem Status Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
2	ELSI	Enable Line Status Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
1	ETBEI	Enable Transmit Buffer Empty Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W
0	ERBFI	Enable Receive Buffer Full Interrupt Mask Status 0: Interrupt is masked. 1: Interrupt is unmasked.	0x0	R/W

INTERRUPT MASK SET REGISTER

Address: 0xF0012018, Reset: 0x00000000, Name: IMSK_SET

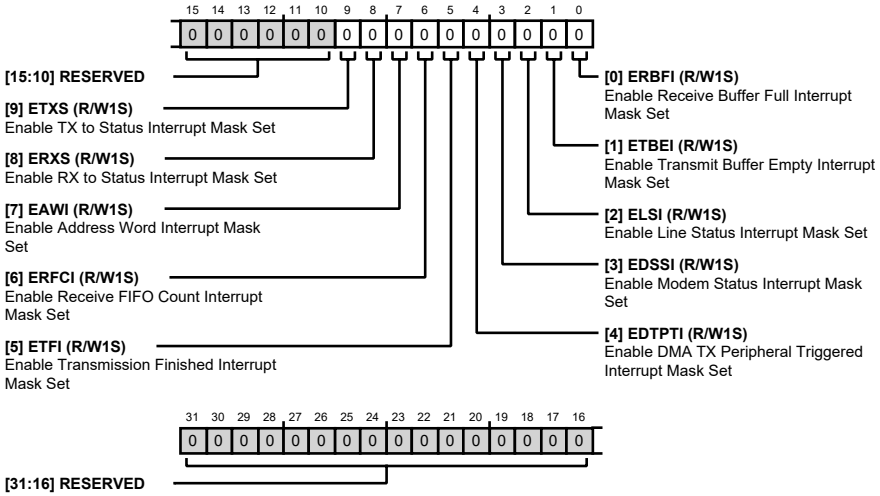


Table 381. Bit Descriptions for IMSK_SET

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	ETXS	Enable Tx to Status Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
8	ERXS	Enable Rx to Status Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
7	EAWI	Enable Address Word Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
6	ERFCI	Enable Receive FIFO Count Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
5	ETFI	Enable Transmission Finished Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
4	EDTPTI	Enable DMA Tx Peripheral Triggered Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
3	EDSSI	Enable Modem Status Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
2	ELSI	Enable Line Status Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
1	ETBEI	Enable Transmit Buffer Empty Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S
0	ERBFI	Enable Receive Buffer Full Interrupt Mask Set 0: No action. 1: Unmask interrupt.	0x0	R/W1S

INTERRUPT MASK CLEAR REGISTER

Address: 0xF001201C, Reset: 0x00000000, Name: IMSK_CLR

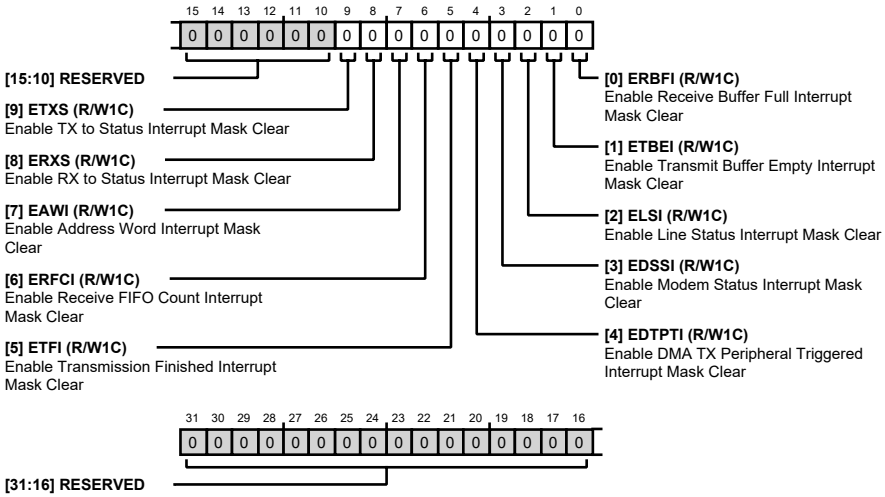


Table 382. Bit Descriptions for IMSK_CLR

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
9	ETXS	Enable Tx to Status Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
8	ERXS	Enable Rx to Status Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
7	EAWI	Enable Address Word Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
6	ERFCI	Enable Receive FIFO Count Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
5	ETFI	Enable Transmission Finished Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
4	EDTPTI	Enable DMA Tx Peripheral Triggered Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
3	EDSSI	Enable Modem Status Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
2	ELSI	Enable Line Status Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
1	ETBEI	Enable Transmit Buffer Empty Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C
0	ERBFI	Enable Receive Buffer Full Interrupt Mask Clear 0: No action. 1: Mask interrupt.	0x0	R/W1C

RECEIVE BUFFER REGISTER

Address: 0xF0012020, Reset: 0x00000000, Name: RBR

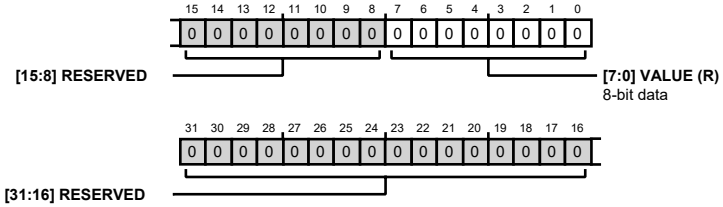


Table 383. Bit Descriptions for RBR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	VALUE	8-Bit Data	0x0	R

TRANSMIT HOLD REGISTER

Address: 0xF0012024, Reset: 0x00000000, Name: THR

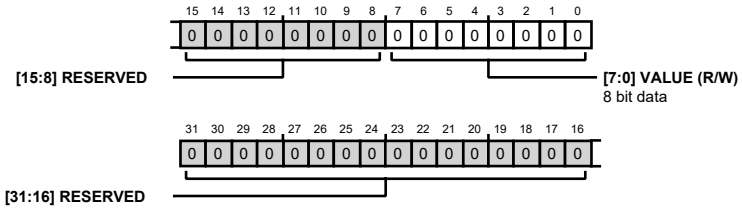


Table 384. Bit Descriptions for THR

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	VALUE	8-Bit Data	0x0	R/W

TRANSMIT ADDRESS/INSERT PULSE REGISTER

Address: 0xF0012028, Reset: 0x00000000, Name: TAIP

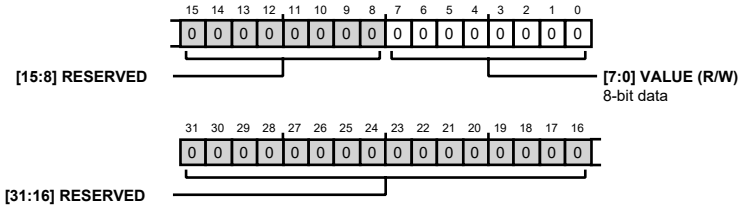


Table 385. Bit Descriptions for TAIP

Bits	Bit Name	Description	Reset	Access
[31:8]	RESERVED	Reserved	0x0	R
[7:0]	VALUE	8-Bit Data	0x0	R/W

TRANSMIT SHIFT REGISTER

Address: 0xF001202C, Reset: 0x000007FF, Name: TSR

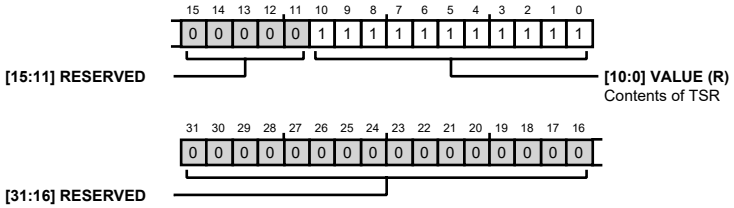


Table 386. Bit Descriptions for TSR

Bits	Bit Name	Description	Reset	Access
[31:11]	RESERVED	Reserved	0x0	R
[10:0]	VALUE	Contents of TSR	0x7FF	R

RECEIVE SHIFT REGISTER

Address: 0xF0012030, Reset: 0x00000000, Name: RSR

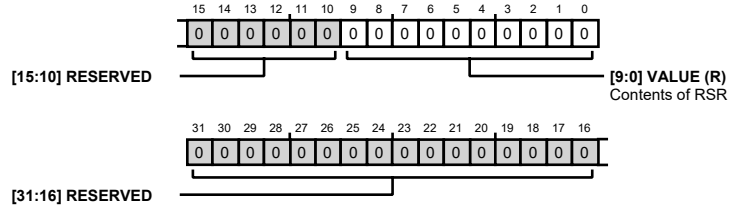


Table 387. Bit Descriptions for RSR

Bits	Bit Name	Description	Reset	Access
[31:10]	RESERVED	Reserved	0x0	R
[9:0]	VALUE	Contents of RSR	0x0	R

TRANSMIT COUNTER REGISTER

Address: 0xF0012034, Reset: 0x00000000, Name: TXCNT

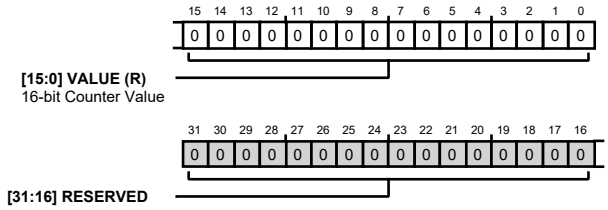


Table 388. Bit Descriptions for TXCNT

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	16-Bit Counter Value	0x0	R

RECEIVE COUNTER REGISTER

Address: 0xF0012038, Reset: 0x00000000, Name: RXCNT

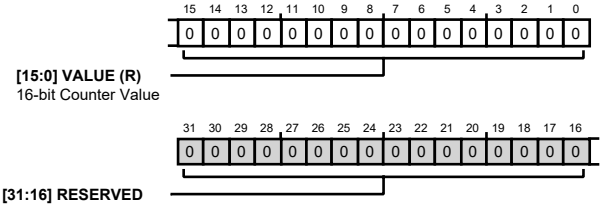


Table 389. Bit Descriptions for RXCNT

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved	0x0	R
[15:0]	VALUE	16-Bit Counter Value	0x0	R

REGISTER DETAILS: UART DDE0

POINTER TO NEXT INITIAL DESCRIPTOR REGISTER

Address: 0xF0012100, Reset: 0x00000000, Name: DSCPTR_NXT

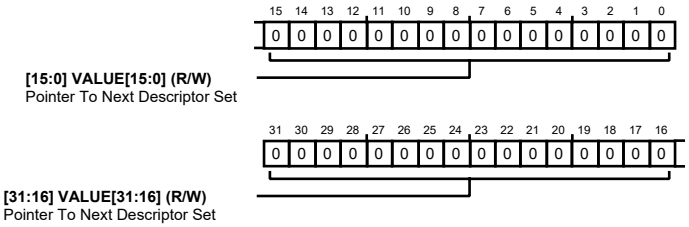


Table 390. Bit Descriptions for DSCPTR_NXT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer To Next Descriptor Set.	0x0	R/W

START ADDRESS OF CURRENT BUFFER

Address: 0xF0012104, Reset: 0x00000000, Name: ADDRSTART

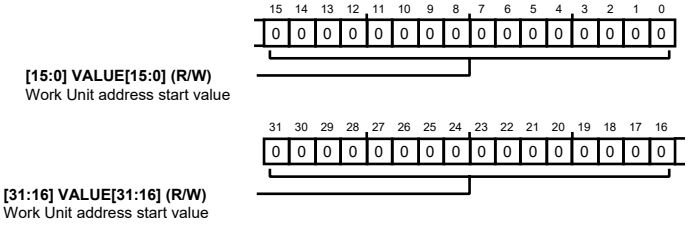


Table 391. Bit Descriptions for ADDRSTART

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit address start value.	0x0	R/W

CONFIGURATION REGISTER

Address: 0xF0012108, Reset: 0x00000000, Name: CFG

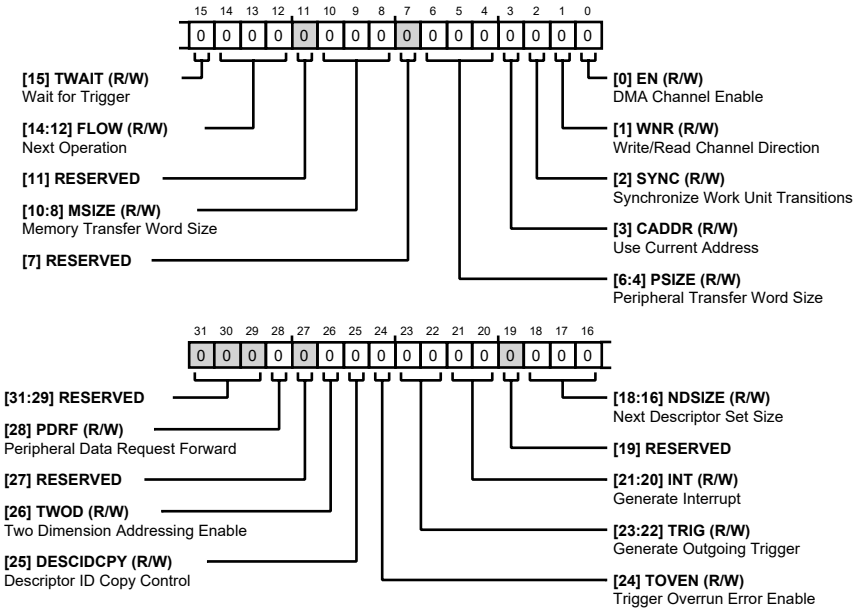


Table 392. Bit Descriptions for CFG

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved	0x0	R
28	PDRF	Peripheral Data Request Forward. 0: Peripheral data request not forwarded. 1: Peripheral data request forwarded.	0x0	R/W
27	RESERVED	Reserved	0x0	R
26	TWOD	Two Dimension Addressing Enable. 0: One-Dimensional addressing. 1: Two-Dimensional addressing.	0x0	R/W
25	DESCIDCPY	Descriptor ID Copy Control. 0: Never copy 1: Copy on work unit complete	0x0	R/W
24	TOVEN	Trigger Overrun Error Enable. 0: Ignore trigger overrun. 1: Error on trigger overrun	0x0	R/W
[23:22]	TRIG	Generate Outgoing Trigger. 00: Never assert trigger. 01: Trigger when XCNTCUR reaches 0. 10: Trigger when YCNTCUR reaches 0. 11: Reserved	0x0	R/W
[21:20]	INT	Generate Interrupt 00: Never assert interrupt. 01: Interrupt when X Count Expires.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		10: Interrupt when Y Count Expires. 11: Peripheral Interrupt.		
19	RESERVED	Reserved	0x0	R
[18:16]	NDSIZE	Next Descriptor Set Size. 000: Fetch one Descriptor Element. 001: Fetch two Descriptor Elements. 010: Fetch three Descriptor Elements. 011: Fetch four Descriptor Elements. 100: Fetch five Descriptor Elements. 101: Fetch six Descriptor Elements. 110: Fetch seven Descriptor Elements. 111: Reserved.	0x0	R/W
15	TWAIT	Wait for Trigger. 0: Begin Work Unit Automatically (No Wait). 1: Wait for Trigger (Halt before Work Unit).	0x0	R/W
[14:12]	FLOW	Next Operation. 000: Stop. 001: Autobuffer. 010: Reserved. 011: Reserved. 100: Descriptor List. 101: Descriptor Array. 110: Descriptor On Demand List. 111: Descriptor On Demand Array.	0x0	R/W
11	RESERVED	Reserved	0x0	R
[10:8]	MSIZE	Memory Transfer Word Size. 000: 1 Byte. 001: 2 Bytes. 010: 4 Bytes. 011: 8 Bytes. 100: 16 Bytes. 101: 32 Bytes.	0x0	R/W
7	RESERVED	Reserved	0x0	R
[6:4]	PSIZE	Peripheral Transfer Word Size. 000: 1 Byte. 001: 2 Bytes. 010: 4 Bytes. 011: 8 Bytes.	0x0	R/W
3	CADDR	Use Current Address. 0: Load starting address. 1: Use current address.	0x0	R/W
2	SYNC	Synchronize Work Unit Transitions. 0: No synchronization. 1: Synchronize channel.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	WNR	Write/Read Channel Direction. 0: Transmit. 1: Receive.	0x0	R/W
0	EN	DMA Channel Enable. 0: Disable. 1: Enable.		R/W

INNER LOOP COUNT START VALUE REGISTER

Address: 0xF001210C, Reset: 0x00000000, Name: XCNT

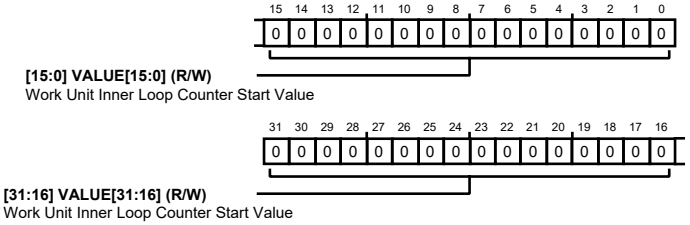


Table 393. Bit Descriptions for XCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Start Value.	0x0	R/W

INNER LOOP ADDRESS INCREMENT REGISTER

Address: 0xF0012110, Reset: 0x00000000, Name: XMOD

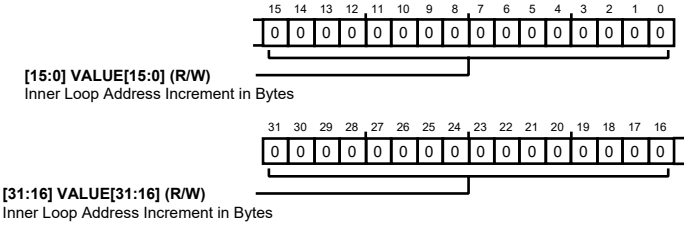


Table 394. Bit Descriptions for XMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Inner Loop Address Increment in Bytes.	0x0	R/W

OUTER LOOP COUNT START VALUE (2D ONLY) REGISTER

Address: 0xF0012114, Reset: 0x00000000, Name: YCNT

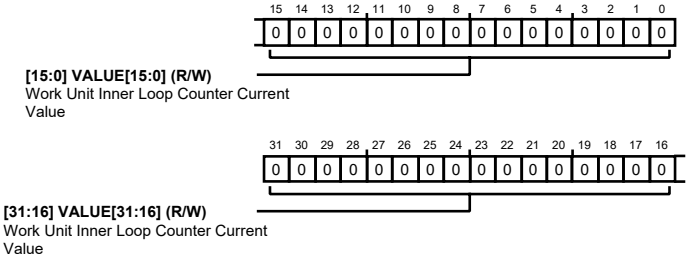


Table 395. Bit Descriptions for YCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Current Value.	0x0	R/W

OUTER LOOP ADDRESS INCREMENT (2D ONLY) REGISTER

Address: 0xF0012118, Reset: 0x00000000, Name: YMOD

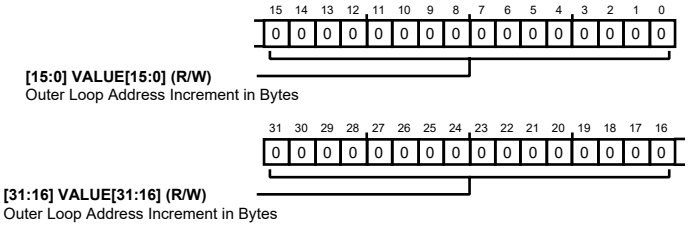


Table 396. Bit Descriptions for YMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Outer Loop Address Increment in Bytes.	0x0	R/W

CURRENT DESCRIPTOR POINTER REGISTER

Address: 0xF0012124, Reset: 0x00000000, Name: DSCPTR_CUR

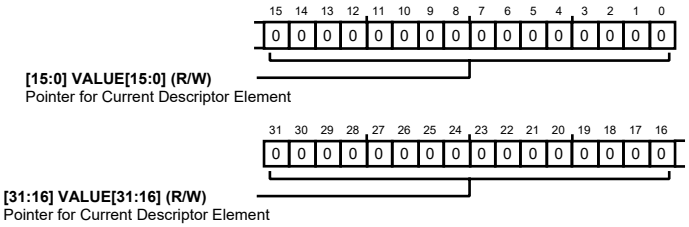


Table 397. Bit Descriptions for DSCPTR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer for Current Descriptor Element.	0x0	R/W

PREVIOUS INITIAL DESCRIPTOR POINTER REGISTER

Address: 0xF0012128, Reset: 0x00000000, Name: DSCPTR_PRV

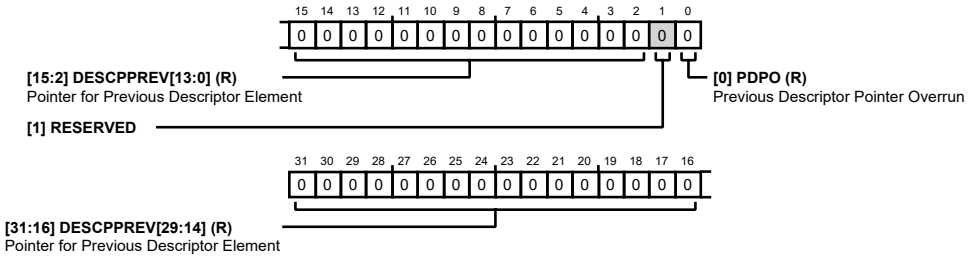


Table 398. Bit Descriptions for DSCPTR_PRV

Bits	Bit Name	Description	Reset	Access
[31:2]	DESCPPREV	Pointer for Previous Descriptor Element.	0x0	R
1	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
0	PDPO	Previous Descriptor Pointer Overrun.	0x0	R

CURRENT ADDRESS REGISTER

Address: 0xF001212C, Reset: 0x00000000, Name: ADDR_CUR

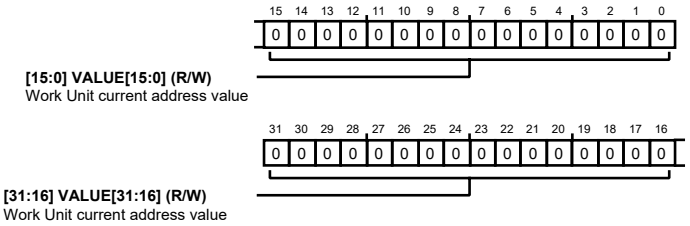


Table 399. Bit Descriptions for ADDR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit current address value.	0x0	R/W

STATUS REGISTER

Address: 0xF0012130, Reset: 0x00006000, Name: STAT

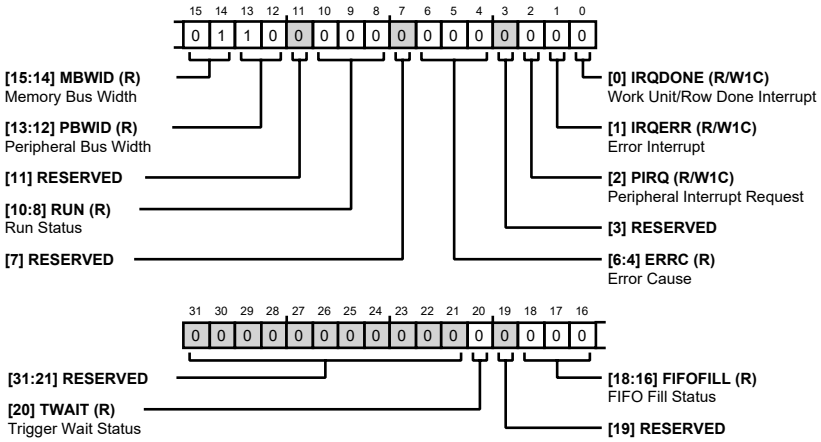


Table 400. Bit Descriptions for STAT

Bits	Bit Name	Description	Reset	Access
[31:21]	RESERVED	Reserved.	0x0	R
20	TWAIT	Trigger Wait Status. 0: No trigger received. 1: Trigger received.	0x0	R
19	RESERVED	Reserved.	0x0	R
[18:16]	FIFOFILL	FIFO Fill Status. 000: Empty. 001: Empty < FIFO = 1/4 Full. 010: 1/4 Full < FIFO = 1/2 Full. 011: 1/2 Full < FIFO = 3/4 Full. 100: 3/4 Full < FIFO = Full. 101: Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
		110: Reserved. 111: Full.		
[15:14]	MBWID	Memory Bus Width. 00: 2 Bytes. 01: 4 Bytes. 10: 8 Bytes. 11: 16 Bytes.	0x1	R
[13:12]	PBWID	Peripheral Bus Width. 00: 1 Byte. 01: 2 Bytes. 10: 4 Bytes. 11: 8 Bytes.	0x2	R
11	RESERVED	Reserved.	0x0	R
[10:8]	RUN	Run Status. 000: Idle/Stop State. 001: Descriptor Fetch. 010: Data Transfer. 011: Waiting for Trigger. 100: Waiting for Write ACK/FIFO Drain to Peripheral. 101: Reserved. 110: Reserved. 111: Reserved.	0x0	R
7	RESERVED	Reserved.	0x0	R
[6:4]	ERRC	Error Cause. 000: Configuration Error. 001: Illegal Write Occurred While Channel Running. 010: Address Alignment Error. 011: Memory Access/Fabric Error. 100: Reserved. 101: Trigger Overrun. 110: Bandwidth Monitor Error. 111: Reserved.	0x0	R
3	RESERVED	Reserved.	0x0	R
2	PIRQ	Peripheral Interrupt Request. 0: No Interrupt. 1: Interrupt Signaled by Peripheral.	0x0	R/W1C
1	IRQERR	Error Interrupt. 0: No Error. 1: Error Occurred.	0x0	R/W1C
0	IRQDONE	Work Unit/Row Done Interrupt. 0: Inactive.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: Active.		

CURRENT COUNT(1D) OR INTRA-ROW XCNT (2D) REGISTER

Address: 0xF0012134, Reset: 0x00000000, Name: XCNT_CUR

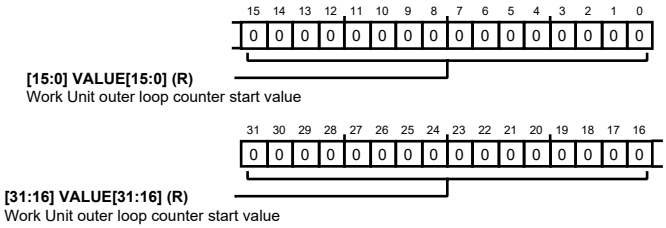


Table 401. Bit Descriptions for XCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit outer loop counter start value.	0x0	R

CURRENT ROW COUNT (2D ONLY) REGISTER

Address: 0xF0012138, Reset: 0x00000000, Name: YCNT_CUR

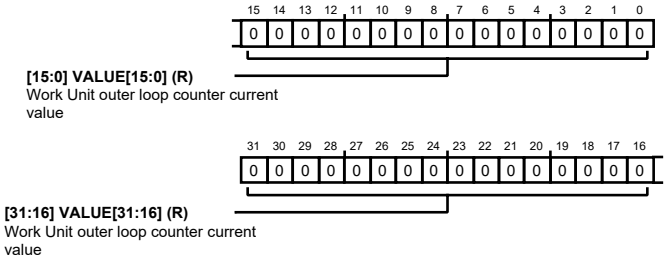


Table 402. Bit Descriptions for YCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit outer loop counter current value.	0x0	R

BANDWIDTH LIMIT COUNT REGISTER

Address: 0xF0012140, Reset: 0x00000000, Name: BWLCNT

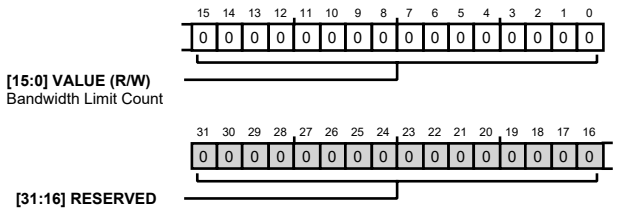


Table 403. Bit Descriptions for BWLCNT

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	VALUE	Bandwidth Limit Count.	0x0	R/W

BANDWIDTH LIMIT COUNT CURRENT REGISTER

Address: 0xF0012144, Reset: 0x00000000, Name: BWLCNT_CUR

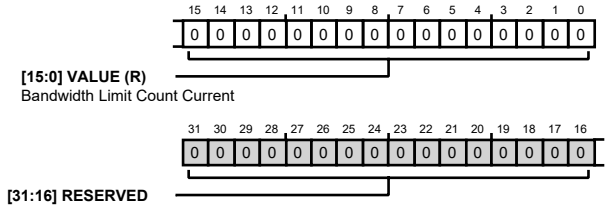


Table 404. Bit Descriptions for BWLCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	VALUE	Bandwidth Limit Count Current.	0x0	R

BANDWIDTH MONITOR COUNT REGISTER

Address: 0xF0012148, Reset: 0x00000000, Name: BWMCNT

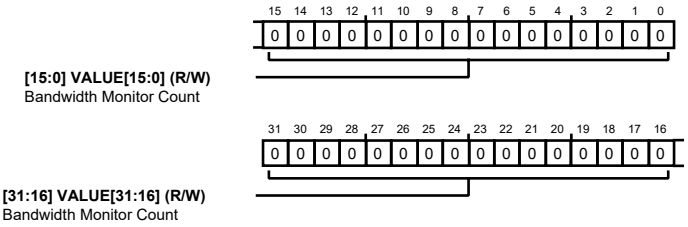


Table 405. Bit Descriptions for BWMCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count.	0x0	R/W

BANDWIDTH MONITOR COUNT CURRENT REGISTER

Address: 0xF001214C, Reset: 0x00000000, Name: BWMCNT_CUR

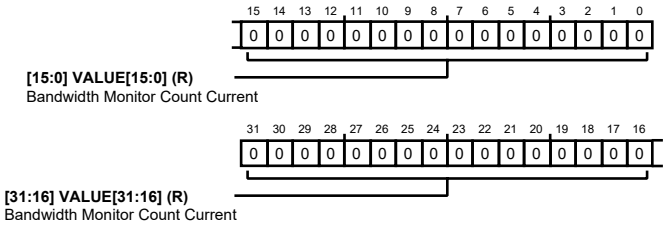


Table 406. Bit Descriptions for BWMCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count Current.	0x0	R

REGISTER DETAILS: UART DDE1

POINTER TO NEXT INITIAL DESCRIPTOR REGISTER

Address: 0xF0012180, Reset: 0x00000000, Name: DSCPTR_NXT

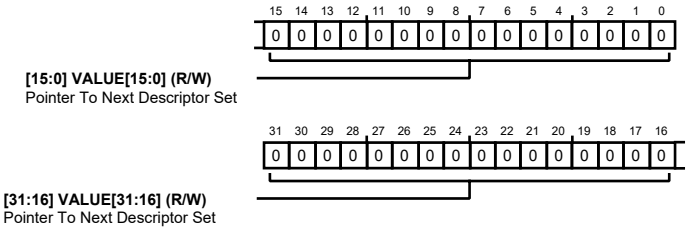


Table 407. Bit Descriptions for DSCPTR_NXT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer To Next Descriptor Set.	0x0	R/W

START ADDRESS OF CURRENT BUFFER REGISTER

Address: 0xF0012184, Reset: 0x00000000, Name: ADDRSTART

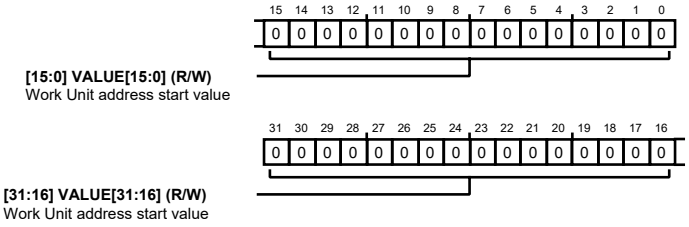


Table 408. Bit Descriptions for ADDRSTART

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit address start value.	0x0	R/W

CONFIGURATION REGISTER

Address: 0xF0012188, Reset: 0x00000000, Name: CFG

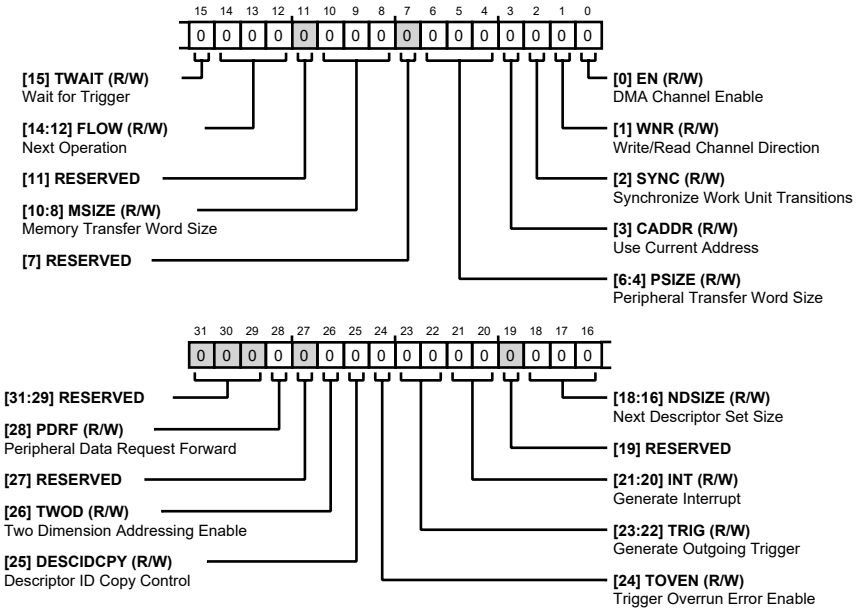


Table 409. Bit Descriptions for CFG

Bits	Bit Name	Description	Reset	Access
[31:29]	RESERVED	Reserved.	0x0	R
28	PDRF	Peripheral Data Request Forward. 0: Peripheral Data Request Not Forwarded. 1: Peripheral Data Request Forwarded.	0x0	R/W
27	RESERVED	Reserved.	0x0	R
26	TWOD	Two Dimension Addressing Enable. 0: One-Dimensional Addressing. 1: Two-Dimensional Addressing.	0x0	R/W
25	DESCIDCPY	Descriptor ID Copy Control. 0: Never Copy. 1: Copy on Work Unit Complete.	0x0	R/W
24	TOVEN	Trigger Overrun Error Enable. 0: Ignore Trigger Overrun. 1: Error on Trigger Overrun.	0x0	R/W
[23:22]	TRIG	Generate Outgoing Trigger. 00: Never assert Trigger. 01: Trigger when XCNTCUR reaches 0. 10: Trigger when YCNTCUR reaches 0. 11: Reserved.	0x0	R/W
[21:20]	INT	Generate Interrupt. 00: Never assert Interrupt. 01: Interrupt when X Count Expires. 10: Interrupt when Y Count Expires. 11: Peripheral Interrupt.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
19	RESERVED	Reserved.	0x0	R
[18:16]	NDSIZE	Next Descriptor Set Size. 000: Fetch one Descriptor Element. 001: Fetch two Descriptor Elements. 010: Fetch three Descriptor Elements. 011: Fetch four Descriptor Elements. 100: Fetch five Descriptor Elements. 101: Fetch six Descriptor Elements. 110: Fetch seven Descriptor Elements. 111: Reserved.	0x0	R/W
15	TWAIT	Wait for Trigger. 0: Begin Work Unit Automatically (No Wait). 1: Wait for Trigger (Halt before Work Unit).	0x0	R/W
[14:12]	FLOW	Next Operation. 000: Stop. 001: Autobuffer 010: Reserved. 011: Reserved. 100: Descriptor List. 101: Descriptor Array. 110: Descriptor On Demand List. 111: Descriptor On Demand Array.	0x0	R/W
11	RESERVED	Reserved.	0x0	R
[10:8]	MSIZE	Memory Transfer Word Size. 000: 1 Byte. 001: 2 Bytes. 010: 4 Bytes. 011: 8 Bytes. 100: 16 Bytes. 101: 32 Bytes.	0x0	R/W
7	RESERVED	Reserved.	0x0	R
[6:4]	PSIZE	Peripheral Transfer Word Size. 000: 1 Byte. 001: 2 Bytes. 010: 4 Bytes. 011: 8 Bytes.	0x0	R/W
3	CADDR	Use Current Address. 0: Load Starting Address. 1: Use Current Address.	0x0	R/W
2	SYNC	Synchronize Work Unit Transitions. 0: No Synchronization. 1: Synchronize Channel.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	WNR	Write/Read Channel Direction. 0: Transmit (Read from memory). 1: Receive (Write to memory).	0x0	R/W

INNER LOOP COUNT START VALUE REGISTER

Address: 0xF001218C, Reset: 0x00000000, Name: XCNT

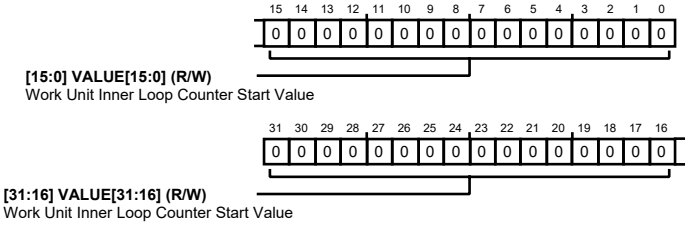


Table 410. Bit Descriptions for XCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Start Value.	0x0	R/W

INNER LOOP ADDRESS INCREMENT REGISTER

Address: 0xF0012190, Reset: 0x00000000, Name: XMOD

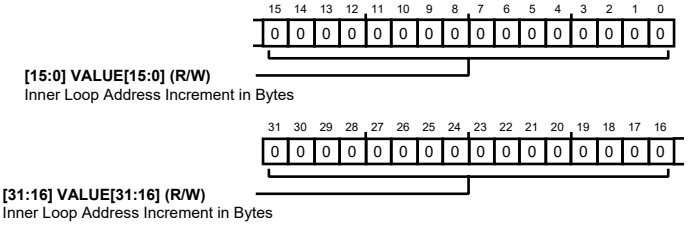


Table 411. Bit Descriptions for XMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Inner Loop Address Increment in Bytes.	0x0	R/W

OUTER LOOP COUNT START VALUE (2D ONLY) REGISTER

Address: 0xF0012194, Reset: 0x00000000, Name: YCNT

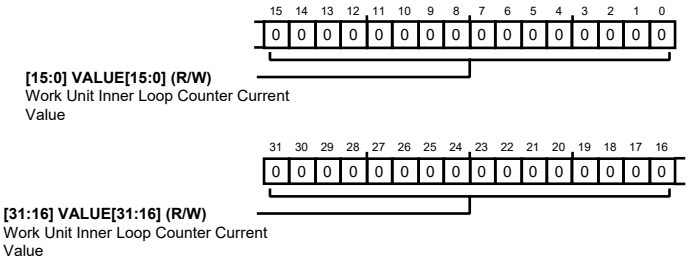


Table 412. Bit Descriptions for YCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit Inner Loop Counter Current Value.	0x0	R/W

OUTER LOOP ADDRESS INCREMENT (2D ONLY) REGISTER

Address: 0xF0012198, Reset: 0x00000000, Name: YMOD

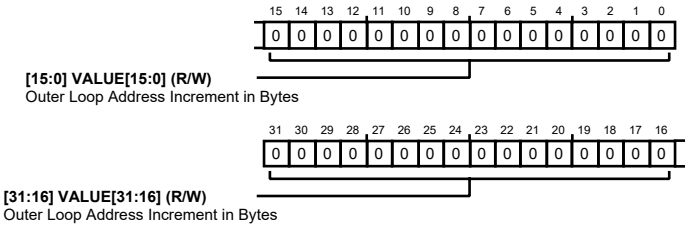


Table 413. Bit Descriptions for YMOD

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Outer Loop Address Increment in Bytes.	0x0	R/W

CURRENT DESCRIPTOR POINTER REGISTER

Address: 0xF00121A4, Reset: 0x00000000, Name: DSCPTR_CUR

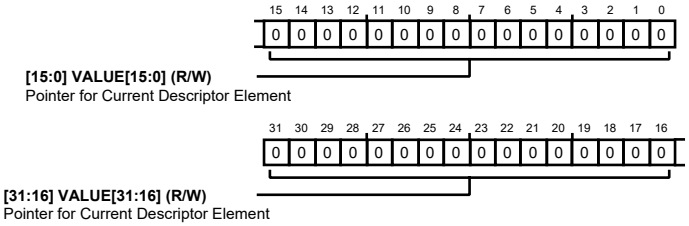


Table 414. Bit Descriptions for DSCPTR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Pointer for Current Descriptor Element.	0x0	R/W

PREVIOUS INITIAL DESCRIPTOR POINTER REGISTER

Address: 0xF00121A8, Reset: 0x00000000, Name: DSCPTR_PRV

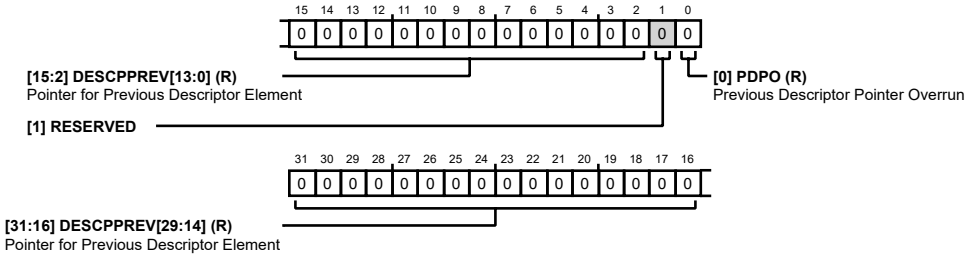


Table 415. Bit Descriptions for DSCPTR_PRV

Bits	Bit Name	Description	Reset	Access
[31:2]	DESCPPREV	Pointer for Previous Descriptor Element.	0x0	R
1	RESERVED	Reserved.	0x0	R
0	PDPO	Previous Descriptor Pointer Overrun.	0x0	R

CURRENT ADDRESS REGISTER

Address: 0xF00121AC, Reset: 0x00000000, Name: ADDR_CUR

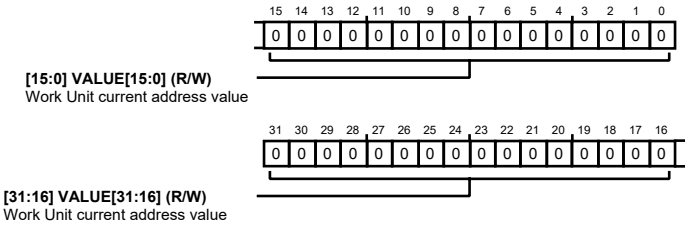


Table 416. Bit Descriptions for ADDR_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit current address value.	0x0	R/W

STATUS REGISTER

Address: 0xF00121B0, Reset: 0x00006000, Name: STAT

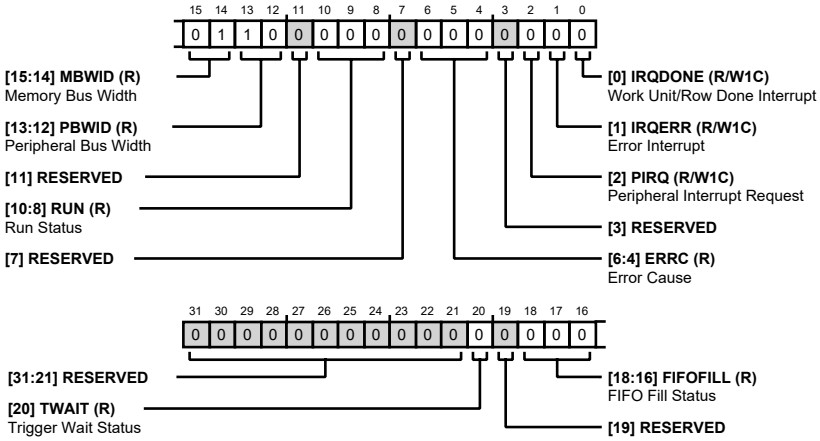


Table 417. Bit Descriptions for STAT

Bits	Bit Name	Description	Reset	Access
[31:21]	RESERVED	Reserved.	0x0	R
20	TWAIT	Trigger Wait Status. 0: No trigger received. 1: Trigger received.	0x0	R
19	RESERVED	Reserved.	0x0	R
[18:16]	FIFOFILL	FIFO Fill Status 000: Empty. 001: Empty < FIFO = 1/4 Full. 010: 1/4 Full < FIFO = 1/2 Full. 011: 1/2 Full < FIFO = 3/4 Full. 100: 3/4 Full < FIFO = Full. 101: Reserved. 110: Reserved. 111: Full.	0x0	R

Bits	Bit Name	Description	Reset	Access
[15:14]	MBWID	Memory Bus Width 00: 2 Bytes. 01: 4 Bytes. 10: 8 Bytes. 11: 16 Bytes.	0x1	R
[13:12]	PBWID	Peripheral Bus Width. 00: 1 Byte. 01: 2 Bytes. 10: 4 Bytes. 11: 8 Bytes.	0x2	R
11	RESERVED	Reserved.	0x0	R
[10:8]	RUN	Run Status. 000: Idle/Stop State. 001: Descriptor Fetch. 010: Data Transfer. 011: Waiting for Trigger. 100: Waiting for Write ACK/FIFO Drain to Peripheral. 101: Reserved. 110: Reserved. 111: Reserved.	0x0	R
7	RESERVED	Reserved.	0x0	R
[6:4]	ERRC	Error Cause. 000: Configuration Error. 001: Illegal Write Occurred While Channel Running. 010: Address Alignment Error. 011: Memory Access/Fabric Error. 100: Reserved. 101: Trigger Overrun. 110: Bandwidth Monitor Error. 111: Reserved.	0x0	R
3	RESERVED	Reserved.	0x0	R
2	PIRQ	Peripheral Interrupt Request. 0: No Interrupt. 1: Interrupt Signaled by Peripheral.	0x0	R/W1C
1	IRQERR	Error Interrupt. 0: No Error. 1: Error Occurred.	0x0	R/W1C
0	IRQDONE	Work Unit/Row Done Interrupt. 0: Inactive. 1: Active.	0x0	R/W1C

CURRENT COUNT(1D) OR INTRA-ROW XCNT (2D) REGISTER

Address: 0xF00121B4, Reset: 0x00000000, Name: XCNT_CUR

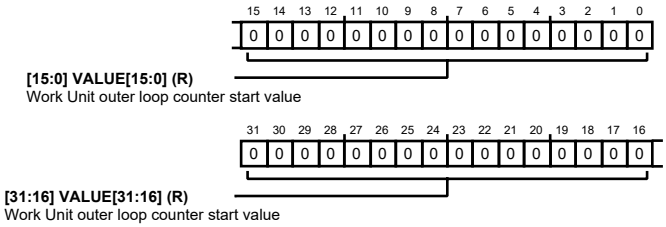


Table 418. Bit Descriptions for XCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit outer loop counter start value.	0x0	R

CURRENT ROW COUNT (2D ONLY) REGISTER

Address: 0xF00121B8, Reset: 0x00000000, Name: YCNT_CUR

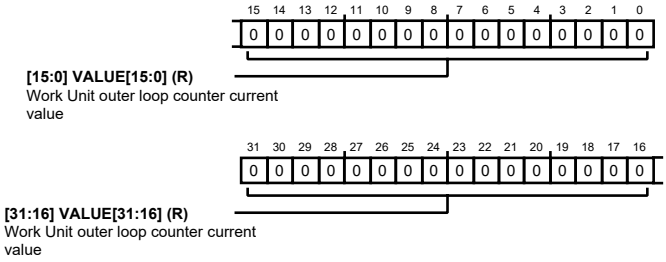


Table 419. Bit Descriptions for YCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Work Unit outer loop counter current value.	0x0	R

BANDWIDTH LIMIT COUNT REGISTER

Address: 0xF00121C0, Reset: 0x00000000, Name: BWLCNT

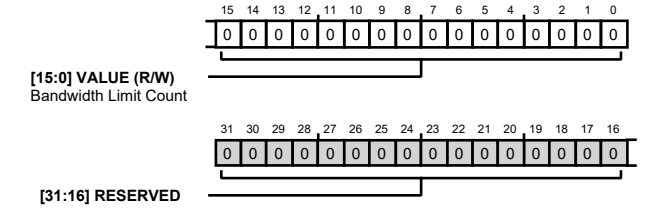


Table 420. Bit Descriptions for BWLCNT

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	VALUE	Bandwidth Limit Count.	0x0	R/W

BANDWIDTH LIMIT COUNT CURRENT REGISTER

Address: 0xF00121C4, Reset: 0x00000000, Name: BWLCNT_CUR

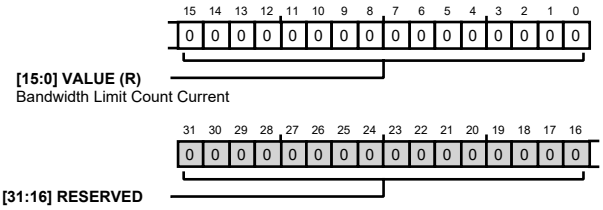


Table 421. Bit Descriptions for BWLCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:16]	RESERVED	Reserved.	0x0	R
[15:0]	VALUE	Bandwidth Limit Count Current.	0x0	R

BANDWIDTH MONITOR COUNT REGISTER

Address: 0xF00121C8, Reset: 0x00000000, Name: BWMCNT

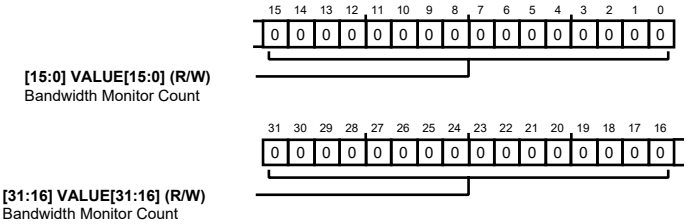


Table 422. Bit Descriptions for BWMCNT

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count.	0x0	R/W

BANDWIDTH MONITOR COUNT CURRENT REGISTER

Address: 0xF00121CC, Reset: 0x00000000, Name: BWMCNT_CUR

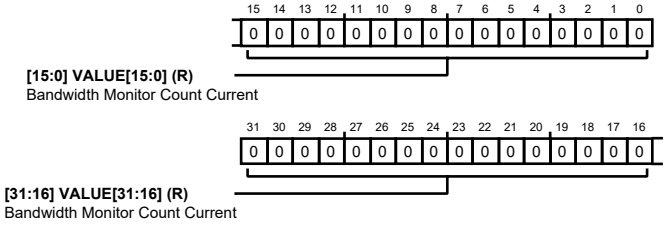


Table 423. Bit Descriptions for BWMCNT_CUR

Bits	Bit Name	Description	Reset	Access
[31:0]	VALUE	Bandwidth Monitor Count Current.	0x0	R

REGISTER DETAILS: I3C MASTER SLAVE

MASTER MODE CONFIGURATION REGISTER

Address: 0xF0013000, Reset: 0x00000000, Name: MCONFIG

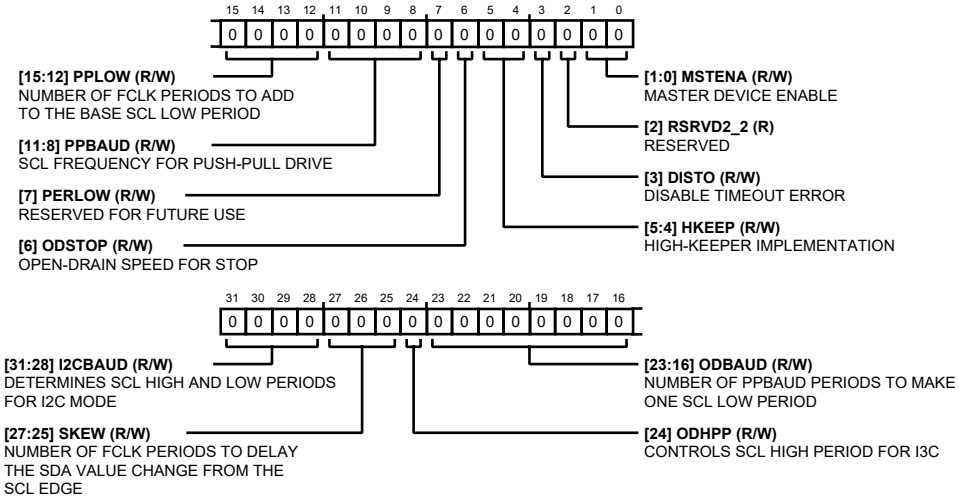


Table 424. Bit Descriptions for MCONFIG

Bits	Bit Name	Description	Reset	Access
[31:28]	I2CBAUD	Determines SCL High and Low Periods for I2c Mode, in units of ODBAUD period. The I2C mode SCL high period is (I2CBAUD >> 1) + 1 ODBAUD periods. For example, if I2CBAUD = 0001, then I2CBAUD >> 1 = 0 and the SCL high period is 0 + 1 = 1 ODBAUD period. If I2CBAUD[28] = 1 (I2CBAUD is an odd value), the SCL low period is one ODBAUD period longer than the SCL high period. Otherwise, the SCL low and high periods are equal. For example, if the ODBAUD period is 200 ns, setting I2CBAUD to 0x3 creates an I2C mode SCL waveform of 2 ODBAUD (400 ns) high and 3 ODBAUD (600 ns) low for an SCL period time of 1 s, which matches I2C Fm+. Similarly, for I2C Fm with the same ODBAUD period, I2CBAUD = 7 creates a 2.6- s SCL period and I2CBAUD = 6 creates a 2.4- s SCL period.	0x0	R/W
[27:25]	SKEW	Number Of FCLK Periods to Delay. The SDA Value Change From The SCL Edge for I3C push-pull operation. SKEW can be used to directly control the SCL-to-SDA skew if the inherent delay caused by SCL propagating SCL to the SCL pad and back to the I3C_MS does not provide sufficient skew. For details, see. The I3C_MS automatically uses an internally delayed version of SCL to create the necessary SCL-to-SDA skew for I2C operation and for I3C open-drain operation.	0x0	R/W
24	ODHPP	Controls SCL High Period for I3C Open-Drain Operation. 0: SCL high period is the same as the SCL low period for I3C open-drain operation 1: One PPBAUD period (typically used to make SCL high period short enough in duration to be masked by an I2C 50ns spike filter).	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[23:16]	ODBAUD	Number Of PPbaud Periods to Make One SCL Low Period for I3C open-drain operation. For example, if FCLK is 24 MHz (41.67 ns period) and PPBAUD = 0000, then one PPBAUD period is 41.67 ns. To exceed the minimum 200-ns SCL low period for I3C open-drain operation, set ODBAUD to 4 (4 + 1 = 5; 5 x 41.67 ns = 208.35 ns). If ODHPP = 1, the resulting SCL waveform for I3C open-drain operation would be 41.67-ns high and 208.35-ns low (250-ns period, 4 MHz).	0x0	R/W
[15:12]	PPLOW	Number Of Fclk Periods To Add To The Base SCL Low Period (set by PPBAUD) for push-pull operation. PPLOW can be used to extend the low period of SCL by up to fifteen fclk periods, thereby altering the SCL duty cycle and the SCL base frequency for push-pull operation as set by PPBAUD: PPLOW = 0001 adds one fclk period to the SCL low period set by PPBAUD. PPBAUD = 0000 the SCL high period is 20 ns. The SCL low period of 20 ns is extended one additional fclk period to 20 + 20 = 40 ns to create an SCL period of 60 ns (20 ns high and 40 ns low). PPLOW = 0010 adds two fclk periods to the SCL low period set by PPBAUD. … PPLOW = 1111 adds fifteen fclk periods to the SCL low period set by PPBAUD.	0x0	R/W
[11:8]	PPBAUD	Scl Frequency for Push-Pull Drive. PPBAUD sets the width of the SCL high period for push-pull operation as a function of the fclk frequency. PPBAUD also sets the base width of the SCL low period for push-pull operation. The SCL low period can be extended by setting a non-zero value for PPLOW. When PPLOW = 0, the SCL high and low periods are the same (50% duty cycle) for push-pull operation. The SCL high period (and unextended low period) are determined by PPBAUD and the fclk frequency as follows: PPBAUD = 0000: SCL high period is one fclk period. For example, if fclk is 50 MHz (20 ns period), the SCL high period is 20 ns. PPBAUD = 0001: SCL high period is two fclk periods. For example, if fclk is 50 MHz (20 ns period), the SCL high period is 40 ns. PPBAUD = 0010: SCL high period is three fclk periods. For example, if fclk is 50 MHz (20 ns period), the SCL high period is 60 ns. PPBAUD = 0011: SCL high period is four fclk periods. …. PPBAUD = 1111: SCL high period is sixteen fclk periods.	0x0	R/W
7	PERLOW	Reserved For Future Use.	0x0	R/W
6	ODSTOP	Open-Drain Speed For Stop: 0: The I3C _MS emits STOP at push-pull speed for I3C messages. 1: The I3C _MS emits STOP at open-drain speed for I3C messages	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[5:4]	HKEEP	High-Keeper Implementation. 00: No high-keeper support. SCL is actively driven in all states when the I3C_MS is the bus master. The PUR control for external pull-up of SDA is active (pin_pur_oena = 1) for both the open-drain and high-keeper states. 01: On chip high keeper support. The SCL and SDA pads have weak pull-ups controlled by the pin_hk_scl and pin_hk_sda signals from the I3C_MS. The PUR control for external SDA pull-up is active (pin_pur_oena = 1) for the open-drain state. 10: External high-keeper support for SDA, SCL is actively driven in all states when the I3C_MS is the bus master. It is expected that there is an external weak pull-up on SDA. For the high-keeper state, SDA from the I3C_MS is high-impedance (pin_sda_oena = 0) and the PUR control is inactive (pin_pur_oena = 0), so the external weak pull-up provides the high-keeper function. For the open-drain state, pin_sda_oena = 0 and the PUR control is active (pin_pur_oena = 1), so the external strong pull-up provides the open-drain pull-up function. 11: External high-keeper support for SCL and SDA. It is expected that there are external weak pull-ups on SCL and SDA. For the high-keeper state, the respective SCL/SDA output from the I3C_MS is high-impedance and the PUR control for SDA is inactive (pin_pur_oena = 0), so the external weak pull-up provides the respective high-keeper function. For the SDA open-drain state, pin_sda_oena = 0 and the PUR control is active (pin_pur_oena = 1), so the external strong pull-up provides the open-drain pull-up function.	0x0	R/W
3	DISTO	Disable Timeout Error. 0: Enable timeout error. 1: Disable timeout error.	0x0	R/W
2	RSRVD2_2	Reserved.	0x0	R
[1:0]	MSTENA	Master Device Enable. 00: Master Mode Off. 01: Master mode on. 10: Master mode capable. 11: Reserved.	0x0	R/W

SLAVE MODE CONFIGURATION REGISTER

Address: 0xF0013004, Reset: 0x00320000, Name: CONFIG

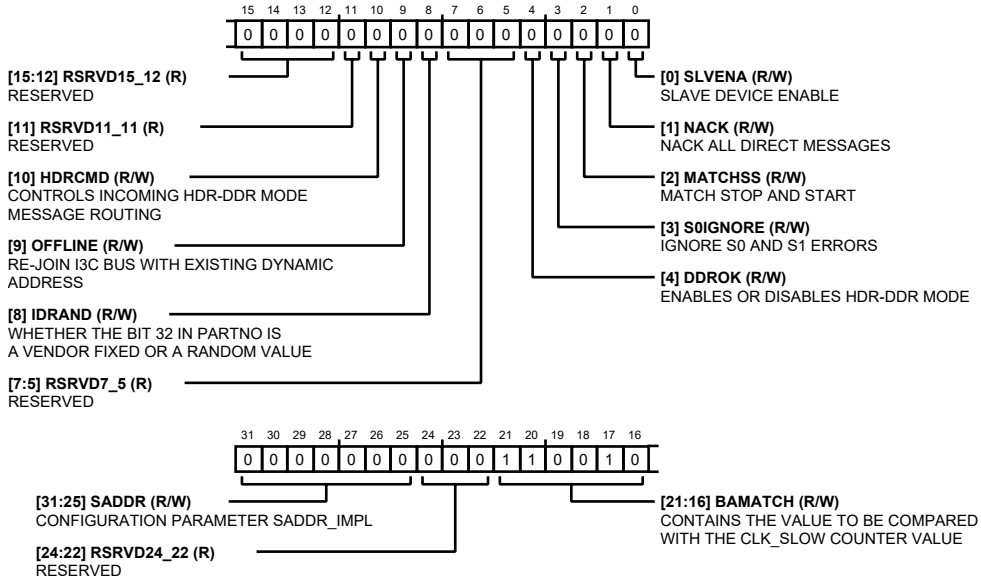


Table 425. Bit Descriptions for CONFIG

Bits	Bit Name	Description	Reset	Access
[31:25]	SADDR	Configuration Parameter SADDR_IMPL. When configuration parameter SADDR_IMPL = 3: SADDR contains the 7-bit I2C-style static address written by the application. When configuration parameter SADDR_IMPL = 0, 1, or 2: SADDR field is not used.	0x0	R/W
[24:22]	RSRVD24_22	Reserved.	0x0	R
[21:16]	BAMATCH	Contains The Value To Be Compared With The Clk_Slow Counter Value. When configuration parameter WITH_BAMATCH = 1: BAMASTCH contains the value to be compared with the clk_slow counter value to determine when the 1- s Bus Available time has elapsed for event generation. The width of the BAMATCH field is equal to the value of configuration parameter CLOCK_SLOW_BITS. If CLOCK_SLOW_BITS < 8, the upper unused bits of BAMATCH are read as 0 and should be written with 0. The reset value of BAMATCH is the value of configuration parameter CLOCK_SLOW_MATCH. When configuration parameter WITH_BAMATCH = 0: The BAMATCH field is not used.	0x32	R/W
[15:12]	RSRVD15_12	Reserved.	0x0	R
11	RSRVD11_11	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
10	HDRCMD	Controls Incoming Hdr-Ddr Mode Message Routing.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		When configuration parameter WITH_HDRCMD = 1: HDRCMD controls whether the command byte of an incoming HDR-DDR mode message is sent to the application through the HDRCMD register or through the receive buffer/FIFO: 0 = Command byte of incoming HDR-DDR mode message is written to the receive buffer/FIFO. 1 = Command byte of incoming HDR-DDR mode message is written to the HDRCMD register.		
		When configuration parameter WITH_HDRCMD = 0: The HDRCMD bit is not used.		
9	OFFLINE	Re-Join I3c Bus With Existing Dynamic Address. When re-enabling the I3C_MS on an I3C bus on which the I3C_MS has already been assigned an I3C dynamic address, set OFFLINE simultaneously with CONFIG.SLVENA. When the OFFLINE bit is set with SLVENA, the I3C_MS waits for either an HDR Exit Pattern or 60 s of I3C bus inactivity, then re-joins the I3C bus using the dynamic address stored in DYNADDR.	0x0	R/W
8	IDRAND	Whether The Bit 32 In Partno Is A Vendor Fixed Or A Random Value. When configuration parameter ID_IMPL = 2 or 3: IDRAND contains the value for bit 32 of the 48-bit Provisional ID, indicating whether the value in the PARTNO register is a Vendor Fixed Value or Random Value: 0 = Vendor Fixed Value 1= Random Value When configuration parameter ID_IMPL = 0 or 1: The IDRAND bit is not used.	0x0	R/W
[7:5]	RSRVD7_5	Reserved.	0x0	R
4	DDROK	Enables Or Disables Hdr-Ddr Mode. When configuration parameter WITH_DDR = 1: DDROK enables or disabled HDR-DDR mode by controlling the BCR[5] value that the I3C_MS provides to the I3C bus master: 1 = Enable HDR-DDR mode (BCR[5] = 1). 0 = Disable HDR-DDR mode (BCR[5] = 0). When configuration parameter WITH_DDR = 0: The DDROK bit is not used.	0x0	R/W
3	S0IGNORE	Ignore S0 And S1 Errors. When S0IGNORE = 0, and the I3C_MS detects an S0 or S1 error, the I3C_MS ignores further I3C bus activity until it detects the HDR Exit Pattern. When the I3C_MS is used on a bus on which there are no HDR commands, S0IGNORE can be set to 1 to avoid the possibility of detecting an S0 or S1 error and going to a locked state waiting for the HDR Exit Pattern. 0 = Detect S0 And S1 Errors. 1 = Ignore S0 And S1 Errors.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	MATCHSS	Match Stop and Start. 0: Set STATUS.STOP and STATUS.START when the respective conditions occur regardless of the state of STATUS.MATCHED. 1: Set STATUS.STOP and STATUS.START only when STATUS.MATCHED is set.	0x0	R/W
1	NACK	Nack All Direct Messages. The NACK bit should only be updated when the I3C bus is in the stopped state. 0: Process incoming messages normally. 1: NACK all incoming direct messages, including messages that match the assigned dynamic address or static address, and direct CCCs that match the assigned dynamic address. In addition, the I3C_MS ignores incoming unhandled CCCs instead of sending them to the application.	0x0	R/W
0	SLVENA	Slave Device Enable. Set up the required configuration registers such as CONFIG and (if used) PARTNO and IDEXT before setting the SLVENA bit. When requesting a Hot-Join event, write the Hot-Join request to the CTRL register before setting SLVENA. 0: Disable 1: Enable	0x0	R/W

SLAVE MODE STATUS REGISTER

Address: 0xF0013008, Reset: 0x00001000, Name: STATUS

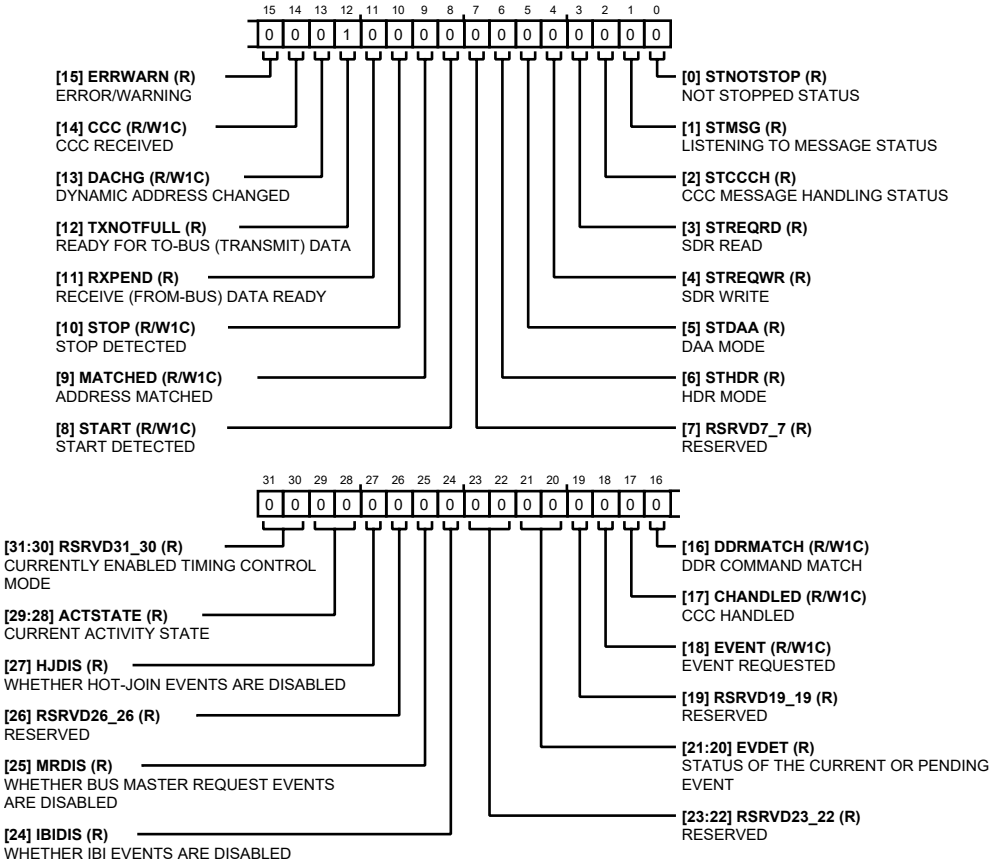


Table 426. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
[31:30]	RSRVD31_30	Currently Enabled Timing Control Mode. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
[29:28]	ACTSTATE	Current Activity State.	0x0	R
		When configuration parameter WITH_BASIC_CCC = 0 the ACTSTATE field is not used.		
		When configuration parameter WITH_BASIC_CCC = 1, ACTSTATE holds the current activity state, as set by most recent ENTASn CCC from the I3C bus master: 00: No Latency; normal bus operation. 01: 1ms latency. 10: 100ms latency. 11: 10s latency.		
27	HJDIS	Indicates whether Hot-Join Events Are Disabled. When configuration parameter WITH_BASIC_CCC = 0, the HJDIS bit is not used. When configuration parameter WITH_BASIC_CCC = 1 0: Indicates Hot-Join events are disabled	0x0	R

Bits	Bit Name	Description	Reset	Access
		1: Indicates Hot-Join events are disabled by I3C bus master through a DISEC CCC		
26	RSRVD26_26	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
25	MRDIS	Indicates whether Bus Master Request Events Are Disabled. When configuration parameter WITH_BASIC_CCC = 0, the MRDIS bit is not used. When configuration parameter WITH_BASIC_CCC = 1: 0: Indicates Bus master events are enabled 1: Indicates Bus master events been disabled by the I3C bus master through a DISEC CCC.	0x0	R
24	IBIDIS	Indicates whether Ibi Events Are Disabled. When configuration parameter WITH_BASIC_CCC = 0, the IBIDIS bit is not used. When configuration parameter WITH_BASIC_CCC = 1: 0: IBI events are enabled. 1: IBI events have been disabled by the I3C bus master through a DISEC CCC.	0x0	R
[23:22]	RSRVD23_22	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
[21:20]	EVDET	Status Of the Current Or Pending Event. 00: None 01: Request not yet sent. Either no START has occurred or the I3C_MS is waiting for Bus Available or Bus Idle. 10: Request was sent and NACKed and will be tried again. 11: Request was sent and ACKed.	0x0	R
19	RSRVD19_19	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
18	EVENT	Event Requested. 0: The I3C_MS has not requested an IBI, Hot-Join or bus mastership since the EVENT bit was last cleared. 1: The I3C_MS requested an IBI, Hot-Join or bus mastership.	0x0	R/W1C
17	CHANDLED	Ccc Handled. 0: The I3C_MS has not handled a CCC since the the CHANDLED bit was last cleared. 1: The I3C_MS handled a CCC.	0x0	R/W1C
16	DDRMATCH	Ddr Command Match. 0: I3C_MS has not received an HDR-DDR command that matched this device's I3C dynamic address since the DDRMATCH bit was last cleared	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: An HDR-DDR command matched this device's I3C dynamic address. Depending on configuration parameter WITH_HDRCMD and the value of CONFIG.HDRCMD, the command byte of the incoming HDR-DDR is available in either the HDRCMD register or in the receive buffer/FIFO. When the command byte is written to the receive buffer/FIFO, the RXPEND bit is also set. The MSb of the command byte indicates if the command is a read or a write. If the command is a read, and there are to-bus bytes available to be sent, the I3C_MS ACKs the command and sends the data. If there is no to-bus data available, the I3C_MS NACKs the command.		
15	ERRWARN	Error/Warning. 0: No error or warning is active in the ERRWARN register. 1: An error or warning has occurred. The ERRWARN register indicates the active error or warning. To clear the STATUS.ERRWARN bit, write 1 to the required bit(s) in the ERRWARN register.	0x0	R
14	CCC	Ccc Received. 0: The I3C_MS has not received a CCC that it does not automatically handle since the CCC bit was last cleared. 1: The I3C_MS has not received a CCC that it does not automatically handle	0x0	R/W1C
13	DACHG	Dynamic Address Changed. 0: The device's I3C dynamic address has not changed since the DACHG bit was last cleared. 1: The device's I3C dynamic address changed, due to dynamic address being assigned, re-assigned, or reset	0x0	R/W1C
12	TXNOTFULL	Ready For To-Bus (Transmit) Data. 0: The I3C_MS to-bus buffer cannot accept another byte of data. 1: The I3C_MS to-bus buffer can accept another byte of data.	0x1	R
11	RXPEND	Receive (From-Bus) Data Ready. 0: No receive data is available. 1: Receive data is available.	0x0	R
10	STOP	Stop Detected: 0: The I3C _MS has not detected a STOP state since the STOP bit was last cleared. 1: The I3C _MS has detected a STOP on the I3C or I2C bus since the STOP bit was last cleared.	0x0	R/W1C
9	MATCHED	Address Matched. 0: No incoming header matched this device's I3C dynamic address or I2C statis address since the MATCHED bit was last cleared. 1: An incoming header matched this device's I3C dynamic address or I2C statis address.	0x0	R/W1C
8	START	Start Detected.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		0: The I3C_MS has not detected a START or repeated START condition the I3C or I2C bus. 1: The I3C_MS has not detected a START or repeated START condition since the START bit was last cleared.		
7	RSRVD7_7	Reserved.	0x0	R
6	STHDR	HDR Mode. 0: The I3C bus is not in HDR mode. 1: The I3C bus is in HDR mode.	0x0	R
5	STDAA	DAA Mode. 0: The I3C bus is not in DAA mode. 1: The I3C bus is in DAA mode.	0x0	R
4	STREQWR	SDR Write. 0: The current bus request is not an SDR mode write. 1: The current bus request is an SDR mode write to this slave device or to all I3C bus slaves and the bus is not in DAA mode.	0x0	R
3	STREQRD	SDR Read. 0: The current bus request is not an SDR mode read to this slave device or an IBI is not being sent. 1: The current bus request is an SDR mode read to this slave device or an IBI is being sent.	0x0	R
2	STCCCH	CCC Message Handling Status. 0: The I3C-MS is not handling a CCC message. 1: The I3C-MS is handling a CCC message.	0x0	R
1	STMSG	Listening To Message Status. 0: The I3C-MS is not listening to bus traffic or responding. 1: The I3C-MS is listening to bus traffic or responding.	0x0	R
0	STNOTSTOP	Not Stopped Status. 0: The I3C or I2C bus is in a STOP condition. 1: The I3C or I2C bus is busy or the I3C_MS has detected an I3C S0 or S1 error and is waiting for an HDR Exit Pattern.	0x0	R

SLAVE MODE I3C CONTROL REGISTER

Address: 0xF001300C, Reset: 0x00000000, Name: CTRL

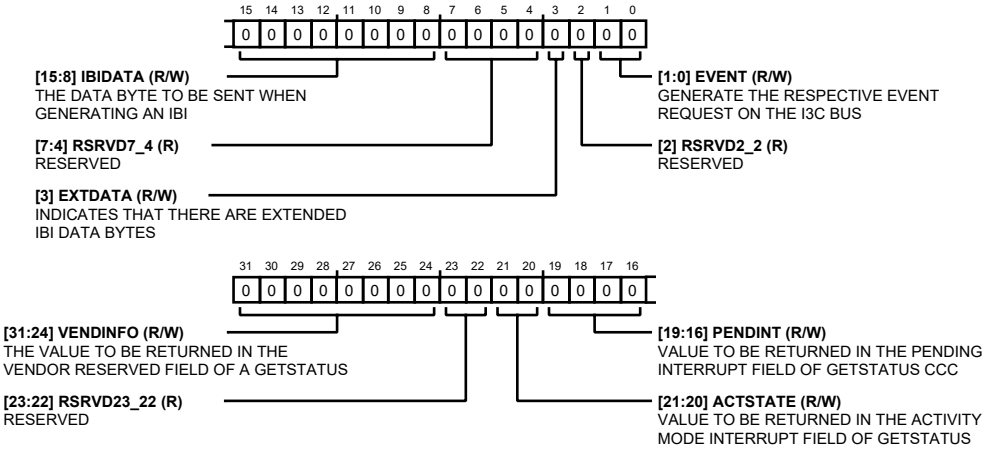


Table 427. Bit Descriptions for CTRL

Bits	Bit Name	Description	Reset	Access
[31:24]	VENDINFO	The Value to Be Returned In The Vendor Reserved Field Of A Getstatus. When configuration parameter WITH_STAT_VENDOR = 0: The VENDINFO field is not implemented. When configuration parameter WITH_STAT_VENDOR = 1: VENDINFO contains the value to be returned in the Vendor Reserved field of a GETSTATUS CCC.	0x0	R/W
[23:22]	RSRVD23_22	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
[21:20]	ACTSTATE	Value To Be Returned in The Activity Mode Interrupt Field Of Getstatus. When configuration parameter WITH_STAT_INFO = 0: The ACTSTATE field is not implemented. When configuration parameter WITH_STAT_INFO = 1: ACTSTATE contains the value to be returned in the Activity Mode field of a GETSTATUS CCC.	0x0	R/W
[19:16]	PENDINT	Value To Be Returned In The Pending Interrupt Field Of Getstatus Ccc. When configuration parameter WITH_STAT_INFO = 0: PENDINT field is not implemented. When configuration parameter WITH_STAT_INFO = 1: PENDINT contains the value to be returned in the Pending Interrupt field of a GETSTATUS CCC.	0x0	R/W
[15:8]	IBIDATA	The Data Byte to Be Sent When Generating An IBI. When configuration parameter IBI_IMPL = 0 or 1: IBIDATA field is not implemented. When configuration parameter IBI_IMPL = 2: IBIDATA contains the data byte to be sent when generating an IBI.	0x0	R/W
[7:4]	RSRVD7_4	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
3	EXTDATA	Indicates That There Are Extended Ibi Data Bytes. When configuration parameter IBI_IMPL = 0 or 1: EXTDATA field is not implemented. When configuration parameter IBI_IMPL = 2: EXTDATA= 0 indicates that there is no additional data to be sent when generating an IBI other than the mandatory byte and any timing control bytes. EXTDATA= 1 indicates that there are extended IBI data bytes data to be sent when generating an IBI, in addition to the one mandatory byte. After sending the IBI mandatory byte, the I3C_MS transmits additional extended IBI data bytes from either the transmit buffer/FIFO or the IBIEXT1/IBIEXT2 registers. If timing control bytes are sent with the IBI, the extended IBI data bytes are transmitted after the timing control bytes.	0x0	R/W
2	RSRVD2_2	Reserved.	0x0	R
[1:0]	EVENT	Generate The Respective Event Request On The I3c Bus. 00: Normal Mode- If event is set to 00 after being set to a non-zero value, the event request generated by the non-zero value is canceled 01: IBI- Generate an IBI on the I3C bus. If the I3C_MS is configured to supply a payload data byte with the IBI (configuration parameter IBI_IMPL = 2), the I3C_MS uses CTRL.IBIDATA as the payload data byte. If Timing Control Asynchronous Mode 0 is enabled, the IBI includes timing control related bytes and bit 7 of the IBIDATA byte is automatically set to 1. If CTRL.EXTDATA = 1, the I3C_MS sends extended IBI data bytes after the mandatory data byte and any timing control related bytes. 10: Master request- Request mastership of the I3C bus. 11: Hot-Join- Generate a Hot-Join request.	0x0	R/W

SLAVE MODE INTERRUPT ENABLE SET REGISTER

Address: 0xF0013010, Reset: 0x00000000, Name: INTSET

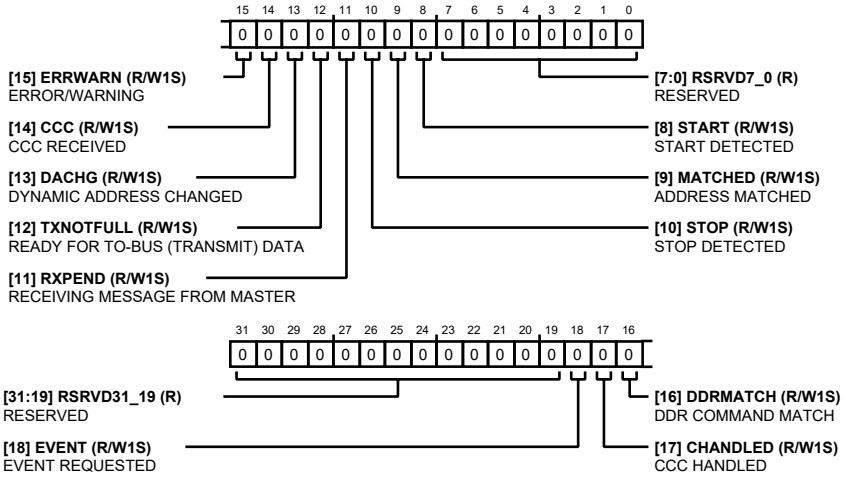


Table 428. Bit Descriptions for INTSET

Bits	Bit Name	Description	Reset	Access
[31:19]	RSRVD31_19	Reserved.	0x0	R
18	EVENT	Event Requested. 0: Event Request interrupt disabled. 1: Event Request interrupt enabled	0x0	R/W1S
17	CHANDLED	CCC Handled. 0: CCC Handled interrupt disabled. 1: CCC Handled interrupt enabled	0x0	R/W1S
16	DDRMATCH	DDR Command Match. 0: DDR Command Match interrupt disabled. 1: DDR Command Match interrupt enabled	0x0	R/W1S
15	ERRWARN	Error/Warning. 0: Error/Warning interrupt disabled. 1: Error/Warning interrupt enabled.	0x0	R/W1S
14	CCC	CCC Received. 0: CCC Received interrupt disabled. 1: CCC Received interrupt enabled.	0x0	R/W1S
13	DACHG	Dynamic Address Changed. 0: Dynamic Address Changed interrupt disabled. 1: Dynamic Address Changed interrupt enabled.	0x0	R/W1S
12	TXNOTFULL	Ready For To-Bus (Transmit) Data. 0: Ready for To-Bus data interrupt disabled. 1: Ready for To-Bus data interrupt enabled.	0x0	R/W1S
11	RXPEND	Receiving Message from Master. 0: Receiving Message from Master interrupt disabled. 1: Receiving Message from Master interrupt enabled.	0x0	R/W1S
10	STOP	Stop Detected. 0: Stop Detected interrupt disabled. 1: Stop Detected interrupt enabled.	0x0	R/W1S
9	MATCHED	Address Matched. 0: Address Matched interrupt disabled. 1: Address Matched interrupt enabled.	0x0	R/W1S
8	START	Start Detected. 0: Start Detected interrupt disabled. 1: Start Detected interrupt enabled.	0x0	R/W1S
[7:0]	RSRVD7_0	Reserved. Reserved.	0x0	R

SLAVE MODE INTERRUPT ENABLE CLEAR REGISTER

Address: 0xF0013014, Reset: 0x00000000, Name: INTCLR

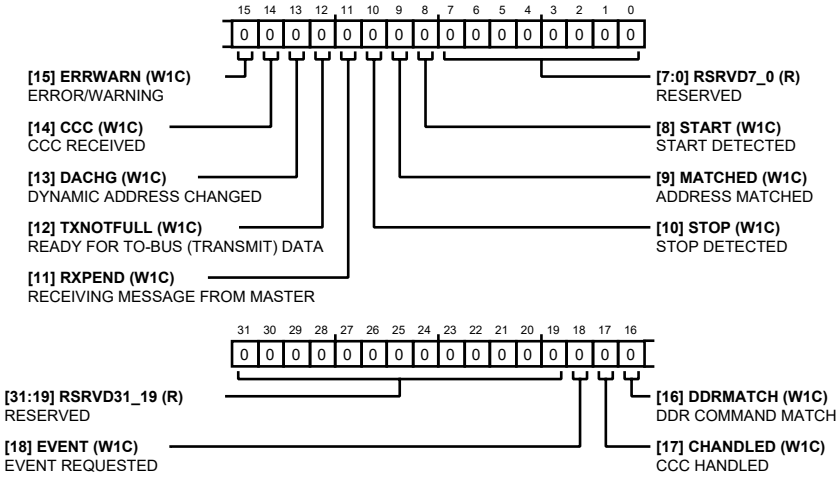


Table 429. Bit Descriptions for INTCLR

Bits	Bit Name	Description	Reset	Access
[31:19]	RSRVD31_19	Reserved.	0x0	R
18	EVENT	Event Requested. 0: No effect 1: Disable event request interrupt	0x0	W1C
17	CHANDLED	CCC Handled. 0: No effect 1: Disable CCC handled interrupt	0x0	W1C
16	DDRMATCH	DDR Command Match. 0: No effect 1: Disable DDR command match interrupt.	0x0	W1C
15	ERRWARN	Error/Warning. 0: No effect 1: Disable error/warning interrupt.	0x0	W1C
14	CCC	CCC Received. 0: No effect 1: Disable CCC received interrupt.	0x0	W1C
13	DACHG	Dynamic Address Changed. 0: No effect 1: Disable dynamic address change interrupt.	0x0	W1C
12	TXNOTFULL	Ready For To-Bus (Transmit) Data. 0: No effect 1: Disable ready for to-bus data interrupt.	0x0	W1C
11	RXPEND	Receiving Message from Master. 0: No effect 1: Disable receiving message from master interrupt.	0x0	W1C
10	STOP	Stop Detected.	0x0	W1C

Bits	Bit Name	Description	Reset	Access
		0: No effect 1: Disable STOP detected interrupt.		
9	MATCHED	Address Matched. 0: No effect 1: Disable address matched interrupt.	0x0	W1C
8	START	Start Detected. 0: No effect 1: Disable START detected interrupt.	0x0	W1C
[7:0]	RSRVD7_0	Reserved.	0x0	R

INTERRUPT MASKED REGISTER

Address: 0xF0013018, Reset: 0x00000000, Name: INTMASKED

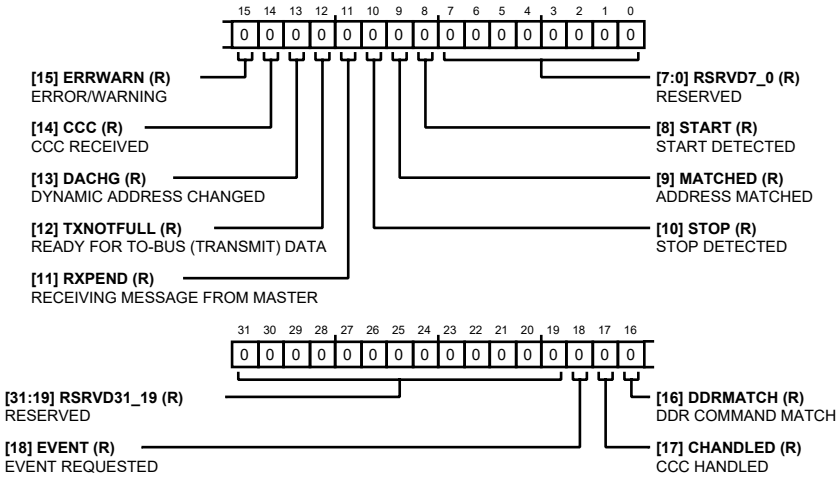


Table 430. Bit Descriptions for INTMASKED

Bits	Bit Name	Description	Reset	Access
[31:19]	RSRVD31_19	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
18	EVENT	Event Requested. 0: The I3C_MS has not requested an IBI, Hot-Join or bus mastership and the EVENT interrupt source is enabled in the INTSET register. 1: The I3C_MS has requested an IBI, Hot-Join or bus mastership and the EVENT interrupt source is enabled in the INTSET register.	0x0	R
17	CHANDLED	CCC Handled. 0: The I3C_MS has not handled a CCC and the CHANDLED interrupt source is disabled 1: The I3C_MS handled a CCC and the CHANDLED interrupt source is enabled in the INTSET register	0x0	R
16	DDRMATCH	DDR Command Match.	0x0	R

Bits	Bit Name	Description	Reset	Access
		0: I3C_MS did not receive an HDR-DDR command that matched this device's dynamic address or the DDRMATCH interrupt source is disabled. 1: An HDR-DDR command matched this device's dynamic address and the DDRMATCH interrupt source is enabled in the INTSET register.		
15	ERRWARN	Error/Warning. 0: No error or warning is active in the ERRWARN register or the ERRWARN interrupt source is disabled. 1: An error or warning has occurred and the ERRWARN interrupt source is enabled in the INTSET register. The ERRWARN register indicates the active error or warning. To clear the STATUS.ERRWARN bit, write 1 to the required bit(s) in the ERRWARN register.	0x0	R
14	CCC	CCC Received. 0: The I3C_MS has not received a CCC that it does not automatically handle and the CCC interrupt source is enabled in the INTSET register. 1: The I3C_MS has received a CCC that it does not automatically handle and the CCC interrupt source is enabled in the INTSET register.	0x0	R
13	DACHG	Dynamic Address Changed. 0: The device's I3C dynamic address has not changed since the DACHG bit was last cleared. 1: The device's I3C dynamic address changed, due to the dynamic address being assigned, re-assigned, or reset.	0x0	R
12	TXNOTFULL	Ready For To-Bus (Transmit) Data. 0: The I3C_MS to-bus buffer cannot accept another byte of data or the TXTNOFULL interrupt source is disabled 1: The I3C_MS to-bus buffer can accept another byte of data the TXTNOFULL interrupt source is enabled in the INTSET register.	0x0	R
11	RXPEND	Receiving Message From Master. 0: The I3C_MS is not receiving a message or the received message is a CCC that the I3C_MS is handling automatically or the RXPEND interrupt source is disabled. 1: The I3C_MS is receiving a message that is not a CCC that the I3C_MS is handling automatically and the RXPEND interrupt source is enabled in the INTSET register.	0x0	R
10	STOP	Stop Detected. 0: The I3C_MS has not detected a STOP state or the STOP interrupt source is disabled. 1: The I3C_MS has detected a STOP state on the I3C or I2C bus and the STOP interrupt source is enabled in the INTSET register.	0x0	R

Bits	Bit Name	Description	Reset	Access
9	MATCHED	Address Matched. 0: No incoming header has matched this device's I3C dynamic address or I2C static address or the MATCHED interrupt source is disabled. 1: An incoming header has matched this device's I3C dynamic address or I2C static address and the MATCHED interrupt source is enabled in the INTSET register.	0x0	R
8	START	Start Detected. 0: The I3C_MS has not detected a START or repeated START condition or the START interrupt source is disabled. 1: The I3C_MS has detected a START or repeated START condition or the START interrupt source is enabled in the INTSET register.	0x0	R
[7:0]	RSRVD7_0	Reserved.	0x0	R

ERROR AND WARNING REGISTER

Address: 0xF001301C, Reset: 0x00000000, Name: ERRWARN

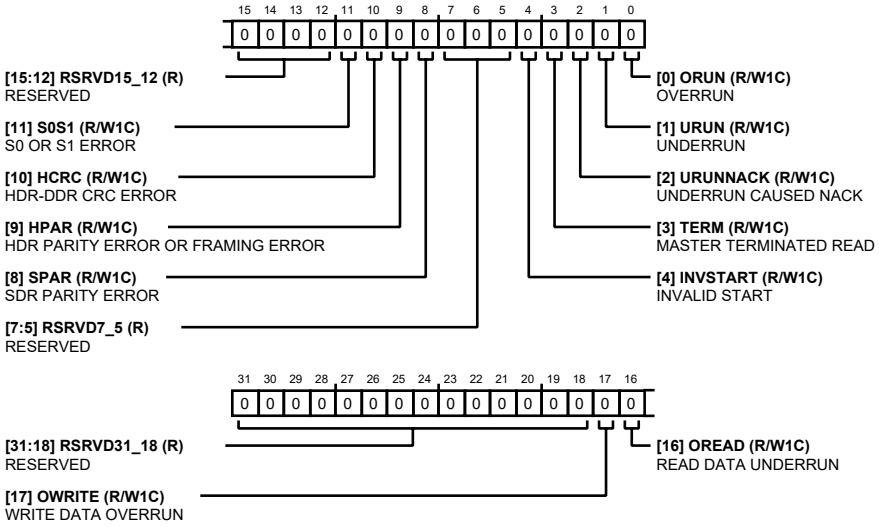


Table 431. Bit Descriptions for ERRWARN

Bits	Bit Name	Description	Reset	Access
[31:18]	RSRVD31_18	Reserved.	0x0	R
17	OWRITE	Write Data Overrun. 0: The WDATAB(E) or WDATAH(E) register was not written to when full. 1: The WDATAB(E) or WDATAH(E) register was written to when full.	0x0	R/W1C
16	OREAD	Read Data Underrun. 0: The RDATAB or RDATAH register was not read when empty. 1: The RDATAB or RDATAH register was not read when empty.	0x0	R/W1C
[15:12]	RSRVD15_12	Reserved.	0x0	R
11	S0S1	S0 Or S1 Error. 0: An SO or S1 error has not occurred.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: An SO or S1 error has occurred and the I3C_MS is locked waiting for an HDR Exit Pattern. Note: When S0S1 = 1 and the I3C_MS is locked waiting for an HDR Exit Pattern, writing 1 to S0S1 releases the lock. The I3C_MS then waits for a START (or repeated START) or STOP and returns to normal operation. However, writing 1 to release the lock should only be done in controlled circumstances, such as testing. In normal operation, the I3C_MS releases the lock after detecting the HDR Exit Pattern on the I3C bus.		
10	HCRC	Hdr-Ddr Crc Error. 0: No CRC error was detected in an HDR-DDR message from the I3C master. 1: A CRC error was detected in an HDR-DDR message from the I3C master.	0x0	R/W1C
9	HPAR	Hdr Parity Error Or Framing Error. 0: No parity error or framing was detected in an HDR message from the I3C bus master 1: A parity error or framing was detected in an HDR message from the I3C bus master.	0x0	R/W1C
8	SPAR	Sdr Parity Error. 0: No parity error was detected or read timeout occurred in an SDR message from the I3C master. 1: A parity error was detected in an SDR message from the I3C master or a read timeout occurred in an SDR read message. A read timeout occurs when the I3C_MS is configured to support IBIs, Hot-Join requests, and/or master requests (i3c_slow_counters block is implemented), and the I3C master stalls a read message for 100 s or longer). Note: When SPAR is set to 1, the Protocol Error sticky bit for the GETSTATUS CCC is also set to 1. The Protocol Error sticky bit is cleared when read in response to a GETSTATUS CCC.	0x0	R/W1C
[7:5]	RSRVD7_5	Reserved.	0x0	R
4	INVSTART	Invalid Start. 0: An invalid START condition did not occur. 1: An invalid START condition occurred. (SCL line went from high to low when the SDA line was high in a STOP condition.)	0x0	R/W1C
3	TERM	Master Terminated Read. 0: The I3C bus master did not terminate a read before the slave sent End-of-Data. 1: The I3C bus master terminated a read before the slave sent End-of-Data.	0x0	R/W1C
2	URUNNACK	Underrun Caused NACK. 0: No NACK occurred due to to-bus underrun. 1: The internal to-bus buffer or FIFO was underrun when receiving the address header for a read, so the I3C_MS NACKed the address header.	0x0	R/W1C
1	URUN	Underrun. 0: The internal to-bus buffer or FIFO was not underrun when sending read data.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: The internal to-bus buffer or FIFO was underrun when sending read data because the application did not supply data fast enough.		
0	ORUN	Overrun. 0: The internal from-bus buffer or FIFO was not overrun. 1: The internal from-bus buffer or FIFO was overrun because the application did not drain data fast enough.	0x0	R/W1C

DATA CONTROL REGISTER

Address: 0xF001302C, Reset: 0x80000030, Name: DATACTRL

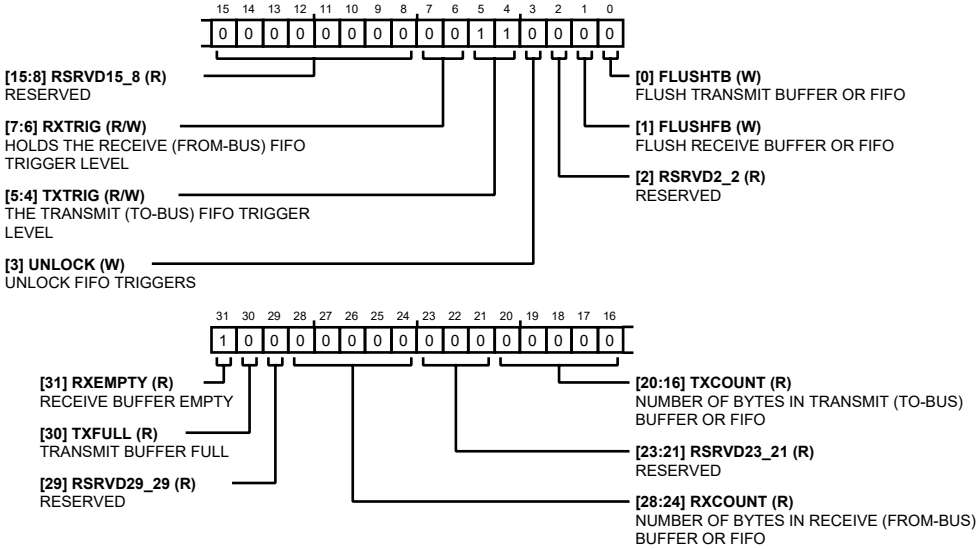


Table 432. Bit Descriptions for DATACTRL

Bits	Bit Name	Description	Reset	Access
31	RXEMPTY	Receive Buffer Empty. 0: The receive (from-bus) buffer or FIFO is not empty. 1: The receive (from-bus) buffer or FIFO is empty.	0x1	R
30	TXFULL	Transmit Buffer Full. 0: The transmit (to-bus) buffer or FIFO is not empty. 1: The transmit (to-bus) buffer or FIFO is empty.	0x0	R
29	RSRVD29_29	Reserved.	0x0	R
[28:24]	RXCOUNT	Number Of Bytes In Receive (from-bus) Buffer Or FIFO.	0x0	R
[23:21]	RSRVD23_21	Reserved.	0x0	R
[20:16]	TXCOUNT	Number Of Bytes In Transmit (to-bus) Buffer Or FIFO.	0x0	R
[15:8]	RSRVD15_8	Reserved.	0x0	R
[7:6]	RXTRIG	When configuration parameter FIFO_IMPL = 1 (internal FIFOs), RXTRIG holds the receive (from-bus) FIFO trigger level: 00: Trigger when not empty. 01: Trigger when 1/4 full or more. 10: Trigger when 1/2 full or more.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		11: Trigger when 3/4 full or more. When the receive FIFO fullness reaches the trigger level, the I3C_MS generates an interrupt (if configured and enabled). When configuration parameter FIFO_IMPL = 0, RXTRIG controls the trigger level for the receive (from-bus) ping-pong buffer: 00,01,10: Trigger when not empty (1 or more bytes are available in the receive buffer). 11: Trigger when there are 2 bytes in the receive buffer (so half-word read can be used). Note: RXTRIG can only be written when bit 3 (UNLOCK) is also written as 1 in the same write operation.		
[5:4]	TXTRIG	When configuration parameter FIFO_IMPL = 1 (internal FIFOs), TXTRIG holds the transmit (to-bus) FIFO trigger level: 00: Trigger when empty. 01: Trigger when 1/4 full or less. 10: Trigger when 1/2 full or less. 11: Trigger when 3/4 full or less. When the transmit FIFO emptiness reaches the trigger level, the I3C_MS generates an interrupt (if configured and enabled). When configuration parameter FIFO_IMPL = 0, TXTRIG controls the trigger level for the transmit (to-bus) ping-pong buffer: 01,10,11: Trigger when not full (1 or more bytes are available in the transmit buffer). 00: Trigger when the transmit buffer is empty (so half-word write can be used).	0x3	R/W
3	UNLOCK	Unlock FIFO Triggers. 0: Disable writing to bits [7:4] in the current write cycle. 1: Enable writing to bits [7:4] in the current write cycle.	0x0	W
2	RSRVD2_2	Reserved.	0x0	R
1	FLUSHFB	Flush Receive Buffer Or FIFO. 0: Do not flush the receive (from-bus) buffer or FIFO. 1: Flush the receive (from-bus) buffer or FIFO.	0x0	W
0	FLUSHTB	Flush Transmit Buffer Or FIFO. 0: Do not Flush the transmit (to-bus) buffer or FIFO. 1: Flush the transmit (to-bus) buffer or FIFO.	0x0	W

WRITE BYTE DATA REGISTER

Address: 0xF0013030, Reset: 0x00000000, Name: WDATAB

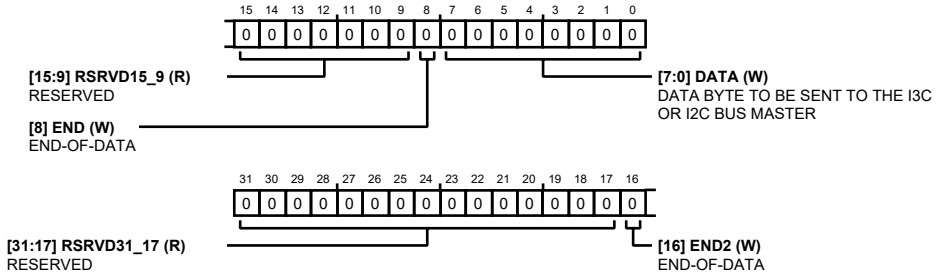


Table 433. Bit Descriptions for WDATAB

Bits	Bit Name	Description	Reset	Access
[31:17]	RSRVD31_17	Reserved.	0x0	R
16	END2	End-Of-Data. 0: The byte in the DATA field is not the last data byre of the message. 1: The byte in the DATA field is the last data byre of the message. Note: Either bit [16] or bit [8] (or both) can be set to indicate end-of-data. Note: For I3C, setting END for the last data byte of the message is required. For I2C, setting END for the last data byte of the message is optional.	0x0	W
[15:9]	RSRVD15_9	Reserved.	0x0	R
8	END	End-Of-Data. 0: The byte in the DATA field is not the last data byre of the message. 1: The byte in the DATA field is the last data byre of the message. Note: Either bit [16] or bit [8] (or both) can be set to indicate end-of-data. Note: For I3C, setting END for the last data byte of the message is required. For I2C, setting END for the last data byte of the message is optional.	0x0	W
[7:0]	DATA	Data Byte to Be Sent to The I3C Or I2C Bus Master.	0x0	W

WRITE BYTE DATA AS END REGISTER

Address: 0xF0013034, Reset: 0x00000000, Name: WDATABE

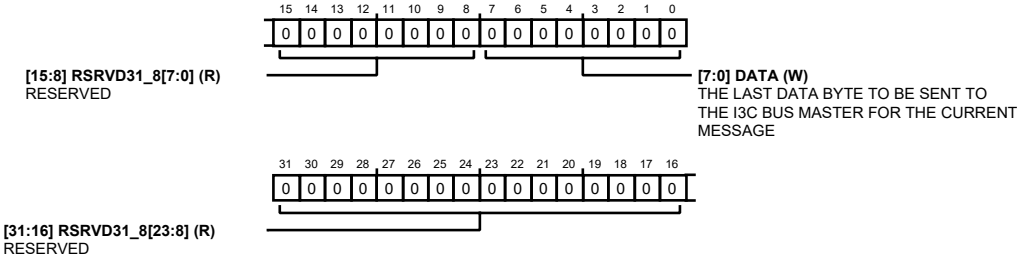


Table 434. Bit Descriptions for WDATABE

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:0]	DATA	The last data byte to be sent to the i3c bus master for the current message.	0x0	W

WRITE HALF-WORD DATA REGISTER

Address: 0xF0013038, Reset: 0x00000000, Name: WDATAH

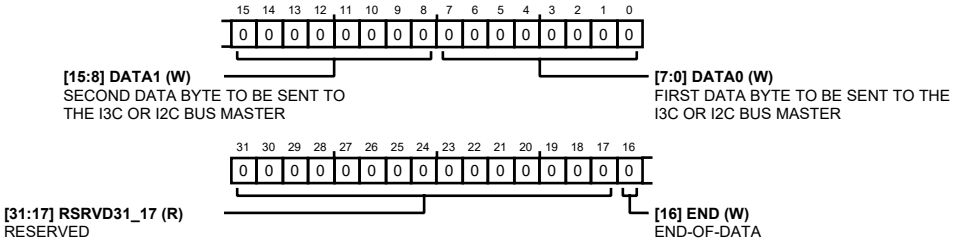


Table 435. Bit Descriptions for WDATAH

Bits	Bit Name	Description	Reset	Access
[31:17]	RSRVD31_17	Reserved. Reserved. The Read Value Is 0. Writes Have No Effect. Use 0 For Writes.	0x0	R
16	END	End-Of-Data. 0: The byte in the DATA field is not the last data byre of the message. 1: The byte in the DATA field is the last data byre of the message.	0x0	W
[15:8]	DATA1	Second Data Byte To Be Sent To The I3c Or I2c Bus Master.	0x0	W
[7:0]	DATA0	First Data Byte To Be Sent To The I3c Or I2c Bus Master.	0x0	W

WRITE HALF-WORD DATA AS END REGISTER

Address: 0xF001303C, Reset: 0x00000000, Name: WDATAHE

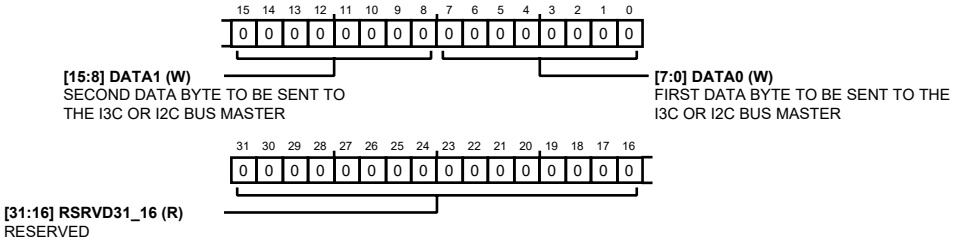


Table 436. Bit Descriptions for WDATAHE

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved	0x0	R
[15:8]	DATA1	Second Data Byte To Be Sent To The I3c Or I2c Bus Master. The I3C_AS sets the End-of-Data bit when transmitting DATA1 on the I3C bus	0x0	W
[7:0]	DATA0	First Data Byte To Be Sent To The I3c Or I2c Bus Master.	0x0	W

READ BYTE DATA REGISTER

Address: 0xF0013040, Reset: 0x00000000, Name: RDATAB

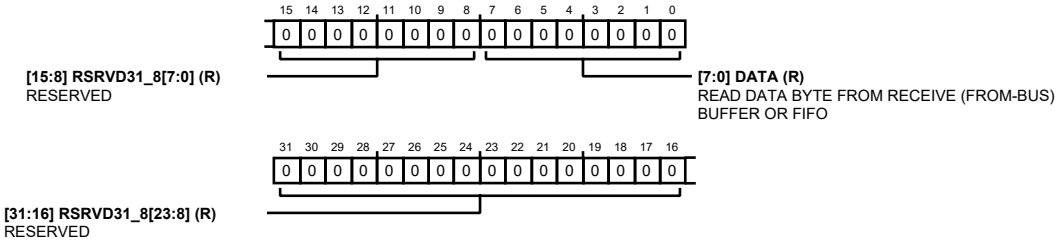


Table 437. Bit Descriptions for RDATAB

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:0]	DATA	Read data byte from receive (from-bus) buffer or FIFO.	0x0	R

READ HALF-WORD DATA REGISTER

Address: 0xF0013048, Reset: 0x00000000, Name: RDATAH

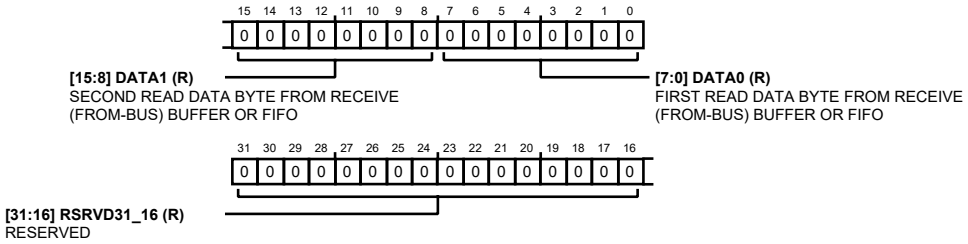


Table 438. Bit Descriptions for RDATAH

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved.	0x0	R
[15:8]	DATA1	Second Read Data Byte from Receive (From-Bus) Buffer Or FIFO.	0x0	R
[7:0]	DATA0	First Read Data Byte from Receive (From-Bus) Buffer Or FIFO.	0x0	R

BYTE-ONLY WRITE BYTE DATA REGISTER

Address: 0xF0013054, Reset: 0x00000000, Name: WDATAB1

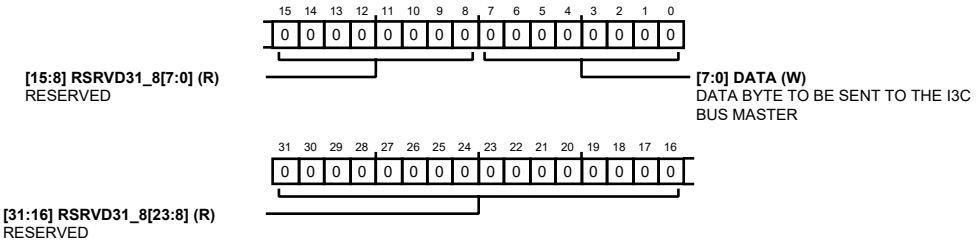


Table 439. Bit Descriptions for WDATAB1

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:0]	DATA	Data Byte to Be Sent to The I3C Bus Master.	0x0	W

CAPABILITIES REGISTER

Address: 0xF0013060, Reset: 0x7C1FFE78, Name: CAPABILITIES

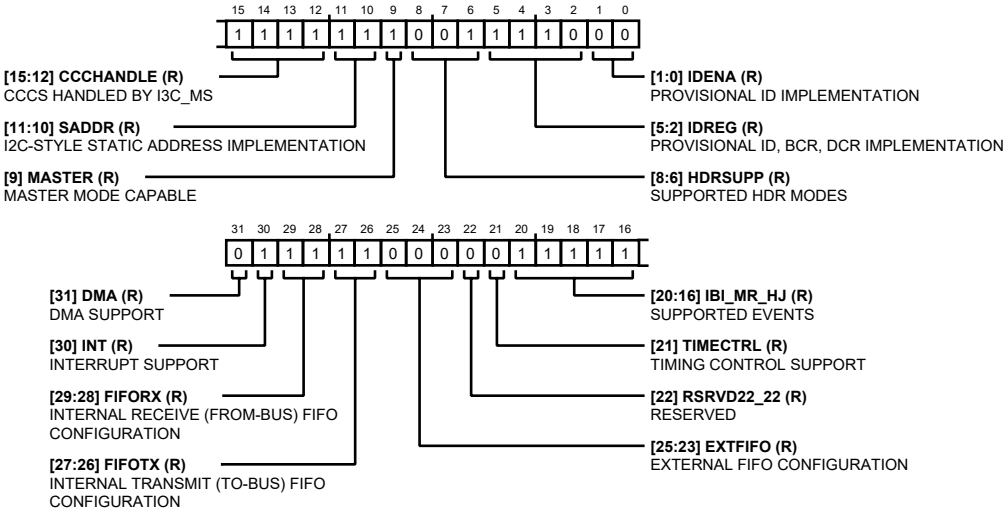


Table 440. Bit Descriptions for CAPABILITIES

Bits	Bit Name	Description	Reset	Access
31	DMA	DMA Support. 0: DMA is not supported (DMA_IMPL = 0). 1: DMA is supported (configuration parameter DMA_IMPL = 1, 2, or 3).	0x0	R
30	INT	Interrupt Support. 0: Interrupt is not supported (WITH_INTERRUPT = 0). 1: Interrupt is supported (WITH_INTERRUPT = 1).	0x1	R
[29:28]	FIFORX	Internal Receive (From-Bus) FIFO Configuration: 00: No internal receive FIFO (FIFO_IMPL = 0). The internal receive ping-pong buffer is present. 01: 4-byte receive FIFO (FIFO_IMPL = 1 and FROMBUS_FIFO_SIZE =2). 10: 8-byte receive FIFO (FIFO_IMPL = 1 and FROMBUS_FIFO_SIZE =3). 11: 16-byte receive FIFO (FIFO_IMPL = 1 and FROMBUS_FIFO_SIZE =4).	0x3	R
[27:26]	FIFOTX	Internal Transmit (To-Bus) FIFO Configuration. 00: No internal transmit FIFO (FIFO_IMPL = 0). The internal transmit ping-pong buffer is present. 01: 4-byte transmit FIFO (FIFO_IMPL = 1 and TOBUS_FIFO_SIZE = 2). 10: 8-byte transmit FIFO (FIFO_IMPL = 1 and TOBUS_FIFO_SIZE = 3). 11: 16-byte transmit FIFO (FIFO_IMPL = 1 and TOBUS_FIFO_SIZE = 4).	0x3	R
[25:23]	EXTFIFO	External FIFO Configuration (not supported, hardwired to 000).	0x0	R
22	RSRVD22_22	Reserved.	0x0	R
21	TIMECTRL	Timing Control Support. 0: No Timing Control modes are supported. 1: At least one Timing Control mode is supported .	0x0	R
[20:16]	IBI_MR_HJ	Supported Events:	0x1F	R

Bits	Bit Name	Description	Reset	Access
		[20]: Use BAMATCH field of CONFIG register to measure 1- s Bus Available timing: 0: Do not use BAMATCH (WITH_BAMATCH = 0). Instead, use the fixed value from CLOCK_SLOW_MATCH parameter. 1: Use BAMATCH (WITH_BAMATCH = 1).		
		[19]: Hot-Join support: 0: I3C_MS does not support generation of Hot-Join events (WITH_HJM = 0). 1: I3C_MS supports generation of Hot-Join events (WITH_HJM = 1).		
		[18]: Master request support: 0: I3C_MS does not support generation of master requests (WITH_MASTER_REQUEST = 0). 1: I3C_MS supports generation of master requests (WITH_MASTER_REQUEST = 1).		
		[17]: IBI has payload: 0: Generated IBIs do not include payload data (IBI_IMPL = 1) or IBIs are not supported (IBI_IMPL = 0). 1: Generated I Bis include payload data (IBI_IMPL = 2).		
		[16]: IBI support: 0: I3C_MS does not support generation of IBIs (IBI_IMPL = 0). 1: I3C_MS supports generation of In-Band Interrupts (IBIs) (IBI_IMPL = 1 or 2).		
[15:12]	CCCHANDLE	CCCs Handled by I3C_MS (in addition to the minimum set of CCCs required for basic I3C operation): [15]: Vendor Reserved field of GETSTATUS CCC: 0: I3C_MS does not support Vendor Reserved field of GETSTATUS CCC (WITH_STAT_VENDOR = 0). 1: I3C_MS supports Vendor Reserved field of GETSTATUS CCC using VENDINFO field of CTRL register (WITH_STAT_VENDOR = 1).	0xF	R
		[14]: Pending Interrupt and Activity Mode fields of GETSTATUS CCC: 0: I3C_MS does not support Pending Interrupt and Activity Mode fields of GETSTATUS CCC (WITH_STAT_INFO = 0). 1: I3C_MS supports Pending interrupt and Activity Mode fields of GETSTATUS CCC using PENDINT and ACTSTATE fields of CTRL register (WITH_STAT_INFO = 1).		
		[13]: CCCs related to maximum read/write length and maximum data speed: 0: I3C_MS does not support SETMWL/GETMWL, SETMRL/GETMRL, and GETMXDS CCCs (WITH_MAX_CCC = 0). 1: MS supports SETMWL/GETMWL, SETMRL/GETMRL, and GETMXDS CCCs (WITH_MAX_CCC = 1).		

Bits	Bit Name	Description	Reset	Access
		[12]: Basic CCCs: 0: I3C_MS does not support GETPID, GETBCR, GETDCR, GETHDRCAP, ENTAS*, and ENEC/DISEC CCCs (WITH_BASIC_CCC = 0). 1: I3C_MS supports GETPID, GETBCR, GETDCR, GETHDRCAP, ENTAS*, and ENEC/DISEC CCCs (WITH_BASIC_CCC = 1).		
[11:10]	SADDR	I2c-Style Static Address Implementation.	0x3	R
		00: No static address. The device supports I3C dynamic addresses only (SADDR_IMPL = 0).		
		01: The device has a 7-bit static address set by hardware parameter SADDR (SADDR_IMPL = 1).		
		10: The device has a 7-bit static address set through input pin ext_slvsa[7:0] (SADDR_IMPL = 2). ext_slvsa[7:1] hold the 7-bit static address; ext_slvsa[0] indicates the address is valid.		
		11: The static address is software-programmable through CONFIG[31:25] (SADDR_IMPL = 3).		
9	MASTER	Master Mode Capable. Hardwired to 1.	0x1	R
[8:6]	HDRSUPP	Supported HDR Modes: [8]: HDR-TSL- Hardwired to 0 (HDR-TSL mode not supported). [7]: HDR-TSP- Hardwired to 0 (HDR-TSP mode not supported) [6]: HDR-DDR: 0: I3C_MS does not support HDR- DDR mode (WITH_DDR = 0). 1: I3C_MS supports HDR- DDR mode (WITH_DDR = 1).	0x1	R
[5:2]	IDREG	Provisional ID, BCR, DCR Implementation. [5]: BCR: 0: BCR value is hardwired (BCR_AS_REG = 0). 1: BCR is available as a register (BCR_AS_REG = 1). The BCR value is in IDEXT[23:16]. [4]: DCR: 0: DCR value is hardwired (DCR_AS_REG = 0). 1: DCR is available as a register (DCR_AS_REG = 1). The DCR value is in IDEXT[15:8]. [3]: IDRAND bit: 0: Bit 32 of the Provisional ID is hardwired to 0 (ID_IMPL < 2). 1: Bit 32 of the Provisional ID is programmable through the IDRAND bit of the CONFIG register (ID_IMPL = 2 or 3). [2]: Instance ID: 0: The Instance ID field of the Provisional ID is set by hardware parameter ID_INST (ID_IMPL = 0, 2, or 3). 1: The Instance ID field of the Provisional ID is programmable through the IDEXT register (ID_IMPL = 1).	0xE	R
[1:0]	IDENA	Provisional Id Implementation. 00: Provisional ID is programmable 01: Provisional ID is set by hardware parameters ID_MAN, ID_PART, ID_INST, and ID_VENDOR (ID_IMPL = 0).	0x0	R

Bits	Bit Name	Description	Reset	Access
		10: Provisional ID is set by hardware parameters ID_MAN, ID_PART, and ID_VENDOR; Instance ID is programmable (ID_IMPL = 1). 11: Manufacturer ID field is set by hardware parameter ID_MAN; Part Number field is programmable (ID_IMPL = 2).		

DYNAMIC ADDRESS REGISTER

Address: 0xF0013064, Reset: 0x00000000, Name: DYNADDR

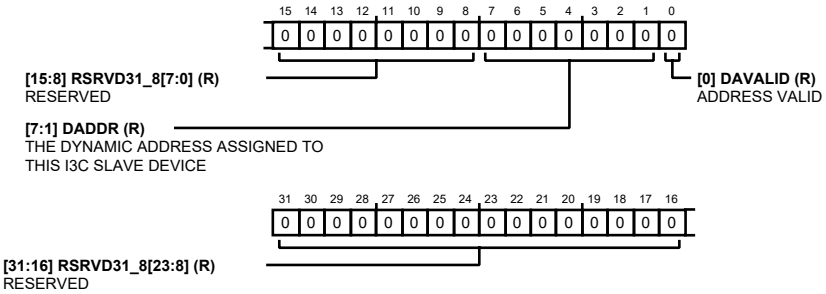


Table 441. Bit Descriptions for DYNADDR

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:1]	DADDR	The Dynamic Address Assigned to This I3C Slave Device.	0x0	R
0	DAVALID	Address Valid: 0: The address in the DADDR field is not valid. 1: The address in the DADDR field is valid.	0x0	R

MAXIMUM LIMITS REGISTER

Address: 0xF0013068, Reset: 0x0FFF0FFF, Name: MAXLIMITS

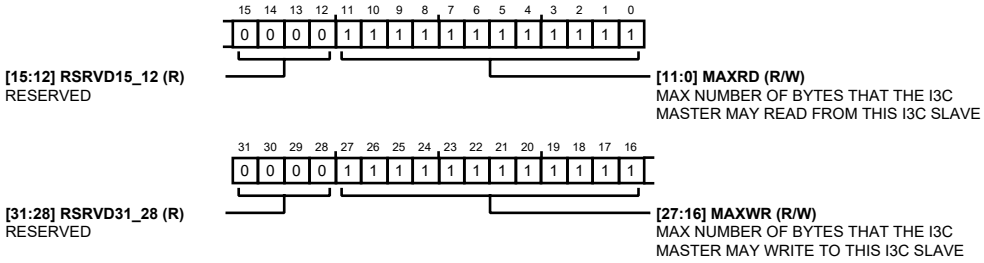


Table 442. Bit Descriptions for MAXLIMITS

Bits	Bit Name	Description	Reset	Access
[31:28]	RSRVD31_28	Reserved.	0x0	R
[27:16]	MAXWR	The maximum number of bytes that the I3C bus master may write to this I3C slave device per message, with the exception of broadcast CCCs. The minimum MAXWR value is 8 and the maximum is 4095. When the I3C bus master issues a SETMWL CCC, the lower 12 bits of the 2-byte SETMWL value are written to MAXWR; the upper 4 bits are disregarded. The default MAXWR value is set by hardware configuration parameter MWL. When writing to MAXWR from the application, do not set a value higher than was set by the I3C bus master.	0xFFF	R/W
[15:12]	RSRVD15_12	Reserved.	0x0	R
[11:0]	MAXRD	The maximum number of bytes that the I3C bus master may read from this I3C slave device per message. The minimum MAXRD value is 16 and the maximum is 4095. When the I3C bus master issues a SETMRL CCC, the lower 12 bits of the 2-byte SETMRL value are written to MAXRD; the upper 4 bits are disregarded. The default MAXRD value is set by hardware configuration parameter MRL. When writing to MAXRD from the application, do not set a value higher than was set by the I3C bus master.	0xFFF	R/W

PART NUMBER REGISTER

Address: 0xF001306C, Reset: 0x00000000, Name: PARTNO

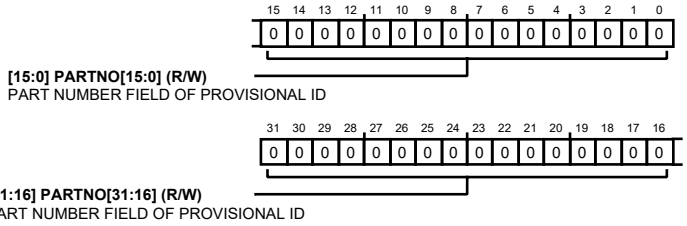


Table 443. Bit Descriptions for PARTNO

Bits	Bit Name	Description	Reset	Access
[31:0]	PARTNO	Part Number Field of Provisional ID. [31:16]: Part ID [15:12]: Instance ID [11:0]: Vendor-Defined	0x0	R/W

ID EXTENSION REGISTER

Address: 0x F0013070, Reset: 0x00000000, Name: IDEXT

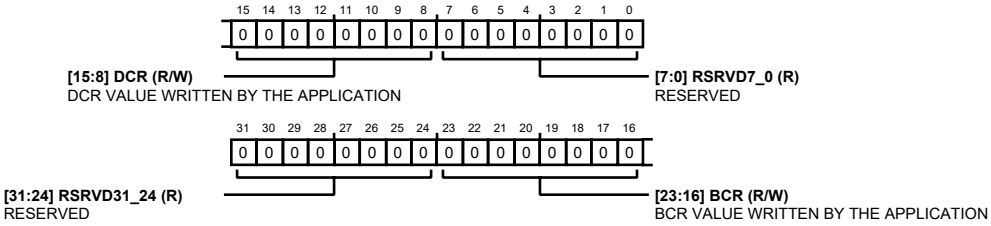


Table 444. Bit Descriptions for IDEXT

Bits	Bit Name	Description	Reset	Access
[31:24]	RSRVD31_24	Reserved.	0x0	R
[23:16]	BCR	When configuration parameter BCR_AS_REG = 1: BCR contains the 8-bit BCR value written by the application. Note: When configuration parameter WITH_DDR = 1, the BCR[5] value that the I3C_MS provides to the I3C bus master is the logical OR of IDEXT[21] and CONFIG[4] (DDROK). To disable HDR-DDR mode, set both IDEXT[21] and DDROK to 0. To enable HDR-DDR mode, set IDEXT[21] to 0 and DDROK to 1. When configuration parameter BCR_AS_REG = 0: The BCR field is not used. The read value is 0. Writes have no effect.	0x0	R/W
[15:8]	DCR	When configuration parameter DCR_AS_REG = 1: OCR contains the 8-bit OCR value written by the application.	0x0	R/W
		When configuration parameter DCR_AS_REG = 0: The OCR field is not used. The read value is 0. Writes have no effect.		
[7:0]	RSRVD7_0	Reserved.	0x0	R

VENDOR ID REGISTER

Address: 0xF0013074, Reset: 0x00000177, Name: VENDORID

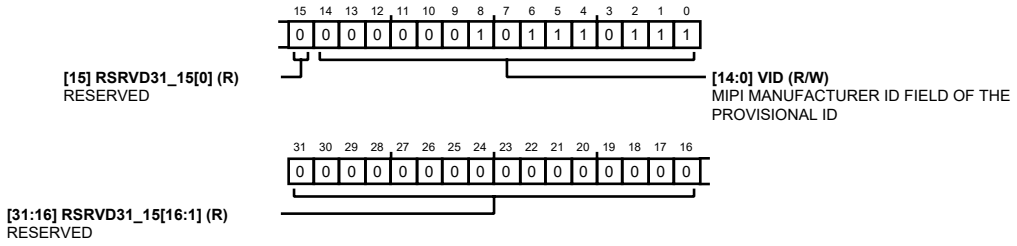


Table 445. Bit Descriptions for VENDORID

Bits	Bit Name	Description	Reset	Access
[31:15]	RSRVD31_15	Reserved.	0x0	R
[14:0]	VID	MIPI Manufacturer Id Field Of The Provisional Id.	0x177	R/W

MASTER CONTROL REGISTER

Address: 0x F0013084, Reset: 0x00000000, Name: MCTRL

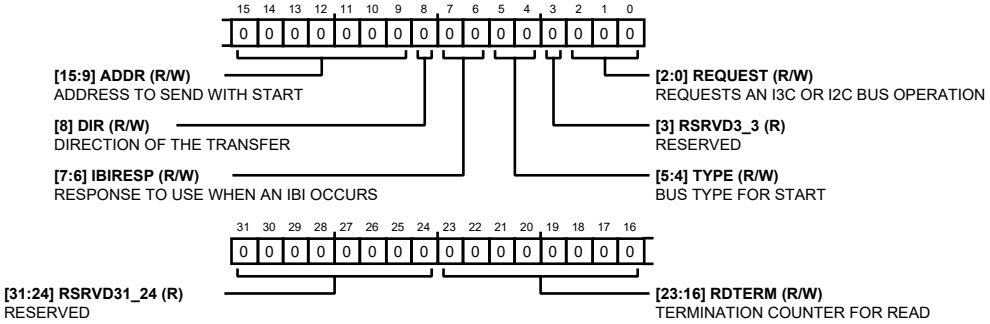


Table 446. Bit Descriptions for MCTRL

Bits	Bit Name	Description	Reset	Access
[31:24]	RSRVD31_24	Reserved.	0x0	R
[23:16]	RDTERM	Termination Counter For Read:	0x0	R/W
		For I2C mode read, the I3C_MS NACKs the read after receiving RDTERM bytes. For I3C SOR mode read, the I3C_MS aborts the read after RDTERM bytes if the slave has not yet sent End-of-Data. For I3C HDR-DDR mode read, the I3C_MS terminates the read after RDTERM words if the slave has not yet sent the CRC to end the read. An RDTERM value of O has no effect. The RDTERM field self-clears when the message is complete as indicated by the MSTATUS.COMPLETE flag. Note: The value 1 can be written to RDTERM at any time to terminate the current read after the next byte/word. Writing a value larger than 1 should only be done when starting a message by setting REQUEST to EmitStartAddr.		
[15:9]	ADDR	Address To Send with Start.	0x0	R/W
8	DIR	Direction Of the Transfer.	0x0	R/W
		0: Write.		
		1: Read.		
[7:6]	IBIRESP	Response to use when an IBI occurs. The meaning differs depending on whether the I3C_MS is automatically sending ACK/NACK for an IBI that occurs when REQUEST = EmitStartAddr or AutoIBI or the application is controlling the ACK/NACK (REQUEST = IBIAckNack). See Table 4. The IBIRESP field is used both for messages controlled through MCTRL and messages generated in message mode using MWMSG_SDR and MWMSG_DDR. Note: For Hot-Join requests and master requests, there is no automatic response. It is up to the application to ACK or NACK the request by writing 00 or 01 to IBIRESP in response to the incoming Hot-Join or master request event.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
[5:4]	TYPE	Bus Type for Start.	0x0	R/W
		00: I3C		
		01: I2C		
		10: Enter HDR-DDR mode (if not already in HDR-DDR mode). The I3C_MS issues address 7'h7E and the ENTHDR0 CCC with the START. The first byte written to the transmit buffer is the first HDR-DDR command.		
3	RSRVD3_3	Reserved.	0x0	R
[2:0]	REQUEST	Requests An I3c Or I2c Bus Operation:	0x0	R/W
		000: None. The REQUEST field returns to 000 when the I3C_MS completes the previous request. The MSTATUS register indicates the current state of the I3C_MS. The application should only write 000 to REQUEST when setting RDTERM to stop a read that is in progress, when setting the IBIRESP field for use in message mode, or to cancel an AutoIBI request while the I3C bus is in the stopped state.		
		001: EmitStartAddr. Emit a START with address and read/write bit from stopped state or in the middle of an SDR message (for a repeated START).		
		010: EmitStop. Emit a STOP. For the I3C_MS to emit a STOP, the I3C bus must be in SDR mode. If the STOP is emitted in DAA mode, DAA mode is exited.		
		011: IBIAckNack. Manually ACK or NACK an 181. When IBI RESP = 11, STATUS.STATE becomes 110 (IBIACK) when the I3C_MS is waiting for the application to make an ACK/NACK decision for an IBI. Writing 011 to REQUEST along with a new IBIRESP value completes the ACK or NACK using the newly written IBIRESP value.		
		100: ProcessDAA. If the I3C_MS is not already in DAA mode, I3C_MS starts the DAA process by emitting START with address 7'h7Efollowed by an ENTDAA CCC. If DAA mode is already started and the MSTATUS register indicates STATE = DAA and BETWEEN = 1, then writing 100 to REQUEST causes the I3C_MS to assign the dynamic address in the MWDATAB register to the current slave, then continue the DAA process.		
		101: Reserved		
		110: ForceExit: Emit HDR Exit Pattern. If I3C_MS is in HDR-DDR mode, the I3C_MS exits HDR-DDR mode. The HDR Exit Pattern is followed by a STOP.		
		111: Auto I BI. The I3C MS remains in the stopped state but emits a START with address 7'h7E when a slave pulls SDA low to request an IBI. The IBIRESP field controls how the I3C_MS handles the IBI.		

MASTER STATUS REGISTER

Address: 0x F0013088, Reset: 0x00001000, Name: MSTATUS

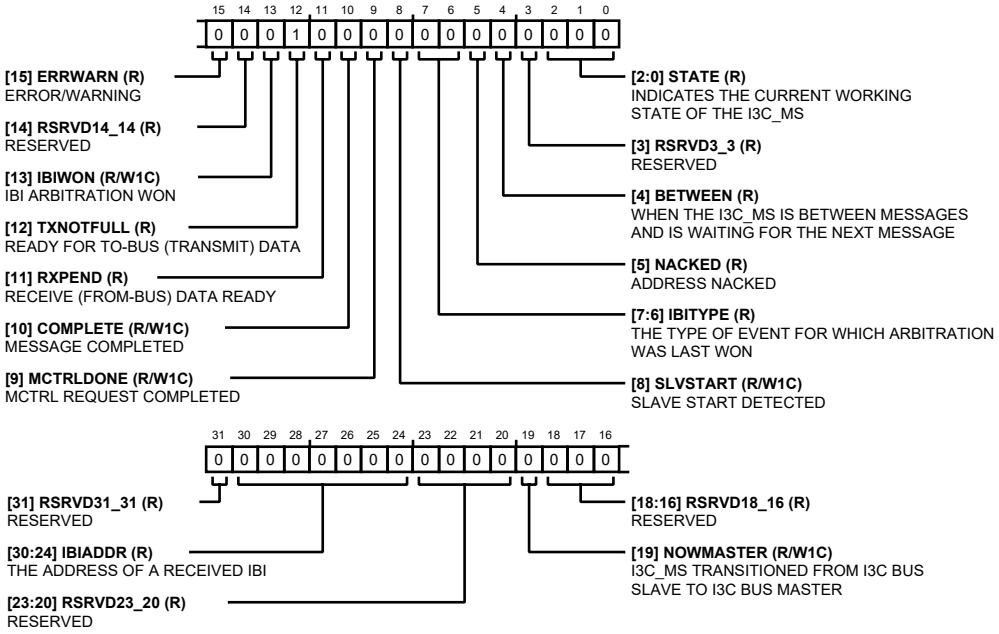


Table 447. Bit Descriptions for MSTATUS

Bits	Bit Name	Description	Reset	Access
31	RSRVD31_31	Reserved.	0x0	R
[30:24]	IBIADDR	The address of a received IBI (when IBITYPE = 1) or master request (when IBITYPE = 2) or 7'h2 for a Hot-Join request (I8ITYPE = 3).	0x0	R
[23:20]	RSRVD23_20	Reserved.	0x0	R
19	NOWMASTER	I3c_Ms Transitioned From I3c Bus Slave To I3c Bus Master: 0: The I3C_MS has not transitioned from I3C bus slave to I3C bus master since NOWMASTER was last cleared. 1: As an I3C bus slave, the I3C_MS was assigned bus mastership and is now the I3C bus master.	0x0	R/W1C
[18:16]	RSRVD18_16	Reserved.	0x0	R
15	ERRWARN	Error/Warning: 0: No error or warning is active in the MERRWARN register. 1: An error or warning has occurred. The MERRWARN register indicates the active error or warning. To clear the STATUS.ERRWARN bit, write 1 to the required bit(s) in the MERRWARN register.	0x0	R
14	RSRVD14_14	Reserved.	0x0	R
13	IBIWON	IBI Arbitration Won: 0: A slave has not won address arbitration for an 181, master request, or Hot-Join request since the IBIWON bit was last cleared.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: A slave emitting an 181, master request, or Hot-Join request has won arbitration on a message header address. For an IBI, the I3C_MS responds according to the value of MCTRL.IBIRESP. For a Hot-Join request or master request, the application must decide whether to ACK or NACK the request.		
12	TXNOTFULL	Ready For To-Bus (Transmit) Data: 0: The I3C_MS to-bus buffer cannot accept another byte or half-word of data. 1: The I3C_MS to-bus buffer can accept another byte or half-word of data. When internal FIFO operation is enabled, TXNOTFULL status is determined by the amount of data in the to-bus FIFO relative to the value of the TXTRIG field in the DATACTRL register. The TXNOTFULL bit automatically self-clears when the to-bus buffer is not ready to accept more data.	0x1	R
11	RXPEND	Receive (From-Bus) Data Ready: 0: No receive data is available. The I3C_MS is not receiving data. When internal FIFO operation is enabled, RXPEND status is determined by the amount of data in the from-bus FIFO relative to the value of the RXTRIG field in the DATACTRL register. 1: Receive data is available. The I3C_MS is receiving data from a slave.	0x0	R
10	COMPLETE	Message Completed: 0: A message has not completed on the I3C or I2C bus since the COMPLETE bit was last cleared. 1: message has completed on the I3C or I2C bus. The meaning of COMPLETE depends on how the message was initiated: For a message initiated using the MWMSG_SDR or MWMSB_DDR register, COMPLETE is set when the message byte count decrements to 0. For a message initiated by setting MCTRL.REQUEST to EmitStartAddr, COMPLETE is set when the message is terminated or End-of-Data occurs. For an 181 that occurs when MCTRL.REQUEST is AutoIBI or EmitStartAddr, COMPLETE is set at the end of IBI data (if the IBI includes a mandatory byte) or simultaneously with IBIWON if the IBI does not COMPLETE automatically clears upon a write to MCTRL, MWMSG_SDR, or MWMSG_DDR. include a mandatory byte.	0x0	R/W1C
9	MCTRLDONE	MCTRL Request Completed: 0: No request from MCTRL. REQUEST has completed since MCTRLDONE was last cleared.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
		1: A request from MCTRL.REQUEST completed. When MCTRL.REQUEST = EmitStartAddr, MCTRLDONE is set when the I3C_MS emits the address and the address is either ACKed, NACKed, or ends with an IBI. COMPLETE is set when the data write or read completes. When MCTRL.REQUEST = ProcessDAA, MCTRLDONE is set when the I3C_MS is ready to emit a dynamic address for a slave (in which case BETWEEN = 1) or when no slave ACKs the broadcast address 7'h7E (in which case BETWEEN = 0 and the DAA process is complete). MCTRLDONE automatically clears when a new request is written to MCTRL.REQUEST.		
8	SLVSTART	Slave Start Detected: 0: An I3C slave has not requested a START since the SLVSTART bit was last cleared. 1: An I3C slave requested a START by holding SDA low.	0x0	R/W1C
[7:6]	IBITYPE	The Type Of Event For Which Arbitration Was Last Won: 00: None 01: IBI 10: Master request 11: Hot-Join request	0x0	R
5	NACKED	Address NACKed: 0: The last START+ Address was ACKed. 1: The last START+ Address was NACKed.	0x0	R
4	BETWEEN	When STATE = MSGSDR or DDR, BETWEEN is 1 when the I3C_MS is between messages and is waiting for the next message to be initiated. When STATE = DAA, BETWEEN is 1 when the I3C_MS is waiting for the application to provide a dynamic address for the slave for which the Provisional ID was just read. When STATE = NORMACT, BETWEEN is 1 when the I3C_MS is stalled waiting for the transmit buffer to be not-empty or the receive buffer to be not-full.	0x0	R
3	RSRVD3_3	Reserved.	0x0	R
[2:0]	STATE	Indicates The Current Working State of The I3c_Ms. 000: IDLE. The I3C bus is stopped. 001: SLVREQ. The I3C bus is stopped and a slave is holding SDA low. If MCTRL.REQUEST = AutoIBI, IBI processing starts automatically and the I3C_MS does not remain in the SLVREQ state. 010: MSGSDR. The I3C_MS is in SDR message mode initiated using MWMSG_SDR. 011: NORMACT. The I3C_MS is in SDR message mode, using MCTRL and MWDATAB/H(E) and MRDATAB/H. The I3C_MS remains in NORMACT mode until STOP is issued. 100: DDR. The I3C_MS is in DDR message mode initiated using either MWMSG_DDR or MCTRL. The I3C_MS remains in the DDR state until it issues the HDR Exit Pattern.	0x0	R

Bits	Bit Name	Description	Reset	Access
		101: DAA. The I3C_MS is in DAAmode. 110: IBIACK: The I3C_MS is waiting for the application to provide an ACK/NACK decision. 111: IBIRCV. The I3C_MS is receiving an IBI. The I3C_MS enters the IBIRCV state when an IBI, master request, or Hot-Join request wins arbitration and remains in the IBIRCV state through the IBI mandatory byte (if included with the IBI) and any bytes that follow the mandatory byte.		

IBI REGISTRY AND RULES REGISTER

Address: 0x F001308C, Reset: 0x00000000, Name: IBIRULES

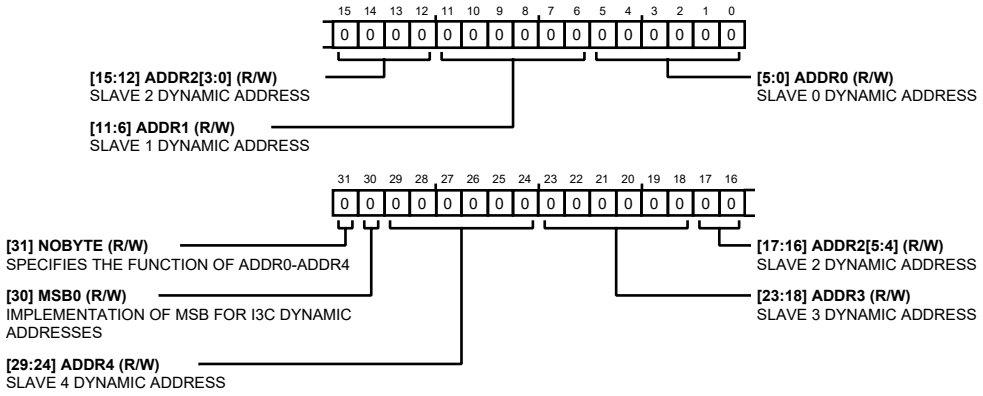


Table 448. Bit Descriptions for IBIRULES

Bits	Bit Name	Description	Reset	Access
31	NOBYTE	Specifies The Function of Addr0-Addr4. 0: ADDR0-ADDR4 are dynamic addresses of I3C slaves that provide a mandatory byte when sending an IBI. 1: ADDR0-ADDR4 are dynamic addresses of I3C slaves that do not provide a mandatory byte when sending an IBI.	0x0	R/W
30	MSB0	Implementation Of Msb for I3c Dynamic Addresses. 0: I3C dynamic addresses may have MSb = 0 or MSb = 1. 1: All I3C dynamic addresses have MSb = 0.	0x0	R/W
[29:24]	ADDR4	Slave 4 Dynamic Address. Slave at dynamic address ADDR4 either provides or does not provide a mandatory byte with IBIs, as indicated by the value of NOBYTE. Each slave dynamic address (ADDR0-ADDR4) in this register is six bits. The MSb of the 7-bit dynamic address is assumed to be 0. If MSB0 = 0 and slaves may have dynamic addresses with MSb = 1, then it is up to the application to only use ADDR0-ADDR4 for slaves with dynamic addresses below 7'h40 (dynamic address MSb = 0).	0x0	R/W
[23:18]	ADDR3	Slave 3 Dynamic Address. Same function as ADDR4.	0x0	R/W
[17:12]	ADDR2	Slave 2 Dynamic Address. Same function as ADDR4.	0x0	R/W
[11:6]	ADDR1	Slave 1 Dynamic Address. Same function as ADDR4.	0x0	R/W
[5:0]	ADDR0	Slave 0 Dynamic Address. Same function as ADDR4.	0x0	R/W

MASTER INTERRUPT ENABLE SET REGISTER

Address: 0x F0013090, Reset: 0x00000000, Name: MINTSET

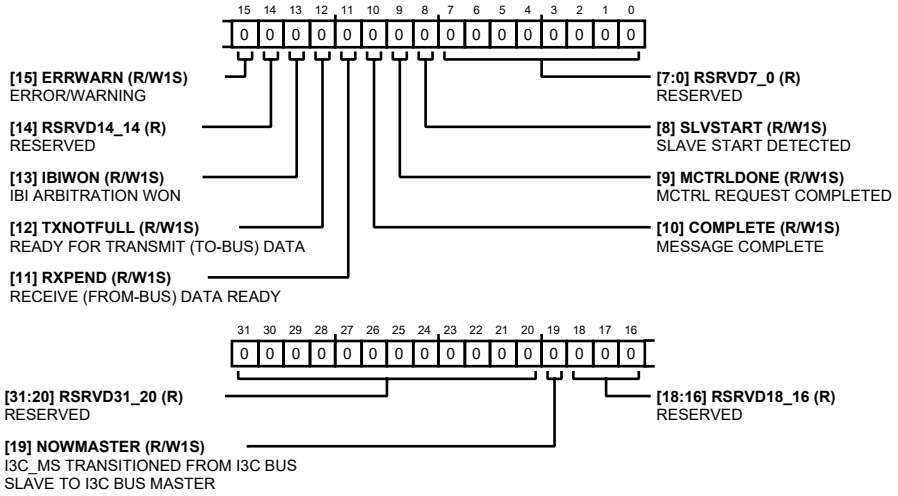


Table 449. Bit Descriptions for MINTSET

Bits	Bit Name	Description	Reset	Access
[31:20]	RSRVD31_20	Reserved.	0x0	R
19	NOWMASTER	I3c_Ms Transitioned from I3c Bus Slave To I3c Bus Master. 0: Now master interrupt disabled. 1: Now master interrupt enabled.	0x0	R/W1S
[18:16]	RSRVD18_16	Reserved.	0x0	R
15	ERRWARN	Error/Warning. 0: Error/warning interrupt disabled. 1: Error/warning interrupt enabled.	0x0	R/W1S
14	RSRVD14_14	Reserved	0x0	R
13	IBIWON	IBI Arbitration Won. 0: IBI arbitration won interrupt disabled. 1: IBI arbitration won interrupt enabled.	0x0	R/W1S
12	TXNOTFULL	Ready For Transmit (To-Bus) Data. 0: Ready for transmit data interrupt disabled. 1: Ready for transmit data interrupt enabled.	0x0	R/W1S
11	RXPEND	Receive (From-Bus) Data Ready. 0: Receive data ready interrupt disabled. 1: Receive data ready interrupt enabled.	0x0	R/W1S
10	COMPLETE	Message Complete. 0: Message complete interrupt disabled. 1: Message complete interrupt enabled.	0x0	R/W1S

Bits	Bit Name	Description	Reset	Access
9	MCTRLDONE	MCTRL Request Completed. 0: MCTRL request completed interrupt disabled. 1: MCTRL request completed interrupt enabled.	0x0	R/W1S
8	SLVSTART	Slave Start Detected. 0: Slave START detected interrupt disabled. 1: Slave START detected interrupt enabled.	0x0	R/W1S
[7:0]	RSRVD7_0	Reserved.	0x0	R

MASTER INTERRUPT ENABLE CLEAR REGISTER

Address: 0x F0013094, Reset: 0x00000000, Name: MINTCLR

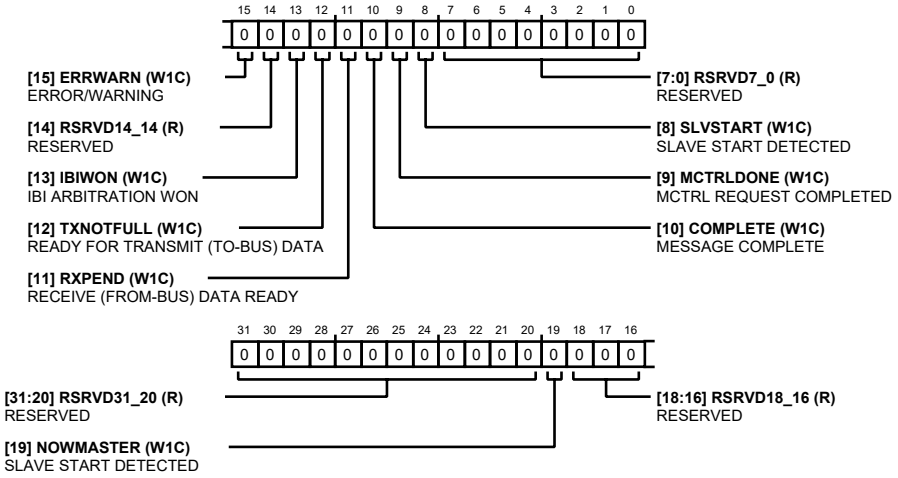


Table 450. Bit Descriptions for MINTCLR

Bits	Bit Name	Description	Reset	Access
[31:20]	RSRVD31_20	Reserved.	0x0	R
19	NOWMASTER	Slave Start Detected. 0: No effect. 1: Disable now master interrupt.	0x0	W1C
[18:16]	RSRVD18_16	Reserved.	0x0	R
15	ERRWARN	Error/Warning. 0: No effect. 1: Disable error/warning interrupt.	0x0	W1C
14	RSRVD14_14	Reserved.	0x0	R
13	IBIWON	IBI Arbitration Won. 0: No effect. 1: Disable arbitration won interrupt.	0x0	W1C
12	TXNOTFULL	Ready For Transmit (To-Bus) Data. 0: No effect. 1: Disable ready for transmit data interrupt.	0x0	W1C
11	RXPEND	Receive (From-Bus) Data Ready.	0x0	W1C

Bits	Bit Name	Description	Reset	Access
		0: No effect. 1: Disable receive data ready interrupt.		
10	COMPLETE	Message Complete. 0: No effect. 1: Disable message complete interrupt.	0x0	W1C
9	MCTRLDONE	MCTRL Request Completed. 0: No effect. 1: Disable MCTRL request completed interrupt.	0x0	W1C
8	SLVSTART	Slave Start Detected. 0: No effect. 1: Disable slave START detected interrupt.	0x0	W1C
[7:0]	RSRVD7_0	Reserved.	0x0	R

MASTER INTERRUPT MASKED REGISTER

Address: 0x F0013098, Reset: 0x00000000, Name: MINTMASKED

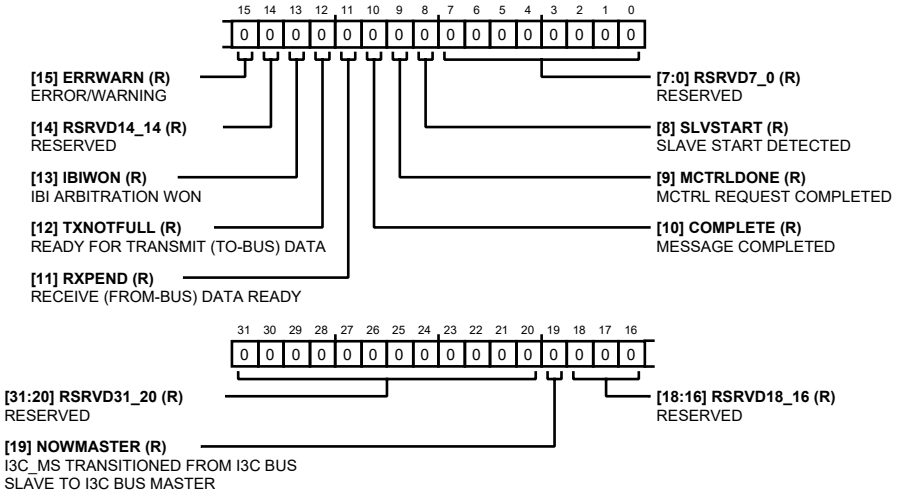


Table 451. Bit Descriptions for MINTMASKED

Bits	Bit Name	Description	Reset	Access
[31:20]	RSRVD31_20	Reserved.	0x0	R
19	NOWMASTER	I3c_Ms Transitioned from I3c Bus Slave To I3c Bus Master: 0: The I3C_MS has not transitioned from I3C bus slave to I3C bus master or the NOWMASTER interrupt is disabled. 1: The I3C_MS was assigned bus mastership and is now the I3Cbus master and the NOWMASTER interrupt is enabled in the MINTSET register.	0x0	R
[18:16]	RSRVD18_16	Reserved.	0x0	R
15	ERRWARN	Error/Warning: 0: No error or warning is active in the MERRWARN register or the ERRWARN interrupt source is disabled.	0x0	R

Bits	Bit Name	Description	Reset	Access
		1: An error or warning has occurred and the ERRWARN interrupt source is enabled in the MINTSET register. The MERRWARN register indicates the active error or warning. To clear the STATUS.ERRWARN bit, write 1 to the required bit(s) in the MERRWARN register.		
14	RSRVD14_14	Reserved.	0x0	R
13	IBIWON	IBI Arbitration Won: 0: A slave has not won address arbitration for an 181, master request, or Hot-Join request or the IBIWON interrupt is disabled. 1: A slave emitting an 181, master request, or Hot-Join request has won arbitration on a message header address and the IBIWON interrupt is enabled in the MINTSET register.	0x0	R
12	TXNOTFULL	Ready For Transmit (To-Bus) Data. 0: The I3C_MS transmit buffer cannot accept another byte of data or the TXNOTFULL interrupt source is disabled. 1: The I3C_MS transmit buffer can accept another byte of data and the TXNOTFULL interrupt source is enabled in the MINTSET register.	0x0	R
11	RXPEND	Receive (From-Bus) Data Ready. 0: No receive data is available or the RXPEND interrupt source is disabled. 1: Receive data is available and the RXPEND interrupt source is enabled in the MINTSET register.	0x0	R
10	COMPLETE	Message Completed. 0: A message has not completed on the I3C bus or the COMPLETE interrupt source is disabled. 1: A message has completed on the I3C bus and the COMPLETE interrupt source is enabled in the MINTSET register.	0x0	R
9	MCTRLDONE	MCTRL Request Completed.	0x0	R
		0: No request from MCTRL. REQUEST has completed or the MCTRLDONE interrupt source is disabled.		
		1: A request from MCTRL. REQUEST completed and the MCTRLDONE interrupt source is enabled in the MINTSET register.		
8	SLVSTART	Slave Start Detected. 0: An I3C slave has not requested a START or the SLVSTART interrupt source is disabled. 1: An I3C slave requested a START by holding SDA low and the SLVSTART interrupt source is enabled in the MINTSET register.	0x0	R
[7:0]	RSRVD7_0	Reserved.	0x0	R

MASTER ERROR AND WARNING REGISTER

Address: 0x F001309C, Reset: 0x00000000, Name: MERRWARN

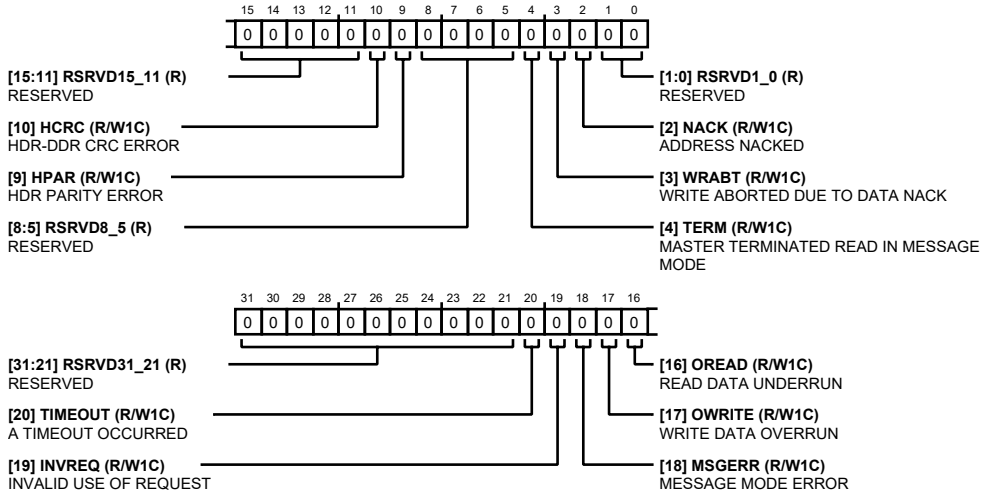


Table 452. Bit Descriptions for MERRWARN

Bits	Bit Name	Description	Reset	Access
[31:21]	RSRVD31_21	Reserved.	0x0	R
20	TIMEOUT	When configuration parameter WITH_TIMEOUT = 1, TIMEOUT indicates that the I3C_MS has stalled for too long in a frame and a timeout occurred: 0: Timeout did not occur. 1: Timeout occurred. A timeout occurs when the I3C_MS remains stalled in a state other than stopped for 100 s or more. Conditions that can cause a timeout are: The I3C_MS stalls during a message because the transmit buffer is empty or the receive buffer is full. The I3C_MS stalls because the application takes to long to make a ACK/NACK decision for an IBI. When configuration parameter WITH_TIMEOUT = 0, the TIMEOUT bit is not used. The read value is 0.	0x0	R/W1C
19	INVREQ	Invalid Use of Request: 0: The application did not write an invalid request to MCTRL.REQUEST. 1: The application wrote a request to MCTRL.REQUEST that is not allowed in the current state of the I3C_MS. Examples of invalid requests include: Requesting EmitStartAddr or EmitStop when in HDR-DDR mode. Any request other than ProcessOAA or EmitStop when in DAA mode. Any request other than IBIAckNack when the I3C_MS is waiting for an ACK/NACK decision from the application. Any request other than EmitStartAddr, ForceExit, or AutoIBI when in the stopped state. Any request other than EmitStartAddr or EmitStop when at the end of a read, write, or IBI.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
18	MSGERR	Message Mode Error:	0x0	R/W1C
		0: A message mode error did not occur.		
		1: A message mode error occurred.		
		Examples of message mode errors include: Writing to MWMSG_SOR while processing an HOR-OOR mode message. Writing to MWMSG_OOR while processing an SOR mode message. Reading from MRMSG_SOR while processing an HOR-OOR mode message. Reading from MRMSG_OOR while processing an SOR mode message. Writing IBIAckNack, ProcessDAA, or AutoIBI to MCTRL.REQUEST when a message mode operation is in progress.		
17	OWRITE	Write Data Overrun. 0: The transmit buffer/FIFO was not written to when full. 1: The transmit buffer/FIFO was written to when full (through either WDATAB(E), WDATAH(E), MWMSG_SDR.DATA, or MWMSG_DDR.DATA).	0x0	R/W1C
16	OREAD	Read Data Underrun: 0: The receive buffer/FIFO was not read when empty. 1: The receive buffer/FIFO was read when empty (through either RDATAB, RDATAH, MRMSG_SDR.DATA, or MRMSG_DDR.DATA).	0x0	R/W1C
[15:11]	RSRVD15_11	Reserved.	0x0	R
10	HCRC	HDR-DDR CRC Error. 0: No CRC error was detected in an HDR-DDR mode read. 1: A CRC error was detected in an HDR-DDR mode read	0x0	R/W1C
9	HPAR	HDR Parity Error. 0: No parity error was detected in an HDR-DDR mode read. 1: A parity error was detected in an HDR-DDR mode read.	0x0	R/W1C
[8:5]	RSRVD8_5	Reserved.	0x0	R
4	TERM	Master Terminated Read in Message Mode. 0: The I3C_MS did not terminate a read because the received byte count exceeds the byte count for the message. 1: The I3C_MS terminated a read because the received byte count exceeds the byte count for the message. TERM applies only to message mode reads initiated using MWMSG_SDR or MWMSG_DDR. TERM automatically self-clears when MWMSG_SDR or MWMSG_DDR is written.	0x0	R/W1C

Bits	Bit Name	Description	Reset	Access
3	WRABT	Write Aborted Due to Data NACK. 0: An I2C mode write data NACK did not occur. 1: An I2C mode write was terminated because the addressed I2C bus slave NACKed the write data. WRABT automatically self-clears when MCTRL is written.	0x0	R/W1C
2	NACK	Address NACKed. 0: An address NACK did not occur. 1: The I3C or I2C mode address emitted by the I3C_MS was NACKed by the I3C/I2C bus slave(s). NACK automatically self-clears when MCTRL is written.	0x0	R/W1C
[1:0]	RSRVD1_0	Reserved.	0x0	R

MASTER DATA CONTROL REGISTER

Address: 0x F00130AC, Reset: 0x80000030, Name: MDATACTRL

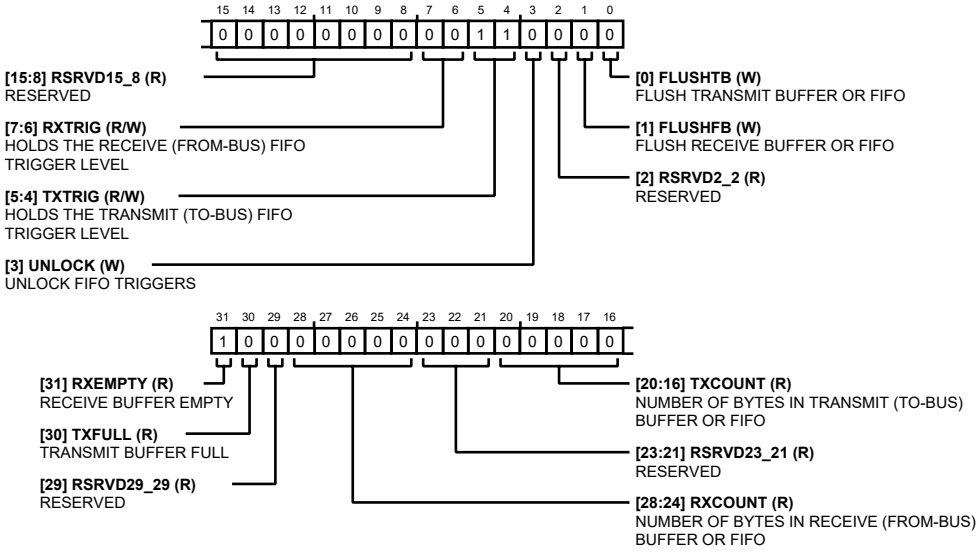


Table 453. Bit Descriptions for MDATACTRL

Bits	Bit Name	Description	Reset	Access
31	RXEMPTY	Receive Buffer Empty. 0: The receive (from-bus) buffer or FIFO is not empty. 1: The receive (from-bus) buffer or FIFO is empty.	0x1	R
30	TXFULL	Transmit Buffer Full. 0: The transmit (to-bus) buffer or FIFO is not full. 1: The transmit (to-bus) buffer or FIFO is full.	0x0	R
29	RSRVD29_29	Reserved.	0x0	R
[28:24]	RXCOUNT	Number Of Bytes In Receive (From-Bus) Buffer Or FIFO.	0x0	R
[23:21]	RSRVD23_21	Reserved.	0x0	R
[20:16]	TXCOUNT	Number Of Bytes In Transmit (To-Bus) Buffer Or FIFO.	0x0	R
[15:8]	RSRVD15_8	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
[7:6]	RXTRIG	When configuration parameter FIFO_IMPL = 1 (internal FIFOs), RXTRIG holds the receive (from-bus) FIFO trigger level: 00: Trigger when not empty. 01: Trigger when 1/4 full or more. 10: Trigger when 1/2 full or more. 11: Trigger when 3/4 full or more. When the receive FIFO fullness reaches the trigger level, the I3C_MS generates an interrupt (if configured and enabled). When configuration parameter FIFO_IMPL = 0, RXTRIG controls the trigger level for the receive (from-bus) ping-pong buffer: 00, 01, or 10: Trigger when not empty (1 or more bytes are available in the receive buffer). 11: Trigger when there are 2 bytes in the receive buffer (so half-word read can be used). Note: RXTRIG can only be written when bit 3 (UNLOCK) is also written as 1 in the same write operation.	0x0	R/W
[5:4]	TXTRIG	When configuration parameter FIFO_IMPL = 1 (internal FIFOs), TXTRIG holds the transmit (to-bus) FIFO trigger level: 00: Trigger when empty. 01: Trigger when 1/4 full or less. 10: Trigger when 1/2 full or less. 11: Trigger when 1 less than full or less. When the transmit FIFO emptiness reaches the trigger level, the I3C_MS generates an interrupt (if configured and enabled). When configuration parameter FIFO_IMPL = 0, TXTRIG controls the trigger level for the transmit (to-bus) ping-pong buffer: 01, 10, or 11: Trigger when not full (1 or more bytes of space are available in the transmit buffer). 00: Trigger when the transmit buffer is empty (so half-word write can be used). Note: TXTRIG can only be written when bit 3 (UNLOCK) is also written as 1 in the same write operation.	0x3	R/W
3	UNLOCK	Unlock FIFO Triggers. 0: Disable writing to bits [7:4] in the current write cycle. 1: Enable writing to bits [7:4] in the current write cycle.	0x0	W
2	RSRVD2_2	Reserved.	0x0	R
1	FLUSHFB	Flush Receive Buffer Or FIFO. 0: Do not flush the receive(from-bus) buffer or FIFO. 1: Flush the receive (from-bus) buffer or FIFO.	0x0	W
0	FLUSHTB	Flush Transmit Buffer Or FIFO. 0: Do not flush the transmit (to-bus) buffer or FIFO. 1: Flush the transmit (to-bus) buffer or FIFO.	0x0	W

MASTER WRITE BYTE DATA REGISTER

Address: 0x F00130B0, Reset: 0x00000000, Name: MWDATAB

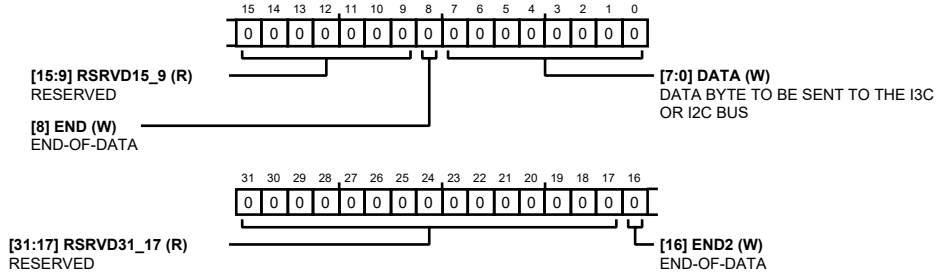


Table 454. Bit Descriptions for MWDATAB

Bits	Bit Name	Description	Reset	Access
[31:17]	RSRVD31_17	Reserved.	0x0	R
16	END2	End-Of-Data. 0: The byte in the DATA field is not the last data byre of the message. 1: The byte in the DATA field is the last data byre of the message.	0x0	W
[15:9]	RSRVD15_9	Reserved.	0x0	R
8	END	End-Of-Data. 0: The byte in the DATA field is not the last data byre of the message. 1: The byte in the DATA field is the last data byre of the message.	0x0	W
[7:0]	DATA	Data Byte to Be Sent to The I3c Or I2c Bus.	0x0	W

MASTER WRITE BYTE DATA AS END REGISTER

Address: 0x F00130B4, Reset: 0x00000000, Name: MWDATABE

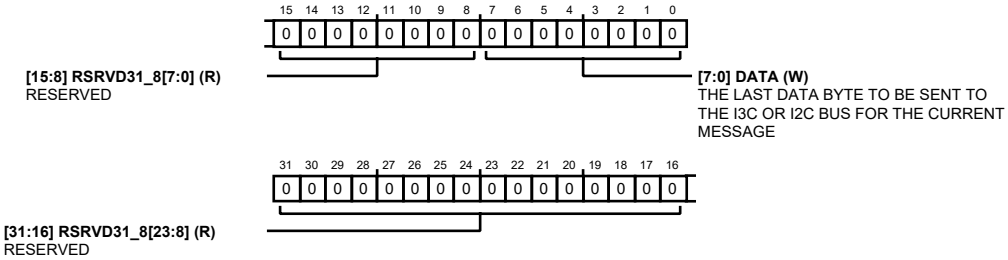


Table 455. Bit Descriptions for MWDATABE

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved	0x0	R
[7:0]	DATA	The last data byte to be sent to the i3c or i2c bus for the current message.	0x0	W

MASTER WRITE HALF-WORD DATA REGISTER

Address: 0x0B8, Reset: 0x00000000, Name: MWDATAH

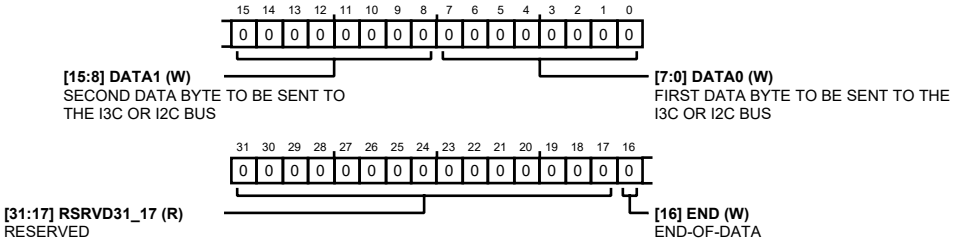


Table 456. Bit Descriptions for MWDATAH

Bits	Bit Name	Description	Reset	Access
[31:17]	RSRVD31_17	Reserved	0x0	R
16	END	End-Of-Data. 0: The byte in the DATA1 field is not the last data byre of the message. 1: The byte in the DATA1 field is the last data byre of the message.	0x0	W
[15:8]	DATA1	Second Data Byte to Be Sent to The I3c Or I2c Bus.	0x0	W
[7:0]	DATA0	First Data Byte to Be Sent to The I3c Or I2c Bus.	0x0	W

MASTER WRITE HALF-WORD DATA AS END REGISTER

Address: 0x F00130BC, Reset: 0x00000000, Name: MWDATAHE

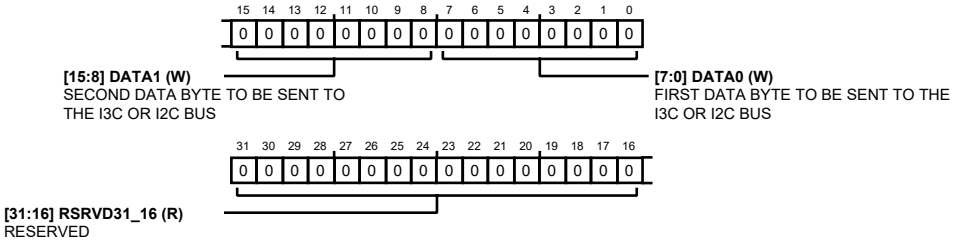


Table 457. Bit Descriptions for MWDATAHE

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved.	0x0	R
[15:8]	DATA1	Second data byte to be sent to the i3c or i2c bus.	0x0	W
[7:0]	DATA0	First data byte to be sent to the i3c or i2c bus.	0x0	W

MASTER READ BYTE DATA REGISTER

Address: 0x0C0, Reset: 0x00000000, Name: MRDATAB

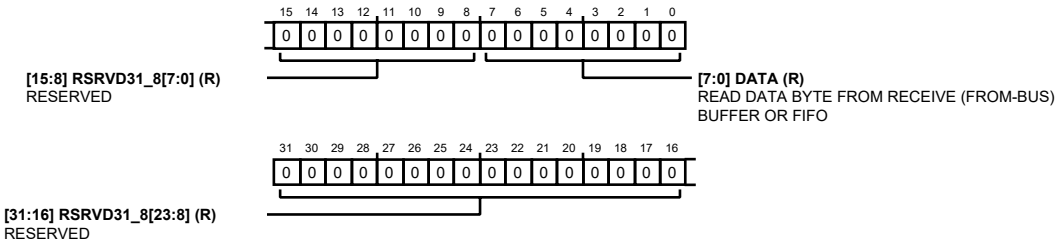


Table 458. Bit Descriptions for MRDATAB

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:0]	DATA	Read Data Byte from Receive (from-bus) Buffer Or FIFO.	0x0	R

MASTER READ HALF-WORD DATA REGISTER

Address: 0x F00130C8, Reset: 0x00000000, Name: MRDATAH

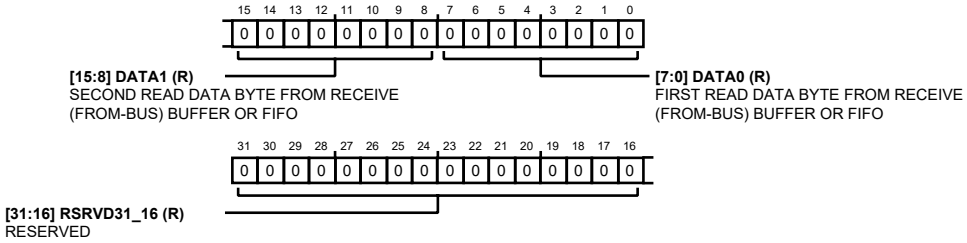


Table 459. Bit Descriptions for MRDATAH

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	RESERVED. Reserved. The read value is 0. Writes have no effect. Use 0 for writes.	0x0	R
[15:8]	DATA1	Second read data byte from receive (from-bus) buffer or FIFO.	0x0	R
[7:0]	DATA0	First read data byte from receive (from-bus) buffer or FIFO.	0x0	R

MASTER BYTE-ONLY WRITE BYTE DATA REGISTER

Address: 0x F00130CC, Reset: 0x00000000, Name: MWDATAB1

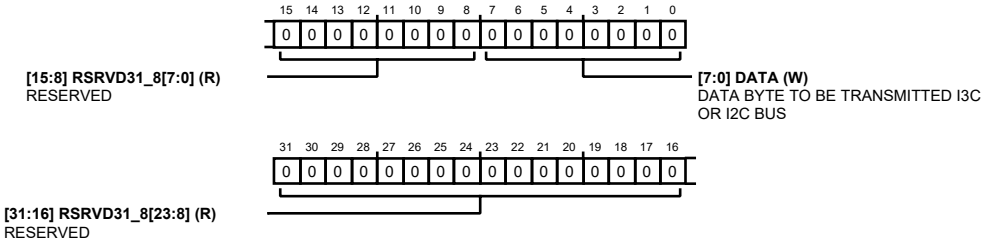


Table 460. Bit Descriptions for MWDATAB1

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:0]	DATA	Data byte to be transmitted i3c or i2c bus.	0x0	W

START OR CONTINUE SDR MESSAGE REGISTER

Address: 0x0D0, Reset: 0x00000000, Name: MWMSG_SDR

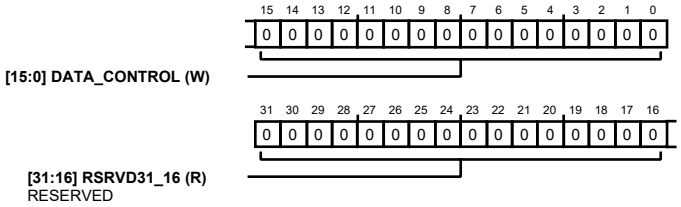


Table 461. Bit Descriptions for MWMSG_SDR

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved.	0x0	R
[15:0]	DATA_CONTROL	Data for SDR write message after control information for the message has been written. LSB is in bits [7:0]; MSB is in bits [15:8]. If the message length is odd, write the last byte of the message to bits [7:0]. The I3C_MS ends the message after transmitting bits [7:0] as the last data byte of the message. However, the value written to bits [15:8] remains in the transmit buffer. To flush the transmit buffer after transmitting an odd number of bytes, write 1 to MDATACTRL.TBFLUSH.	0x0	W
[15:11]	LEN	Control information - Message length in bytes. If LEN = 0, then the generated frame consists of only the END action. If LEN = 0 and END = 1, the I3C_MS generates a STOP without using the ADDR field.		W
10	I2C	Control information - I2C mode: 0: I3C mode. 1: I2C mode.		W
9	RSRVD9_9	Reserved.		R
8	END	Control information - How to end message: 0: End waiting for new SDR message. The I3C_MS issues a repeated START for the new message. 1: End by emitting STOP. The I3C_MS sets STATUS.COMPLETE when the message is complete. The message may complete before LEN bytes are written/read in the following cases: An I2C slave NACKs write data before LEN bytes are written. An I3C slave sends End-of-Data before LEN bytes are read.		W
[7:1]	ADDR	Control information - Destination address of message		W
0	DIR	Control information - Direction: 0: Write. 1: Read.		W

READ SDR MESSAGE DATA REGISTER

Address: 0x F00130D4, Reset: 0x00000000, Name: MRMSG_SDR

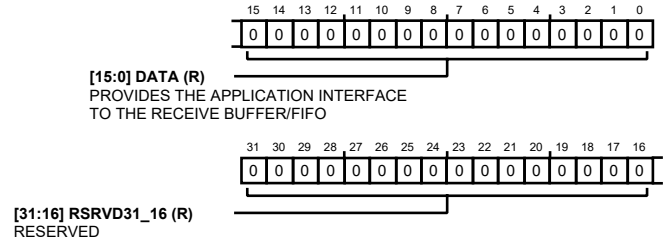


Table 462. Bit Descriptions for MRMSG_SDR

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	RESERVED. Reserved. The read value is 0. Writes have no effect. Use 0 for writes.	0x0	R
[15:0]	DATA	Read data (16 bits). MSB is in bits [15:8]; LSB is in bits [7:0]. When the final byte of an odd length read message is read from DATA: Bits [7:0] hold the last read data byte. Bits [15:8] are 0x00. MERRWARN, OREAD is set due to te half-word read of DATA, which contains only one valid byte. A MERRWARN interrupt is generated if enabled.	0x0	R

START OR CONTINUE DDR MESSAGE REGISTER

Address: 0x F00130D8, Reset: 0x00000000, Name: MWMSG_DDR

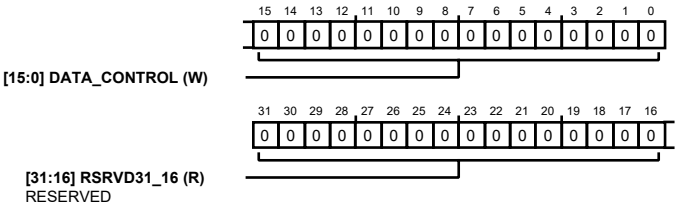


Table 463. Bit Descriptions for MWMSG_DDR

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved.	0x0	R
[15:0]	DATA_CONTROL	Data for HDR-DDR write message, written after control and DDR address/command information for the message has been written. MSB is in bits [15:8]; LSB is in bits [7:0].	0x0	W
[15:0]	AADRCMD	HDR-DDR mode address and command, written after control information has been written: [15:9]: ADDR - Address for HDR-DDR mode message. [8]: Reserved, write value should be 0. [7]: DIR - Read (1) or write (0) [6:0]: CMD- 7-bit HDR-DDR mode command		W
[15:0]	CONTROL	Control information: [15]: Reserved [14]: END - How to end message:		

Bits	Bit Name	Description	Reset	Access
		0: End waiting for new DDR message. The I3C_MS issues an HDR Restart for the new message. 1: End by emitting HDR Exit Pattern. [13: 1 0]: Reserved [9:0]: LEN - Message length (including HDR-DDR command) in half-words. For a read message, LEN also includes one half-word for CRC. For example, to read 8 bytes, set LEN to 6 (one half-word for HDR-DDR command, four half-words of data, one half-word for CRC). If LEN = 0, then the generated frame consists of only the END action. The I3C_MS sets STATUS.COMPLETE when the message is complete. The message may complete before LEN bytes are read if the slave ends the read sooner.		

READ DDR MESSAGE DATA REGISTER

Address: 0x F00130DC, Reset: 0x00000000, Name: MRMSG_DDR

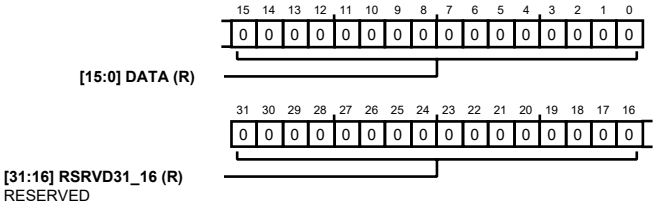


Table 464. Bit Descriptions for MRMSG_DDR

Bits	Bit Name	Description	Reset	Access
[31:16]	RSRVD31_16	Reserved.	0x0	R
[15:0]	DATA	Read data (16 bits). MSB is in bits [15:8]; LSB is in bits [7:0].	0x0	R

MASTER DYNAMIC ADDRESS REGISTER

Address: 0x F00130E4, Reset: 0x00000000, Name: MDYNADDR

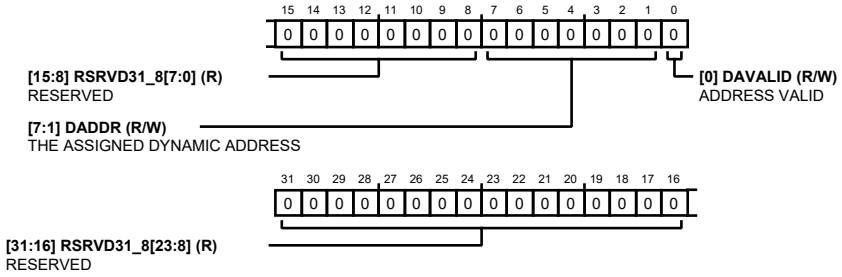


Table 465. Bit Descriptions for MDYNADDR

Bits	Bit Name	Description	Reset	Access
[31:8]	RSRVD31_8	Reserved.	0x0	R
[7:1]	DADDR	The Assigned Dynamic Address.	0x0	R/W
0	DAVALID	Address Valid. 0: The address in the DADDR field is not valid 1: The address in the DADDR field is not valid	0x0	R/W

HDR COMMAND REGISTER

Address: 0x108, Reset: 0x00000000, Name: HDRCMD

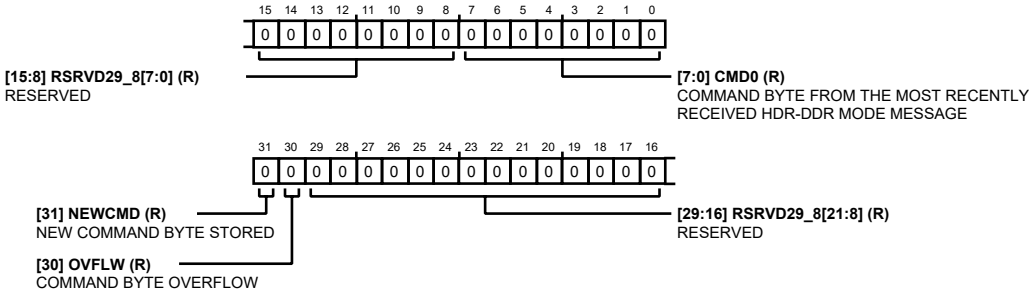


Table 466. Bit Descriptions for HDRCMD

Bits	Bit Name	Description	Reset	Access
31	NEWCMD	NEW COMMAND BYTE STORED. 0: No new HDR-DDR mode command byte was stored in CMD0 since the last time the HDRCMD register was read. 1: A new HDR-DDR mode command byte was stored in CMD0 since the last time the HDRCMD register was read.	0x0	R
30	OVFLW	COMMAND BYTE OVERFLOW. 0: The CMD0 field was not overwritten with a newly received HDR-DDR mode command byte before the previously stored command byte was read. 1: The CMD0 field was overwritten with a newly received HDR-DDR mode command byte before the previously stored command byte was read.	0x0	R
[29:8]	RSRVD29_8	RESERVED.	0x0	R
[7:0]	CMD0	The HDR-DDR mode command byte from the most recently received HDR-DDR mode message.	0x0	R

EXTENDED IBI DATA REGISTER 1

Address: 0x F0013140, Reset: 0x00000070, Name: IBIEXT1

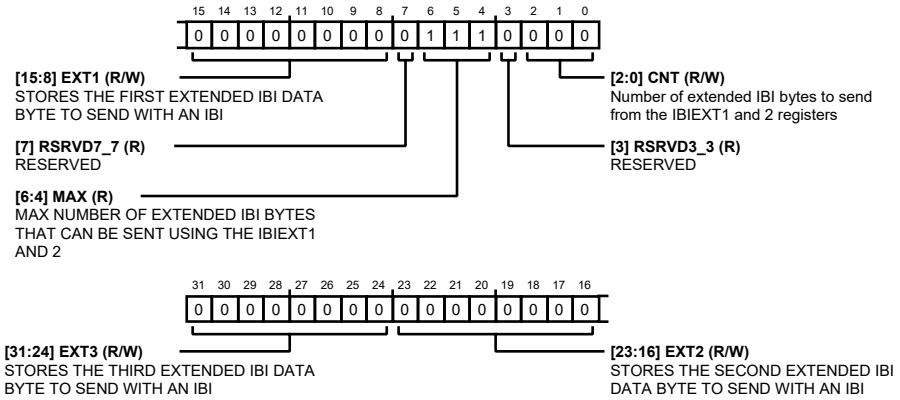


Table 467. Bit Descriptions for IBIEXT1

Bits	Bit Name	Description	Reset	Access
[31:24]	EXT3	STORES THE THIRD EXTENDED IBI DATA BYTE TO SEND WITH AN IBI. When configuration parameter IBI_MAX_EXT_CNT > 2: EXT3 stores the third extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT < 3: The EXT3 field is reserved.	0x0	R/W
[23:16]	EXT2	STORES THE SECOND EXTENDED IBI DATA BYTE TO SEND WITH AN IBI. When configuration parameter IBI_MAX_EXT_CNT > 1: EXT2 stores the second extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT < 2: The EXT2 field is reserved.	0x0	R/W
[15:8]	EXT1	EXT1 stores the first extended IBI data byte to send with an IBI. EXT1 is present whenever the IBIEXT1 register is present (IBI_MAX_EXT_CNT > 0).	0x0	R/W
7	RSRVD7_7	RESERVED.	0x0	R
[6:4]	MAX	The maximum number of extended IBI data bytes that can be sent using the IBIEXT1 and IBIEXT2 registers. The read value of MAX is equal to the value of configuration parameter IBI_MAX_EXT_CNT.	0x7	R
3	RSRVD3_3	RESERVED.	0x0	R
[2:0]	CNT	The number of extended IBI data bytes to send from the IBIEXT1 and IBIEXT2 registers. When requesting an IBI with the CTRL.EXTDATA bit set, the I3C_MS transmits CNT extended IBI data bytes from the IBIEXT1 and IBIEXT2, after sending the mandatory byte. If CNT = 0 when requesting an IBI with the CTRL.EXTDATA bit set, the I3C_MS uses the transmit buffer/FIFO as the source for extended IBI data bytes.	0x0	R/W

EXTENDED IBI DATA REGISTER 2

Address: 0x F0013144, Reset: 0x00000000, Name: IBIEXT2

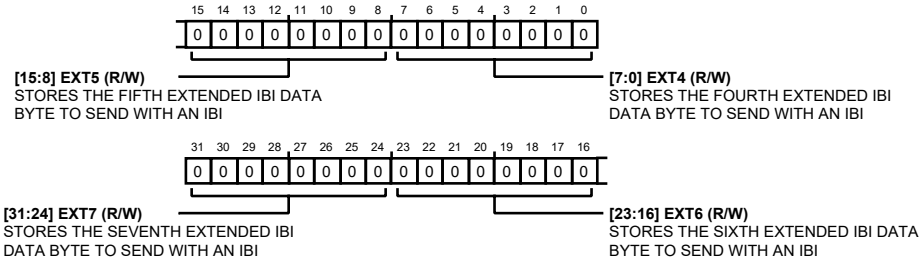


Table 468. Bit Descriptions for IBIEXT2

Bits	Bit Name	Description	Reset	Access
[31:24]	EXT7	Stores the seventh extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT > 6: EXT7 stores the seventh extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT < 7: The EXT7 field is reserved.	0x0	R/W
[23:16]	EXT6	STORES THE SIXTH EXTENDED IBI DATA BYTE TO SEND WITH AN IBI. When configuration parameter IBI_MAX_EXT_CNT > 5: EXT6 stores the sixth extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT < 6: The EXT6 field is reserved.	0x0	R/W
[15:8]	EXT5	STORES THE FIFTH EXTENDED IBI DATA BYTE TO SEND WITH AN IBI. When configuration parameter IBI_MAX_EXT_CNT > 4: EXT5 stores the fifth extended IBI data byte to send with an IBI. When configuration parameter IBI_MAX_EXT_CNT < 5: The EXT5 field is reserved.	0x0	R/W
[7:0]	EXT4	EXT4 stores the fourth extended IBI data byte to send with an IBI. EXT4 is present whenever the IBIEXT2 register is present (IBI_MAX_EXT_CNT > 3).	0x0	R/W

BLOCK ID REGISTER

Address: 0x F0013FFC, Reset: 0x000003F5, Name: ID

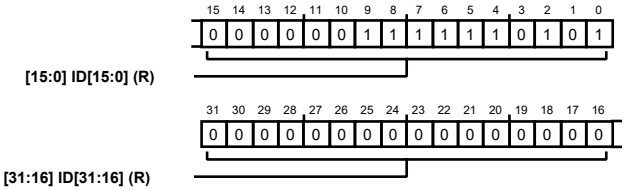


Table 469. Bit Descriptions for ID

Bits	Bit Name	Description	Reset	Access
[31:0]	ID	Vendor-specific information set by hardware configuration parameter BLOCK_ID.	0x3F5	R

REGISTER DETAILS: L2 MEMORY CONTROLLER (L2CTL)

STATUS REGISTER

Address: 0xF0015000, Reset: 0x00000000, Name: L2_STAT

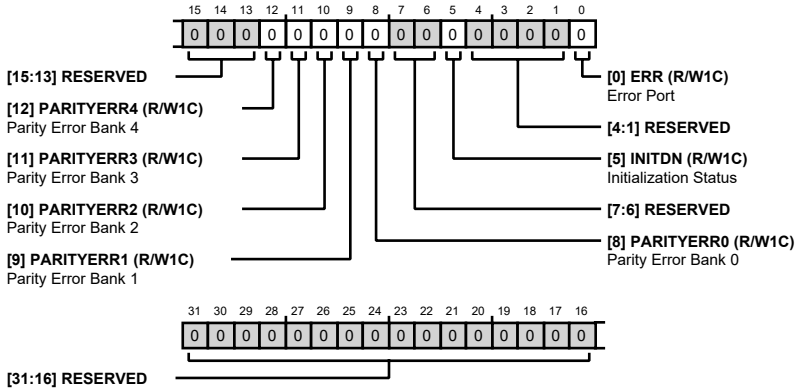


Table 470. Bit Descriptions for L2_STAT

Bits	Bit Name	Description	Reset	Access
[31:13]	RESERVED	Reserved	0x0	R
12	PARITYERR4	Parity Error Bank 4. This bit indicates that an ECC double-bit error occurred inside L2 bank 4. 0: No Status 1: Parity Error	0x0	R/W1C
11	PARITYERR3	Parity Error Bank 3. This bit indicates that an ECC double-bit error occurred inside L2 bank 3. 0: No Status 1: Parity Error	0x0	R/W1C
10	PARITYERR2	Parity Error Bank 2. This bit indicates that an ECC double-bit error occurred inside L2 bank 2. 0: No Status 1: Parity Error	0x0	R/W1C
9	PARITYERR1	Parity Error Bank 1. This bit indicates that an ECC double-bit error occurred inside L2 bank 1. 0: No Status 1: Parity Error	0x0	R/W1C
8	PARITYERR0	Parity Error Bank 0. This bit indicates that an ECC double-bit error occurred inside L2 bank 0. 0: No Status 1: Parity Error	0x0	R/W1C
[7:6]	RESERVED	Reserved	0x0	R
5	INITDN	Initialization Status. Initialization Status. This bit indicates whether the initialization has completed. 0: Initialization Not Complete 1: Initialization Completed	0x0	R/W1C
[4:1]	RESERVED	Reserved	0x0	R

Bits	Bit Name	Description	Reset	Access
0	ERR	Error Port. Error Port. This bit indicates whether a bus access error on the L2 bus port has been detected. 0: No Error 1: Bus Access Error	0x0	R/W1C

INITIALIZATION REGISTER

Address: 0xF0015004, Reset: 0x00000000, Name: L2_INIT

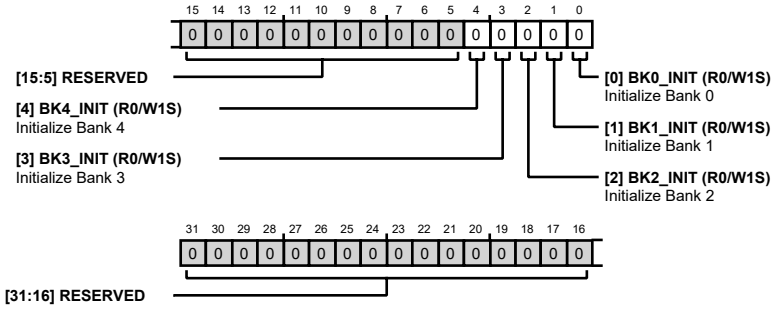


Table 471. Bit Descriptions for L2_INIT

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	BK4_INIT	Initialize Bank 4. Asserting this bit will initialize bank4 with 64'b0 and Parity bits corresponding to 64'b0. Any writes to this bit while initialization is happening to any of the banks are ignored.	0x0	R0/W1S
3	BK3_INIT	Initialize Bank 3. Asserting this bit will initialize bank3 with 64'b0 and Parity bits corresponding to 64'b0. Any writes to this bit while initialization is happening to any of the banks are ignored.	0x0	R0/W1S
2	BK2_INIT	Initialize Bank 2. Asserting this bit will initialize bank2 with 64'b0 and Parity bits corresponding to 64'b0. Any writes to this bit while initialization is happening to any of the banks are ignored.	0x0	R0/W1S
1	BK1_INIT	Initialize Bank 1. Asserting this bit will initialize bank1 with 64'b0 and Parity bits corresponding to 64'b0. Any writes to this bit while initialization is happening to any of the banks are ignored.	0x0	R0/W1S
0	BK0_INIT	Initialize Bank 0. Asserting this bit will initialize bank0 with 64'b0 and Parity bits corresponding to 64'b0. Any writes to this bit while initialization is happening to any of the banks are ignored.	0x0	R0/W1S

INITIALIZATION STATUS REGISTER

Address: 0xF0015008, Reset: 0x00000000, Name: L2_ISTAT

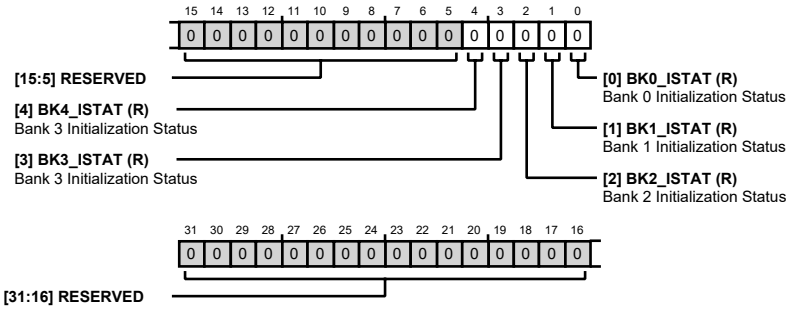


Table 472. Bit Descriptions for L2_ISTAT

Bits	Bit Name	Description	Reset	Access
[31:5]	RESERVED	Reserved	0x0	R
4	BK4_ISTAT	Bank 4 Initialization Status. A W1A on a BK4INIT bit clears this bit when initialization starts, and the bit is set when initialization completes.	0x0	R
3	BK3_ISTAT	Bank 3 Initialization Status. A W1A on a BK3INIT bit clears this bit when initialization starts, and the bit is set when initialization completes.	0x0	R
2	BK2_ISTAT	Bank 2 Initialization Status. A W1A on a BK2INIT bit clears this bit when initialization starts, and the bit is set when initialization completes.	0x0	R
1	BK1_ISTAT	Bank 1 Initialization Status. A W1A on a BK1INIT bit clears this bit when initialization starts, and the bit is set when initialization completes.	0x0	R
0	BK0_ISTAT	Bank 0 Initialization Status. A W1A on a BK0INIT bit clears this bit when initialization starts, and the bit is set when initialization completes.	0x0	R

PARITY ERROR ADDRESS 0 REGISTER

Address: 0xF001500C, Reset: 0x10000000, Name: L2_ERRADDR0

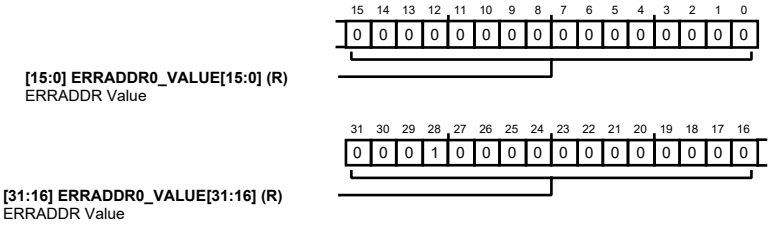


Table 473. Bit Descriptions for L2_ERRADDR0

Bits	Bit Name	Description	Reset	Access
[31:0]	ERRADDR0_VALUE	ERRADDR Value. These bits hold the address containing the Parity error for Bank0.	0x10000000	R

PARITY ERROR ADDRESS 1 REGISTER

Address: 0xF0015010, Reset: 0x10020000, Name: L2_ERRADDR1

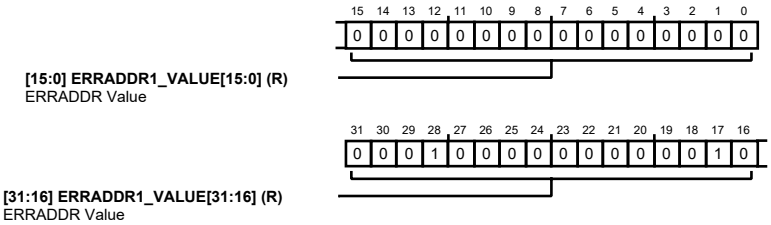


Table 474. Bit Descriptions for L2_ERRADDR1

Bits	Bit Name	Description	Reset	Access
[31:0]	ERRADDR1_VALUE	ERRADDR Value. These bits hold the address containing the Parity error for Bank1.	0x10020000	R

PARITY ERROR ADDRESS 2 REGISTER

Address: 0xF0015014, Reset: 0x10040000, Name: L2_ERRADDR2

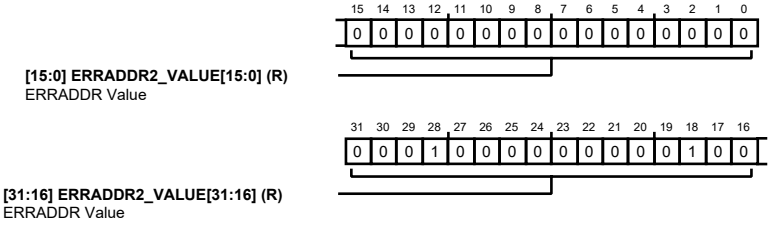


Table 475. Bit Descriptions for L2_ERRADDR2

Bits	Bit Name	Description	Reset	Access
[31:0]	ERRADDR2_VALUE	ERRADDR Value. These bits hold the address containing the Parity error for Bank2.	0x10040000	R

PARITY ERROR ADDRESS 3 REGISTER

Address: 0xF0015018, Reset: 0x10060000, Name: L2_ERRADDR3

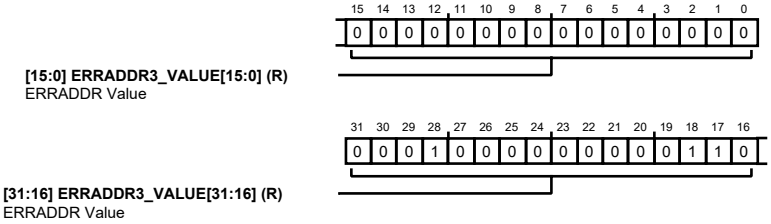


Table 476. Bit Descriptions for L2_ERRADDR3

Bits	Bit Name	Description	Reset	Access
[31:0]	ERRADDR3_VALUE	ERRADDR Value. These bits hold the address containing the Parity error for Bank3.	0x10060000	R

PARITY ERROR ADDRESS 4 REGISTER

Address: 0xF001501C, Reset: 0x10080000, Name: L2_ERRADDR4

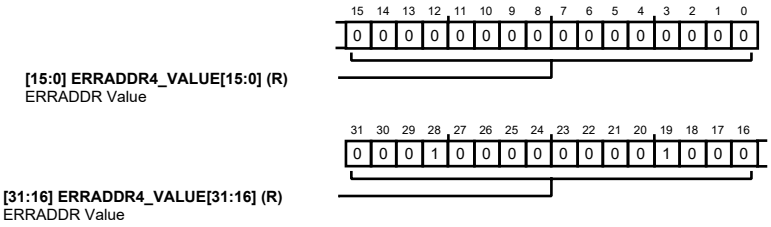


Table 477. Bit Descriptions for L2_ERRADDR4

Bits	Bit Name	Description	Reset	Access
[31:0]	ERRADDR4_VALUE	ERRADDR Value. These bits hold the address containing the Parity error for Bank4.	0x10080000	R

ERROR TYPE 0 REGISTER

Address: 0xF0015020, Reset: 0x00000000, Name: L2_ET0

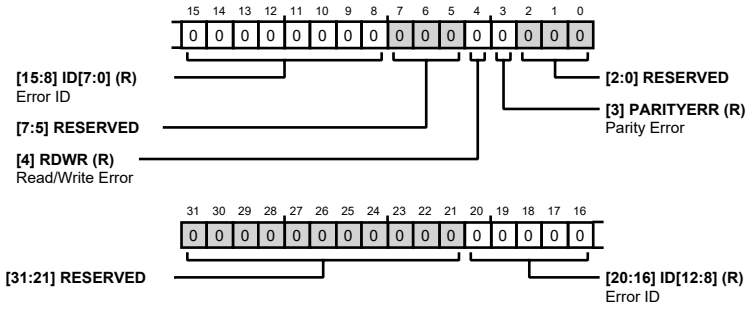


Table 478. Bit Descriptions for L2_ET0

Bits	Bit Name	Description	Reset	Access
[31:21]	RESERVED	Reserved	0x0	R
[20:8]	ID	Error ID. These bits hold the bus master ID of the access that caused an error.	0x0	R
[7:5]	RESERVED	Reserved	0x0	R
4	RDWR	Read/Write Error. This bit indicates whether a read or write access caused an error. 0: No Error 1: Error	0x0	R
3	PARITYERR	Parity Error. This bit indicates whether the access had an ECC double-bit error. 0: No Error 1: Error	0x0	R
[2:0]	RESERVED	Reserved	0x0	R

L2 EADDR0 REGISTER

Address: 0xF0015024, Reset: 0x00000000, Name: L2_EADDR0

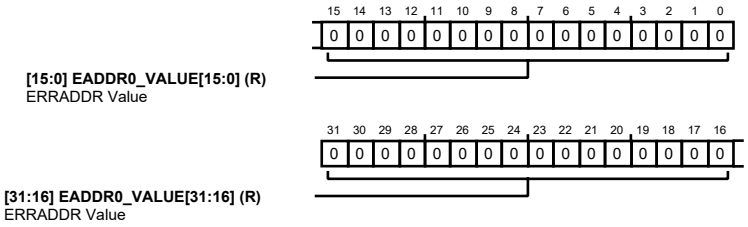


Table 479. Bit Descriptions for L2_EADDR0

Bits	Bit Name	Description	Reset	Access
[31:0]	EADDR0_VALUE	ERRADDR Value. These bits hold the address causing the bus error.	0x0	R

OUTLINE DIMENSIONS

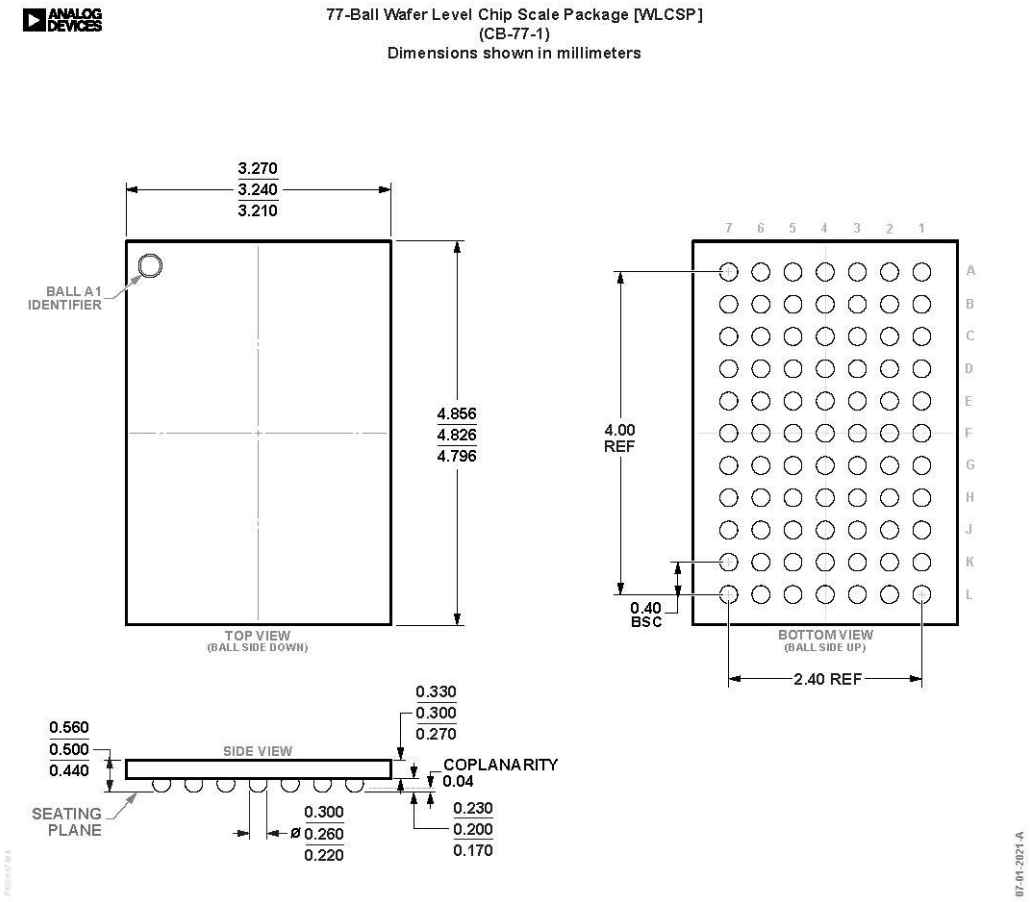


Figure 77. 77-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-77-1)
Dimensions Shown in Millimeters

ORDERING GUIDE

▶ **Table 398. Ordering Guide**

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADAU1797ABCBZRL	-40°C to +85°C	77-Ball Wafer Level Chip Scale Package [WLCSP]	CB-77-1
ADAU1797ABCBZRL7	-40°C to +85°C	77-Ball Wafer Level Chip Scale Package [WLCSP]	CB-77-1
EVAL-ADAU1797Z	—	Evaluation Board	—

[1] Z = RoHS Compliant Part.